19-3155; Rev 0; 5/04

MAXIM

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

General Description

The MAX8543/MAX8544 current-mode, constant-frequency PWM buck controllers operate from a 3V to 13.2V input supply and generate adjustable 0.8V to 0.9 x V_{IN} output voltages at loads up to 25A. They feature adjustable switching frequency and synchronization for noise-sensitive applications.

The MAX8543/MAX8544 can start with (or without) a preexisting bias on the output, without discharging the output. This feature simplifies tracking supply designs for core and I/O applications and redundant supply designs.

The MAX8543/MAX8544 use the DC resistance of the output inductor as the current-sense element for lossless, low-cost current sensing. The current-sense threshold can be set to four discrete levels to accommodate inductors with different DC resistance values.

The MAX8544 features a power-OK monitor and two MAX8544 controllers that can operate at 180° out-of-phase for dual-output applications.

Applications

Base Stations

Networks and Telecom

Storage

Servers

Features

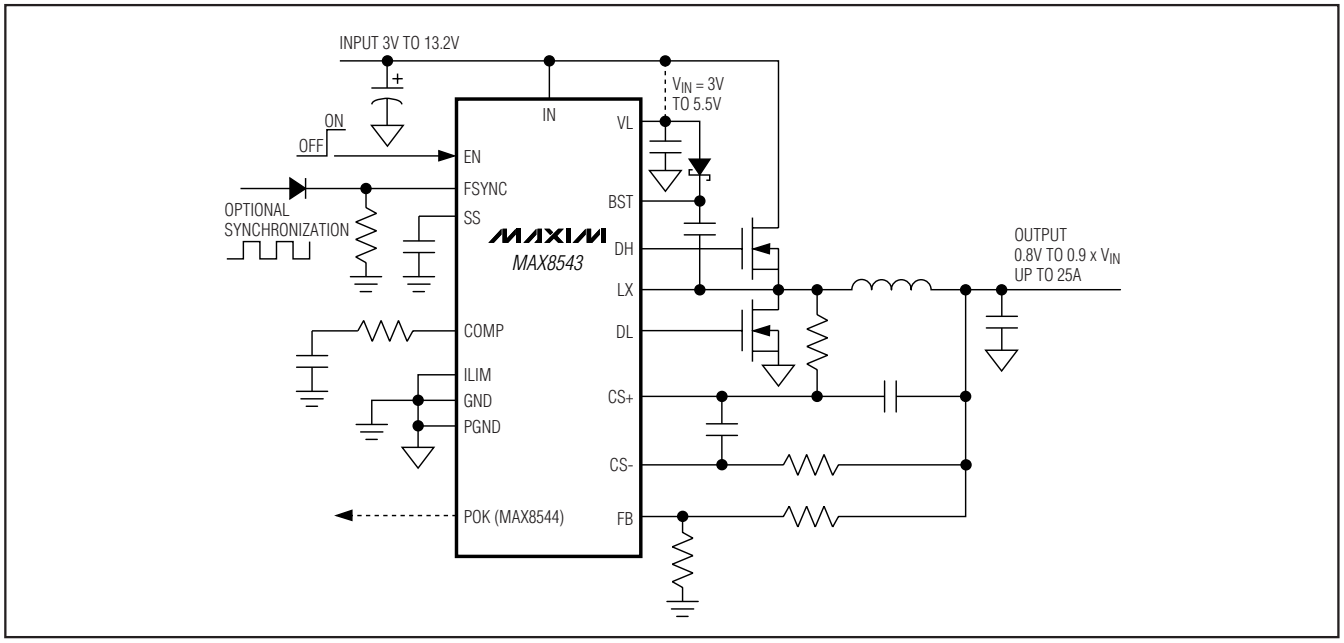
- ♦ **Prebias Startup/Monotonic**
- ♦ **1% Output Accuracy**
- ♦ **Ceramic, Polymer, or Electrolytic Capacitors**
- ♦ **200kHz to 1MHz Adjustable Frequency**
- ♦ **160kHz to 1.2MHz Synchronization**
- ♦ **Lossless, Foldback Current Limit**
- ♦ **Overvoltage Protection**
- ♦ **Enable (On/Off)**
- ♦ **Adjustable Soft-Start**
- ♦ **MAX8544**
  - **Latch-Off/Autorecovery**
  - **Power-OK Monitor**
  - **Out-of-Phase Clock Output**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8543EEE	-40°C to +85°C	16 QSOP
MAX8544EEP	-40°C to +85°C	20 QSOP

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

ABSOLUTE MAXIMUM RATINGS

IN, EN, CS+, CS- to GND .....-0.3V to +14V
BST, DH to LX .....-0.3V to +6V
BST to GND .....-0.3V to +20V
DL, COMP, ILIM2, SS, SYNCO, FSYNC to GND .....-0.3V to (V_{VL} + 0.3V)
VL, FB, POK, ILIM1, ILIM, MODE to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C) 666.7mW
20-Pin QSOP (derate 9.1mW/°C above +70°C) 727.3mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage Range	VL connected to IN for V_{IN} < 5.5V		3.0		13.2	V
Quiescent Supply Current	V_{FB} = 0.9V, no switching			2	3	mA
Shutdown Supply Current	EN = GND, MODE = GND, IN not connected to VL				10	µA
	EN = GND, VL = IN, MODE = GND				20	
VL Undervoltage-Lockout Trip Level	V_{VL} rising, typical hysteresis is 80mV		2.52	2.7	2.88	V
Output Voltage Adjust Range (V_{OUT})	(Note 1)		0.8			V
VL Output Voltage	5.5V < V_{IN} < 13.2V, 1mA < I_{VL} < 75mA		4.5	5	5.5	V
VL Output Current					75	mA
VOLTAGE REFERENCE						
SS Shutdown Resistance	From SS to GND, V_{EN} = 0V			20	100	Ω
SS Soft-Start Current	V_{REF} = 0.625V		14	24	34	µA
Soft-Start Ramp Time	Output from 0% to 100%, C_{REF} = 0.01µF to 1µF			33		ms/µF
ERROR AMPLIFIER						
FB Regulation Voltage			0.792	0.8	0.808	V
Transconductance			70	110	160	µS
COMP Shutdown Resistance	From COMP to GND, V_{EN} = 0V			20	100	Ω
FB Input Leakage Current	V_{FB} = 0.9V			5	100	nA
FB Input Common-Mode Range			-0.1		+0.9	V
CURRENT-SENSE AMPLIFIER						
Voltage Gain	V_{OUT} = 0 to 13V	V_{ILIM1} = 0V	8.8	11	13.2	V/V
		V_{ILIM1} = (1/3)V_{VL}	4.8	6	7.2	
		V_{ILIM1} = (2/3)V_{VL}	3.2	4	4.8	
		V_{ILIM1} = V_{VL}	2.4	3	3.6	
CURRENT LIMIT						
ILIM2 Output Current (MAX8544 Only)	R_{ILIM2} = 50kΩ to 200kΩ		4.5	5	5.5	µA
ILIM1 Input Current	V_{ILIM1} = 0V or V_{VL}		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Threshold	V_{CS+} - V_{CS-}, V_{ILIM1} = 0V	38.5	50	56.5	mV
	V_{CS+} - V_{CS-}, V_{ILIM1} = (1/3)V_{VL}	85	100	115	
	V_{CS+} - V_{CS-}, V_{ILIM1} = (2/3)V_{VL}	127.5	150	172.5	
	V_{CS+} - V_{CS-}, V_{ILIM1} = V_{VL}	170	200	230	
	V_{LX} - V_{PGND}, R_{ILIM2} = 50kΩ (MAX8544 only)	-42.5	-50	-57.5	
	V_{LX} - V_{PGND}, R_{ILIM2} = 200kΩ (MAX8544 only)	-160	-200	-240	
	V_{LX} - V_{PGND}, V_{FB} = 0.8V (MAX8543 only)	-110	-130	-150	
	V_{LX} - V_{PGND}, V_{FB} = 0V (MAX8543 only)	-20	-30	-40	
Negative Current-Limit Threshold	% of positive-direction current limit V_{LX} - V_{PGND}	-25	-50	-85	%
CS+, CS- Input Current	V_{CS+} = V_{CS-} = 0 or 5V	-40		+40	µA
CS+, CS- Input Common-Mode Range		0		13.2	V
OSCILLATOR					
Switching Frequency	R_{FSYNC} = 18.2kΩ	800	1000	1200	kHz
	R_{FSYNC} = 158kΩ		200		
Minimum Off-Time	Measured at DH	150	220	270	ns
Minimum On-Time	Measured at DH		90	145	ns
FSYNC Synchronization Range		160		1200	kHz
FSYNC Input High Pulse Width		100			ns
FSYNC Input Low Pulse Width		100			ns
FSYNC Rise/Fall Time				100	ns
SYNCO Phase Shift from DH Rising	R_{FSYNC} = 18.2kΩ, free-running mode, at maximum duty cycle	165	180	195	Degrees
SYNCO Output Low Level	I_{SYNCO} = 5mA			0.4	V
SYNCO Output High Level	I_{SYNCO} = 5mA	V_{VL} - 1V			V
MOSFET DRIVERS					
DH On-Resistance, High State	(V_{BST} - V_{LX}) = 5V		1	2.5	Ω
	(V_{BST} - V_{LX}) = 3V		1.2		
DH On-Resistance, Low State	(V_{BST} - V_{LX}) = 5V		1	2.5	Ω
	(V_{BST} - V_{LX}) = 3V		1.2		
DL On-Resistance, High State	V_{VL} = 5V		1	2.5	Ω
	V_{VL} = 3V		1.2		
DL On-Resistance, Low State	V_{VL} = 5V		0.6	1.7	Ω
	V_{VL} = 3V		0.8		
Break-Before-Make Dead Time	Low-side off to high-side on		55		ns
	High-side off to low-side on		40		
LX, BST, IN Leakage Current	V_{BST} = 18.7V, V_{LX} = 13.2V, V_{IN} = 13.2V			5	µA
THERMAL PROTECTION					
Thermal Shutdown	Rising temperature		+160		°C
Thermal-Shutdown Hysteresis			15		°C

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POK					
Power-OK Threshold	V_{FB} rising, percent of V_{OUT}, typical hysteresis is 3%	88	91	94	%
POK Output Voltage, Low	V_{FB} = 0.6V, I_{POK} = 2mA		25	200	mV
POK Leakage Current, High	V_{POK} = 5.5V		0.001	1	µA
OVERVOLTAGE PROTECTION (OVP)					
Output Overvoltage Fault-Trip level	Rising edge compared to regulation set point; triggers after one or two clock cycles	+110	+115	+120	%
MODE CONTROL					
MODE Logic-Level Low	3V ≤ V_{VL} ≤ 5.5V			0.4	V
MODE Logic-Level High	3V ≤ V_{VL} ≤ 5.5V	1.8			V
MODE Input Current	V_{MODE} = 0V	-1		+1	µA
	MODE = VL		5	10	
SHUTDOWN CONTROL					
EN Logic-Level Low	3V ≤ V_{VL} ≤ 5.5V			0.45	V
EN Logic-Level High	3V ≤ V_{VL} ≤ 5.5V	2			V
EN Input Current	V_{EN} = 0 or 5.5V	-1		+4	µA
	V_{EN} = 13.2V		1.5	6	

ELECTRICAL CHARACTERISTICS

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Input Voltage Range	VL connected to IN for V_{IN} < 5.5V	3.0	13.2	V
Quiescent Supply Current	V_{FB} = 0.9V, no switching		3	mA
Shutdown Supply Current	EN = GND, MODE = GND, IN not connected to VL		10	µA
	EN = GND, VL = IN, MODE = GND		20	
VL Undervoltage-Lockout Trip Level	V_{VL} rising, typical hysteresis is 80mV	2.52	2.88	V
Output Voltage Adjust Range (V_{OUT})	(Note 1)	0.8		V
VL Output Voltage	5.5V < V_{IN} < 13.2V, 1mA < I_{VL} < 75mA	4.5	5.5	V
VL Output Current			75	mA
VOLTAGE REFERENCE				
SS Shutdown Resistance	From SS to GND, V_{EN} = 0V		100	Ω
SS Soft-Start Current	V_{REF} = 0.625V	14	34	µA
ERROR AMPLIFIER				
FB Regulation Voltage		0.788	0.808	V
Transconductance		70	160	µS
COMP Shutdown Resistance	From COMP to GND, V_{EN} = 0V		100	Ω
FB Input Leakage Current	V_{FB} = 0.9V		100	nA
FB Input Common-Mode Range		-0.1	+0.9	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
CURRENT-SENSE AMPLIFIER					
Voltage Gain	V_{OUT} = 0 to 13V	V_{ILIM1} = 0V	8.8	13.2	V/V
		V_{ILIM1} = (1/3)V_{VL}	4.8	7.2	
		V_{ILIM1} = (2/3)V_{VL}	3.2	4.8	
		V_{ILIM1} = V_{VL}	2.4	3.6	
CURRENT LIMIT					
ILIM2 Output Current (MAX8544 Only)	R_{ILIM2} = 50kΩ to 200kΩ		4.2	5.5	µA
ILIM1 Input Current	V_{ILIM1} = 0V or V_{VL}		-1	+1	µA
Current-Limit Threshold	V_{CS+} - V_{CS-}, V_{ILIM1} = 0V		38.5	56.5	mV
	V_{CS+} - V_{CS-}, V_{ILIM1} = (1/3)V_{VL}		85	115	
	V_{CS+} - V_{CS-}, V_{ILIM1} = (2/3)V_{VL}		127.5	172.5	
	V_{CS+} - V_{CS-}, V_{ILIM1} = V_{VL}		170	230	
	V_{LX} - V_{PGND}, R_{ILIM2} = 50kΩ (MAX8544 only)		-40	-60	
	V_{LX} - V_{PGND}, R_{ILIM2} = 200kΩ (MAX8544 only)		-160	-240	
	V_{LX} - V_{PGND}, V_{FB} = 0.8V (MAX8543 only)		-110	-150	
	V_{LX} - V_{PGND}, V_{FB} = 0V (MAX8543 only)		-20	-40	
Negative Current-Limit Threshold	% of positive-direction current limit V_{LX} - V_{PGND}		-25	-85	%
CS+, CS- Input Current	V_{CS+} = V_{CS-} = 0V or 5V		-40	+40	µA
CS+, CS- Input Common-Mode Range			0	13.2	V
OSCILLATOR					
Switching Frequency	R_{FSYNC} = 18.2kΩ		800	1200	kHz
Minimum Off-Time	Measured at DH		150	270	ns
Minimum On-Time	Measured at DH			140	ns
FSYNC Synchronization Range			160	1200	kHz
FSYNC Input High Pulse Width			100		ns
FSYNC Input Low Pulse Width			100		ns
FSYNC Rise/Fall Time				100	ns
SYNCO Phase Shift from DH Rising	R_{FSYNC} = 18.2kΩ		165	195	Degrees
SYNCO Output Low Level	I_{SYNCO} = 5mA			0.4	V
SYNCO Output High Level	I_{SYNCO} = 5mA		V_{VL} - 1V		V
MOSFET DRIVERS					
DH On-Resistance, High State	(V_{BST} - V_{LX}) = 5V			2.5	Ω
DH On-Resistance, Low State	(V_{BST} - V_{LX}) = 5V			2.5	Ω
DL On-Resistance, High State	V_{VL} = 5V			2.5	Ω
DL On-Resistance, Low State	V_{VL} = 5V			1.7	Ω
LX, BST, IN Leakage Current	V_{BST} = 18.7V, V_{LX} = 13.2V, V_{IN} = 13.2V			5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 13.2V, V_{BST} - V_{LX} = 5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

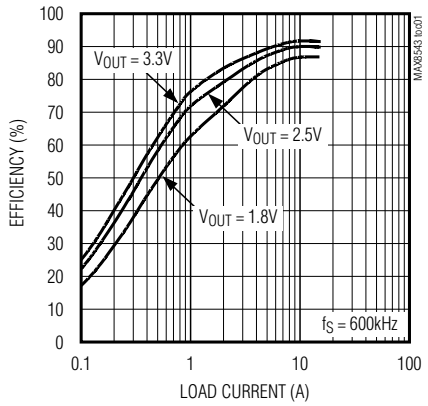
PARAMETER	CONDITIONS	MIN	MAX	UNITS
POK				
Power-OK Threshold	V_{FB} rising, percent of V_{OUT}, typical hysteresis is 3%	88	94	%
POK Output Voltage, Low	V_{FB} = 0.6V, I_{POK} = 2mA		200	mV
POK Leakage Current, High	V_{POK} = 5.5V		1	µA
OVERVOLTAGE PROTECTION (OVP)				
Output Overvoltage Fault-Trip level	Rising edge compared to regulation set point; triggers after one or two clock cycles	+110	+120	%
MODE CONTROL				
MODE Logic-Level Low	3V ≤ V_{VL} ≤ 5.5V		0.4	V
MODE Logic-Level High	3V ≤ V_{VL} ≤ 5.5V	1.8		V
MODE Input Current	V_{MODE} = 0V	-1	+1	µA
	MODE = VL		10	
SHUTDOWN CONTROL				
EN Logic-Level Low	3V ≤ V_{VL} ≤ 5.5V		0.45	V
EN Logic-Level High	3V ≤ V_{VL} ≤ 5.5V	2		V
EN Input Current	V_{EN} = 0V or 5.5V	-1	+4	µA
	V_{EN} = 13.2V		6	

Note 1: Maximum output voltage is limited by maximum duty cycle and external components.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

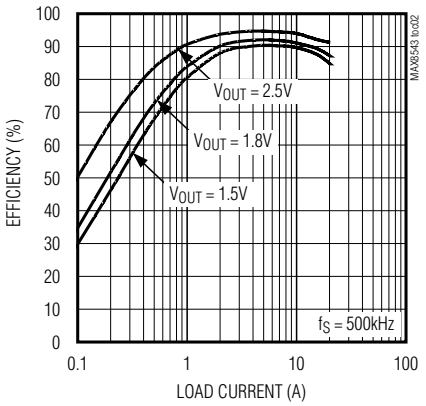
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

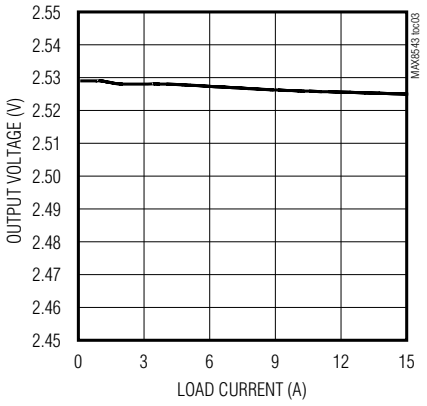
EFFICIENCY vs. LOAD CURRENT WITH 12V INPUT



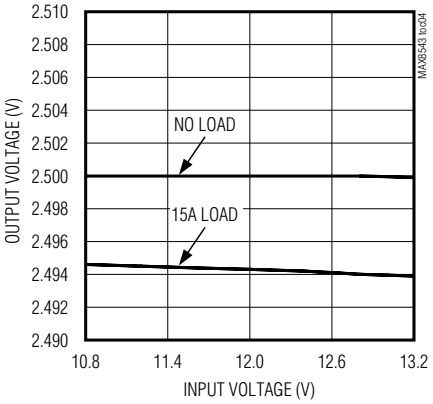
EFFICIENCY vs. LOAD CURRENT WITH 3.3V INPUT



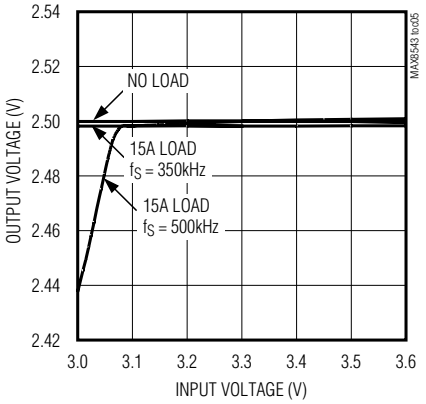
LOAD REGULATION WITH 12V INPUT



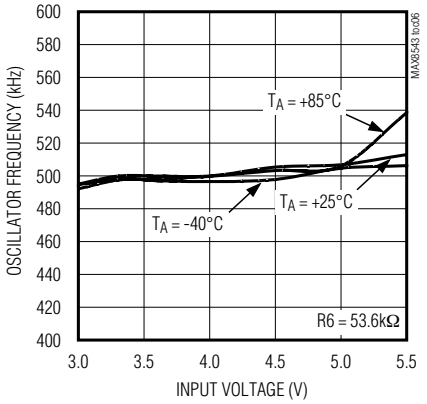
LINE REGULATION WITH 12V INPUT AND 2.5V OUTPUT



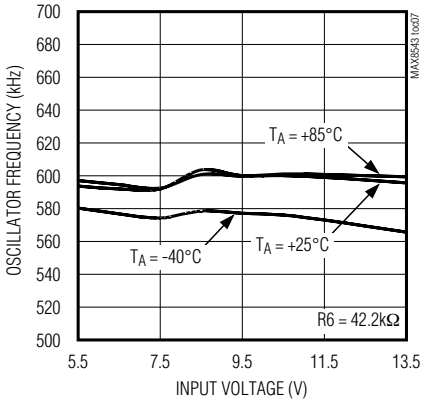
LINE REGULATION 3.0V TO 3.6V INPUT



OSCILLATOR FREQUENCY vs. INPUT VOLTAGE



OSCILLATOR FREQUENCY vs. INPUT VOLTAGE

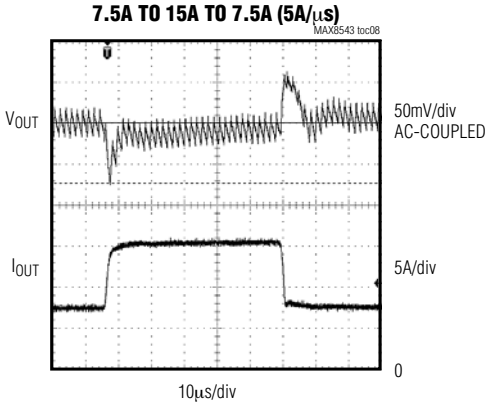


Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

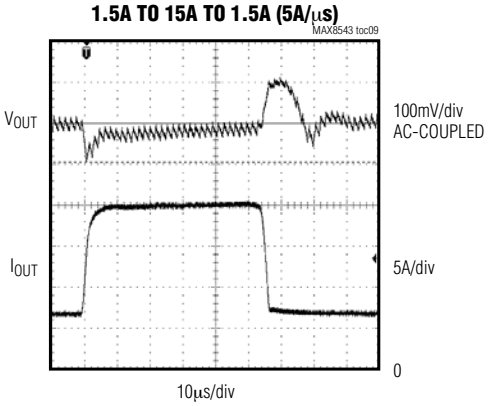
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

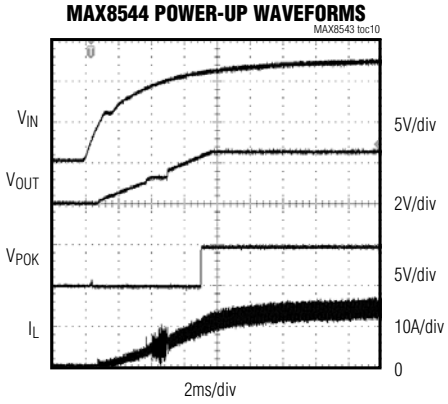
MAX8544 STEP-LOAD RESPONSE
7.5A TO 15A TO 7.5A (5A/µs)



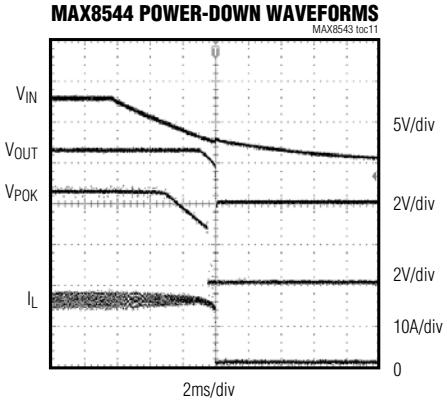
MAX8544 STEP-LOAD RESPONSE
1.5A TO 15A TO 1.5A (5A/µs)



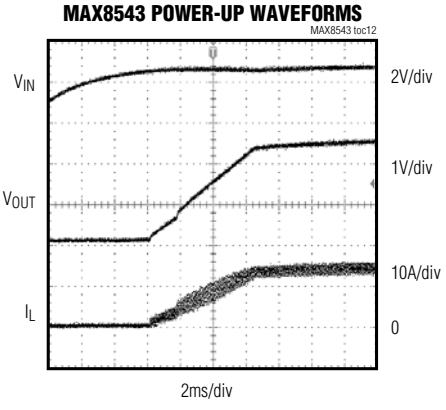
MAX8544 POWER-UP WAVEFORMS



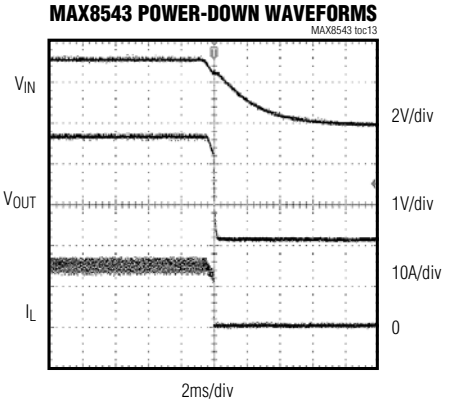
MAX8544 POWER-DOWN WAVEFORMS



MAX8543 POWER-UP WAVEFORMS



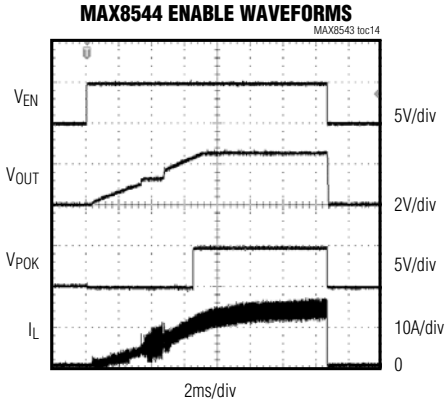
MAX8543 POWER-DOWN WAVEFORMS



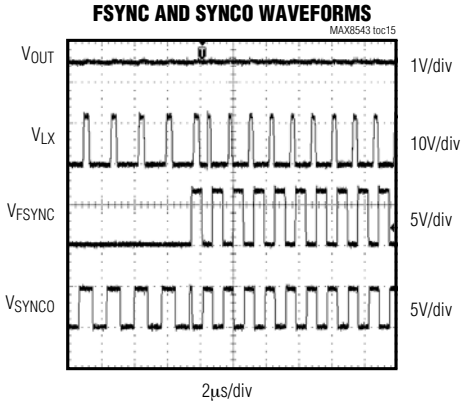
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

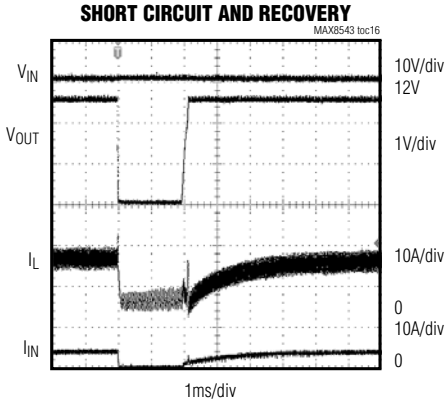
MAX8544 ENABLE WAVEFORMS



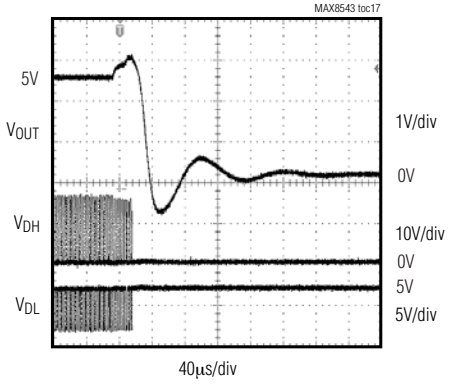
FSYNC AND SYNCO WAVEFORMS



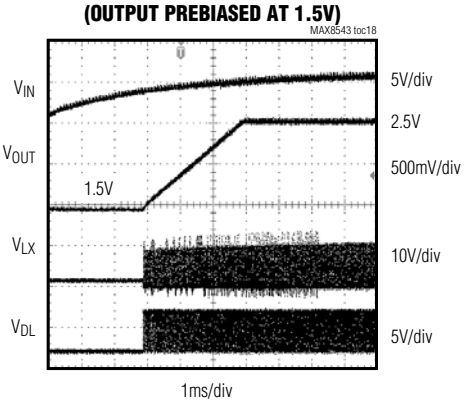
SHORT CIRCUIT AND RECOVERY



OVERVOLTAGE PROTECTION WITH 15A LOAD



PREBIASED STARTUP (OUTPUT PREBIASED AT 1.5V)

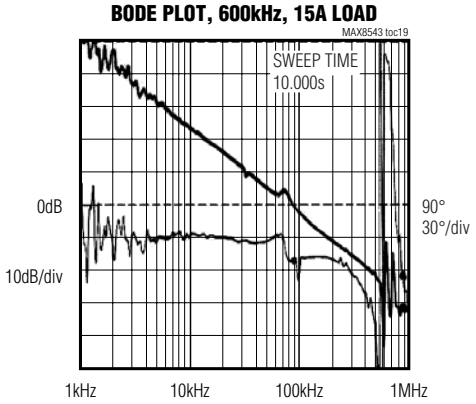


Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

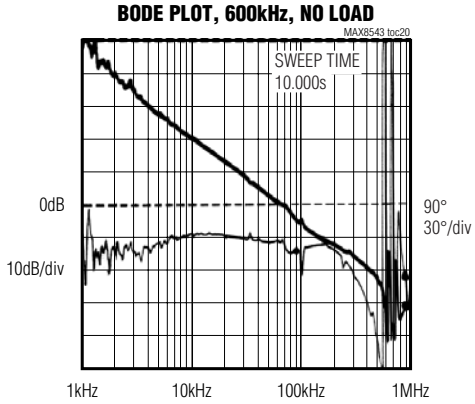
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

BODE PLOT, 600kHz, 15A LOAD



BODE PLOT, 600kHz, NO LOAD



Pin Description

PIN		NAME	FUNCTION
MAX8543	MAX8544		
1	2	GND	Ground. Connect to the analog ground plane.
2	3	SS	Soft-Start. Connect a 0.1µF to 1µF ceramic capacitor from SS to GND. This capacitor sets the soft-start period during startup. See the *Startup and Soft-Start* section. SS is internally pulled to GND in shutdown.
3	4	COMP	Compensation. Connect to an external RC network to compensate the feedback loop. See the *Compensation Design* section. COMP is internally pulled to GND in shutdown.
4	5	FB	Output Feedback. Connect to the center of a voltage-divider connected between OUT and GND to set the output voltage. The FB threshold voltage is 0.8V.
5	6	EN	Enable. Drive EN logic high to enable the output, or drive logic low for shutdown. Connect EN to IN for always-on operation.
6	7	CS-	Negative Differential Current-Sensing Input
7	8	CS+	Positive Differential Current-Sensing Input
—	9	ILIM1	Digital Programmable Current-Limit Input for Inductor Current Sensing (V_{CS+} - V_{CS-}). See Table 3.
8	—	ILIM	
9	12	PGND	Power Ground. Connect to the power ground plane and to the source of the low-side external MOSFETs. Connect PGND to GND at a single point.
10	13	DL	Low-Side MOSFET Gate-Driver Output. Connect to the gate of the low-side external MOSFETs. DL is pulled low in shutdown.
11	14	VL	Internal 5V Linear-Regulator Output. Connect a 1µF to 10µF ceramic capacitor from VL to PGND. Connect VL to IN for V_{IN} less than 5.5V. VL provides power for bias and gate drive.
12	15	IN	Input Supply Voltage. IN is the input to the internal linear regulator. Connect VL to IN for V_{IN} less than 5.5V.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8543	MAX8544		
13	16	LX	Inductor Connection
14	17	DH	High-Side MOSFET Gate-Driver Output. Connect DH to the gate of the high-side external MOSFETs. DH is pulled low in shutdown.
15	18	BST	Boost Capacitor Connection. Connect a 0.1µF or larger ceramic capacitor from BST to LX. BST provides power for the high-side MOSFET gate drive.
16	19	FSYNC	Frequency Set and Synchronization. Connect a resistor from FSYNC to GND to set the switching frequency or drive with a clock signal to synchronize between 160kHz and 1.2MHz. See the *Switching Frequency and Synchronization* section.
—	1	ILIM2	Analog Programmable Current-Limit Input for Low-Side MOSFET (V_{LX} - V_{PGND}). Connect a resistor from ILIM2 to ground to set the overcurrent threshold. See the *Setting the Current Limits* section.
—	10	MODE	Current-Limit Operating-Mode Selection. Connect MODE to VL for latch-off current limit or connect to GND for automatic-recovery current limit with the MAX8544. The MAX8543 always uses automatic-recovery current limit.
—	11	POK	Power-OK. POK is an open-drain output that is high impedance when the output is above 91% of its nominal regulation voltage. POK is pulled low when the output is out of regulation and when the part is in shutdown. To use POK as a logic-level signal, connect a pullup resistor from POK to the logic supply.
—	20	SYNCO	Synchronization Output. Provides a clock output that is 180° out of phase with the rising edge of DH for out-of-phase synchronization of another MAX8544.

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

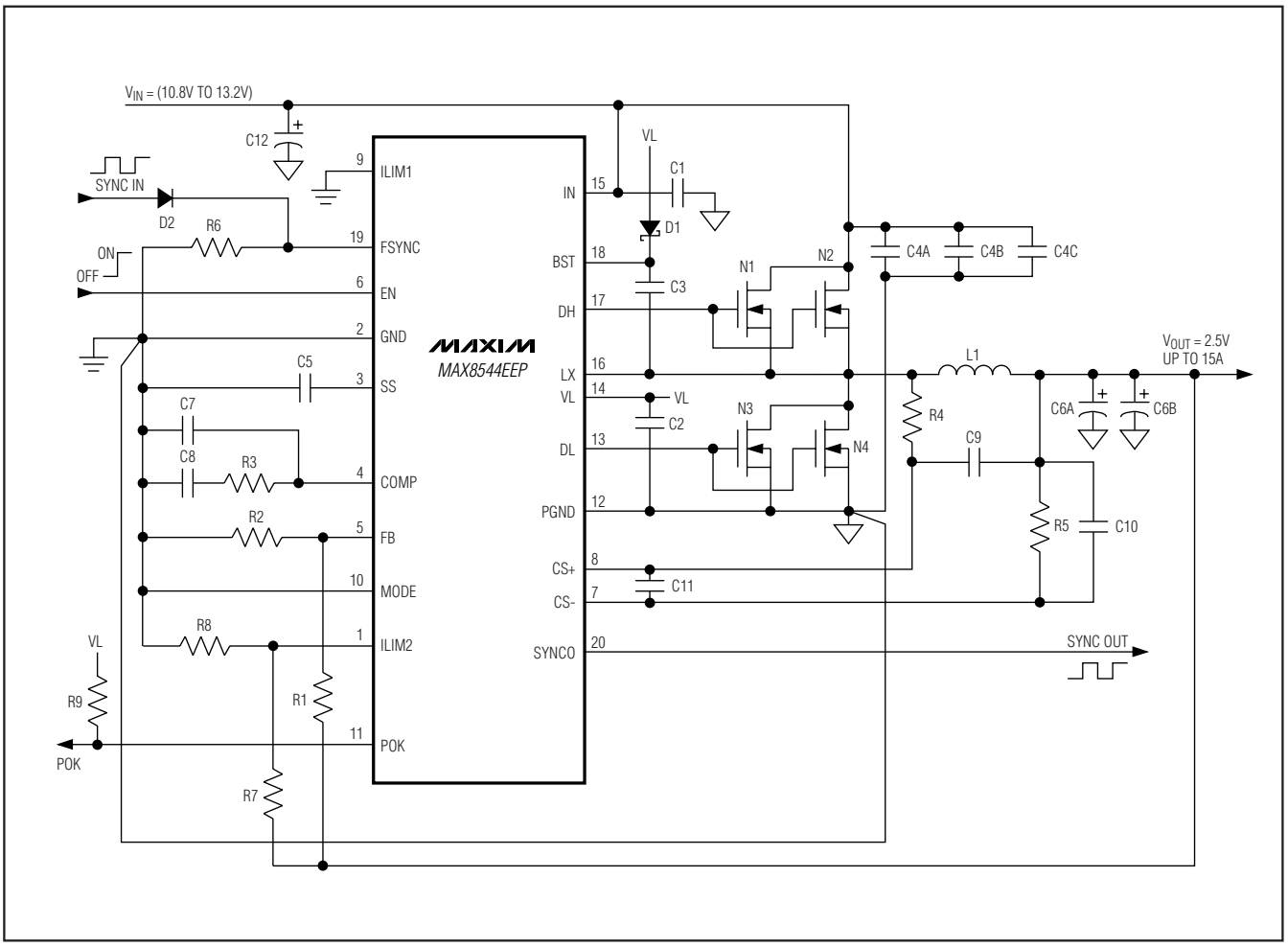


Figure 1. Typical Applications Circuit with 12V (±10%) Input, 2.5V Output at Up to 15A, and 600kHz Switching Frequency

Table 1. Suggested Components for Figure 1

DESIGNATION	QTY	DESCRIPTION
C1	1	1µF ±20%, 16V X5R ceramic capacitor (0603) Panasonic ECJ1VB1C105M or equivalent
C2	1	10µF ±20%, 6.3V X5R ceramic capacitor (0805) Panasonic ECJ2FB0J106M or Taiyo Yuden JMK212BJ106MG
C3	1	0.1µF ±10%, 50V X7R ceramic capacitor (0603) TDK C1608X7R1H104KT or equivalent
C4A, C4B, C4C	2	10µF ±20%, 16V X5R ceramic capacitors (1206) Panasonic ECJ3YB1C106M or equivalent
C5	1	0.22µF ±10%, 10V X7R ceramic capacitor (0603) Taiyo Yuden LMK107BJ224KA or equivalent
C6A, C6B	2	180µF, 4V aluminum poly SPCAPs Panasonic EEFUE0G181XR
C7	1	10pF, 50V C0G ceramic capacitor (0603)
C8	1	220pF ±10%, 50V X7R ceramic capacitor (0603)
C9, C10	2	0.47µF ±10% X7R ceramic capacitors (0603)
C11	1	100pF, 50V C0G ceramic capacitor (0603)
C12	1	470µF ±20%, 16V aluminum electrolytic capacitor Rubycon 16MBZ470M
D1	1	100mA, 30V Schottky diode (SOT-323) Central CMSSH-3
D2	1	250mA, 100V switching diode (SOT23) Central CMPD914
L1	1	0.82µH, 33A, 1.6mΩ inductor Vishay IHLP-5050FD-01 0.82µH
N1, N2	2	N-channel MOSFETs IRF IRF7821
N3, N4	2	N-channel MOSFETs IRF IRF7832
R1	1	17.4kΩ ±1% resistor (0603)
R2	1	8.06kΩ ±1% resistor (0603)
R3	1	220kΩ ±5% resistor (0603)
R4, R5	2	1.3kΩ ±5% resistors (0603)
R6	1	42.2kΩ ±1% resistor (0603)
R7	1	90.9kΩ ±1% resistor (0603)
R8	1	9.31kΩ ±1% resistor (0603)
R9	1	100kΩ ±5% resistor (0603)

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

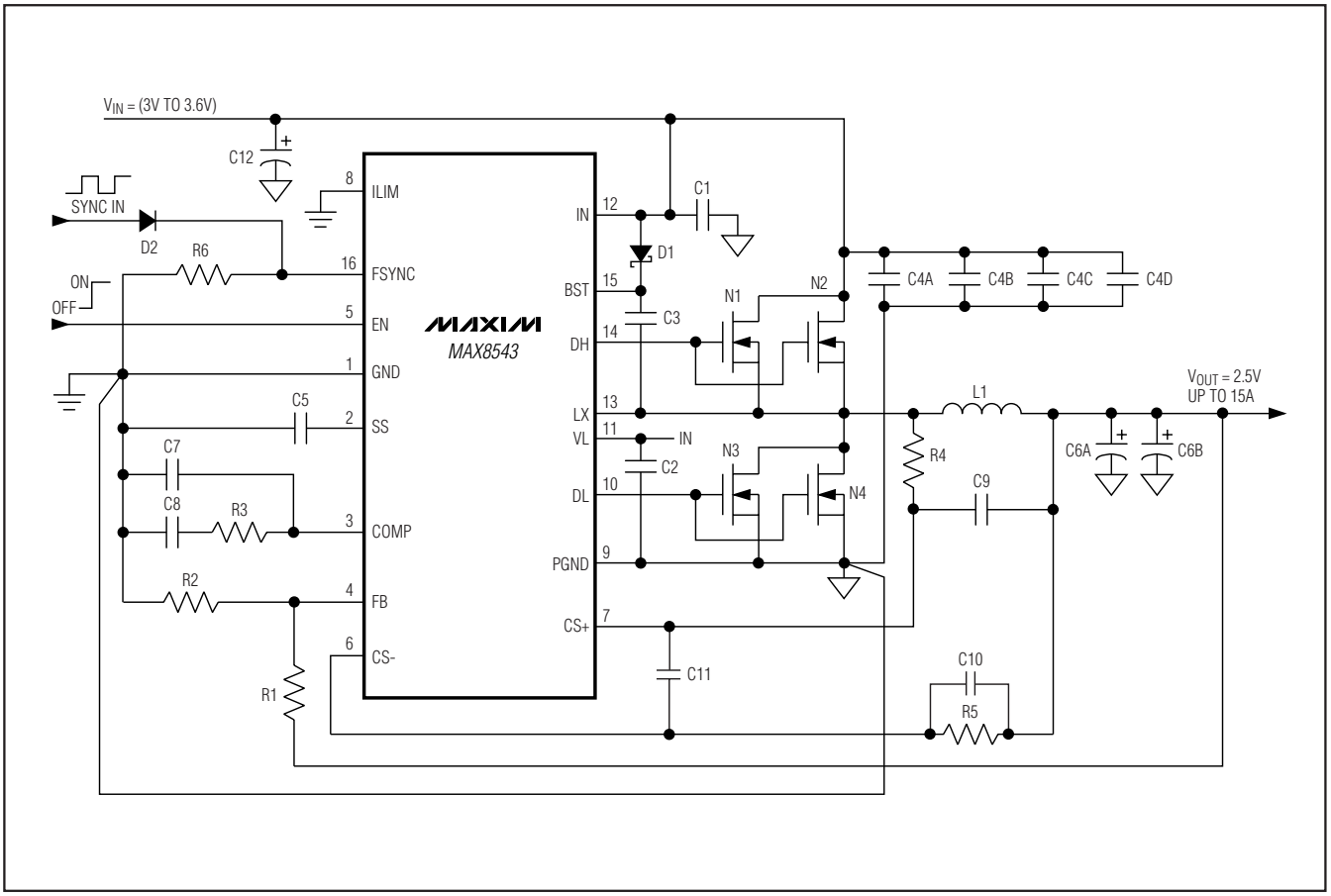


Figure 2. Typical Applications Circuit with 3.3V (±10%) Input, 2.5V Output at Up to 15A, and 500kHz Switching Frequency

Table 2. Suggested Components for Figure 2

DESIGNATION	QTY	DESCRIPTION
C1	1	1µF ±10%, 16V X5R ceramic capacitor (0603) Panasonic ECJ1VB1C105K or equivalent
C2	1	10µF ±20%, 6.3V X5R ceramic capacitor (0805) Panasonic ECJ2FB0J106M or Taiyo Yuden JMK212BJ106MG
C3	1	0.1µF ±10%, 50V X7R ceramic capacitor (0603) TDK C1608X7R1H104KT or equivalent
C4A, C4B, C4C, C4D	4	10µF ±20%, 16V X5R ceramic capacitors (1206) Panasonic ECJ3YB1C106M or equivalent
C5	1	0.22µF ±10%, 10V X7R ceramic capacitor (0603) Taiyo Yuden LMK107BJ224KA or equivalent
C6A, C6B	2	180µF, 4V, 10mΩ aluminum poly SPCAPs Panasonic EEFUE0G181XR
C7	1	12pF, 50V C0G ceramic capacitor (0603)
C8	1	220pF ±10%, 50V X7R ceramic capacitor (0603)
C9, C10	2	0.47µF ±10% X7R ceramic capacitors (0603)
C11	1	100pF, 50V C0G ceramic capacitor (0603)
C12	1	470µF ±20%, 6.3V POSCAP Sanyo 6PB470M
D1	1	100mA, 30V Schottky diode (SOT-323) Central CMSSH-3
D2	1	250mA, 100V switching diode (SOT23) Central CMPD914
L1	1	0.33µH, 16A, 2mΩ inductor (13 x 10 x 6.35) Coilcraft DO3316P-331HC
N1, N2	2	N-channel MOSFETs Vishay Si4866DY
N3, N4	2	N-channel MOSFETs Vishay Si4866DY
R1	1	17.4kΩ ±1% resistor (0603)
R2	1	8.06kΩ ±1% resistor (0603)
R3	1	150kΩ ±5% resistor (0603)
R4, R5	2	680Ω ±5% resistors (0603)
R6	1	53.6kΩ ±1% resistor (0603)

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

Detailed Description

DC-DC Converter Control Architecture

The MAX8543/MAX8544 step-down controllers use a PWM, current-mode control scheme. An internal transconductance amplifier establishes an integrated error voltage. The heart of the PWM controller is an open-loop comparator that compares the integrated voltage-feedback signal against the amplified current-sense signal plus the slope-compensation ramp, which are summed into the main PWM comparator to preserve inner-loop stability and eliminate inductor staircasing. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached or the peak current limit is reached. During this on-time, current ramps up through the inductor, storing energy in a magnetic field and sourcing current to the output. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage-error signal. The circuit acts as a switch-mode transconductance amplifier and pushes the output LC filter pole normally found in a voltage-mode PWM to a higher frequency.

During the second half of the cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as the current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the required load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under soft-overload conditions, when the peak inductor current exceeds the selected current limit (see the *Current-Limit Circuit* section), the high-side MOSFET is turned off immediately and the low-side MOSFET is turned on and remains on to let the inductor current ramp down until the next clock cycle. Under heavy-overload or short-circuit conditions, the valley foldback current limit is enabled to reduce power dissipation of external components.

The MAX8543/MAX8544 operate in a forced-PWM mode. As a result, the controller maintains a constant switching frequency, regardless of load, to allow for easier filtering of the switching noise.

Internal 5V Linear Regulator (VL)

All MAX8543/MAX8544 functions are powered from the on-chip, low-dropout, 5V linear regulator. Connect a 1µF to 10µF ceramic capacitor from VL to PGND. In applications where the input voltage is less than 5.5V, bypass the linear regulator by connecting VL to IN.

Undervoltage Lockout

When VL drops below 2.62V, the MAX8543/MAX8544 assume that the supply voltage is too low for proper operation, so the undervoltage-lockout (UVLO) circuitry inhibits switching and forces the DL and DH gate drivers low. When VL rises above 2.7V, the controller enters the startup sequence and then resumes normal operation.

Startup and Soft-Start

The soft-start circuitry gradually ramps up the reference voltage to control the rate of rise of the step-down controller output and reduce input surge currents during startup. The soft-start period is determined by the value of the capacitor from SS to GND. The soft-start time is approximately (33ms/µF) x C_{SS}. The MAX8543/MAX8544 also feature prebias startup; therefore, both external power MOSFETs are kept off if the voltage at FB is higher than that at SS. This allows the MAX8543/MAX8544 to start up into a prebiased output without pulling the output voltage down.

Before the MAX8543/MAX8544 can begin the soft-start and power-up sequence, the following conditions must be met:

1) V_{VL} exceeds the 2.7V undervoltage-lockout threshold.
2) EN is at logic high.
3) The thermal limit is not exceeded.

Enable

The MAX8543/MAX8544 feature a low-power shutdown mode. A logic low at EN shuts down the controller. During shutdown, the output is high impedance, and both DH and DL are low. Shutdown reduces the quiescent current (I_Q) to less than 10µA. A logic high at EN enables the controller.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX8543/MAX8544 also use the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal. The DL low-side gate-drive waveform is always the complement of the DH high-side gate-drive waveform (with controlled dead time to prevent cross-conduction or shoot-through). An adaptive dead-time circuit monitors the DL voltage and prevents the high-side MOSFET from turning on until DL is fully off. For the dead-time circuit to work properly, there must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate. Otherwise, the sense circuitry in the MAX8543/MAX8544 can interpret the MOSFET gate as off when gate charge actually remains.

Use very short, wide traces, about 10 to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the device) for the gate drive. The dead time at the other edge (DH turning off) also has an adaptive dead-time circuit operating in a similar manner. For both edges, there is an additional fixed dead time after the adaptive dead time expires.

High-Side Gate-Drive Supply (BST)

A flying capacitor boost circuit (Figure 3) generates the gate-drive voltage for the high-side n-channel MOSFET. The capacitor between BST and LX is charged from VL up to V_{VL} minus the diode forward-voltage drop while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. The controller then closes an internal switch between BST and DH to turn the high-side MOSFET on.

Current-Sense Amplifier

The MAX8543/MAX8544 current-sense circuit amplifies the differential current-sense voltage (V_{CS+} - V_{CS-}). The gain of the current-sense amplifier is determined by the states of ILIM and ILIM1. This amplified current-sense signal and the internal slope-compensation signal are summed (V_{SUM}) together and fed into the PWM comparator's inverting input. The PWM comparator shuts off the high-side MOSFET when V_{SUM} exceeds the integrated feedback voltage (V_{COMP}).

The differential current sense is also used to provide peak inductor current limiting. This current limit is more accurate than the valley current limit, which is measured across the low-side MOSFET's on-resistance.

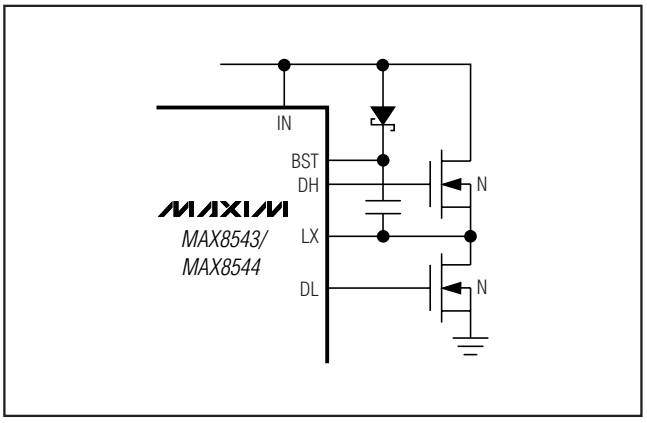


Figure 3. The boost circuit provides voltage for the high-side MOSFET gate drive.

Current-Limit Circuit

The MAX8543/MAX8544 use both valley foldback current limiting and peak constant current limiting, simultaneously (Figure 4). The valley foldback current limit is used to reduce power dissipation of external components, mainly inductor and power MOSFETs, and upstream power source, when output is severely overloaded or short circuited. Thus the circuit can withstand short-circuit conditions indefinitely without causing overheating of any component. The peak constant current limit sets the current-limit point more accurately since it does not have to suffer the wide variation of the low-side power MOSFET's on-resistance due to tolerance and temperature.

The valley current is sensed across the on-resistance of the low-side MOSFET (V_{PGND} - V_{LX}). The valley current limit trips when the sensed current exceeds the valley current-limit threshold. The valley current limit recovers when the sensed current drops below the valley current-limit threshold (except when using the latch-off option with the MAX8544).

Set the minimum valley current-limit threshold, when the output voltage is at a nominal regulated value, higher than the maximum peak current-limit setting. With this method, the current-limit point accuracy is controlled by the peak current limit and is not interfered with by the wide variation of MOSFET on-resistance. See the *Setting the Current Limits* section for how to set these limits.

The MAX8543 has a fixed valley current-limit threshold and fixed foldback ratio. The MAX8544 can select between an adjustable valley current-limit threshold with adjustable foldback ratio and a fixed valley current limit without foldback for latch-off. When latch-off is used (MODE is connected to VL), set the current-limit threshold by only one resistor from ILIM2 to GND and make sure this threshold is higher than the maximum output current required by at least a 20% margin. Cycle EN or input power to reset the current-limit latch.

The peak current limit is used to sense the inductor current, and is more accurate than the valley current limit since it does not depend upon the on-resistance of the low-side MOSFET. The peak current can be measured across the resistance of the inductor for the highest efficiency, or alternatively, a current-sense resistor can be used for more accurate current sensing. The MAX8543/MAX8544 have four selectable peak current-limit thresholds that are selected using ILIM (MAX8543) or ILIM1 (MAX8544). See Table 3 for the current-limit settings.

For more information on the current limit, see the *Setting the Current Limits* section.

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

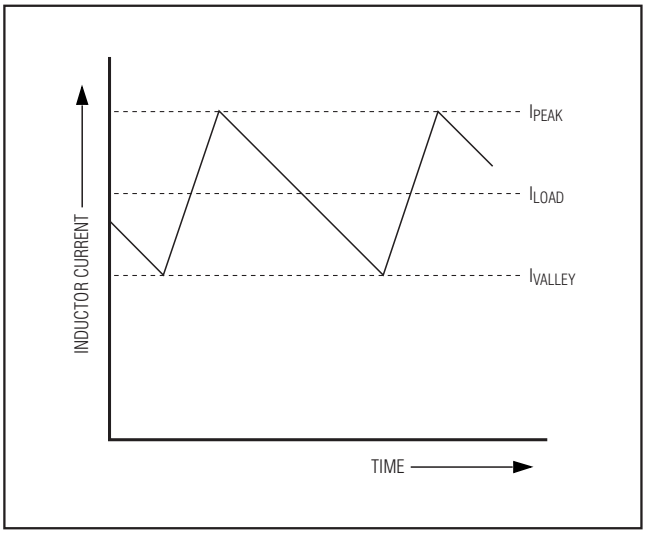


Figure 4. Inductor-Current Waveform

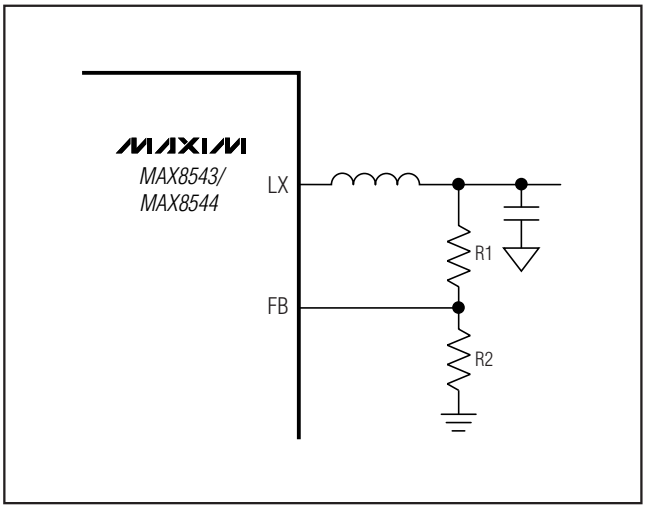


Figure 5. Setting the Output Voltage with a Resistor Voltage-Divider

Switching Frequency and Synchronization

The MAX8543/MAX8544 have an adjustable internal oscillator that can be set to any frequency from 200kHz to 1MHz. To set the switching frequency, connect a resistor from FSYNC to GND. Calculate the resistor value from the following equation:

$$R_{FSYNC} = \left(\frac{1}{2f_S} - 240ns\right)\left(\frac{1k\Omega}{14.18ns}\right)$$

The MAX8543/MAX8544 can also be synchronized to an external clock by connecting the clock signal to FSYNC. When using an external clock, select R_{FSYNC} such that the free-running frequency is within ±30% of the clock frequency. In addition, the MAX8544 has a synchronization output (SYNCO) that provides a clock signal that is 180° out-of-phase with the MAX8544 switching. SYNCO is used to synchronize a second controller 180° out-of-phase with the first by connecting SYNCO of the first controller to FSYNC of the second when the first controller operates in free-running mode. When the first controller is synchronized to an external clock, the external clock is inverted to generate SYNCO.

Power-Good Signal (POK)

POK is an open-drain output on the MAX8544 that monitors the output voltage. When the output is above 91% of its nominal regulation voltage, POK is high impedance. When the output drops below 91% of its nominal regulation voltage, POK is pulled low. POK is also pulled low when the MAX8544 is shut down. To use POK as a logic-level signal, connect a pullup resistor from POK to the logic-supply rail.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8543/MAX8544. When the junction temperature exceeds T_J = +160°C, an internal thermal sensor shuts down the device, allowing the IC to cool. The thermal sensor turns the IC on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

Design Procedure

Setting the Output Voltage

To set the output voltage for the MAX8543/MAX8544, connect FB to the center of an external resistor-divider from the output to GND (Figure 5). Select R2 between 8kΩ and 24kΩ; then calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.8V. R1 and R2 should be placed as close to the IC as possible.

Inductor Selection

There are several parameters that must be examined when determining which inductor is to be used: input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of peak-to peak inductor current ripple to maximum DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple.

A good compromise between size and efficiency is an LIR of 0.3. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard-value inductor close to the calculated value. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. This is especially true if the inductance is increased without also increasing the physical size of the inductor. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

Setting the Current Limits

Valley Current Limit

The valley current limit employs a current foldback scheme. The MAX8543 has a fixed valley current-limit threshold of 130mV, and a fixed foldback ratio (P_{FB}) of 23%. The foldback ratio is the current-limit threshold when the output is at 0V (output shorted to ground), divided by the threshold when the output is at its nominal regulated value. Thus, the minimum output current limit (I_{LIM}) and maximum short-circuit current (I_{SC}) is calculated as:

$$I_{LIM} = \frac{0.11V}{R_{DS(ON)}} + \frac{I_{P-P}}{2}$$

where $R_{DS(ON)}$ is the maximum on-resistance of the low-side MOSFET at the highest expected operating junction temperature, and I_{P-P} is the inductor ripple current, calculated as:

$$I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_S \times L \times V_{IN}}$$

Ensure that I_{LIM} is equal to or greater than the maximum load current at peak current limit (see the *Peak Current Limit* section):

$$I_{SC} = \frac{0.04V}{R_{DS(ON)}} + \frac{I_{P-P}}{2}$$

where 40mV is the maximum current-limit threshold when the output is shorted (V_{OUT} = 0V).

The MAX8544 has an adjustable valley current limit and can be selected for foldback with automatic recovery, or constant current with latch-up. To set the current limit for foldback mode, connect a resistor from ILIM2 to the output (R_{FOBK}), and another resistor from ILIM2 to GND (R_{ILIM}). See Figure 6. The values of R_{FOBK} and R_{ILIM} are calculated as follows:

1) First, select the percentage of foldback (P_{FB}). This percentage corresponds to the current limit when V_{OUT} equals zero, divided by the current limit when V_{OUT} equals a nominal voltage. A typical value of P_{FB} is in the range of 15% to 40%. A lower value of P_{FB} yields lower short-circuit current. The following equations are used to calculate R_{FOBK} and R_{ILIM}:

$$R_{FOBK} = \frac{P_{FB} \times V_{OUT}}{5\mu A \times (1 - P_{FB})}$$

$$R_{ILIM} = \frac{5 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB}) \times R_{FOBK}}{V_{OUT} - [5 \times R_{DS(ON)} \times I_{VALLEY} \times (1 - P_{FB})]}$$

where I_{VALLEY} is the value of the inductor valley current at maximum load ($I_{LOAD(MAX)}$ - 1/2 I_{P-P}), and $R_{DS(ON)}$ is the maximum on-resistance of the low-side MOSFET at the highest operating junction temperature.

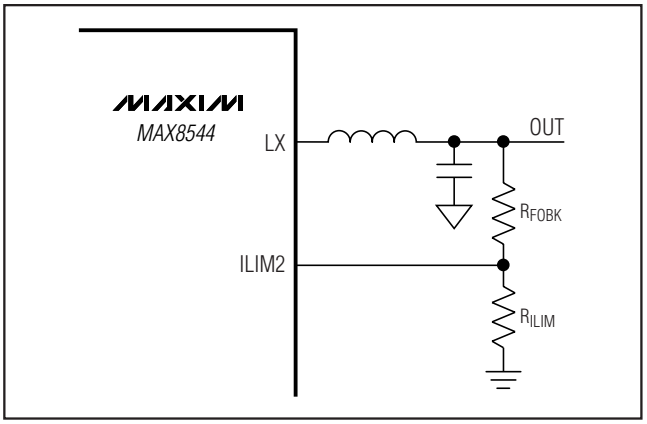


Figure 6. ILIM2 Resistor Connections

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

2) If the resulting value of R_{ILIM} is negative, either increase P_{FB} or choose a low-side MOSFET with a lower $R_{DS(ON)}$. The latter is preferred as it increases the efficiency and results in a lower short-circuit current.

To set the constant current limit for the latch-up mode, only R_{ILIM} is used. The equation for R_{ILIM} below sets the current-limit threshold at 1.2 times the maximum-rated output current:

$$R_{ILIM} = \frac{1.2 \times I_{VALLEY} \times R_{DS(ON)}}{1\mu A}$$

Similarly, I_{VALLEY} is the value of the inductor valley current at maximum load, $R_{DS(ON)}$ is the maximum on-resistance of the low-side MOSFET at the highest operating junction temperature.

Peak Current Limit

Peak inductor current-limit threshold (V_{TH}) has four possible settings through ILIM (MAX8543) or ILIM1 (MAX8544) as shown in Table 3 below. The resulting current limit is calculated as:

$$I_{LIM} = \frac{V_{TH}}{R_{DC}} - \frac{I_{P-P}}{2}$$

where R_{DC} is either the DC resistance of the inductor or the value of the optional current-sense resistor.

Note that V_{ILIM} is a logic-level setting, and can allow a variation of ±0.1 x V_{VL} without affecting V_{TH}. To ensure maximum output current, use the minimum value of V_{TH} from each setting, and the maximum R_{DC} values at the highest expected operating temperature. The DC resistance of the inductor's copper wire has a +0.22%/°C temperature coefficient.

Table 3. ILIM Current-Limit Threshold Settings

V_{ILIM}	RECOMMENDED ILIM CONNECTION	V_{TH} MIN (mV)	V_{TH} TYP (mV)	V_{TH} MAX (mV)
0	GND	38.5	50	56.5
1/3 V_{VL}	Voltage-divider: 100kΩ from ILIM/ILIM1 to GND 200kΩ from ILIM/ILIM1 to VL	85.0	100	115.0
2/3 V_{VL}	Voltage-divider: 200kΩ from ILIM/ILIM1 to GND 100kΩ from ILIM/ILIM1 to VL	127.5	150	172.5
V_{VL}	VL	170.0	200	230.0

To use the DC resistance of the output inductor for current sensing, an RC circuit is added (see Figure 7). The RC time constant is set to be twice the inductor (L / R_{DC}) time constant. Pick the value of R4 in the range of 470Ω to 2kΩ, and then calculate the capacitor value from: C9 = 2L / (R_{DC} × R4). Add a resistor (R5) equal in value to R4 to the CS- connection to minimize input-offset error. The equivalent current-sense resistance is equal to the DC resistance of the inductor (R_{DC}).

To use a current-sense resistor, connect the resistor as shown in Figure 8. Since most current-sense resistors have inductance, the RC circuit is also required and is calculated in the same manner as inductor current sensing. Place C11 close to CS+ and CS- pins to decouple the high-frequency noise pickup. Place C10 (same value as C9) across R5 to aid in short-circuit recovery.

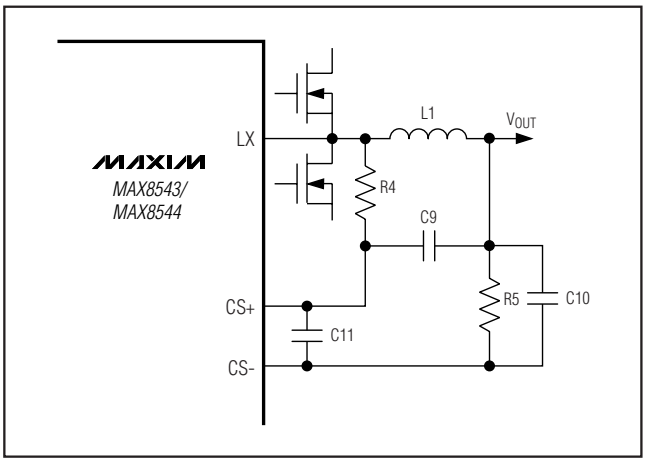


Figure 7. Inductor R_{DC} Current Sensing

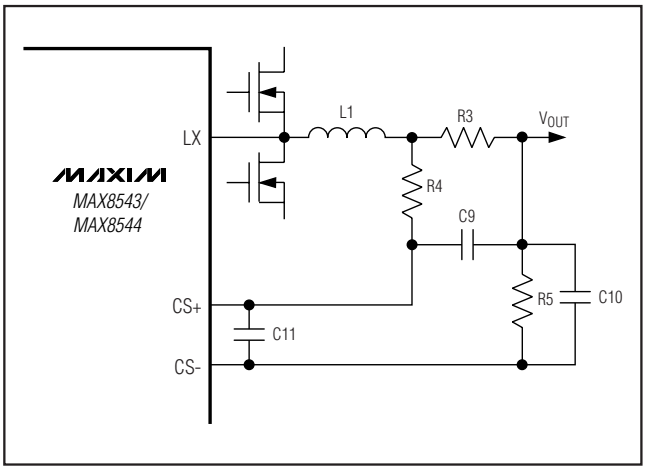


Figure 8. Using a Current-Sense Resistor

MOSFET Selection

The MAX8543/MAX8544 drive two or four external, logic-level, n-channel MOSFETs as the circuit switch elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better.
2) Maximum drain-to-source voltage (V_{DSS}): should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges (Q_G, Q_{GD}, Q_{GS}): the lower, the better.

For a 3.3V input application, choose a MOSFET with a rated $R_{DS(ON)}$ at V_{GS} = 2.5V. For a 5V input application, choose the MOSFETs with rated $R_{DS(ON)}$ at $V_{GS} \le 4.5V$. For a good compromise between efficiency and cost, choose the high-side MOSFET (N1, N2) that has conduction losses equal to the switching loss at nominal input voltage and output current. The selected low-side MOSFET (N3, N4) must have an $R_{DS(ON)}$ that satisfies the current-limit-setting condition above. Ensure that the low-side MOSFET does not spuriously turn on due to dV/dt caused by the high-side MOSFET turning on as this would result in shoot-through current and degrade the efficiency. MOSFETs with a lower Q_{GD} / Q_{GS} ratio have higher immunity to dV/dt. For high-current applications, it is often preferable to parallel two MOSFETs rather than to use a single large MOSFET.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for the low-side MOSFET, worst case is at $V_{IN(MAX)}$; for the high-side MOSFET, it could be either at $V_{IN(MAX)}$ or $V_{IN(MIN)}$). The high-side and low-side MOSFETs have different loss components due to the circuit operation. The low-side MOSFET operates as a zero-voltage switch; therefore, major losses are the channel-conduction loss (P_{LSCC}) and the body-diode conduction loss (P_{LSDC}):

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{LSDC} = 2 \times I_{LOAD} \times V_F \times t_{DT} \times f_S$$

where V_F is the body-diode forward-voltage drop, t_{DT} is the dead time between high-side and low-side switching transitions, and f_S is the switching frequency.

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel-conduction loss (P_{HSCC}), the VI overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current:

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}} \times f_S$$

where I_{GATE} is the average DH-driver output current capability determined by:

$$I_{GATE} \cong \frac{0.5 \times V_{VL}}{R_{DS(ON)(HS)} + R_{GATE}}$$

where $R_{DS(ON)(HS)}$ is the high-side MOSFET driver's on-resistance (1Ω, typ) and R_{GATE} is the internal gate resistance of the MOSFET (≈0.5Ω to 3Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DS(ON)(HS)}}$$

where $V_{GS} \approx V_{VL}$.

In addition to the losses above, allow about 20% more for additional losses due to MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET, but it is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFET, so be sure this does not overheat the MOSFET.

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MOSFET Snubber Circuit

Fast switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series RC snubber circuit is added across each switch. Below is the procedure for selecting the value of the series RC circuit.

Connect a scope probe to measure V_{LX} to GND and observe the ringing frequency, f_R.

Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3rd the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.

The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of the C_{PAR} to be effective. The power loss of the snubber circuit (P_{RSNUB}) is dissipated in the resistor and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD}\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD} / 2$. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency with relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability. Ceramic capacitors with an X5R or better temperature characteristic are recommended. When operating from a soft input source, an additional input capacitor (bulk bypass capacitor) may be required to prevent input from sagging.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and ESL caused by the current into and out of the capacitor. The maximum output voltage ripple is estimated as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN}}{L} \times ESL$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

where I_{P-P} is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit. As a general rule, a smaller current ripple results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output voltage ripple decreases with larger inductance, and increases with higher input voltages. Polymer, tantalum, or aluminum electrolytic capacitors are recommended.

The aluminum electrolytic capacitor is the least expensive; however, it has higher ESR. To compensate for this, use a ceramic capacitor in parallel to reduce the switching ripple and noise. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The response to a load transient depends on the selected output capacitors. After a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output voltage deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output voltage from further deviation from its regulation value.

Compensation Design

The MAX8543/MAX8544 use an internal transconductance error amplifier whose output compensates the control loop. The external inductor, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. Additionally, the compensation resistor and capacitors are selected to optimize control-loop stability. The component values, shown in the *Typical Application Circuits* (Figures 1 and 2), yield stable operation over the given range of input-to-output voltages.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, so the MAX8543/MAX8544 use the voltage drop across the DC resistance of the inductor or the alternate series current-sense resistor to measure the inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring a less elaborate error-amplifier compensation than voltage-mode control. A simple single series R_C and C_C is all that is needed to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor (C_F) from COMP to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has DC gain set by g_{mc} x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. Below are equations that define the power modulator:

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + (f_S \times L)}$$

where $R_{LOAD} = V_{OUT} / I_{OUT(MAX)}$, f_S is the switching frequency, L is the output inductance, and $g_{mc} = 1 / (A_{VCS} \times R_{DC})$, where A_{VCS} is the gain of the current-sense amplifier and R_{DC} is the DC resistance of the inductor (or current-sense resistor). A_{VCS} is dependent on the current-limit selection at ILIM, and ranges from 3 to 11 (see Current-Sense Amplifier Voltage Gain in the *Electrical Characteristics* table).

The frequencies at which the pole and zero created by the power modulator are determined as follows:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + (f_S \times L)} + ESR \right)}$$

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)} / n$. Note that the capacitor zero for a parallel combination of like capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $G_{FB} = V_{FB} / V_{OUT}$, where V_{FB} is equal to 0.8V.

The transconductance error amplifier has a DC gain, $G_{EA(DC)} = g_{mEA} \times R_O$, where g_{mEA} is the error-amplifier transconductance, which is equal to 110µS, R_O is the output resistance of the error amplifier, which is 10MΩ. A dominant pole is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and a zero is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole set by C_F and R_C to cancel the output-capacitor ESR zero if it occurs near the crossover frequency (f_C). Thus:

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The crossover frequency, f_C, should be much higher than the power-modulator pole f_{PMOD}. Also, f_C should be less than or equal to 1/5th the switching frequency. Select a value for f_C in the range:

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

$$G_{EA(fc)} \times G_{MOD(fc)} \times \frac{V_{FB}}{V_{OUT}} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$G_{EA(fc)} = g_{mEA} \times R_C$$

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

then R_C can be calculated as:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(fc)}}$$

where g_{mEA} = 110µS.

The error-amplifier compensation zero formed by R_C and C_C should be set at the modulator pole f_{PMOD}. C_C is calculated by:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + (f_S \times L)\right) \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor C_F from COMP to GND. The value of C_F is calculated as follows:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$G_{EA(fc)} = g_{mEA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

R_C is calculated as:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times G_{MOD(fc)} \times f_{zMOD}}$$

where g_{mEA} = 110µS.

C_C is calculated from:

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + (f_S \times L)\right) \times R_C}$$

C_F is calculated from:

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

Below is a numerical example to calculate R_C and C_C values of the typical operating circuit of Figure 1 (MAX8544):

A_{VCS} = 11 (for ILIM1 = GND)

R_{DC} = 2.5mΩ

g_{mc} = 1 / (A_{VCS} x R_{DC}) = 1 / (11 x 0.0025) = 36.7S

V_{OUT} = 2.5V

$I_{OUT(MAX)}$ = 15A

R_{LOAD} = V_{OUT} / $I_{OUT(MAX)}$ = 2.5 / 15 = 0.167Ω

C_{OUT} = 360µF

ESR = 5mΩ

$$G_{MOD(dc)} = g_{mc} \times \frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + (f_S \times L)}$$

$$= 36.36 \frac{0.167 \times (600 \times 10^3) \times \left(0.8 \times 10^{-6}\right)}{0.167 + (600 \times 10^3) \times \left(0.8 \times 10^{-6}\right)} = 4.50$$

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{R_{LOAD} \times f_S \times L}{R_{LOAD} + f_S \times L} + ESR\right)}$$

$$= \frac{1}{2\pi \times (360 \times 10^{-6}) \times \left(\frac{0.167 \times (600 \times 10^3) \times \left(0.8 \times 10^{-6}\right)}{0.167 + (600 \times 10^3) \times \left(0.8 \times 10^{-6}\right)} + 0.005\right)} = 3.43kHz$$

$$f_{pMOD} << f_C \le \frac{f_S}{5}$$

3.43kHz << f_C ≤ 120kHz; select f_C = 120kHz.

$$f_{zMOD} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

$$= \frac{1}{2\pi \times (360 \times 10^{-6}) \times 0.005} = 88.4kHz$$

Since $f_{zMOD} < f_C$:

$$G_{MOD(fc)} = G_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

$$= 4.5 \times \frac{3.43 \times 10^3}{88.4 \times 10^3} = 0.175$$

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{f_C}{g_{mEA} \times G_{MOD(fc)} \times f_{zMOD}}$$

$$= \frac{2.5}{0.8} \times \frac{120 \times 10^3}{(110 \times 10^{-6}) \times 0.175 \times (88.4 \times 10^3)} = 220k\Omega$$

$$C_C = \frac{R_{LOAD} \times f_S \times L \times C_{OUT}}{\left(R_{LOAD} + f_S \times L\right) \times R_C}$$

$$= \frac{0.167(600 \times 10^3)(0.8 \times 10^{-6})(360 \times 10^{-6})}{\left(0.167 + (600 \times 10^3)(0.8 \times 10^{-6})\right)(220 \times 10^3)} = 202pF$$

Select the nearest standard value: C_C = 220pF

$$C_F = \frac{1}{2\pi \times R_C \times f_{zMOD}}$$

$$= \frac{1}{2\pi \times (220 \times 10^3) \times (88.4 \times 10^3)} = 8.2pF$$

Select the nearest standard value: C_F = 10pF:

R3 = R_C = 220kΩ

C8 = C_C = 220pF

C7 = C_F = 10pF

Applications Information

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place IC decoupling capacitors as close to IC pins as possible. Keep separate the power ground plane and the signal ground plane. Place the input ceramic decoupling capacitor directly across and as close as possible to the high-side MOSFET's drain and the low-side MOSFET's source. This is to help contain the high switching current within this small loop.
2) For output current greater than 10A, a four-layer PC board is recommended. Pour a signal ground plane in the second layer underneath the IC to minimize noise coupling.
3) Connect input, output, snubber, and VL capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
4) Place the inductor current-sense resistor and capacitor as close to the inductor as possible. Make a Kelvin connection to minimize the effect of PC board trace resistance. Place the input bias balance resistor and bypass capacitor (R5 and C10 in Figures 7 and 8) near CS-. Run two closely parallel traces from across the capacitor (C9 in Figures 7 and 8) to CS+ and CS-. Place the decoupling capacitor C11 close to CS+ and CS- pins.
5) Place the MOSFET as close as possible to the IC to minimize trace inductance of the gate-drive loop. If parallel MOSFETs are used, keep the trace lengths to both gates equal.
6) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for recommended copper area.
7) Place the feedback and compensation components as close to the IC pins as possible. Connect the feedback-divider resistor from FB to the output as close as possible to the farthest output capacitor.

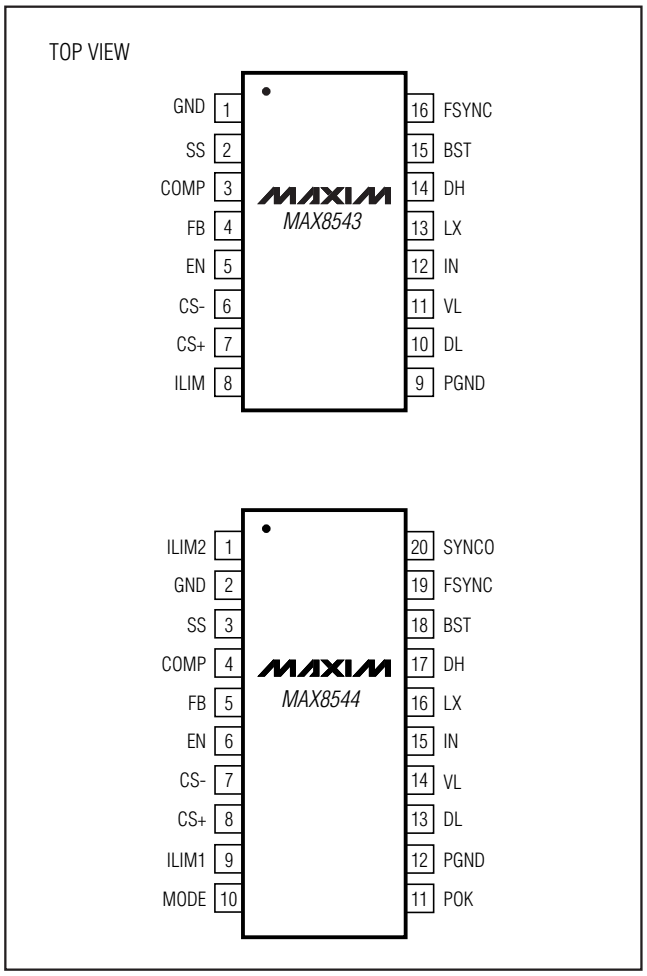
Refer to the MAX8544 evaluation kit for an example layout.

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

Table 4. Suggested Component Manufacturers

MANUFACTURER	COMPONENT	WEBSITE	PHONE
Central Semiconductor	Diodes	www.centralsemi.com	631-435-1110
Coilcraft	Inductors	www.coilcraft.com	800-322-2645
International Rectifier	MOSFETs	www.irf.com	310-322-3331
Kamaya	Resistors	www.kamaya.com	260-489-1533
Panasonic	Capacitors	www.panasonic.com	714-373-7366
Sanyo	Capacitors	www.sanyo.com	619-661-6835
Sumida	Inductors	www.sumida.com	847-956-0666
Taiyo Yuden	Capacitors	www.t-yuden.com	408-573-4150
TDK	Capacitors	www.component.tdk.com	847-803-6100
Vishay/Siliconix	MOSFETs	www.vishay.com	402-564-3131

Pin Configurations



Chip Information

TRANSISTOR COUNT: 4185

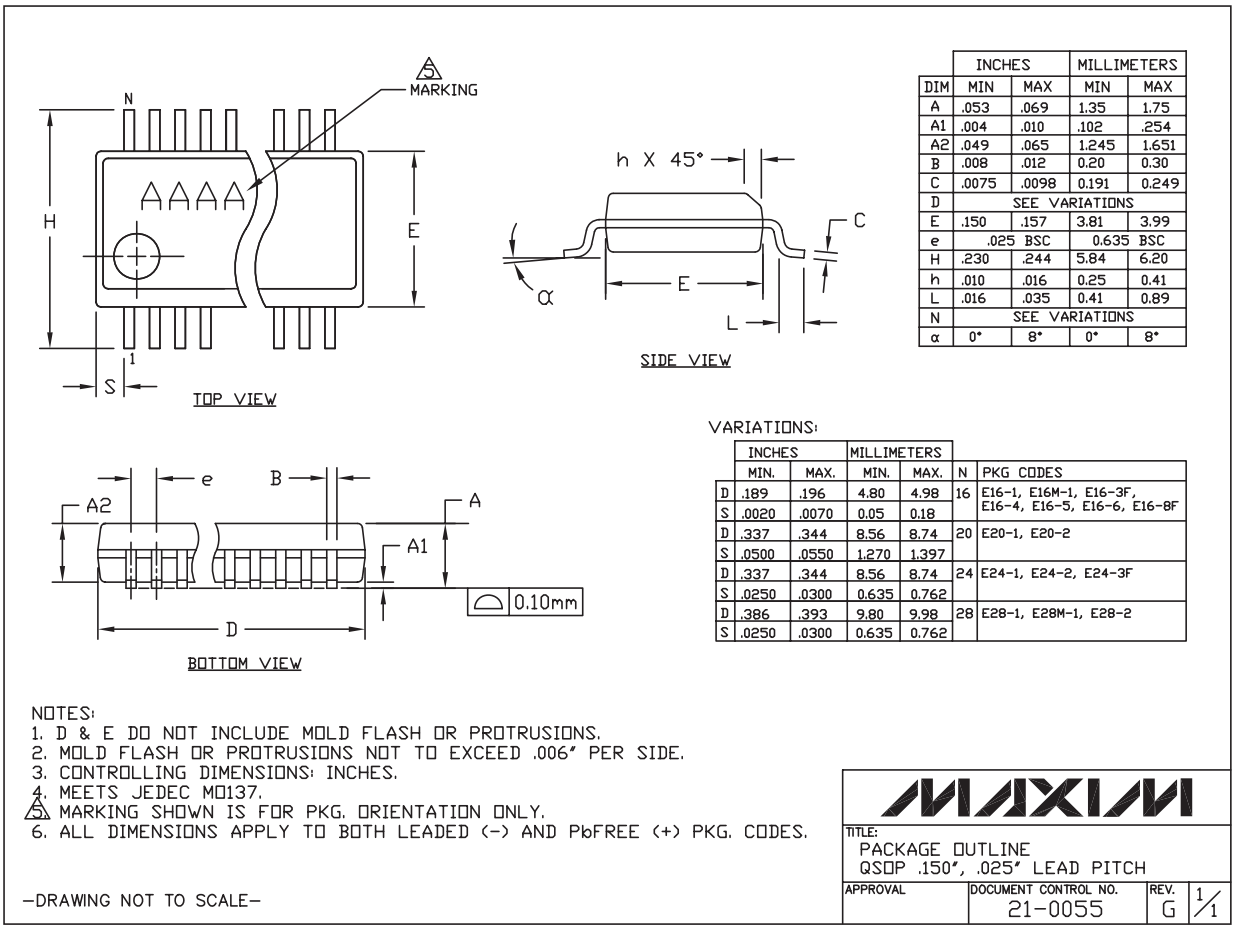
PROCESS: BiCMOS

Step-Down Controllers with Prebias Startup, Lossless Sensing, Synchronization, and OVP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-3F, E16-4, E16-5, E16-6, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3F
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE: PACKAGE OUTLINE QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	G	1/1

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