

Structure Silicon Monolithic Integrated Circuit

Product 1 Channel Step-down Switching Regulator

Type **BD9701FP、BD9701T、BD9701T-V5、BD9701CP-V5**

Function

- Maximum Switching Current 1.5A
- Possible to adjust Output voltage according to external resistor (SW frequency:100kHz)

○Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings		Unit
Supply Voltage (VCC-GND)	VCC	36		V
STBY-GND	V <sub>STBY</sub>	36		V
OUT-GND	V <sub>OUT</sub>	36		V
INV-GND	V <sub>INV</sub>	10		V
Power Dissipation	Pd	TO252	800 <sup>*1</sup>	mW
		TO220	2000 <sup>*2</sup>	
Maximum Switching Current	I <sub>OUT</sub>	1.5 <sup>*3</sup>		A
Operating Temperature	Topr	-40~+85		°C
Storage Temperature	Tstg	-55~+150		°C
Maximum Junction Temperature	Tjmax	150		°C

\*1 Reduced by 6.4mW/°C over 25°C, when mounted on PCB (70×70×1.6tmm).

\*2 With no external heat sink, the power dissipation reduces by 16.0mW/°C over 25°C.  
Reduced by 17.6mW/°C, when mounted on Infinity size heatsink.

\*3 Don't exceed Pd, ASO and Tjmax=150°C.

○Recommended Operating Conditions (Ta=-25~+75°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Input Voltage	VCC	8.0 or Vo+3 <sup>*4</sup>	-	35.0	V
Output Voltage	Vo	1.0	-	32	V

\*4 The minimum value of an input voltage is the higher either 8.0V or Vo+3

Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version.

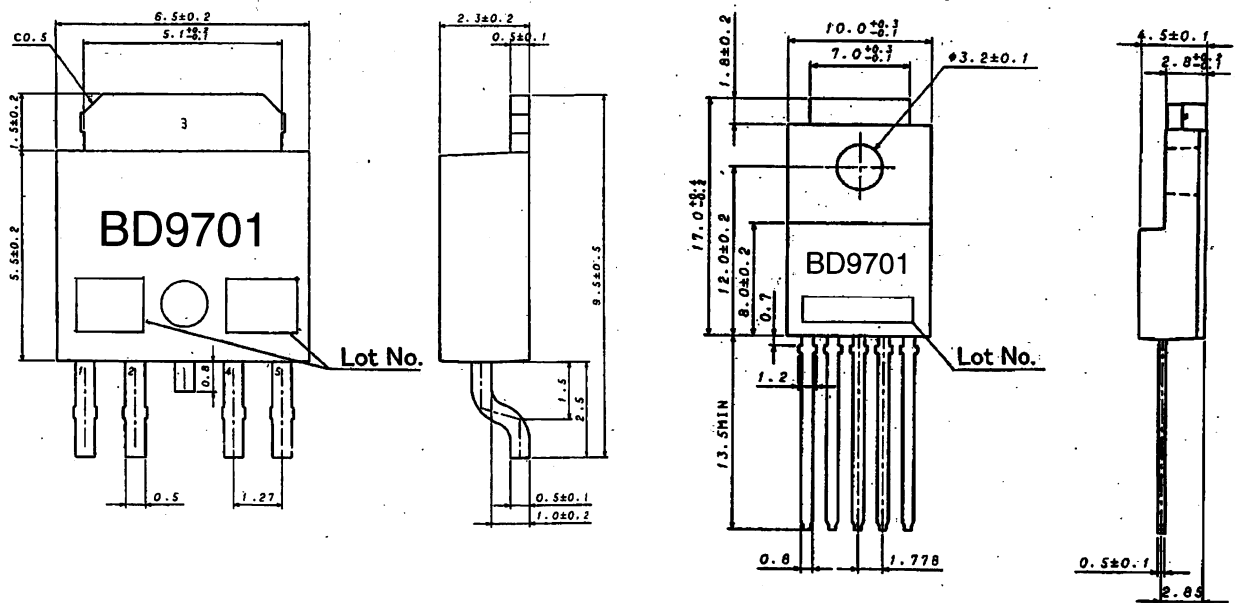
If there is any uncertainty in translation version of this document, official version takes priority.

○Electrical Characteristics (Unless otherwise noted, Ta=25°C, Vcc=12V, Vo=5V, STBY=3V)

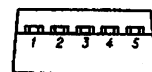
Parameter	Symbol	Limit			Unit	Conditions	
		MIN	TYP	MAX			
Output MOS ON Resistor	Ron	-	1.0	1.5	Ω	Design Guarantee	
Efficiency	η	-	86	-	%	Io=0.5A Design Guarantee	
Switching Frequency	fosc	80	100	120	kHz		
Load Regulation	ΔVOLOAD	-	10	40	mV	Vcc=20V, Io=0.5~1.5A	
Line Regulation	ΔVOLINE	-	40	100	mV	Vcc=10~30V, Io=1.0A	
Over Current Protection Limit	Iocp	1.6	-	-	A		
INV pin Threshold Voltage	VINV	0.98	1.00	1.02	V		
INV pin Threshold Voltage temperature Fluctuation	ΔVINV	-	±0.5	-	%	Tj=0~85°C Design Guarantee	
INV pin input current	IINV	-	1	-	μA	VINV=1.0V	
STBY pin Threshold Voltage	ON	VSTBYON	2.0	-	36	V	
	OFF	VSTBYOFF	-0.3	-	0.3	V	
STBY pin input Current	Istby	5	25	50	μA	STBY=3V	
Circuit Current	Icc	-	4	12	mA		
Stand-by Current	Ist	-	0	5	μA	STBY=0V	

○This product is not design for normal operation with in a radio active environment

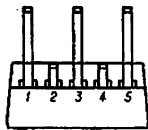
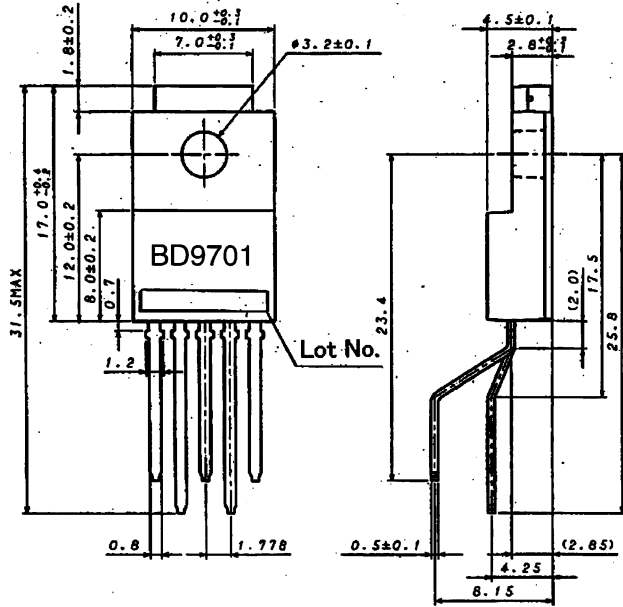
○Package Dimensions



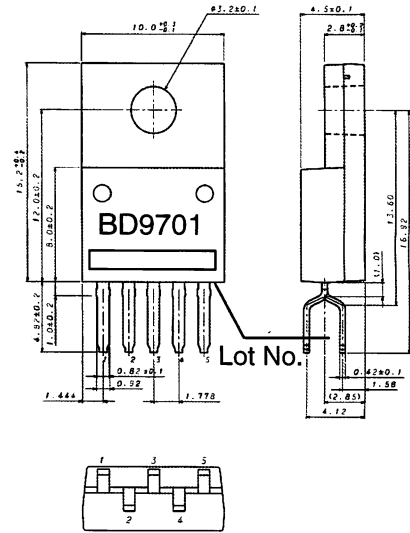
TO252-5 (Unit : mm)



TO220FP-5 (Unit : mm)

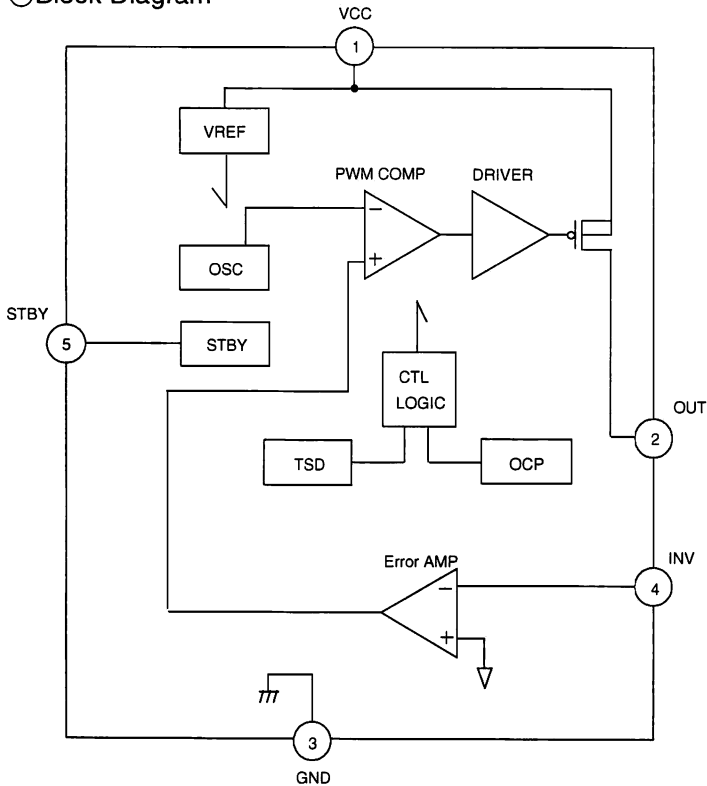


TO220FP-5(V5) (Unit : mm)



TO220CP-V5 (Unit : mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Function
1	VCC	Input Power Supply Pin
2	OUT	Internal Pch FET Drain Pin
3	GND	Ground
4	INV	Output Voltage Feedback Pin
5	STBY	ON/OFF Control Pin

○ Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

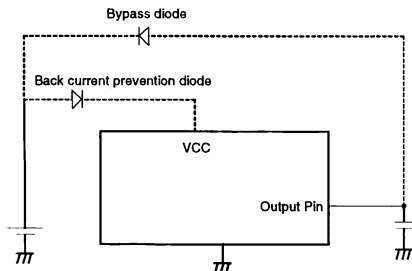
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) IC pin input

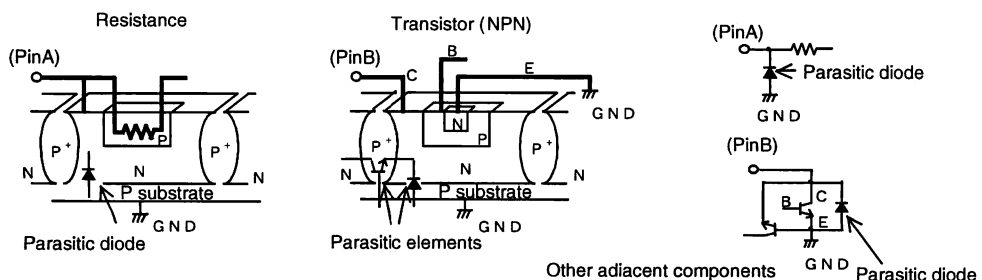
This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.

P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins as shown in Fig. 10,

- the P/N junction functions as a parasitic diode when  $GND > (Pin A)$  for the resistor or  $GND > (Pin B)$  for the transistor (NPN).
- Similarly, when  $GND > (Pin B)$  for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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