19-2992; Rev 1; 9/10

EVALUATION KIT AVAILABLE

16-QSOP 6mm x 4.9mm

3A, 1MHz, 1% Accurate, Internal Switch Step-Down Regulator with Power-OK

General Description

The MAX8505 step-down regulator operates from a 2.6V to 5.5V input and generates an adjustable output voltage from 0.8V to 0.85 × VIN at up to 3A. With a 2.6V to 5.5V bias supply, the input voltage can be as low as 2.25V.

The MAX8505 integrates power MOSFETs and operates at 1MHz/500kHz switching frequency to provide a compact design. Current-mode pulse-width-modulated (PWM) control simplifies compensation with ceramic or polymer output capacitors and provides excellent transient response.

The MAX8505 features 1% accurate output over load, line, and temperature variations. Adjustable soft-start is achieved with an external capacitor. During the soft-start period, the voltage-regulation loop is active. This limits the voltage dip when the active devices, such as microprocessors or ASICs connected to the MAX8505's output, apply a sudden load current step upon passing their undervoltage thresholds.

The MAX8505 features current-limit, short-circuit, and thermal-overload protection and enables a rugged design. Open-drain power-OK (POK) monitors the output voltage.

Applications

µP/ASIC/DSP/FPGA Core and I/O Supplies

Chipset Supplies

Server, RAID, and Storage Systems

Network and Telecom Equipment

Features

- **Saves Space—4.9mm x 6mm Footprint, 1µH Inductor, 47µF Ceramic Output Capacitor**
- **Input Voltage Range**
  2.6V to 5.5V
  Down to 2.25V with Bias Supply
- **0.8V to 0.85 × V_{IN}, 3A Output**
- **Ceramic or Polymer Capacitors**
- **±1% Output Accuracy Over Load, Line, and Temperature**
- **Fast Transient Response**
- **Adjustable Soft-Start**
- **In-Regulation Soft-Start Limits Output-Voltage Dips at Power-On**
- **POK Monitors Output Voltage**

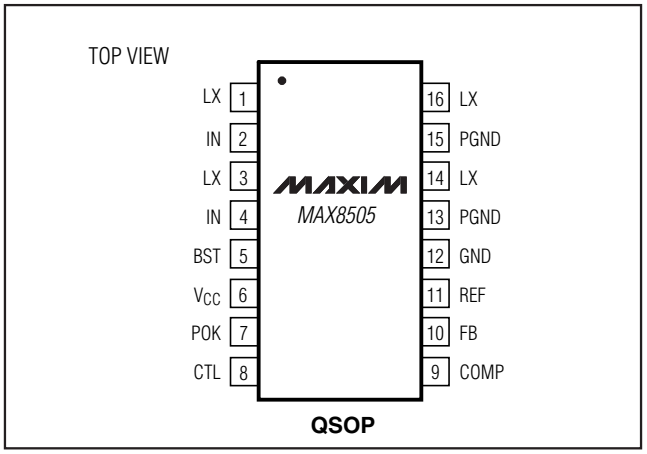
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8505EEE+	-40°C to +85°C	16 QSOP

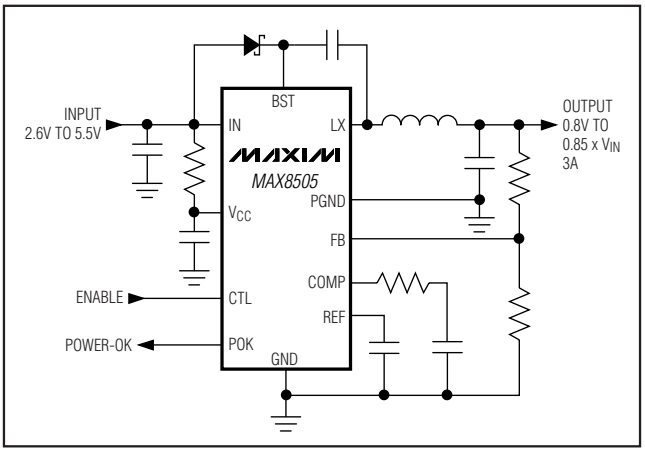
+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram appears at end of data sheet.

Pin Configuration



Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3A, 1MHz, 1% Accurate, Internal Switch Step-Down Regulator with Power-OK

ABSOLUTE MAXIMUM RATINGS

CTL, FB, IN, V_{CC} to GND .....-0.3V to +6V
COMP, REF, POK to GND.....-0.3V to (V_{CC} + 0.3V)
BST to LX.....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 12.5mW/°C above +70°C).....1000mW

Operating Temperature Range
MAX8505EEE.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = V_{CTL} = +3.3V, V_{FB} = 0.8V, V_{COMP} = 1.25V, C_{REF} = 0.01µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN AND V_{CC}							
IN Voltage Range	V_{IN}			2.25		V_{CC}	V
V_{CC} Voltage Range	V_{CC}			2.6		5.5	V
IN Supply Current	I_{IN}	Switching with no load	V_{IN} = 3.3V		6	10	mA
			V_{IN} = 5.5V		10		
V_{CC} Supply Current	I_{CC}	Switching with no load	V_{CC} = 3.3V		3	10	mA
			V_{CC} = 5.5V		6		
Total Shutdown Current into IN and V_{CC}	I_{SHDN}	V_{IN} = V_{CC} = V_{BST} - V_{LX} = 5.5V, V_{CTL} = 0V, V_{LX} = 0V			20	50	µA
V_{CC} Undervoltage Lockout Threshold	$UVLO_{th}$	When LX starts/stops switching	V_{CC} rising		2.40	2.55	V
			V_{CC} falling	2.2	2.35		
REF							
REF Voltage	V_{REF}	I_{REF} = 0µA, V_{IN} = V_{CC} = 2.6V to 5.5V		0.792	0.800	0.808	V
REF Shutdown Resistance		From REF to GND, V_{CTL} = 0V			13	100	Ω
REF Soft-Start Current		V_{REF} = 0.4V		20	25	30	µA
Soft-Start Ramp Time		Output from 0% to 100%, C_{REF} = 0.01µF to 1µF			32		ms/µF
FB							
FB Regulation Voltage		V_{IN} = 2.6V to 5.5V		0.792	0.800	0.808	V
FB Input Bias Current		V_{FB} = 0.7V			0.01	0.1	µA
Maximum Output Current	I_{OUT_MAX}	V_{IN} = V_{CC} = 3.3V, V_{OUT} = 1.2V, L = 1µH/5.9mΩ (Note 1)		3			A
FB Threshold for POK Transition		FB rising or falling	FB high	10.5	12	13.5	%
			FB low	-13.5	-12	-10.5	
FB to POK Delay		FB rising or falling			50		µs
COMP							
COMP Transconductance		From FB to COMP		60	100	160	µS
Gain from FB to COMP		V_{COMP} = 1.25V to 1.75V			80		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL} = +3.3V, V_{FB} = 0.8V, V_{COMP} = 1.25V, C_{REF} = 0.01µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMP Clamp Voltage, Low		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V, V_{FB} = 0.9V		0.45	0.75	1.00	V
COMP Clamp Voltage, High		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V, V_{FB} = 0.7V		1.7	1.9	2.1	V
COMP Shutdown Resistance		From COMP to GND, V_{CTL} = 0V			13	100	Ω
LX (All LX Outputs Connected Together)							
LX On-Resistance, High		V_{IN} = V_{BST} - V_{LX} = 3.3V			38	74	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.6V			42		
LX On-Resistance, Low		V_{IN} = V_{BST} - V_{LX} = 3.3V			38	74	mΩ
		V_{IN} = V_{BST} - V_{LX} = 2.6V			42		
LX Current-Sense Transresistance	R_T	From LX to COMP		0.068	0.086	0.104	Ω
LX Current-Limit Threshold		Sourcing, *Typical Application Circuit*		4.6	5.6	6.6	A
		Sinking, V_{IN} = V_{CC} = 2.6V to 5.5V		-4.3	-2.6	-1.0	
LX Leakage Current		V_{IN} = V_{CC} = 5.5V, V_{CTL} = 0V	V_{LX} = 5.5V			100	µA
			V_{LX} = 0V	-100			
LX Switching Frequency		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	V_{CTL} = V_{CC}	0.85	1	1.15	MHz
			V_{CTL} = 2/3V_{CC}	0.44	0.5	0.56	
LX Minimum Off-Time		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V		95	110	135	ns
LX Maximum Duty Cycle		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	500kHz	90	94		%
			1MHz	84	89		
LX Minimum Duty Cycle		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	500kHz		5	8	%
			1MHz		10	15	
SLOPE COMPENSATION							
Slope Compensation		Extrapolated to 100% duty cycle		245	300	400	mV
BST							
BST Shutdown Supply Current		(V_{BST} - V_{LX}) = V_{IN} = V_{CC} = 5.5V, V_{CTL} = 0V	V_{LX} = 5.5V			10	µA
			V_{LX} = 0V			10	
			LX open			10	
CTL							
CTL Input Threshold		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	For 1MHz	80			% of V_{CC}
			For 500kHz	55		70	
			For shutdown			45	
CTL Input Current		V_{CTL} = 0V or 5.5V, V_{IN} = V_{CC} = 5.5V		-1		+1	µA
POK (Power-OK)							
POK Output Voltage, Low		V_{FB} = 0.6V or 1.0V, I_{POK} = 2mA			25	100	mV
POK Leakage Current		V_{POK} = 5.5V			0.001	1	µA
POK Fault Delay Time		From FB to POK, any threshold		25	50	100	µs
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold		When LX stops switching	T_J rising		+170		°C
Thermal-Shutdown Hysteresis					20		°C

3A, 1MHz, 1% Accurate, Internal Switch Step-Down Regulator with Power-OK

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = V_{CTL} = +3.3V, V_{FB} = 0.8V, V_{COMP} = 1.25V, C_{REF} = 0.01µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN AND V_{CC}							
IN Voltage Range	V_{IN}			2.25		V_{CC}	V
V_{CC} Voltage Range				2.6		5.5	V
IN Supply Current	I_{IN}	Switching with no load	V_{IN} = 3.3V			10	mA
V_{CC} Supply Current	I_{CC}	Switching with no load	V_{CC} = 3.3V			10	mA
Total Shutdown Current into IN and V_{CC}	I_{SHDN}	V_{IN} = V_{CC} = V_{BST} - V_{LX} = 5.5V, V_{CTL} = 0V, V_{LX} = 0V				50	µA
V_{CC} Undervoltage Lockout Threshold	$UVLO_{th}$	When LX starts/stops switching	V_{CC} rising			2.55	V
			V_{CC} falling	2.2			
REF							
REF Voltage	V_{REF}	I_{REF} = 0µA, V_{IN} = V_{CC} = 2.6V to 5.5V		0.791		0.808	V
REF Shutdown Resistance		From REF to GND, V_{CTL} = 0V				100	Ω
REF Soft-Start Current		V_{REF} = 0.4V		20		30	µA
FB							
FB Regulation Voltage	V_{FB}	V_{IN} = 2.6V to 5.5V		0.791		0.808	V
FB Input Bias Current		V_{FB} = 0.7V				0.1	µA
Maximum Output Current	I_{OUT_MAX}	V_{IN} = V_{CC} = 3.3V, V_{OUT} = 1.2V, L = 1µH/5.9mΩ (Note 1)		3			A
FB Threshold for POK Transition		FB rising or falling	FB high	10.5		13.5	%
			FB low	-13.5		-10.5	
COMP							
COMP Transconductance		From FB to COMP		60		160	µS
COMP Clamp Voltage, Low		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V, V_{FB} = 0.9V		0.45		1.00	V
COMP Clamp Voltage, High		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V, V_{FB} = 0.7V		1.7		2.1	V
COMP Shutdown Resistance		From COMP to GND, V_{CTL} = 0V				100	Ω
LX (All LX Outputs Connected Together)							
LX On-Resistance, High		V_{IN} = V_{BST} - V_{LX} = 3.3V				74	mΩ
LX On-Resistance, Low		V_{IN} = V_{BST} - V_{LX} = 3.3V				74	mΩ
LX Current-Sense Transresistance	R_T	From LX to COMP		0.068		0.104	Ω
LX Current-Limit Threshold		Sourcing, *Typical Application Circuit*		4.6		5.6	A
		Sinking, V_{IN} = V_{CC} = 2.6V to 5.5V		-4.3		-1.0	
LX Leakage Current		V_{IN} = V_{CC} = 5.5V, V_{CTL} = 0V	V_{LX} = 5.5V			100	µA
			V_{LX} = 0V	-100			
LX Switching Frequency		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	V_{CTL} = V_{CC}	0.85		1.15	MHz
			V_{CTL} = 2/3 × V_{CC}	0.44		0.56	
LX Minimum Off-Time		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V		95		135	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = V_{CTL} = +3.3V, V_{FB} = 0.8V, V_{COMP} = 1.25V, C_{REF} = 0.01µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Maximum Duty Cycle		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	500kHz	90			%
			1MHz	84			
LX Minimum Duty Cycle		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	500kHz			8	%
			1MHz			15	
SLOPE COMPENSATION							
Slope Compensation		Extrapolated to 100% duty cycle		245		406	mV
BST							
BST Shutdown Supply Current		(V_{BST} - V_{LX}) = V_{IN} = V_{CC} = 5.5V, V_{CTL} = 0V	V_{LX} = 5.5V			10	µA
			V_{LX} = 0V			10	
			LX open			10	
CTL							
CTL Input Threshold		V_{IN} = V_{CC} = 2.6V, 3.3V, 5.5V	For 1MHz	80			% of V_{CC}
			For 500kHz	55		70	
			For shutdown			45	
CTL Input Current		V_{CTL} = 0V or 5.5V, V_{IN} = V_{CC} = 5.5V		-1		+1	µA
POK (Power-OK)							
POK Output Voltage, Low		V_{FB} = 0.6V or 1.0V, I_{POK} = 2mA				100	mV
POK Leakage Current		V_{POK} = 5.5V				1	µA
POK Fault Delay Time		From FB to POK, any threshold		25		100	µs

Note 1: Under normal operating conditions, COMP moves between 1.25V and 2.15V as the duty cycle changes from 10% to 90% and peak inductor current changes from 0 to 3A. Maximum output current is related to peak inductor current, inductor value input voltage, and output voltage by the following equations:

$$I_{OUT\_MAX} = \frac{I_{LIM} - (1-D) \times t_S \times V_{OUT} / 2L}{1 + (1-D) \times t_S \times (R_{NLS} + R_L) / 2L}$$

where V_{OUT} = output voltage; I_{LIM} = current limit of high-side switch; t_S = switching period; R_L = ESR of inductor; R_{NLS} = on-resistance of low-side switch; L = inductor. Equations for I_{LIM} and D are shown as follows:

$$I_{LIM} = I_{LIM\_DC100} + V_{SW} \frac{1-D}{R_T}$$

where I_{LIM_DC100} = current limit at D = 100%; R_T = transresistance from LX to COMP; V_{SW} = slope compensation (310mV ±20%); D = duty cycle:

$$D = \frac{V_{OUT} + I_O(R_{NLS} + R_L)}{V_{IN} + I_O(R_{NLS} - R_{NHS})}$$

where V_{OUT} = output voltage; V_{IN} = input voltage; I_O = output current; R_L = ESR of inductor; R_{NHS} = on-resistance of high-side switch; R_{NLS} = on-resistance of low-side switch. See the *Typical Application Circuit* for external components.

Note 2: Specifications to -40°C are guaranteed by design and not production tested.

Note 3: LX has internal clamp diodes to PGND and IN pins 2 and 4. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

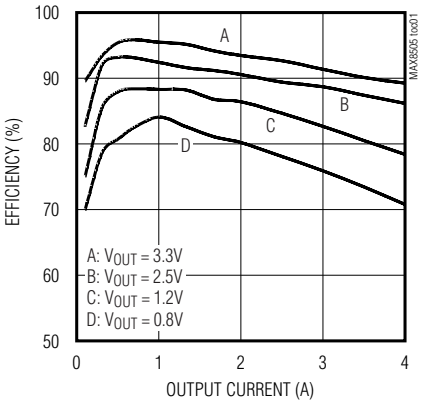
Note 4: When connected together, the LX output is designed to provide 3.5A_{RMS} current.

3A, 1MHz, 1% Accurate, Internal Switch Step-Down Regulator with Power-OK

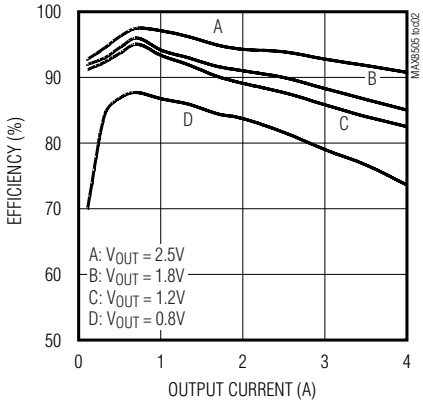
Typical Operating Characteristics

(Typical values are at V_{IN} = V_{CC} = V_{CTL} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, and T_A = +25°C, unless otherwise noted.)

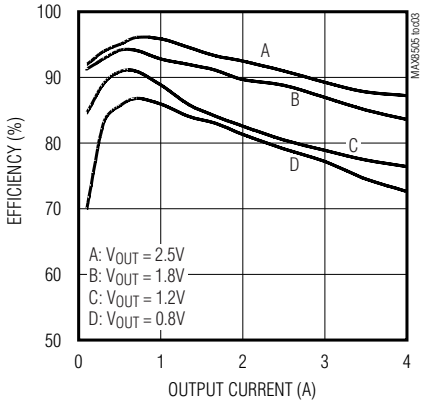
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = V_{CC} = 5V, f_{SW} = 1MHz)



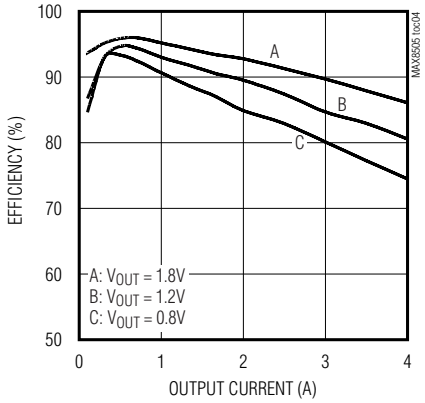
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = V_{CC} = 3.3V, f_{SW} = 500kHz)



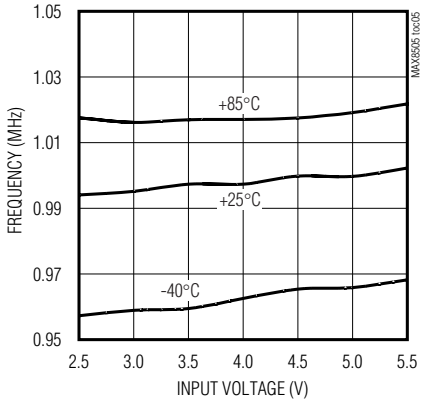
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = V_{CC} = 3.3V, f_{SW} = 1MHz)



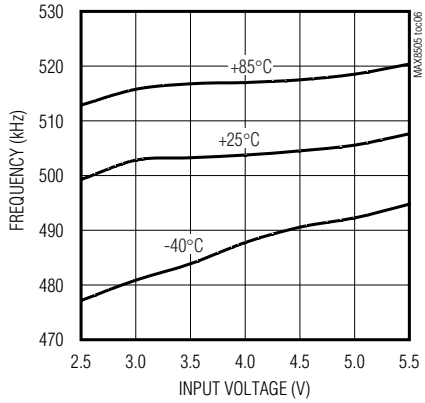
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 2.5V, V_{CC} = 5V, f_{SW} = 1MHz)



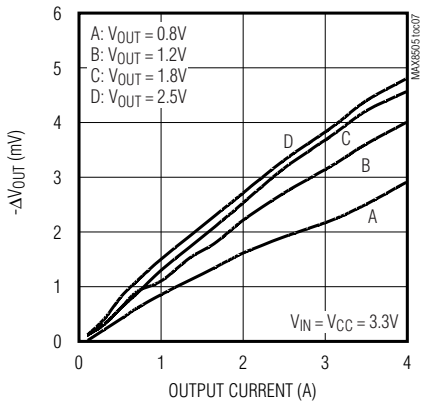
FREQUENCY vs. INPUT VOLTAGE AND TEMPERATURE



FREQUENCY vs. INPUT VOLTAGE AND TEMPERATURE



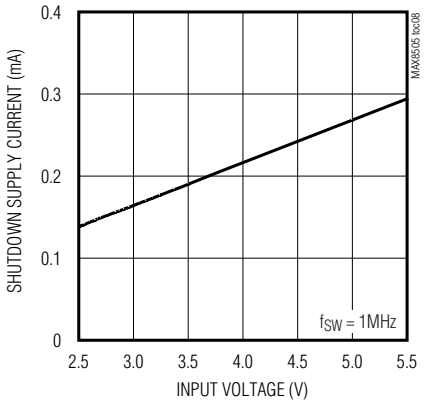
OUTPUT LOAD REGULATION



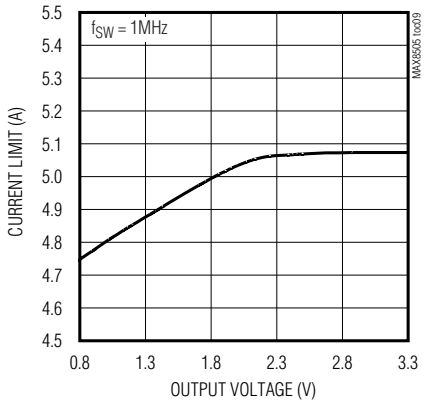
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{CC} = V_{CTL} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, and T_A = +25°C, unless otherwise noted.)

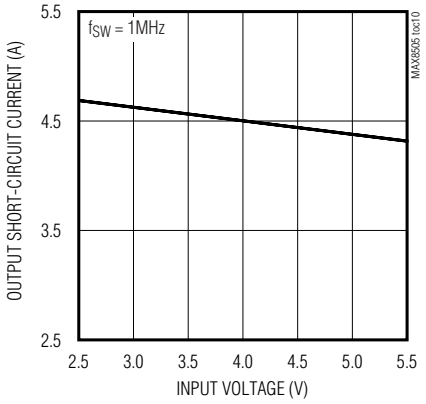
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



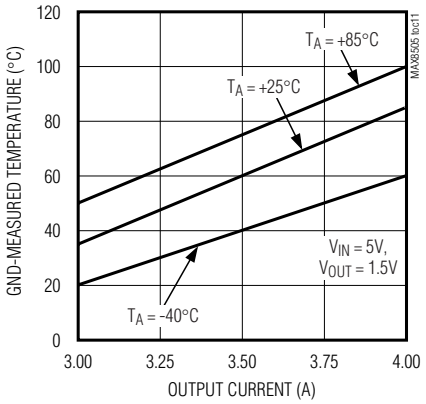
CURRENT LIMIT vs. OUTPUT VOLTAGE



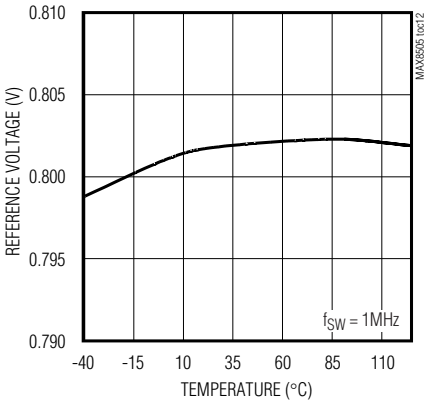
OUTPUT SHORT-CIRCUIT CURRENT vs. INPUT VOLTAGE



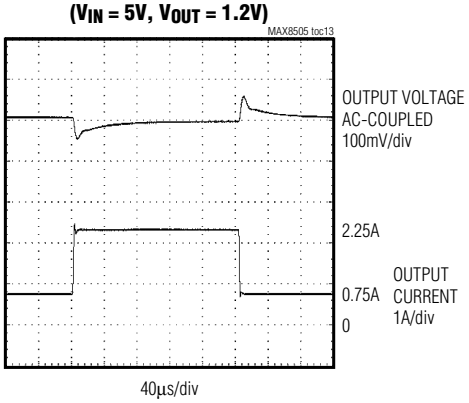
GND-MEASURED TEMPERATURE vs. OUTPUT CURRENT



REFERENCE VOLTAGE vs. TEMPERATURE



TRANSIENT RESPONSE (V_{IN} = 5V, V_{OUT} = 1.2V)

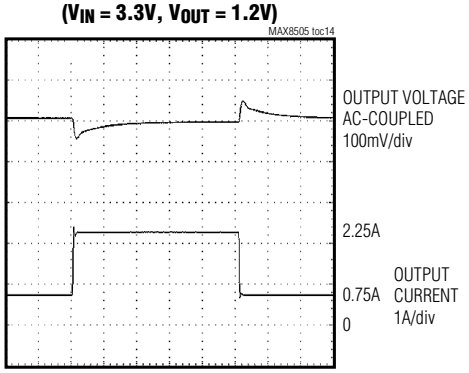


3A, 1MHz, 1% Accurate, Internal Switch Step-Down Regulator with Power-OK

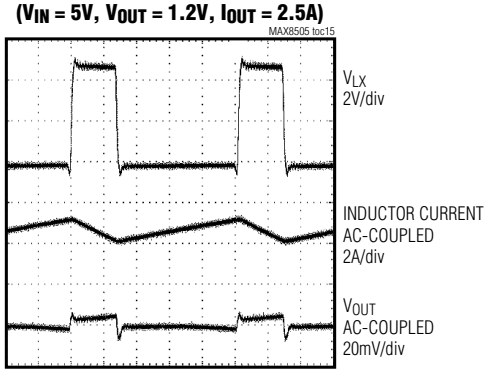
Typical Operating Characteristics (continued)

(Typical values are at V_{IN} = V_{CC} = V_{CTL} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, and T_A = +25°C, unless otherwise noted.)

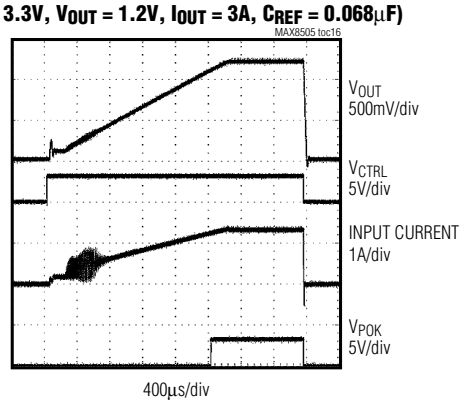
TRANSIENT RESPONSE
(V_{IN} = 3.3V, V_{OUT} = 1.2V)



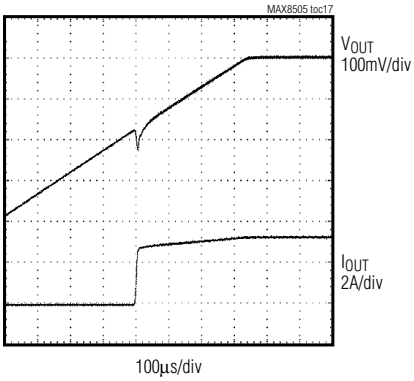
SWITCHING WAVEFORM
(V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2.5A)



SOFT-START/SHUTDOWN WAVEFORM
(V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 3A, C_{REF} = 0.068µF)



TRANSIENT RESPONSE DURING SOFT-START



Pin Description

PIN	NAME	FUNCTION
1, 3, 14, 16	LX	Inductor Connection. Connect an inductor between these pins and the regulator output. All LX pins must be connected together externally. Connect a 3300pF ceramic capacitor from LX to PGND.
2, 4	IN	Power-Supply Inputs. Ranges from 2.6V to 5.5V. Bypass with two ceramic 22µF capacitors to GND. All IN pins must be connected together externally.
5	BST	Bootstrapped Voltage Input. High-side driver supply pin. Bypass to LX with a 0.1µF capacitor. Charged from IN with an external Schottky diode.
6	V_{CC}	Supply Voltage and Gate-Drive Supply for Low-Side Driver. Decouple with a 10Ω resistor and bypass to GND with 0.1µF.
7	POK	Power-OK Output. Open-drain output of a window comparator that pulls POK low when the FB pin is outside the 0.8V ±12% range.
8	CTL	Output Control. When at GND, the regulator is off. When at V_{CC}, the regulator is operating at 1MHz. For a 500kHz application, raise the pin to 2/3 V_{CC}.
9	COMP	Regulator Loop Compensation. Connect a series RC network to GND. This pin is pulled to GND when the output is shut down, or in UVLO or thermal shutdown.
10	FB	Feedback Input. This pin regulates to 0.8V. Use an external resistive-divider from the output to set the output voltage.
11	REF	Place a capacitor at this pin to set the soft-start time. This pin goes to 0V when the part is shut down.
12	GND	Ground
13, 15	PGND	Power Ground. Connect this pin to GND at a single point.

Detailed Description

The MAX8505 is a high-efficiency synchronous buck regulator capable of delivering up to 3A of output current. It operates in PWM mode at a high fixed frequency of 500kHz or 1MHz, thereby reducing external component size. The MAX8505 operates from a 2.6V to 5.5V input voltage and can produce an output voltage from 0.8V to 0.85 × V_{IN}.

Controller Block Function

The MAX8505 step-down converter uses a PWM current-mode control scheme. An open-loop comparator compares the voltage-feedback error signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current-mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. Since the average inductor current is nearly the same as the peak inductor current, the circuit acts as a switch-mode transconductance amplifier. To preserve inner-loop stability and eliminate inductor staircasing, a slope-compensation ramp is summed into the main PWM comparator. During the second half of the cycle, the internal high-side N-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the *Current Limit* section), the high-side MOSFET does not turn on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

Current Sense

An internal current-sense amplifier produces a current signal proportional to the voltage generated by the high-side MOSFET on-resistance and the inductor current ($R_{DS(ON)} \times I_{LX}$). The amplified current-sense signal and the internal slope-compensation signal are summed together into the comparator's inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the feedback voltage from the voltage-error amplifier.

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Current Limit

The MAX8505 offers both high-side and low-side current limits. The high-side current limit monitors the inductor peak current and the low-side current limit monitors the inductor valley current. Current-limit thresholds are 6A (typ) for high side and 3.8A (typ) for low side. If the output inductor current exceeds the high-side current limit during its on-time, the high-side MOSFET turns off and the synchronous rectifier turns on. The inductor current is continuously monitored during the on-time of the low-side MOSFET. If the inductor current is still above the low-side current limit at the moment of the next clock cycle, the high-side MOSFET is not turned on and the low-side MOSFET is kept on to continue discharging the output inductor current. Once the inductor current is below the low-side current limit, the high-side MOSFET is turned on at the next clock cycle. If the inductor current stays less than the high-side current limit during the minimum on duty ratio, the normal operation resumes at the next clock cycle. Otherwise, the current-limit operation continues.

V_{CC} Decoupling

Due to the high switching frequency and tight output tolerance (1%), decouple V_{CC} from IN with a 10Ω resistor and bypass to GND with a 0.1µF capacitor. Place the capacitor as close to V_{CC} as possible.

Bootstrap (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a bootstrapped capacitor boost circuit. The bootstrapped capacitor is connected between the BST pin and LX. When the low-side N-channel MOSFET is on, it forces LX to ground and charges the capacitor to V_{IN} through diode D1. When the low-side N-channel MOSFET turns off and the high-side N-channel MOSFET turns on, LX is pulled to V_{IN}. D1 prevents the capacitor from discharging into V_{IN} and the voltage on the bootstrapped capacitor is boosted above V_{IN}. This provides the necessary voltage for the high driver. A Schottky diode should be used for D1.

Frequency Selection/Enable (CTL)

The MAX8505 includes a frequency selection circuit to allow it to run at 500kHz or 1MHz. The operating frequency is selected through a control input, CTL, which has three input threshold ranges that are ratiometric to the input supply voltage. When CTL is driven to GND, it acts like an enable pin, switching the output off. When the CTL input is driven to >0.8 × V_{CC}, the MAX8505 is enabled with 1MHz switching. When the CTL input is between 0.55 × V_{CC} and 0.7 × V_{CC}, the part operates at 500kHz. When the CTL input is <0.45 x V_{CC}, the device is in shutdown.

Soft-Start

To reduce input transient currents during startup, a programmable soft-start is provided. The soft-start time is given by:

$$t_{SOFT\_START} = C_{REF} \times \frac{0.8V}{25\mu A}$$

A minimum capacitance of 0.01µF at REF is recommended to reduce the susceptibility to switching noise.

Power-OK (POK)

The MAX8505 also includes an open-drain POK output that indicates when the regulator output is within ±12% of its nominal output. If the output voltage moves outside this range, the POK output is pulled to ground. Since this comparator has no hysteresis on either threshold, a 50µs delay time is added to prevent the POK output from chattering between states. The POK should be pulled to V_{IN} or another supply voltage less than 5.5V through a resistor.

UVLO

If V_{CC} drops below +2.25V, the UVLO circuit inhibits switching. Once V_{CC} rises above +2.35V, the UVLO clears, and the soft-start sequence activates.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +170°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins anew.

Design Procedure

Duty Cycle

The equation below shows how to calculate the resulting duty cycle when series losses from the inductor and internal switches are accounted for:

$$D = \frac{V_{OUT} + I_{OUT}(R_{NLS} + R_L)}{V_{IN} + I_{OUT}(R_{NLS} - R_{NHS})} = \frac{V_{OUT} + I_{OUT}(R_{NLS} + R_L)}{V_{IN}}$$

if $R_{NLS} = R_{NHS}$

where V_{OUT} = output voltage; V_{IN} = input voltage; I_{OUT} = output current (3A maximum); R_L = ESR of the inductor; R_{NHS} = on-resistance of the high-side switch; and R_{NLS} = on-resistance of the low-side switch.

Output Voltage Selection

The output voltage of the MAX8505 can be adjusted from 0.8V to 85% of the input voltage at 500kHz or up to 80% of the input voltage at 1MHz. This is done by connecting a resistive-divider (R2 and R3) between the output and the FB pin (see the *Typical Operating Circuit*). For best results, keep R3 below 50kΩ and select R2 using the following equation:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where V_{REF} = 0.8V.

Inductor Design

When choosing the inductor, the key parameters are inductor value (L) and peak current (I_{PEAK}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC current (ripple current) to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately 20% to 30% ripple-current to load-current ratio (LIR = 0.20 to 0.30):

$$L = \frac{V_{OUT} \times (1 - D)}{I_{OUT} \times LIR \times f_S}$$

where f_S is the switching frequency and

$$LIR = 2 \times \frac{(I_{PEAK} - I_{OUT})}{I_{OUT}}$$

Choose an inductor with a saturation current at least as high as the peak inductor current. Additionally, verify the peak inductor current does not exceed the current limit. The inductor selected should exhibit low losses at the chosen operating frequency.

Output Capacitor Design and Output Ripple

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = \sqrt{V_{RIPPLE(C)}^2 + V_{RIPPLE(ESR)}^2 + V_{RIPPLE(ESL)}^2}$$

where the output ripples due to output capacitance, ESR, and ESL are:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL \text{ or } \frac{I_{P-P}}{t_{OFF}} \times ESL,$$

or, whichever is greater.

The ESR is the main contribution to the output voltage ripple.

I_{P-P}, the peak-to-peak inductor current, is:

$$I_{P-P} = \frac{(V_{IN} - V_{OUT})}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial capacitor selection, but determine final values by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for their low ESR and ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load-transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR × I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see Transient Response in the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth, the inductor value, and the slew rate of the transconductance amplifier. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value.

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Input Capacitor Design

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but instead are shunted through the input capacitor. A high source impedance requires larger input capacitance. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}^2}}$$

where I_{RIPPLE} is the input RMS ripple current.

Use sufficient input bypass capacitance to ensure that the absolute maximum voltage rating of the MAX8505 is not exceeded in any condition. When input supply is not located close to the MAX8505, a bulk bypass input capacitor may be needed.

Compensation Design

The double pole formed by the inductor and output capacitor of most voltage-mode controllers introduces a large phase shift, which requires an elaborate compensation network to stabilize the control loop. The MAX8505 controller utilizes a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, eliminating the double pole caused by the inductor and output capacitor, and greatly simplifying the compensation network. A simple type 1 compensation with single compensation resistor (R1) and compensation capacitor (C8) create a stable and high-bandwidth loop (see the *Typical Operating Circuit*).

An internal transconductance error amplifier compensates the control loop. Connect a series resistor and capacitor between COMP (the output of the error amplifier) and GND to form a pole-zero pair. The external inductor, internal current-sensing circuitry, output capacitor, and external compensation circuit determine the loop stability. Choose the inductor and output capacitor based on performance, size, and cost. Additionally, select the compensation resistor and capacitor to optimize control-loop stability. The component values shown in the *Typical Operating Circuit* yield stable operation over a broad range of input-to-output voltages.

For customized compensation networks that increase stability or transient response, the simplified loop gain can be described by the equation:

$$A_{VOL} = \frac{V_{FB}}{V_{OUT}} \times gm_{ERR} \times R_{OERR} \times \left(\frac{s \times C_{COMP} \times R_{COMP} + 1}{(s \times C_{COMP} \times R_{OERR} + 1) \times (s \times C_{PARA} \times R_{COMP} + 1)} \right) \times \frac{R_L}{R_T} \times \left(\frac{s \times C_{OUT} \times R_{ESR} + 1}{s \times C_{OUT} \times R_L + 1} \right)$$

where:

gm_{ERR} (COMP transconductance) = 100µmho

R_{OERR} (output resistance of transconductance amplifier) = 20MΩ

C_{COMP} (compensation capacitor at COMP pin)

R_T (current-sense transresistance) = 0.086Ω

C_{PARA} (parasitic capacitance at COMP pin) = 10pF

R_L (load resistor)

C_{OUT} (output capacitor)

R_{ESR} (series resistance of C_{OUT})

$s = j2\pi f$

In designing the compensation circuit, select an appropriate converter bandwidth (f_C) to stabilize the system while maximizing transient response. This bandwidth should not exceed 1/10 of the switching frequency. Use 100kHz as a reasonable starting point. Calculate C_{COMP} based on this bandwidth using the following equation:

$$R_{COMP} = \frac{I_{OUT} \times R_T \times (R3 + R2) \times 2\pi \times f_C \times C_{OUT}}{V_{OUT} \times gm_{ERR} \times R3}$$

where R2 and R3 are the feedback resistors.

Calculate C_{COMP} to cancel out the pole created by R_L and C_{OUT} using the following equation;

$$C_{COMP} = R_L \times \frac{C_{OUT}}{R_{COMP}}$$

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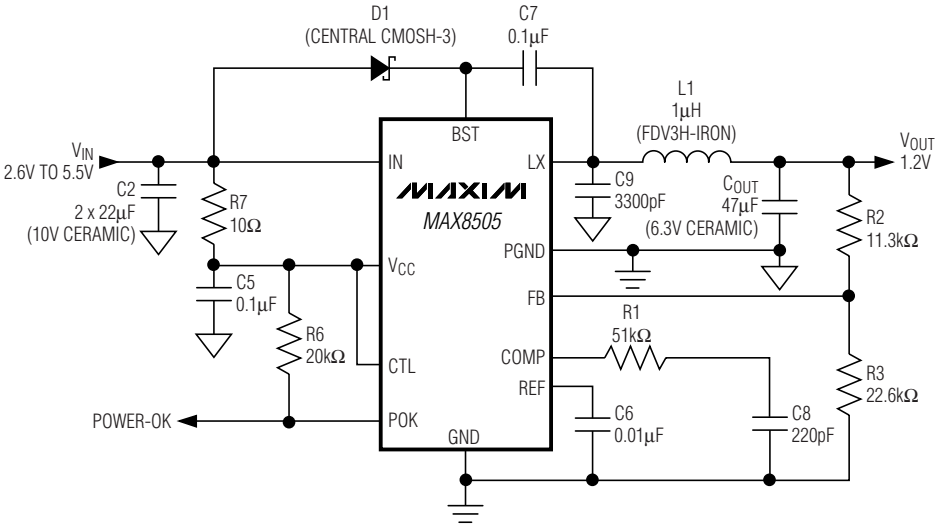
Applications Information

PC Board Layout Considerations

Careful PC board layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by the high-side MOSFET, the low-side MOSFET, and the input capacitors. Avoid vias in the switching paths.
4) If possible, connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

Typical Application Circuit



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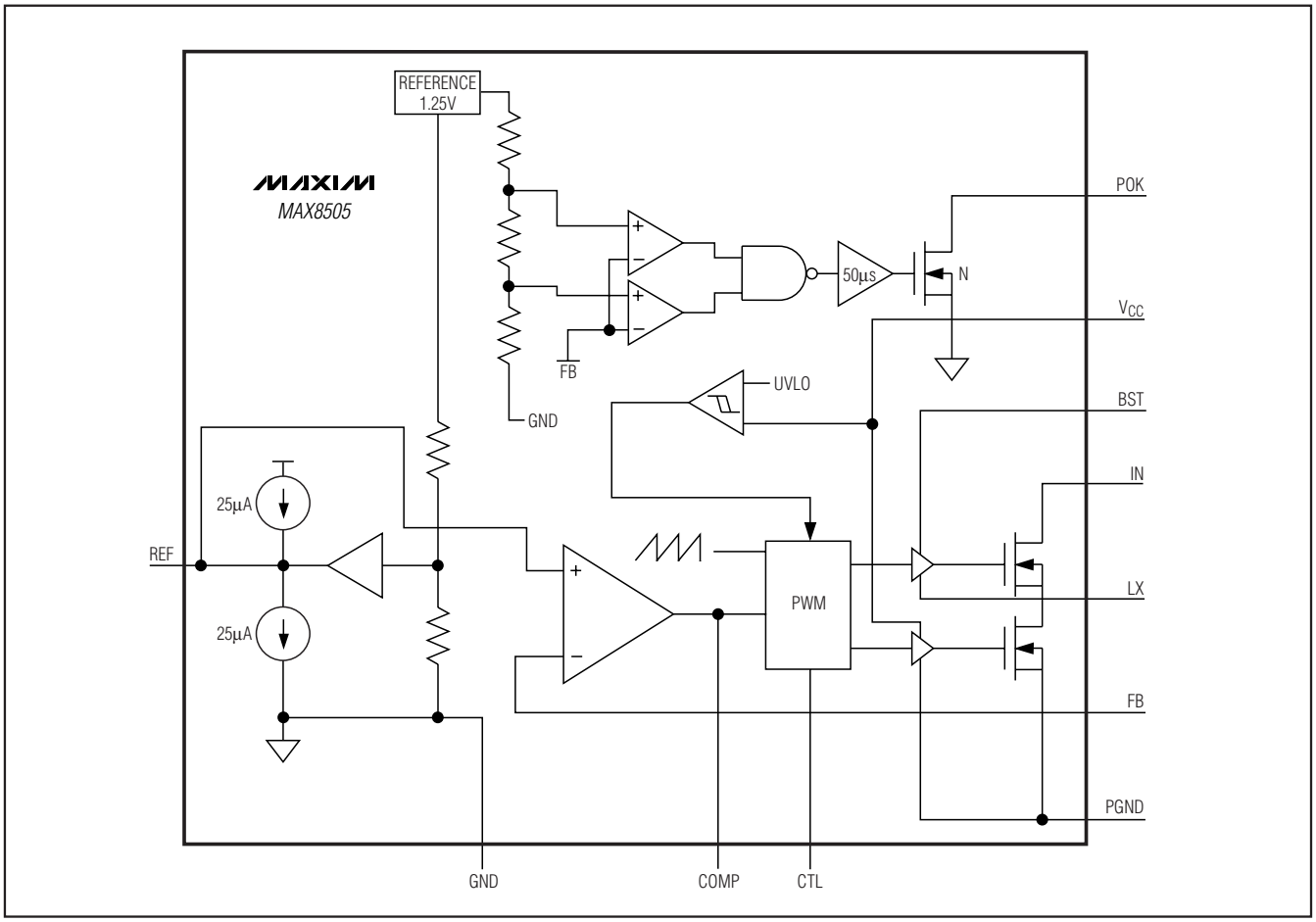
Functional Diagram



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+5	21-0055	90-0167

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/03	Initial release	—
1	9/10	Added lead-free notation to *Ordering Information* and corrected equations in the *Compensation Design* section	1, 12