19-0811; Rev 0; 4/07

EVALUATION KIT AVAILABLE

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

General Description

The MAX15020 high-voltage step-down DC-DC converter operates over an input voltage range of 7.5V to 40V. The device integrates a 0.2Ω high-side switch and is capable of delivering 2A load current with excellent load and line regulation. The output is dynamically adjustable from 0.5V to 36V through the use of an external reference input (REFIN). The MAX15020 consumes only 6µA in shutdown mode.

The device utilizes feed-forward voltage-mode architecture for good noise immunity in the high-voltage switching environment and offers external compensation for maximum flexibility. The switching frequency is selectable to 300kHz or 500kHz and can be synchronized to an external clock signal of 100kHz to 500kHz by using the SYNC input. The IC features a maximum duty cycle of 95% (typ) at 300kHz.

The device includes configurable undervoltage lockout (UVLO) and soft-start. Protection features include cycle-by-cycle current limit, hiccup-mode for output short-circuit protection, and thermal shutdown. The MAX15020 is available in a 20-pin TQFN 5mm x 5mm package and is rated for operation over the -40°C to +125°C temperature range.

Applications

Printer Head Driver Power Supply

Automotive Power Supply

Industrial Power Supply

Step-Down Power Supply

Features

- **Wide 7.5V to 40V Input Voltage Range**
- **2A Output Current, Up to 96% Efficiency**
- **Dynamic Programmable Output Voltage (0.5V to 36V)**
- **Maximum Duty Cycle of 95% (typ) at 300kHz**
- **100kHz to 500kHz Synchronizable SYNC Frequency Range**
- **Configurable UVLO and Soft-Start**
- **Low-Noise, Voltage-Mode Step-Down Converter**
- **Programmable Output-Voltage Slew Rate**
- **Lossless Constant Current Limit with Fixed Timeout to Hiccup Mode**
- **Extremely Low-Power Consumption (< 6µA typ) in Shutdown Mode**
- **20-Pin (5mm x 5mm) Thin QFN Package**

Ordering Information

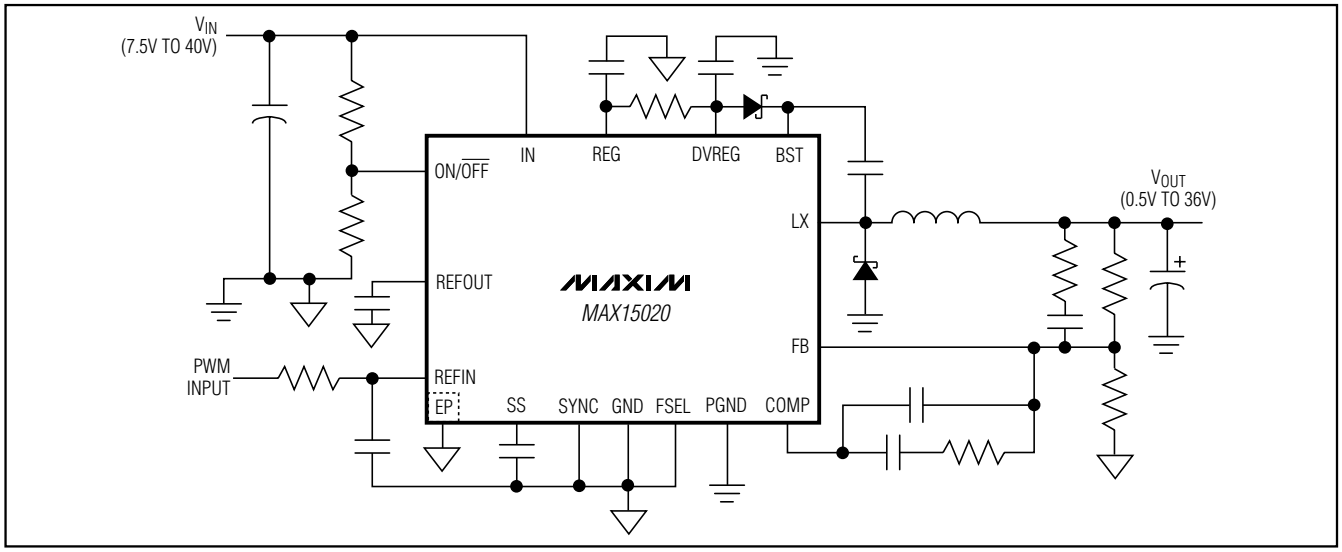
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX15020ATP+	-40°C to +125°C	20 TQFN-EP* (5mm x 5mm)	T2055-5

+Denotes a lead-free package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

ABSOLUTE MAXIMUM RATINGS

IN, ON/$\overline{OFF}$ to GND.....-0.3V to +45V
LX to GND.....-0.715V to (V_{IN} + 0.3V)
BST to GND.....-0.3V to (V_{IN} + 12V)
BST to LX.....-0.3V to +12V
PGND, EP to GND.....-0.3V to +0.3V
REG, DVREG, SYNC to GND.....-0.3V to +12V
FB, COMP, FSEL, REFIN, REFOUT, SS to GND.....-0.3V to (V_{REG} + 0.3V)
Continuous Current through Internal Power MOSFET
T_J = +125°C.....4A
T_J = +150°C.....2.7A

Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN, single-layer board (5mm x 5mm) (derate 21.3mW/°C above +70°C).....1702.1mW
20-Pin Thin QFN, multilayer board (5mm x 5mm) (derate 34.5mW/°C above +70°C).....2758.6mW
Maximum Junction Temperature.....+150°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 36V, V_{REG} = V_{DVREG}, V_{PGND} = V_{GND} = V_{EP} = 0V, V_{SYNC} = 0V, C_{REFOUT} = 0.1µF, T_A = T_J = -40°C to +125°C, FSEL = REG, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		7.5		40.0	V
UVLO Rising Threshold	$UVLO_{RISING}$		6.80	7.20	7.45	V
UVLO Falling Threshold	$UVLO_{FALLING}$		6.0	6.5	7.0	V
UVLO Hysteresis	$UVLO_{HYST}$			0.7		V
Quiescent Supply Current		V_{IN} = 40V, V_{FB} = 1.3V		1.6	2.8	mA
Switching Supply Current		V_{IN} = 40V, V_{FB} = 0V		14.5		mA
Shutdown Current	I_{SHDN}	$V_{ON/\overline{OFF}}$ = 0.2V, V_{IN} = 40V		6	15	µA
ON/$\overline{OFF}$ CONTROL						
Input-Voltage Threshold	$V_{ON/\overline{OFF}}$	$V_{ON/\overline{OFF}}$ rising	1.200	1.225	1.270	V
Input-Voltage Threshold Hysteresis				120		mV
Input Bias Current		$V_{ON/\overline{OFF}}$ = 0V to V_{IN}	-250		+250	nA
Shutdown Threshold Voltage	V_{SD}				0.2	V
INTERNAL VOLTAGE REGULATOR (REG)						
Output Voltage		I_{REG} = 0 to 20mA	7.1		8.3	V
OSCILLATOR						
Frequency	f_{SW}	V_{FSEL} = 0V	450		550	kHz
		V_{FSEL} = V_{REG}	270		330	
Maximum Duty Cycle	D_{MAX}	V_{FSEL} = 0V	85			%
		V_{FSEL} = V_{REG}	90			
SYNC/FSEL High-Level Voltage			2			V
SYNC/FSEL Low-Level Voltage					0.8	V
SYNC Frequency Range	f_{SYNC}	V_{FSEL} = V_{REG}	100		550	kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 36V, V_{REG} = V_{DVREG}, V_{PGND} = V_{GND} = V_{EP} = 0V, V_{SYNC} = 0V, C_{REFOUT} = 0.1µF, T_A = T_J = -40°C to +125°C, FSEL = REG, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START/REFIN/REFOUT/FB						
Soft-Start Current	I_{SS}		8	15	26	µA
REFOUT Output Voltage			0.97	0.98	1.01	V
REFIN Input Range			0		3.6	V
FB Accuracy		REFIN = REFOUT	0.97	0.98	1.01	V
		FB = COMP, V_{REFIN} = 0.2V to 3.6V	V_{REFIN} - 5mV	V_{REFIN}	V_{REFIN} + 5mV	mV
FB Input Current		V_{SS} = 0.2V, V_{FB} = 0V	-250		+250	nA
Open-Loop Gain				80		dB
Unity-Gain Bandwidth				1.8		MHz
PWM Modulator Gain (V_{IN} / V_{RAMP})		f_{SYNC} = 100kHz, V_{IN} = 7.5V		9.4		V/V
		f_{SYNC} = 500kHz, V_{IN} = 40V		8.9		
CURRENT-LIMIT COMPARATOR						
Cycle-by-Cycle Switch Current Limit	I_{ILIM}		2.5	3.5	4.5	A
Number of ILIM Events to Hiccup				4		—
Hiccup Timeout				512		Clock periods
POWER SWITCH						
Switch On-Resistance		V_{BST} - V_{LX} = 6V		0.18	0.35	Ω
BST Leakage Current		V_{BST} = V_{LX} = V_{IN} = 40V			10	µA
Switch Leakage Current		V_{IN} = 40V, V_{LX} = V_{BST} = 0V			10	µA
Switch Gate Charge		V_{BST} - V_{LX} = 6V		10		nC
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	T_{SHDN}			+160		°C
Thermal Shutdown Hysteresis				20		°C

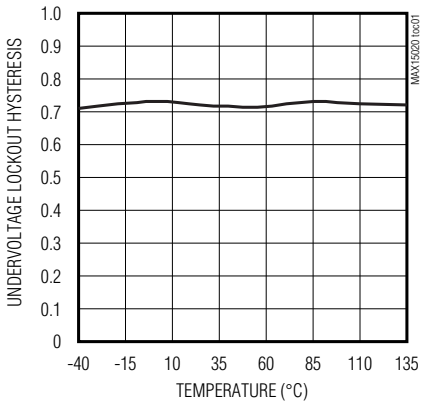
Note 1: Limits are 100% production tested at T_A = T_J = +25°C. Limits at -40°C and +125°C are guaranteed by design.

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

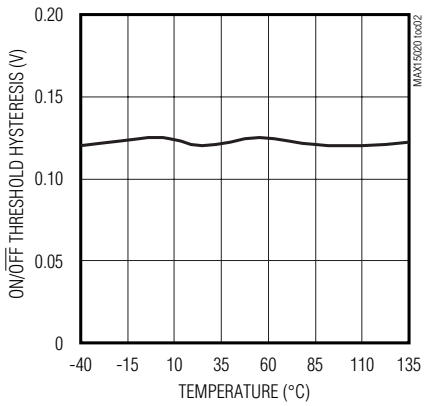
Typical Operating Characteristics

(V_{IN} = 36V, Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

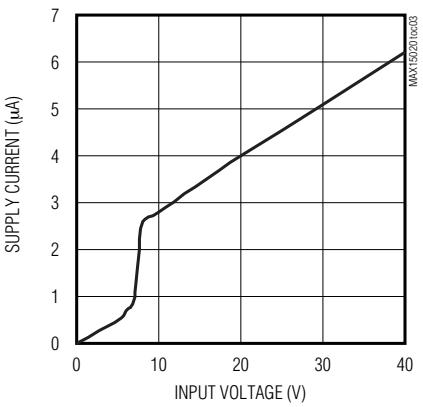
UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE



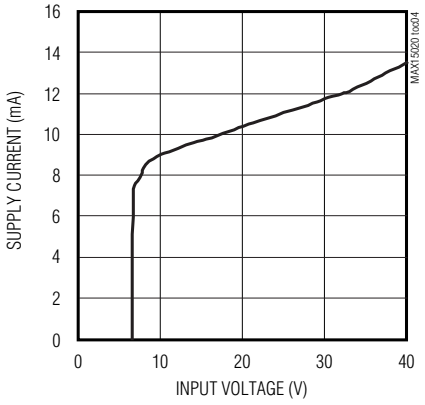
ON/$\overline{OFF}$ THRESHOLD HYSTERESIS vs. TEMPERATURE



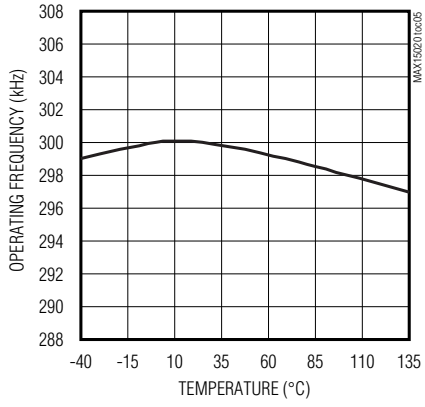
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



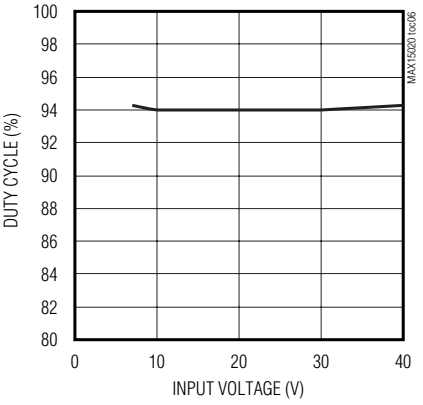
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



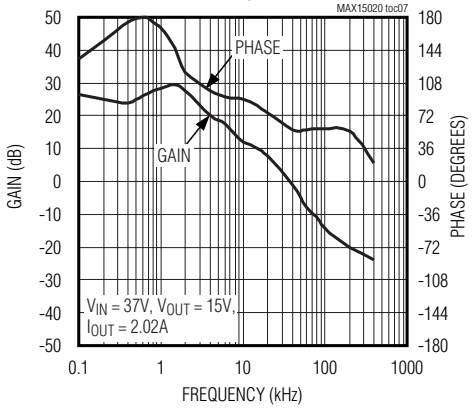
OPERATING FREQUENCY vs. TEMPERATURE



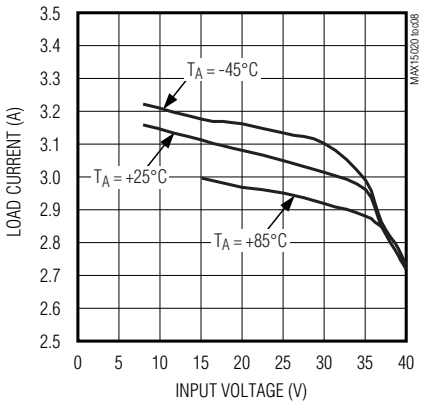
MAXIMUM DUTY CYCLE vs. INPUT VOLTAGE



LOOP GAIN/PHASE vs. FREQUENCY



MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE

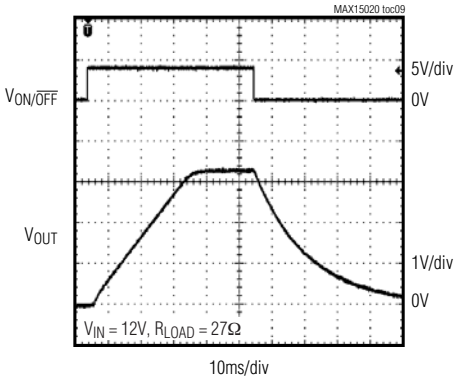


2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

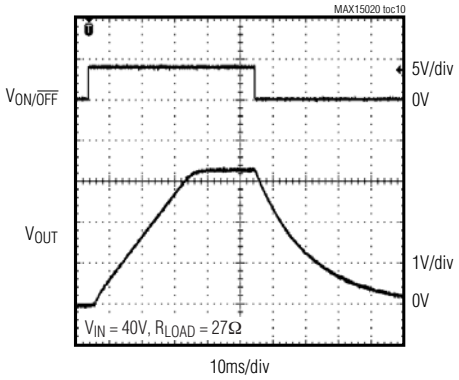
Typical Operating Characteristics (continued)

(V_{IN} = 36V, Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

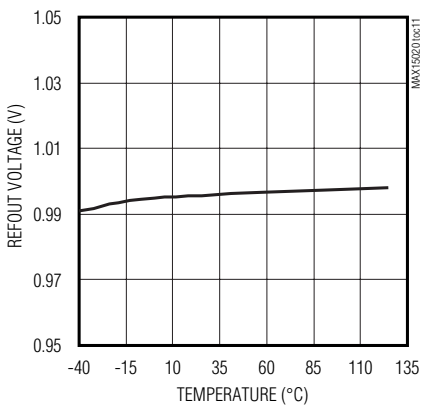
TURN-ON/TURN-OFF WAVEFORM



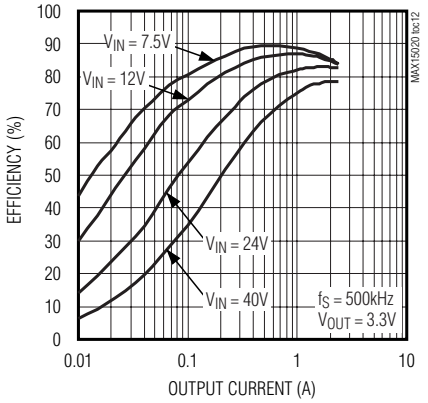
TURN-ON/TURN-OFF WAVEFORM



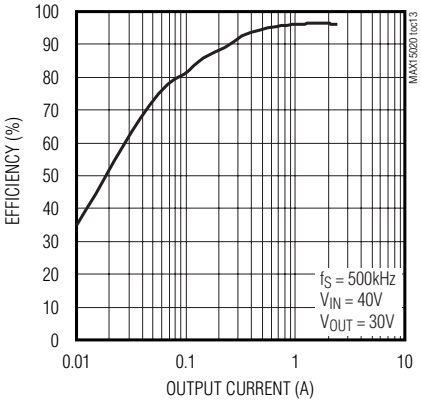
REFOUT VOLTAGE vs. TEMPERATURE



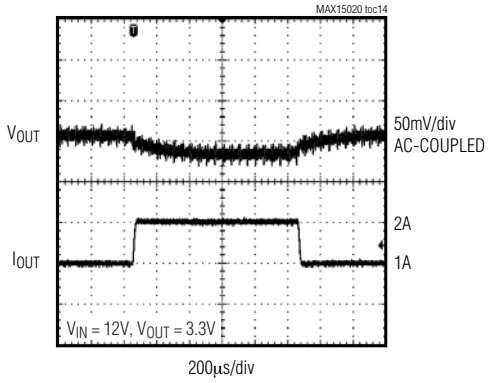
EFFICIENCY vs. LOAD CURRENT



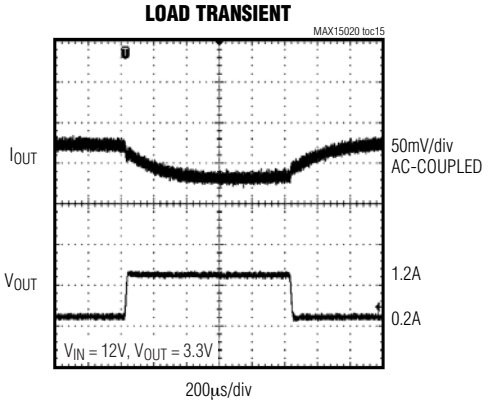
EFFICIENCY vs. LOAD CURRENT



LOAD TRANSIENT



LOAD TRANSIENT

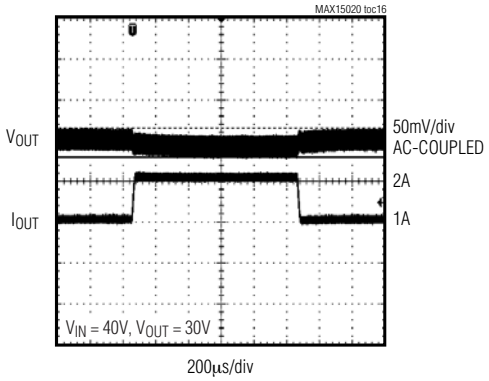


2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

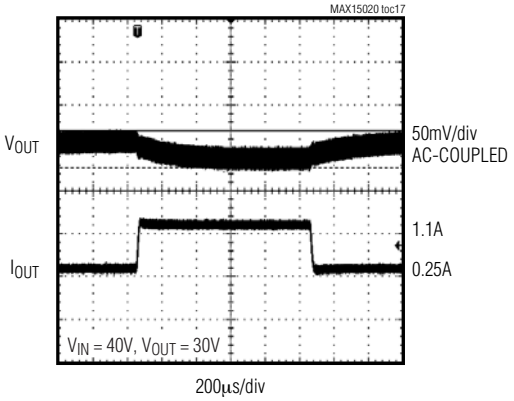
Typical Operating Characteristics (continued)

(V_{IN} = 36V, Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

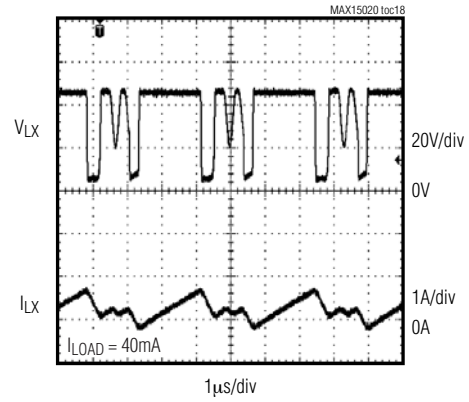
LOAD TRANSIENT



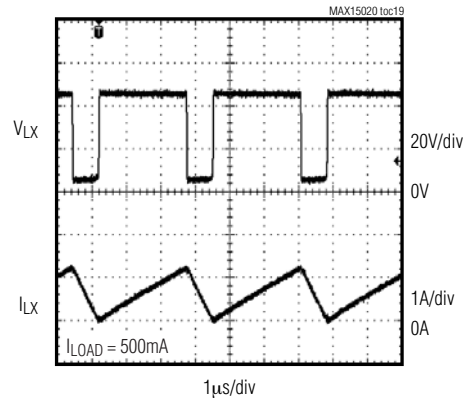
LOAD TRANSIENT



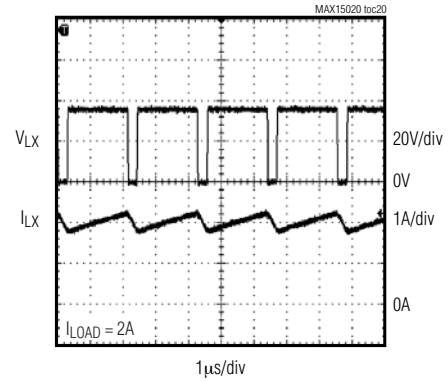
LIGHT-LOAD SWITCHING WAVEFORMS



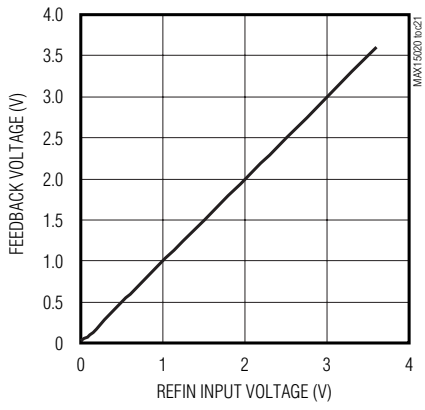
SWITCHING WAVEFORMS



HEAVY-LOAD SWITCHING WAVEFORMS



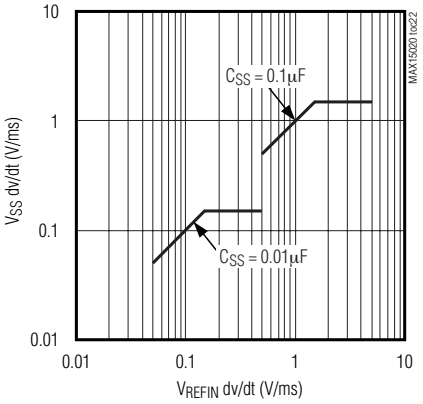
FEEDBACK VOLTAGE vs. REFIN INPUT VOLTAGE



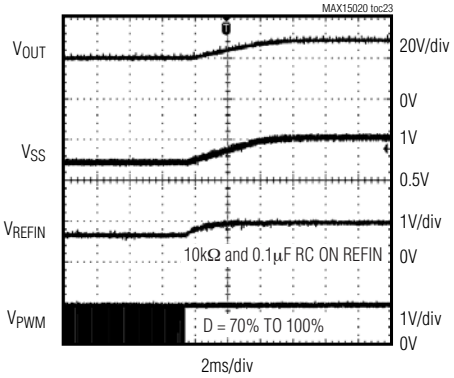
Typical Operating Characteristics (continued)

(V_{IN} = 36V, Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

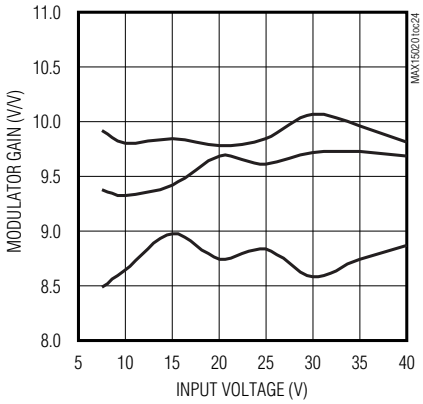
SOFT-START VOLTAGE RISE vs. REFIN VOLTAGE RISE



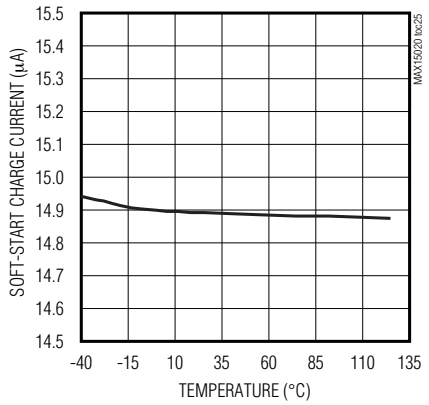
V_{SS} AND V_{OUT} RESPONSE TO REFIN PWM



MODULATOR GAIN vs. INPUT VOLTAGE



SOFT-START CHARGE CURRENT vs. TEMPERATURE



2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Pin Description

PIN	NAME	FUNCTION
1	COMP	Voltage-Error-Amplifier Output. Connect COMP to the necessary compensation feedback network.
2	FB	Feedback Regulation Point. Connect to the center tap of an external resistor-divider connected between the output and GND to set the output voltage. The FB voltage regulates to the voltage applied to REFIN.
3	ON/$\overline{OFF}$	ON/$\overline{OFF}$ Control. The ON/$\overline{OFF}$ rising threshold is set to approximately 1.225V. Connect to the center tap of a resistive divider connected between IN and GND to set the turn-on (rising) threshold. Connect ON/$\overline{OFF}$ to GND to shut down the IC. Connect ON/$\overline{OFF}$ to IN for always-on operation given that V_{IN} has risen above the UVLO threshold. ON/$\overline{OFF}$ can be used for power-supply sequencing.
4	REFOUT	0.98V Reference Voltage Output. Bypass REFOUT to GND with a 0.1µF ceramic capacitor. REFOUT is to be used only with REFIN. It is not to be used to power any other external circuitry.
5	SS	Soft-Start. Connect a 0.01µF or greater ceramic capacitor from SS to GND. See the *Soft-Start (SS)* section.
6	REFIN	External Reference Input. Connect to an external reference. V_{FB} regulates to the voltage applied to REFIN. Connect REFIN to REFOUT to use the internal 1V reference. See the *Reference Input and Output (REFIN, REFOUT)* section.
7	FSEL	Internal Switching Frequency Selection Input. Connect FSEL to REG to select f_{SW} = 300kHz. Connect FSEL to GND to select f_{SW} = 500kHz. When an external clock is connected to SYNC connect FSEL to REG.
8	SYNC	Oscillator Synchronization Input. SYNC can be driven by an external 100kHz to 500kHz clock to synchronize the MAX15020's switching frequency. Connect SYNC to GND to disable the synchronization function. When using SYNC, connect FSEL to REG.
9	DVREG	Power Supply for Internal Digital Circuitry. Connect a 10Ω resistor from REG to DVREG. Connect DVREG to the anode of the boost diode, D2 in Figure 2. Bypass DVREG to GND with at least a 1µF ceramic capacitor.
10	PGND	Power-Ground Connection. Connect the input filter capacitor's negative terminal, the anode of the freewheeling diode, and the output filter capacitor's return to PGND. Connect externally to GND at a single point near the input bypass capacitor's return terminal.
11	N.C.	No Connection. Leave unconnected or connect to GND
12	BST	High-Side Gate Driver Supply. Connect BST to the cathode of the boost diode and to the positive terminal of the boost capacitor.
13, 14, 15	LX	Source Connection of Internal High-Side Switch. Connect the inductor and rectifier diode's cathode to LX.
16, 17, 18	IN	Supply Input Connection. Connect to an external voltage source from 7.5V to 40V.
19	REG	8V Internal Regulator Output. Bypass to GND with at least a 1µF ceramic capacitor. Do not use REG to power external circuitry.
20	GND	Ground Connection. Solder the exposed pad to a large GND plane. Connect GND and PGND together at one point near the input bypass capacitor return terminal.
—	EP	Exposed Pad. Connect EP to GND. Connecting EP does not remove the requirement for proper ground connections to the appropriate pins. See the *PCB Layout and Routing* section.

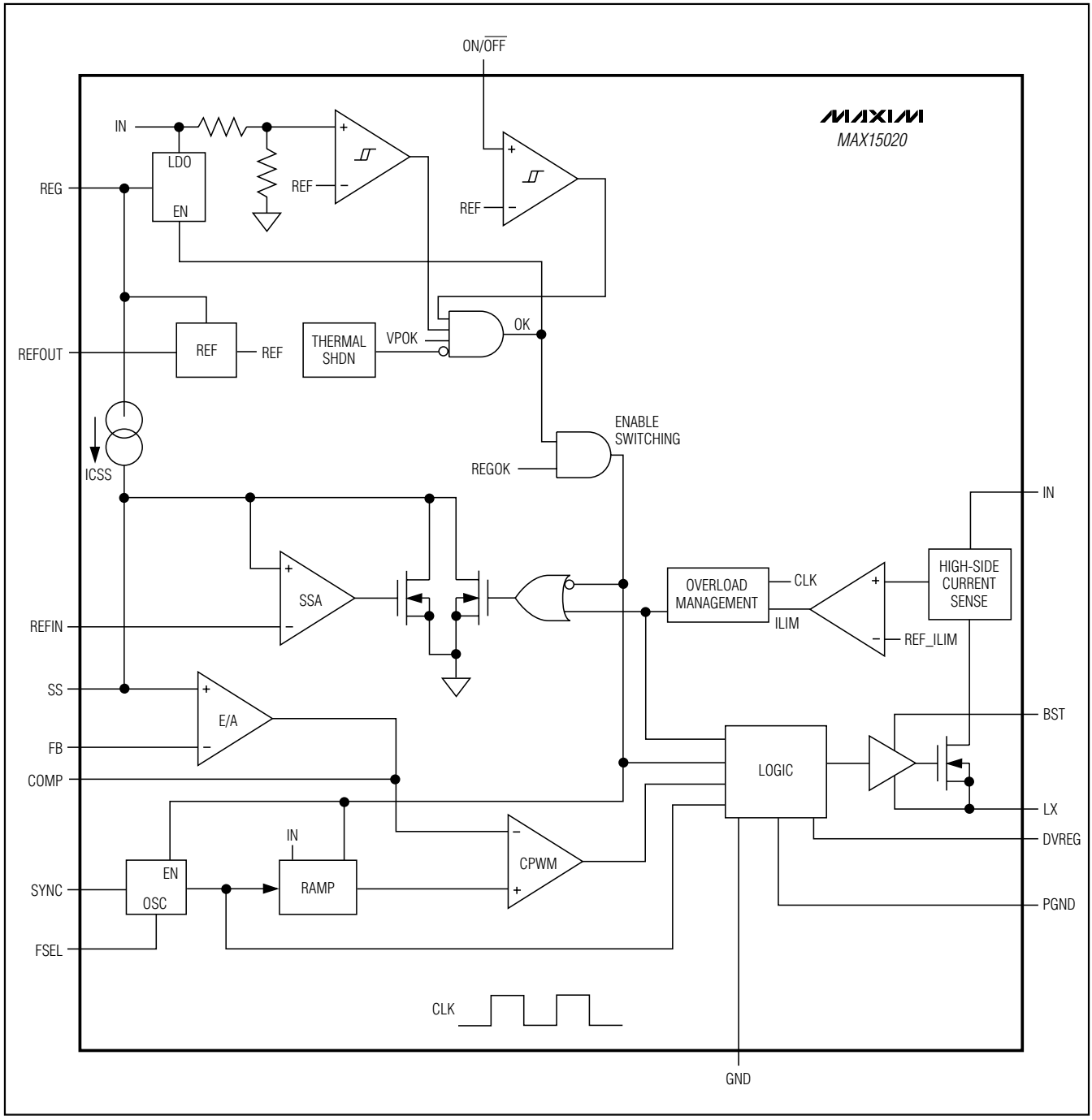


Figure 1. Functional Diagram

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

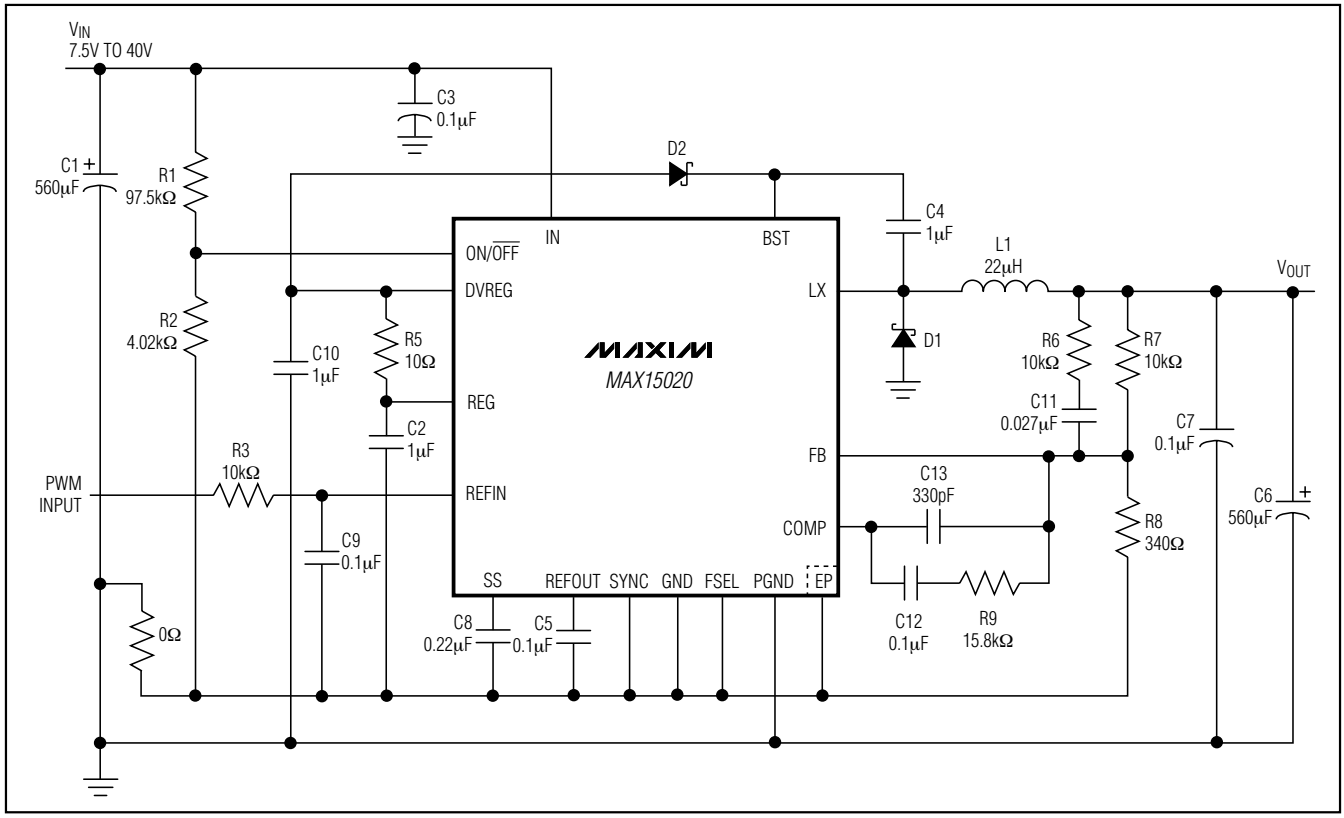


Figure 2. Typical Application Circuit

Detailed Description

The MAX15020 voltage-mode step-down converter contains an internal 0.2Ω power MOSFET switch. The MAX15020 input voltage range is 7.5V to 40V. The internal low $R_{DS(ON)}$ switch allows for up to 2A of output current. The external compensation, voltage feedforward, and automatically adjustable maximum ramp amplitude simplify the loop compensation design allowing for a variety of L and C filter components. In shutdown, the supply current is typically 6µA. The output voltage is dynamically adjustable from 0.5V to 36V. Additional features include an externally programmable UVLO through the ON/$\overline{OFF}$ pin, a programmable soft-start, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

Internal Linear Regulator (REG)

REG is the output terminal of the 8V LDO powered from IN and provides power to the IC. Connect REG externally to DVREG to provide power for the internal digital circuitry. Place a 1µF ceramic bypass capacitor, C2, next to the IC from REG to GND. During normal operation, REG is intended for powering up only the internal circuitry and should not be used to supply power to the external loads.

UVLO/ON/$\overline{OFF}$ Threshold

The MAX15020 provides a fixed 7V UVLO function which monitors the input voltage (V_{IN}). The device is held off until V_{IN} rises above the UVLO threshold.

ON/$\overline{OFF}$ provides additional turn-on/turn-off control. Program the ON/$\overline{OFF}$ threshold by connecting a resistive divider from IN to ON/$\overline{OFF}$ to GND. The device turns on when $V_{ON/\overline{OFF}}$ rises above the ON/$\overline{OFF}$ threshold (1.225V), given that V_{IN} has risen above the UVLO threshold.

Driving ON/$\overline{OFF}$ to ground places the IC in shutdown. When in shutdown the internal power MOSFET turns off, all internal circuitry shuts down, and the quiescent supply current reduces to 6µA (typ.). Connect an RC network from ON/$\overline{OFF}$ to GND to set a turn-on delay that can be used to sequence the output voltages of multiple devices.

Soft-Start (SS)

At startup, after V_{IN} is applied and the UVLO threshold is reached, a 15µA (typ) current is sourced into the capacitor (C_{SS}) connected from SS to GND forcing the V_{SS} voltage to ramp up slowly. If V_{REFIN} is set to a DC voltage or has risen faster than the C_{SS} charge rate, then V_{SS} will stop rising once it reaches V_{REFIN}. If V_{REFIN} rises at a slower rate, V_{SS} will follow the V_{REFIN} voltage rise rate. V_{OUT} rises at the same rate as V_{SS} since V_{FB} follows V_{SS}.

Set the soft-start time (t_{SS}) using following equation:

$$t_{SS} = \frac{V_{REFIN} \times C_{SS}}{15\mu A}$$

where t_{SS} is in seconds and C_{SS} is in Farads.

Reference Input and Output (REFIN, REFOUT)

The MAX15020 features a reference input for the internal error amplifier. The IC regulates FB to the SS voltage which is driven by the DC voltage applied to REFIN. Connect REFIN to REFOUT to use the internal 0.98V reference. Connect REFIN to a variable DC voltage source to dynamically control the output voltage. Alternatively, REFIN can also be driven by a duty-cycle control PWM source through a lowpass RC filter (Figure 2).

Internal Digital Power Supply (DVREG)

DVREG is the supply input for the internal digital power supply. The power for DVREG is derived from the output of the internal regulator (REG). Connect a 10Ω resistor from REG to DVREG. Bypass DVREG to GND with at least a 1µF ceramic capacitor.

Error Amplifier

The output of the internal error amplifier (COMP) is available for frequency compensation (see the *Compensation Design* section). The inverting input is FB, the noninverting input is SS, and the output is COMP. The error amplifier has an 80dB open-loop gain and a 1.8MHz GBW product. When an external clock is used, connect FSEL to REG.

Oscillator/Synchronization Input (SYNC)

With SYNC connected to GND, the IC uses the internal oscillator and switches at a fixed frequency of 300kHz or 500kHz based upon the selection of FSEL. For external synchronization, drive SYNC with an external clock from 100kHz to 500kHz and connect FSEL to REG. When driven with an external clock, the device synchronizes to the rising edge of SYNC.

PWM Comparator/Voltage Feed-Forward

An internal ramp generator is compared against the output of the error amplifier to generate the PWM signal. The maximum amplitude of the ramp (V_{RAMP}) automatically adjusts to compensate for input voltage and oscillator frequency changes. This causes the V_{IN} / V_{RAMP} to be a constant 9V/V across the input voltage range of 7.5V to 40V and the SYNC frequency range of 100kHz to 500kHz. This simplifies loop compensation design by allowing large input voltage ranges and large frequency range selection.

Output Short-Circuit Protection (Hiccup Mode)

The MAX15020 protects against an output short circuit by utilizing hiccup-mode protection. In hiccup mode, a series of sequential cycle-by-cycle current-limit events cause the part to shut down and restart with a soft-start sequence. This allows the device to operate with a continuous output short circuit.

During normal operation, the switch current is measured cycle-by-cycle. When the current limit is exceeded, the internal power MOSFET turns off until the next on-cycle and the hiccup counter increments. If the counter counts four consecutive overcurrent limit events, the device discharges the soft-start capacitor and shuts down for 512 clock periods before restarting with a soft-start sequence. Each time the power MOSFET turns on and the device does not exceed the current limit, the counter is reset.

Thermal-Overload Protection

The MAX15020 features an integrated thermal-overload protection. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, an internal thermal sensor shuts down the part, turning off the power MOSFET and allowing the IC to cool. After the temperature falls by 20°C, the part restarts beginning with the soft-start sequence.

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Applications Information

Setting the ON/$\overline{OFF}$ Threshold

When the voltage at ON/$\overline{OFF}$ rises above 1.225V, the MAX15020 turns on. Connect a resistive divider from IN to ON/$\overline{OFF}$ to GND to set the turn-on voltage (see Figure 2). First select the ON/$\overline{OFF}$ to the GND resistor (R2), then calculate the resistor from IN to ON/$\overline{OFF}$ (R1) using the following equation:

$$R1 = R2 \times \left[\frac{V_{IN}}{V_{ON/\overline{OFF}}} - 1\right]$$

where V_{IN} is the input voltage at which the converter turns on, $V_{ON/\overline{OFF}}$ = 1.225V and R2 is chosen to be less than 600kΩ.

If ON/$\overline{OFF}$ is connected to IN directly, the UVLO feature monitors the supply voltage at IN and allows operation to start when V_{IN} rises above 7.2V.

Setting the Output Voltage

Connect a resistor-divider from OUT to FB to GND to set the output voltage (see Figure 2). First calculate the resistor (R7) from OUT to FB using the guidelines in the *Compensation Design* section. Once R7 is known, calculate R8 using the following equation:

$$R8 = \frac{R7}{\left[\frac{V_{OUT}}{V_{FB}} - 1\right]}$$

where V_{FB} = REFIN and REFIN = 0 to 3.6V.

Setting the Output-Voltage Slew Rate

The output-voltage rising slew rate tracks the V_{SS} slew rate, given that the control loop is relatively fast compared with the V_{SS} slew rate. The maximum V_{SS} upswing slew rate is controlled by the soft-start current charging the capacitor connected from SS to GND according to the formula below:

$$\frac{dV_{OUT}}{dt} = \frac{R_7 + R_8}{R_8} \times \frac{dV_{SS}}{dt} = \frac{R_7 + R_8}{R_8} \frac{I_{SS}}{C_{SS}}$$

when driving V_{SS} with a slow-rising voltage source at REFIN, V_{OUT} will slowly rise according to the V_{REFIN} slew rate.

The output-voltage falling slew rate is limited to the discharge rate of C_{SS} assuming there is enough load current to discharge the output capacitor at this rate. The C_{SS} discharge current is 15µA. If there is no load, then the output voltage falls at a slower rate based upon leakage and additional current drain from C_{OUT}.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15020: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_L). Higher ΔI_L allows for a lower inductor value while a lower ΔI_L requires a higher inductor value. A lower inductor value minimizes size and cost and improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output voltage ripple for the same output capacitor. Higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_{P-P} equal to 40% of the full load current.

Calculate the inductor using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I_L}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is fixed at 300kHz or 500kHz and can vary between 100kHz and 500kHz when synchronized to an external clock (see the *Oscillator/Synchronization Input (SYNC)* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturating current (I_{SAT}) is also important to avoid runaway current during continuous output short circuit. Select an inductor with an I_{SAT} specification higher than the maximum peak current limit of 4.5A.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents and therefore the input capacitor must be carefully chosen to keep the input-voltage ripple within design requirements. The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR (equivalent series resistance) of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT\_MAX} + \frac{\Delta I_L}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT\_MAX} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{OUT_MAX} is the maximum output current, D is the duty cycle, and f_{SW} is the switching frequency.

The MAX15020 includes internal and external UVLO hysteresis and soft-start to avoid possible unintentional chattering during turn-on. However, use a bulk capacitor if the input source impedance is high. Use enough input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitor Selection

The allowable output-voltage ripple and the maximum deviation of the output voltage during load steps determine the output capacitance and its ESR. The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the ESR of the output capacitor). The equations for calculating the peak-to-peak output voltage ripple are:

$$\Delta V_Q = \frac{\Delta I_L}{16 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = ESR \times \Delta I_L$$

Normally, a good approximation of the output-voltage ripple is $\Delta V_{RIPPLE} \approx \Delta V_{ESR} + \Delta V_Q$. If using ceramic capacitors, assume the contribution to the output-voltage ripple from ESR and the capacitor discharge to be equal to 20% and 80%, respectively. ΔI_L is the peak-to-peak inductor current (see the *Input Capacitor Selection* section) and f_{SW} is the converter's switching frequency.

The allowable deviation of the output voltage during fast load transients also determines the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation Design* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL (ΔV_{ESL}), and the capacitor discharge cause a voltage droop during the load step. Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for better transient load and voltage ripple performance. Surface-mount capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output-voltage deviations below the tolerable limits of the electronics powered. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, and $t_{RESPONSE}$ is the response time of the controller.

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Compensation Design

The MAX15020 uses a voltage-mode control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with an internal ramp to produce the required duty cycle. The output lowpass LC filter creates a double pole at the resonant frequency, which has a gain drop of -40dB/decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider, and a voltage error amplifier. The power modulator has a DC gain set by V_{IN} / V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}) (C6 in the Figure 2) and its ESR. The power modulator incorporates a voltage feed-forward feature, which automatically adjusts for variations in the input voltage resulting in a DC gain of 9. The following equations define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}} = 9$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}}$$

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The switching frequency is internally set at 300kHz or 500kHz, or can vary from 100kHz to 500kHz when driven with an external SYNC signal. The crossover frequency (f_C), which is the frequency when the closed-loop gain is equal to unity, should be set as f_{SW} / 2π or lower.

The error amplifier must provide a gain and phase bump to compensate for the rapid gain and phase loss from the LC double pole. This is accomplished by utilizing a Type 3 compensator that introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole (f_{P1}) near the origin.

In reference to Figures 3 and 4, the two zeros are at:

$$f_{Z1} = \frac{1}{2\pi \times R9 \times C12} \text{ and } f_{Z2} = \frac{1}{2\pi \times (R6 + R7) \times C11}$$

And the higher frequency poles are at:

$$f_{P2} = \frac{1}{2\pi \times R6 \times C11} \text{ and } f_{P3} = \frac{1}{2\pi \times R9 \times \left(\frac{C12 \times C13}{C12 + C13}\right)}$$

Compensation when $f_C < f_{ESR}$

Figure 3 shows the error-amplifier feedback as well as its gain response for circuits that use low-ESR output capacitors (ceramic). In this case f_{ZESR} occurs after f_C.

f_{Z1} is set to 0.8 x $f_{LC(MOD)}$ and f_{Z2} is set to f_{LC} to compensate for the gain and phase loss due to the double pole. Choose the inductor (L) and output capacitor (C_{OUT}) as described in the *Inductor Selection* and *Output Capacitor Selection* sections.

Choose a value for the feedback resistor R6 in Figure 3 (values between 1kΩ and 10kΩ are adequate).

C12 is then calculated as:

$$C12 = \frac{1}{2\pi \times 0.8 \times f_{LC} \times R9}$$

f_C occurs between f_{Z2} and f_{P2}. The error-amplifier gain (G_{EA}) at f_C is due primarily to C11 and R9.

Therefore, $G_{EA(fC)} = 2\pi \times f_C \times C11 \times R9$ and the modulator gain at f_C is:

$$G_{MOD(fC)} = \frac{G_{MOD(DC)}}{(2\pi)^2 \times L \times C_{OUT} \times f_C^2}$$

Since $G_{EA(fC)} \times G_{MOD(fC)} = 1$, C11 is calculated by:

$$C11 = \frac{f_C \times L \times C_{OUT} \times 2\pi}{R9 \times G_{MOD(DC)}}$$

f_{P2} is set at 1/2 the switching frequency (f_{SW}). R6 is then calculated by:

$$R6 = \frac{1}{2\pi \times C11 \times 0.5 \times f_{SW}}$$

Since R7 >> R6, R7 + R6 can be approximated as R7. R7 is then calculated as:

$$R7 = \frac{1}{2\pi \times f_{LC} \times C11}$$

f_{P3} is set at 5 x f_C. Therefore, C13 is calculated as:

$$C13 = \frac{C12}{2\pi \times C12 \times R9 \times f_{P3} - 1}$$

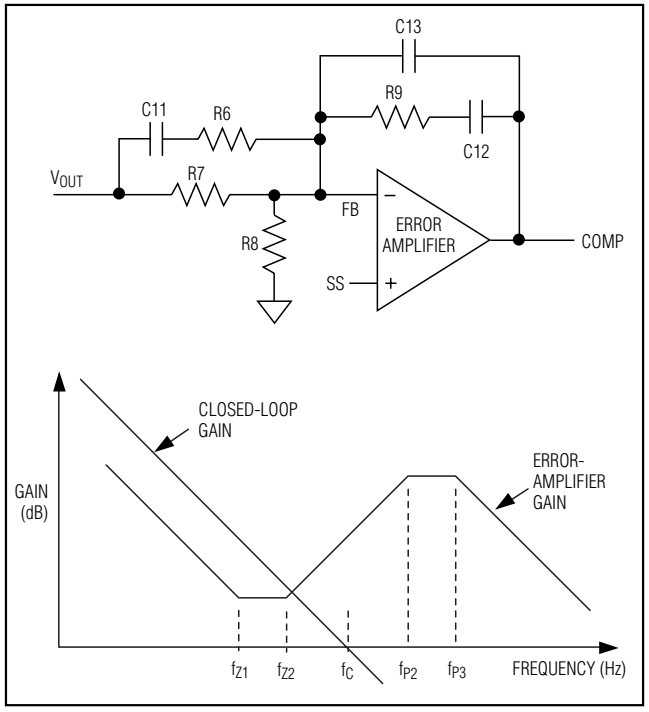


Figure 3. Error-Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Ceramic Capacitors

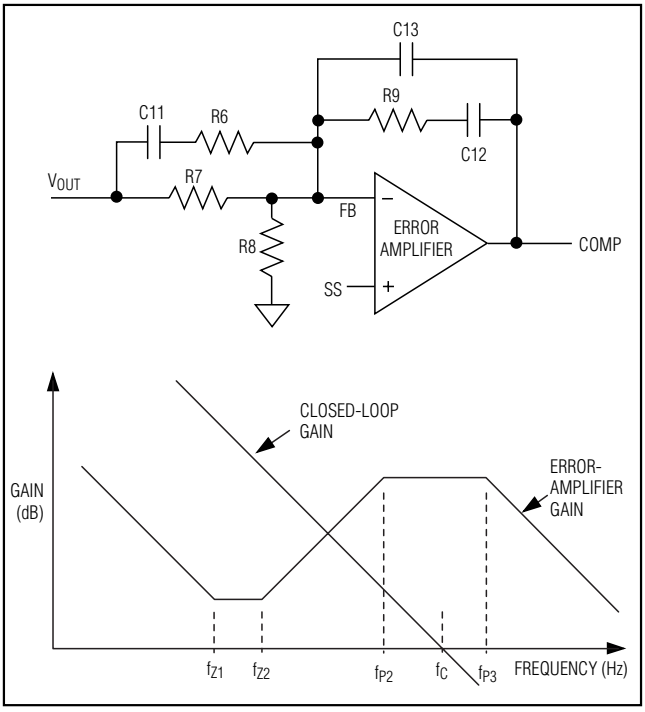


Figure 4. Error-Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Higher ESR Output Capacitors

Compensation when $f_C > f_{ZESR}$

For larger ESR capacitors such as tantalum and aluminum electrolytics, f_{ZESR} can occur before f_C. If $f_{ZESR} < f_C$, then f_C occurs between f_{P2} and f_{P3}. f_{Z1} and f_{Z2} remain the same as before, however, f_{P2} is now set equal to f_{ZESR}. The output capacitor's ESR zero frequency is higher than f_{LC} but lower than the closed-loop crossover frequency. The equations that define the error amplifier's poles and zeros (f_{Z1}, f_{Z2}, f_{P1}, f_{P2}, and f_{P3}) are the same as before. However, f_{P2} is now lower than the closed-loop crossover frequency. Figure 4 shows the error-amplifier feedback as well as its gain response for circuits that use higher-ESR output capacitors (tantalum or aluminum electrolytic).

Pick a value for the feedback resistor R9 in Figure 4 (values between 1kΩ and 10kΩ are adequate).

C12 is then calculated as:

$$C12 = \frac{1}{2\pi \times 0.8 \times f_{LC} \times R9}$$

The error-amplifier gain between f_{P2} and f_{P3} is approximately equal to R9 / R6 (given that R6 << R7). R6 can then be calculated as:

$$R6 = \frac{R9 \times 10 \times f_{LC}^2}{f_C^2}$$

C11 is then calculated as:

$$C11 = \frac{C_{OUT} \times ESR}{R6}$$

Since R7 >> R6, R7 + R6 can be approximated as R7. R7 is then calculated as:

$$R7 = \frac{1}{2\pi \times f_{LC} \times C11}$$

f_{P3} is set at 5 x f_C. Therefore, C13 is calculated as:

$$C13 = \frac{C12}{2\pi \times C12 \times R9 \times f_{P3} - 1}$$

Based on the calculations above, the following compensation values are recommended when the switching frequency of DC-DC converter ranges from 100kHz to 500kHz. (**Note: The compensation parameters in Figure 2 are strongly recommended if the switching frequency is from 300kHz to 500kHz.**)

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Power Dissipation

The MAX15020 is available in a thermally enhanced package and can dissipate up to 2.7W at T_A = +70°C. When the die temperature reaches +160°C, the part shuts down and is allowed to cool. After the parts cool by 20°C, the device restarts with a soft-start.

The power dissipated in the device is the sum of the power dissipated from supply current (P_Q), transition losses due to switching the internal power MOSFET (P_{SW}), and the power dissipated due to the RMS current through the internal power MOSFET (P_{MOSFET}). The total power dissipated in the package must be limited such that the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the MAX15020 using the following equations:

The power loss through the switch:

$$P_{MOSFET} = I_{RMS\_MOSFET}^2 \times R_{ON}$$

$$I_{RMS\_MOSFET} = \sqrt{\left[I_{PK+}^2 + (I_{PK+} \times I_{PK-}) + I_{PK-}\right] \times \frac{D}{3}}$$

$$I_{PK+} = I_{OUT} + \frac{\Delta I_L}{2}$$

$$I_{PK-} = I_{OUT} - \frac{\Delta I_L}{2}$$

R_{ON} is the on-resistance of the internal power MOSFET (see the *Electrical Characteristics* table).

The power loss due to switching the internal MOSFET:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_R \times t_F) \times f_{SW}}{4}$$

where t_R and t_F are the rise and fall times of the internal power MOSFET measured at LX.

The power loss due to the switching supply current (I_{SW}):

$$P_Q = V_{IN} \times I_{SW}$$

The total power dissipated in the device is:

$$P_{TOTAL} = P_{MOSFET} + P_{SW} + P_Q$$

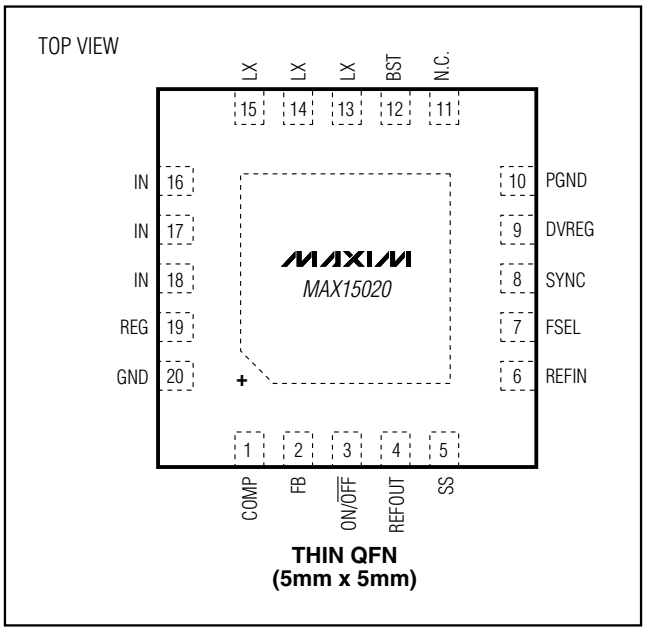
PCB Layout and Routing

Use the following guidelines to layout the switching voltage regulator:

1) Place the IN and DVREG bypass capacitors close to the MAX15020 PGND pin. Place the REG bypass capacitor close to the GND pin.
2) Minimize the area and length of the high-current loops from the input capacitor, switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the switching MOSFET, Schottky diode, and input capacitor.
4) Keep GND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
5) Place the bank of output capacitors close to the load.
6) Distribute the power components evenly across the board for proper heat dissipation.
7) Provide enough copper area at and around the MAX15020 and the inductor to aid in thermal dissipation.
8) Use 2oz copper to keep the trace inductance and resistance to a minimum. Thin copper PCBs can compromise efficiency since high currents are involved in the application. Also, thicker copper conducts heat more effectively, thereby reducing thermal impedance.
9) Place enough vias in the pad for the EP of the MAX15020 so that the heat generated inside can be effectively dissipated by PCB copper.

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Pin Configuration



THIN QFN
(5mm x 5mm)

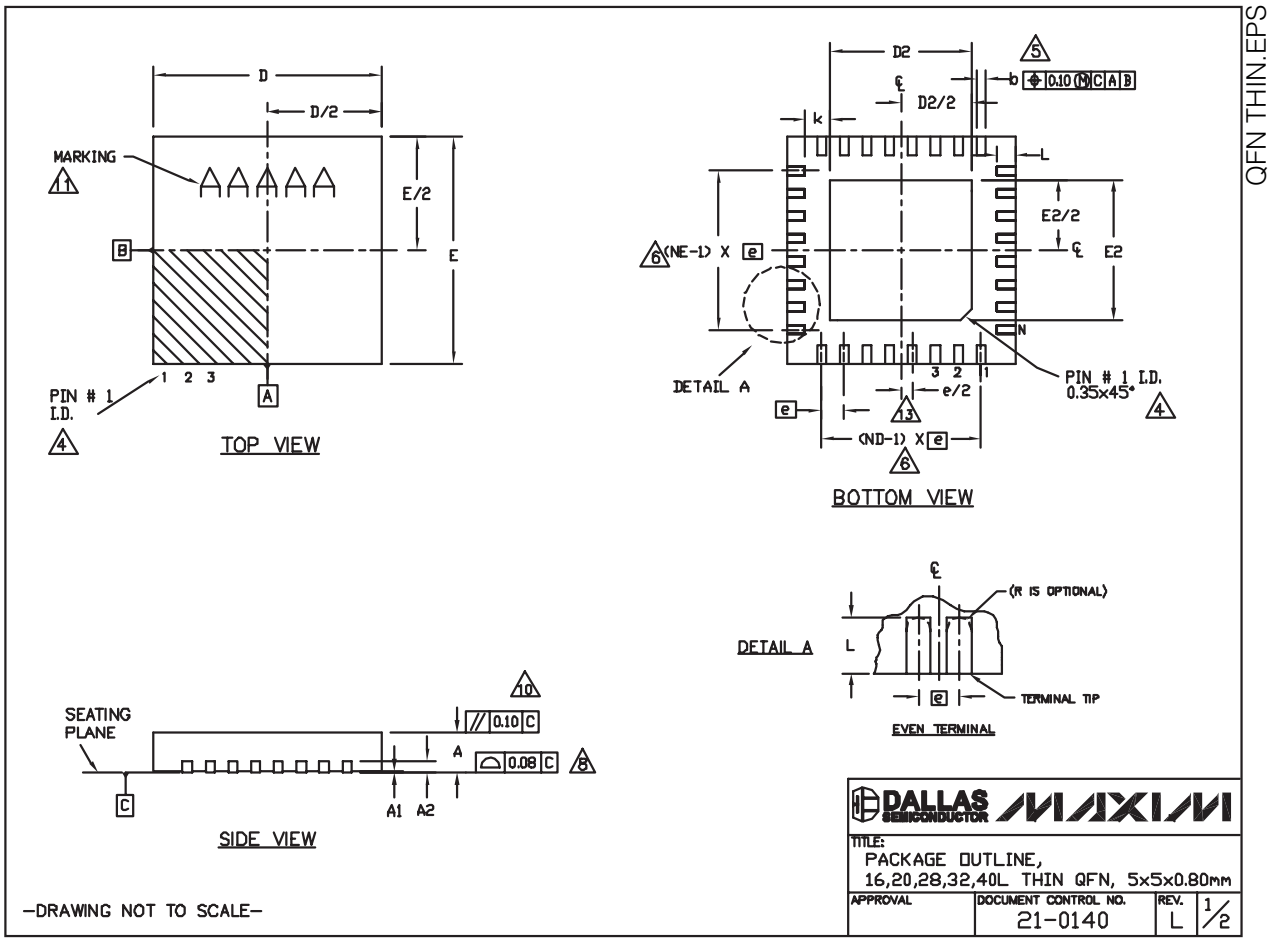
Chip Information

PROCESS: BiCMOS

2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



2A, 40V Step-Down DC-DC Converter with Dynamic Output-Voltage Programming

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

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