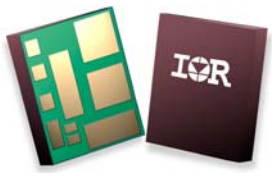
iPOWIR™ TECHNOLOGY

Synchronous Buck Multiphase Optimized LGA Power Block

Integrated Power Semiconductors, Drivers & Passives

Features:

- Full function multiphase building block
- Output current 40A continuous with no derating up to T_{PCB} = 100°C and T_{CASE} = 100°C
- Operating frequency up to 1.0 MHz
- Proprietary packaging enables ultra low $Rth_{j\text{-case top}}$
- Efficient dual sided cooling
- Small footprint low profile (9mm x11mm x 2.2mm) package
- Optimized for very low power losses
- LGA interface
- Ease of design



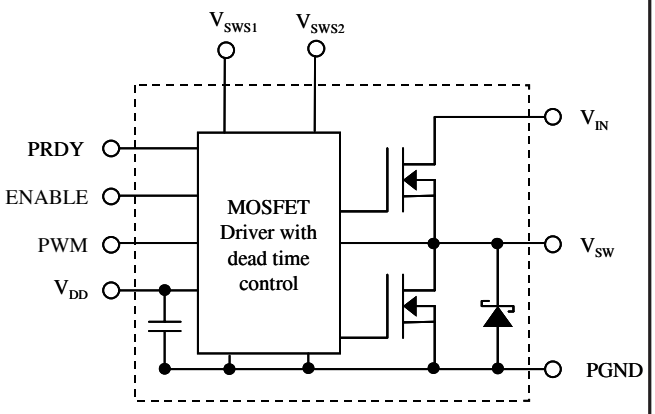
iP2003A Power Block

Description

The iP2003A is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 9mm x 11mm x 2.2mm power block. The only additional components required for a complete multiphase converter are a PWM controller, the output inductors, and the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP2003A Internal Block Diagram



Pin #	Pin Name	Pin Function
1	V_{DD}	Supply voltage for the internal circuitry.
2	ENABLE	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the PRDY pin is forced low, the Control and Sychronous switches are turned off, and the supply current reduces to 10µA.
3	PWM	TTL-level input signal to MOSFET drivers.
4	PRDY	Power Ready - This pin indicates the status of ENABLE or V_{DD}. This output will be driven low when ENABLE is logic low or when V_{DD} is less than 4.4V (typ.). When ENABLE is logic high and V_{DD} is greater than 4.4V (typ.), this output is driven high. This output has a 10mA source and 1mA sink capability.
5, 7	PGND	Power Ground - connection to the ground of bulk and filter capacitors.
6	V_{SW}	Switching Node - connection to the output inductor.
8	V_{IN}	Input voltage pin. External bypass ceramic capacitors must be added directly next to the block.
9	V_{SWS1}	Floating pin. For internal use. Externally, short to V_{SWS2} pin only.
10	V_{SWS2}	Floating pin. For internal use. Externally, short to V_{SWS1} pin only.

All specifications @25°C (unless otherwise specified)

Absolute Maximum Ratings:

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{IN} to PGND	V_{IN}	-	-	16	V	
V_{DD} to PGND	V_{DD}	-	-	6.0	V	
PWM to PGND	PWM	-0.3	-	V_{DD} +0.3	V	Not to exceed 6.0V
Enable to PGND	ENABLE	-0.3	-	V_{DD} +0.3	V	Not to exceed 6.0V
Output RMS Current	I_{OUT}	-	-	40	A	Measured at V_{SW}

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.6	5.0	5.5	V	
Input Voltage	V_{IN}	3.0	-	13.2	V	
Output Voltage	V_{OUT}	0.8	-	3.3	V	
Output Current	I_{OUT}	-	-	40	A	
Operating Frequency	fsw	300	-	1000	kHz	
Operating Duty Cycle	D	-	-	85	%	
Block Temperature	T_{BLK}	-40	-	125	°C	

Electrical Specifications @ V_{DD} = 5V (unless otherwise specified):

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Block Power Loss ①	P_{LOSS}	-	9.4	11.7	W	V_{IN}=12V, V_{OUT}=1.3V
Turn On Delay ②	$t_{d(on)}$	-	63	-	ns	I_{OUT}=40A, f_{SW}=1MHz
Turn Off Delay ②	$t_{d(off)}$	-	26	-		L = 0.3µH
V_{IN} Quiescent Current	I_{Q-VIN}	-	-	1.0	mA	Enable = 0V, V_{IN}=12V
V_{DD} Quiescent Current	I_{Q-VDD}	-	10	-	µA	Enable = 0V, V_{DD}=5V
Under-Voltage Lockout	UVLO					
Start Threshold	V_{START}	4.2	4.4	4.5	V	
Hysteresis	$V_{Hvs-UVLO}$	-	150	-	mV	
Enable	ENABLE					
Input Voltage High	V_{IH}	2.1	-	-	V	
Input Voltage Low	V_{IL}	-	-	0.8		
Power Ready	PRDY					
Logic Level High	V_{OH}	4.5	4.6	-	V	V_{DD}=4.6V, I_{Load}=10mA
Logic Level Low	V_{OL}	-	0.1	0.2		V_{DD} <UVLO Threshold, I_{Load} = 1mA
PWM Input	PWM					
Logic Level High	V_{OH}	2.1	-	-	V	
Logic Level Low	V_{OL}	-	-	0.8		

① Measurement made using six 10uF (TDK C3225X5R1C106KT or equiv.) capacitors across the input (see Fig. 8).

② Not associated with the rise and fall times. Does not affect Power Loss (see Fig. 9).

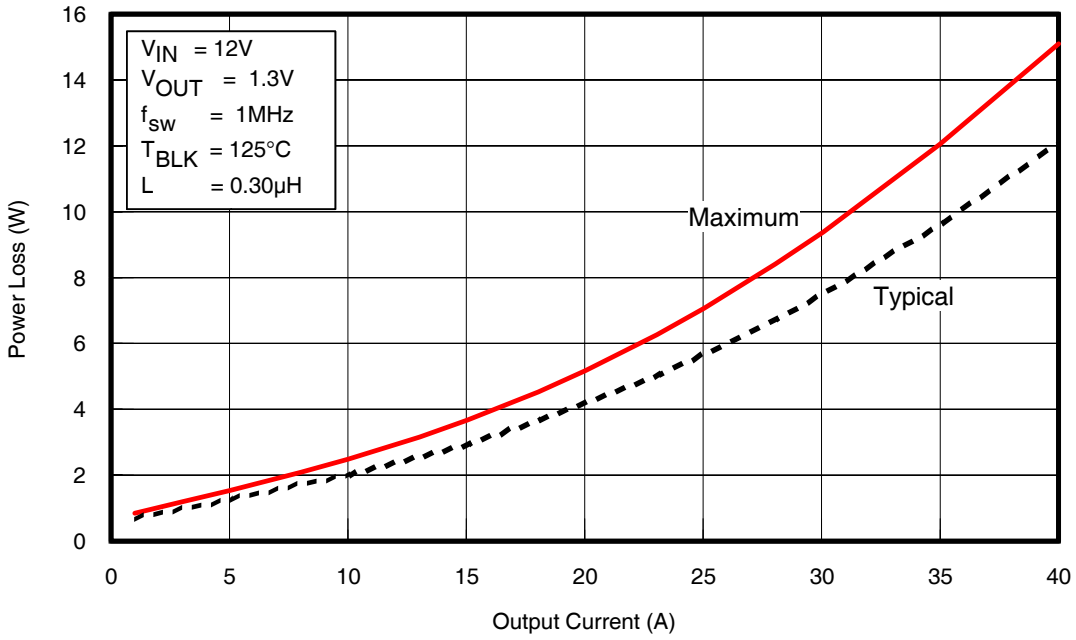


Fig. 1: Power Loss vs. Current

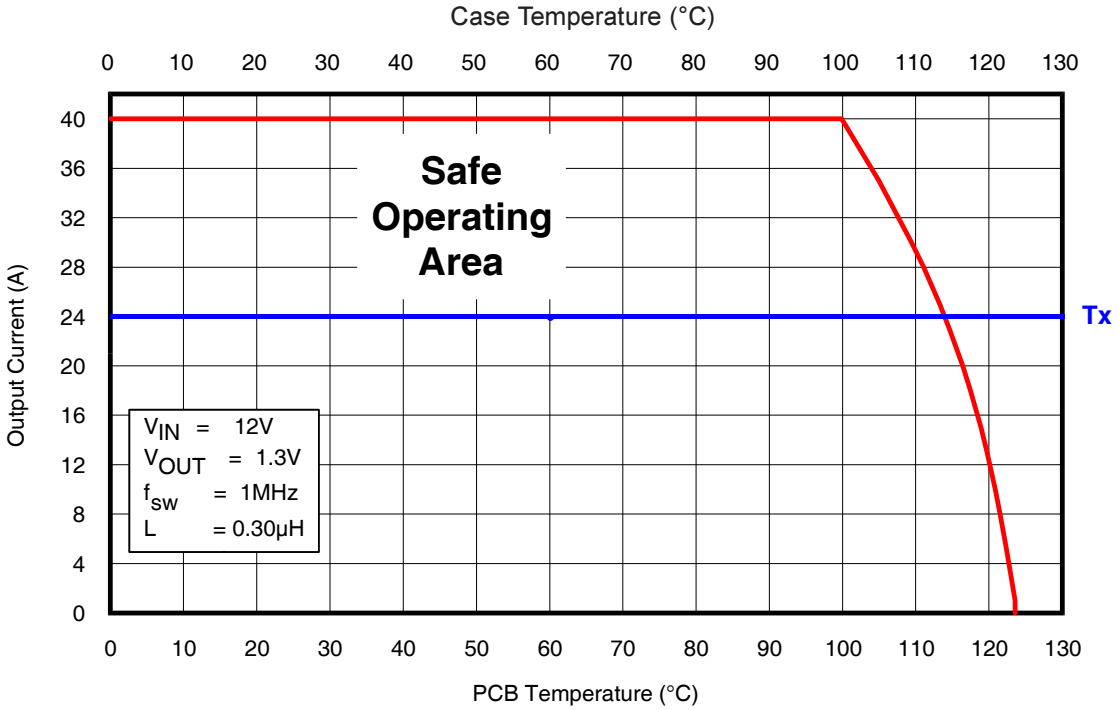


Fig. 2: Safe Operating Area (SOA) vs. T_{PCB} & T_{CASE}

Typical Performance Curves

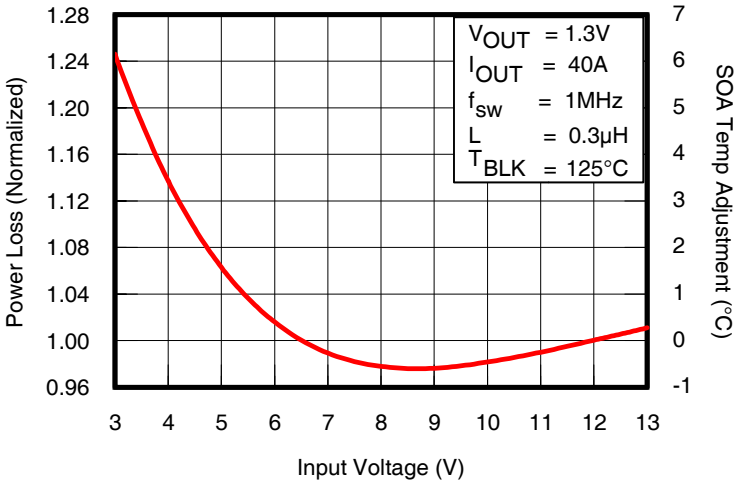


Fig. 3: Normalized Power Loss vs. V_{IN}

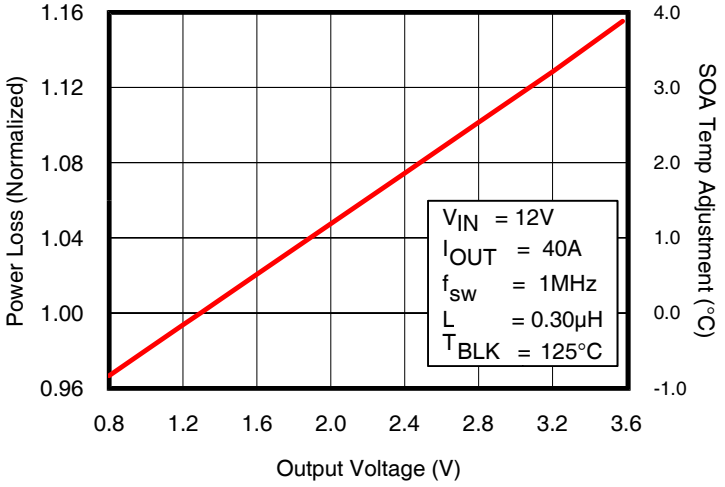


Fig. 4: Normalized Power Loss vs. V_{OUT}

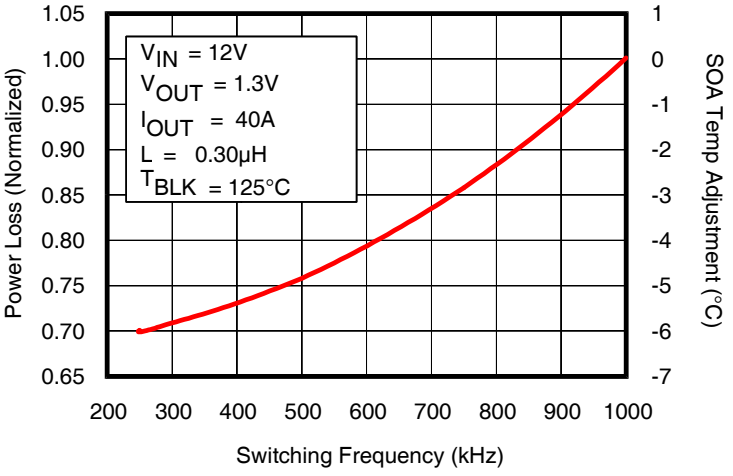


Fig. 5: Normalized Power Loss vs. Frequency

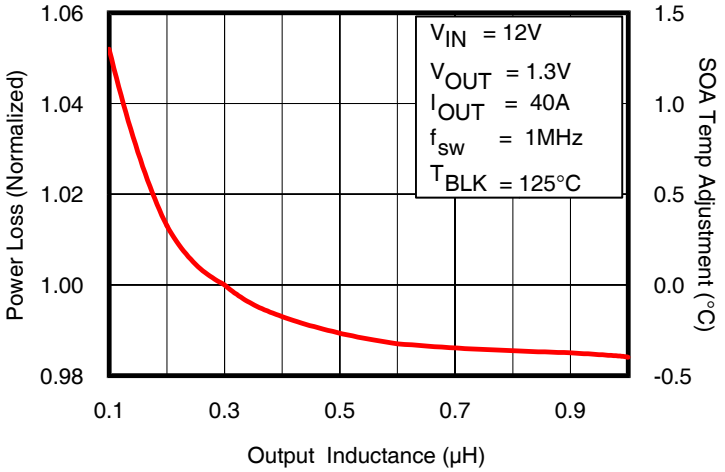


Fig. 6: Normalized Power Loss vs. Inductance

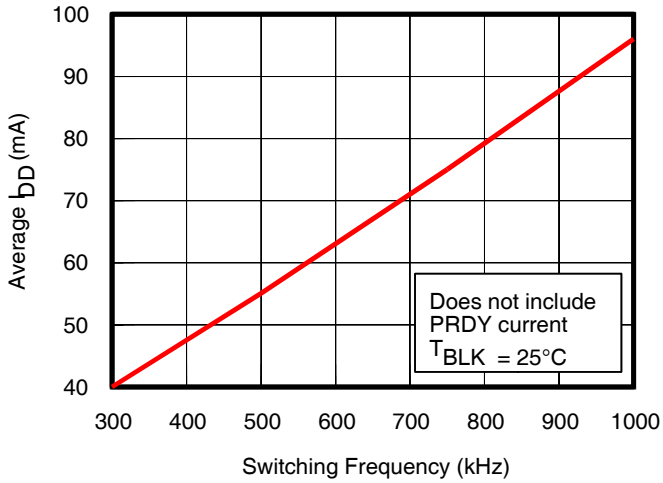


Fig. 7: I_{DD} (V_{DD} current) vs. Frequency

Applying the Safe Operating Area (SOA) Curve

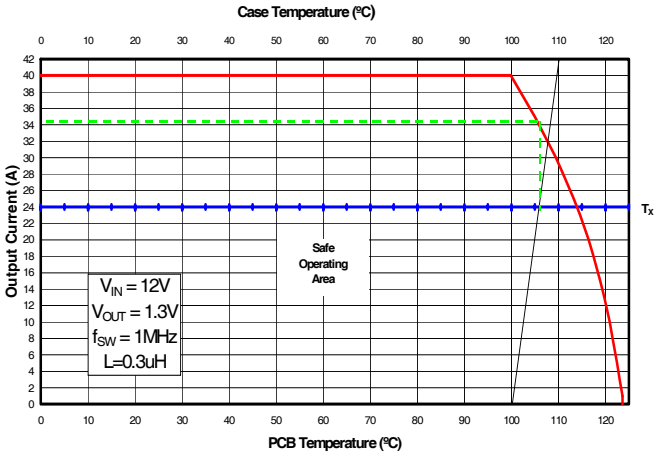
The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case.

Procedure

1) Draw a line from Case Temp axis at T_{CASE} to the PCB Temp axis at T_{PCB}.

2) Draw a vertical line from the T_X axis intercept to the SOA curve.

3) Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis. The point at which the horizontal line meets the Y-axis is the SOA current.



Calculating Power Loss and SOA for Different Operating Conditions

To calculate power loss for a given set of operating conditions, the following procedure should be followed: Determine the maximum current for each iP2003A and obtain the maximum power loss from Fig 1. Use the curves in Figs. 3, 4, 5 and 6 to obtain normalized power loss values that match the operating conditions in the application. The maximum power loss under the operating conditions is then the product of the power loss from Fig. 1 and the normalized values.

To calculate the SOA for a given set of operating conditions, the following procedure should be followed: Determine the maximum PCB temperature and Case temperature at the maximum operating current of each iP2003A. Obtain the SOA temperature adjustments that match the operating conditions in the application from Figs. 3, 4, 5 and 6. Then, add the sum of the SOA temperature adjustments to the Tx axis intercept in Fig 2.

The example below explains how to calculate maximum power loss and SOA.

Example:

Operating Conditions

Output Current = 40A | Input Voltage = 10V | Output Voltage = 3.3V
Sw Freq= 900kHz | Inductor = 0.2µH | T_{PCB} = 100°C, T_{CASE} = 110°C

Calculating Maximum Power Loss:

(Fig. 1) Maximum power loss = 15W
(Fig. 3) Normalized power loss for input voltage ≈ 0.98
(Fig. 4) Normalized power loss for output voltage ≈ 1.14
(Fig. 5) Normalized power loss for frequency ≈ 0.94
(Fig. 6) Normalized power loss for inductor value ≈ 1.013

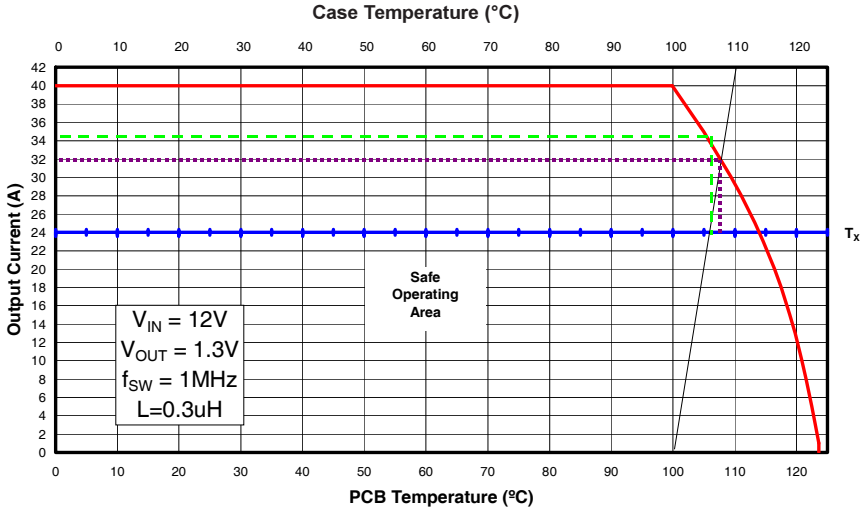
Calculated Maximum Power Loss for given conditions = 15W x 0.98 x 1.14 x 0.94 x 1.013 ≈ 15.96W

Calculating SOA Temperature:

(Fig. 3) SOA Temperature Adjustment for input voltage ≈ -0.5°C
(Fig. 4) SOA Temperature Adjustment for output voltage ≈ 3.3°C
(Fig. 5) SOA Temperature Adjustment for frequency ≈ -1.2°C
(Fig. 6) SOA Temperature Adjustment for inductor value ≈ 0.25°C

T_X axis intercept temp adjustment = - 0.5°C + 3.3°C - 1.2°C + 0.25°C ≈ 1.85°C

Assuming T_{CASE} = 110°C & T_{PCB} = 100°C:
The following example shows how the SOA current is adjusted for a T_X increase of 1.85°C.



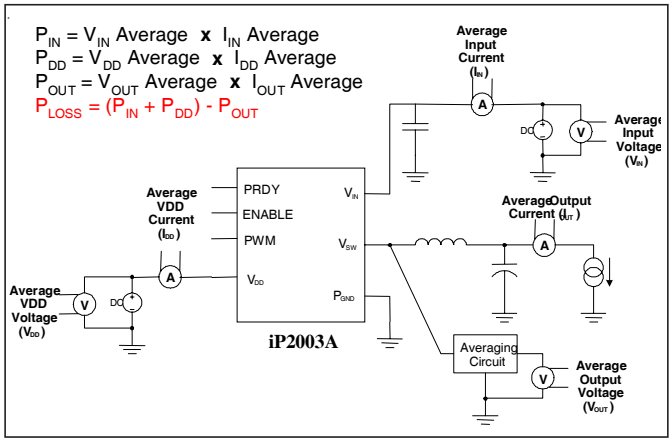


Fig. 8: Power Loss Test Circuit

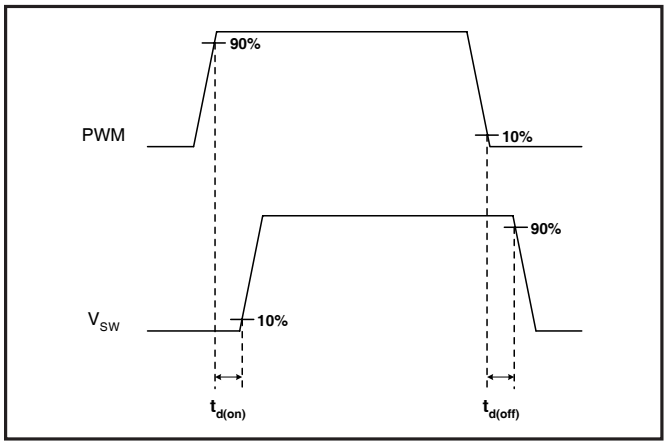


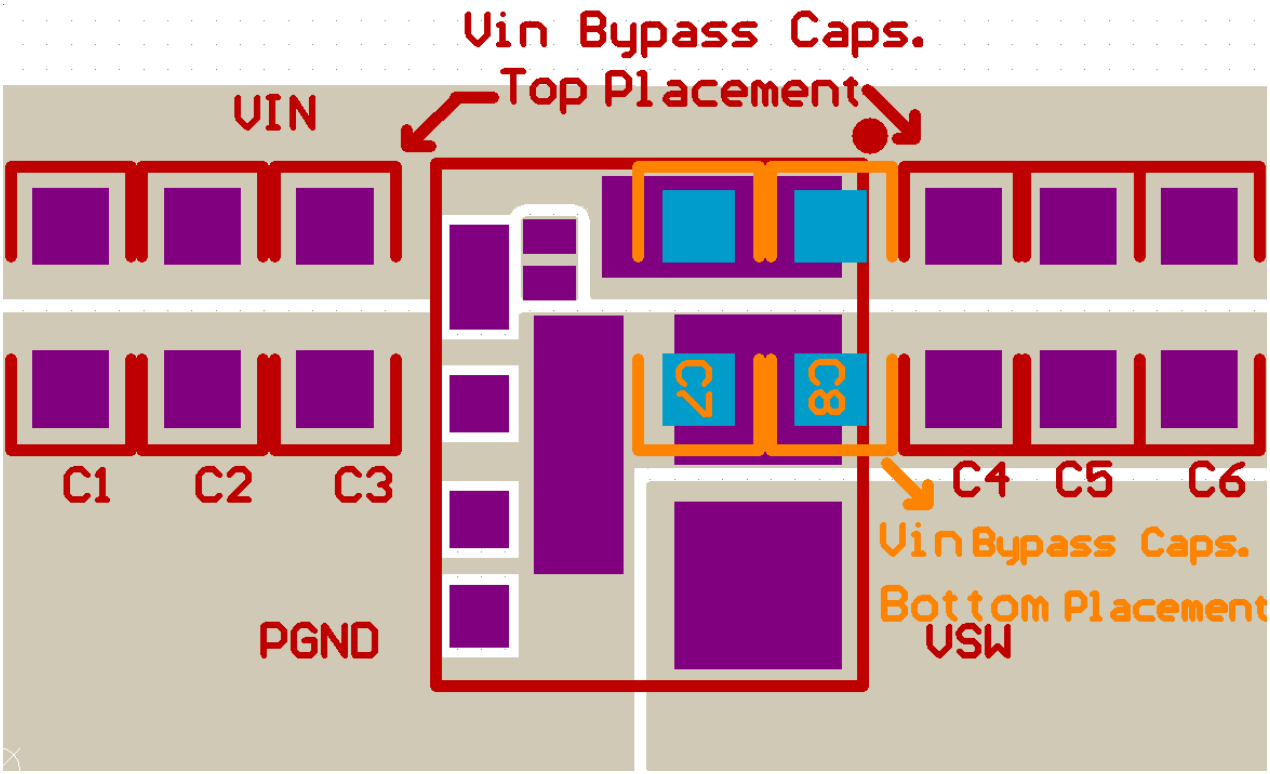
Fig. 9: Timing Diagram

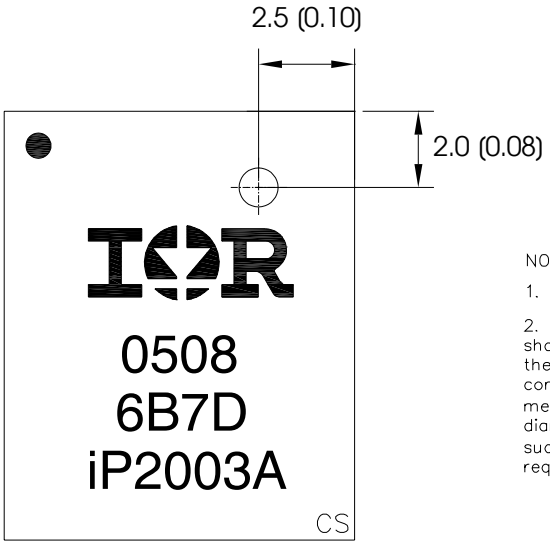
PCB Layout Guidelines

One of the most critical elements of proper PCB layout with iP2003A is the placement of the external input bypass capacitors and the routing of the connecting power tracks.

It is recommended that the designer uses the following guidelines:

1. The diagram below suggests the addition of the input bypass capacitors either on the top side of the PCB (capacitors C1-C6) or top and bottom side (C7, C8), if placement on the bottom side is feasible. The amount of the input capacitors is based on the input ripple current handling requirement of the iP2003A. To support 12A input RMS current, based on 12V input, 1.3V and 40A output and 1MHz, the iP2003A will require enough input ceramic capacitors to support the input RMS AC current. These capacitors must be placed as close to the iPOWIR device as possible.
2. In the diagram below, observe the routing of the power tracks that connect the external bypass capacitors.
3. Provide a mid-layer solid ground plane with connections to the top through vias.
4. Refer to IR application note AN-1029a to determine the size of the vias and the copper weight and thickness when designing the PCB.



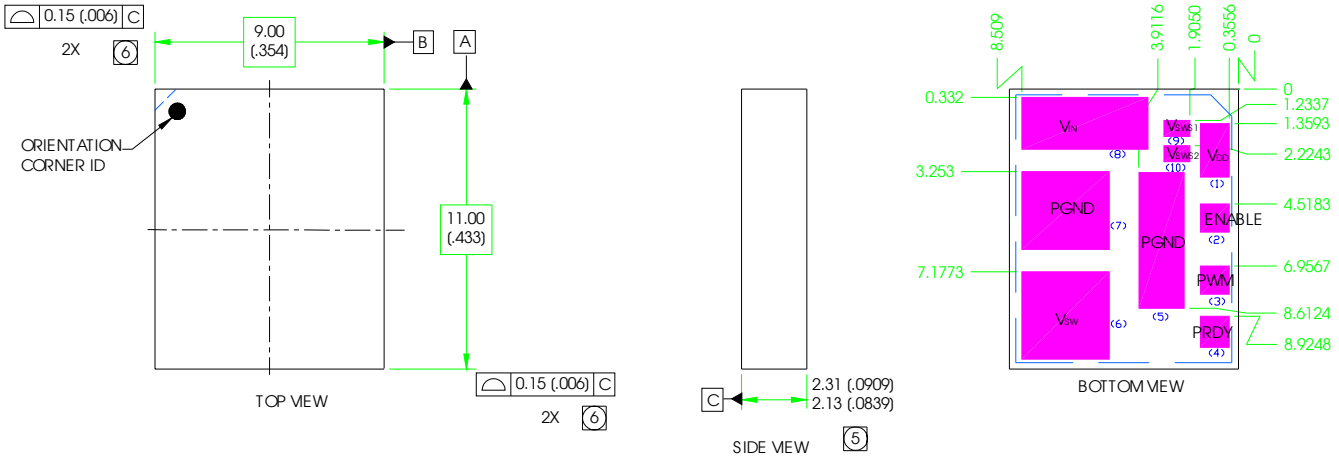


NOTE:

1. Dimensions are in mm[inch].

2. The dimensions refer to the location at which the case temperature should be measured for SOA calculations. In applications with no heatsink, the most accurate method is to use an infra-red camera with emissivity correction. When a heatsink is installed on the module, the most accurate method involves drilling a hole in the heatsink approximately 0.040" in diameter and probing the case temperature with a sheathed thermocouple such as OMEGA P/N KMTSS-020G-12. Contact the factory if assistance is required.

Fig 10: Maximum T_{CASE} measurement location



DIMENSION		NOMINAL	DIMENSION		NOMINAL
(1)	X	1.1430	(6)	X	3.429
	Y	2.1016		Y	3.429
(2),(3)	X	1.1430	(7)	X	3.429
	Y	1.1016		Y	3.048
(4)	X	1.1430	(8)	X	4.953
	Y	1.2192		Y	2.032
(5)	X	1.778	(9),(10)	X	1.016
	Y	5.334		Y	0.635
REF	JEDEC:MO-222				

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: MILLIMETER
4. LAND DESIGNATION PER JESD MO 222, SPP-010.

5 PRIMARY DATUM C IS SEATING PLANE.

6 BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.

LAYOUT NOTES:

1. LAND PATTERN ON USER'S PCB SHOULD BE AN IDENTICAL MIRROR IMAGE OF THE PATTERN SHOWN IN THE BOTTOM VIEW.
2. LANDS SHOULD BE SOLDER MASK DEFINED.

Fig 11: Mechanical Drawing

Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR Technology products:

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

AN-1047: Graphical solution for two branch heatsinking Safe Operating Area
Detailed explanation of the dual axis SOA graph and how it is derived.

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's BGA and LGA Packages
This paper discusses optimization of the layout design for mounting iPowIR BGA and LGA packages on printed circuit boards, accounting for thermal and electrical performance and assembly considerations . Topics discussed includes PCB layout placement, routing, and via interconnect suggestions, as well as soldering, pick and place, reflow, cleaning and reworking recommendations.

AN-1029a: Optimizing a PCB Layout for an iPowir Technology Design

IRDCiP2003A : Reference design for iP2003A

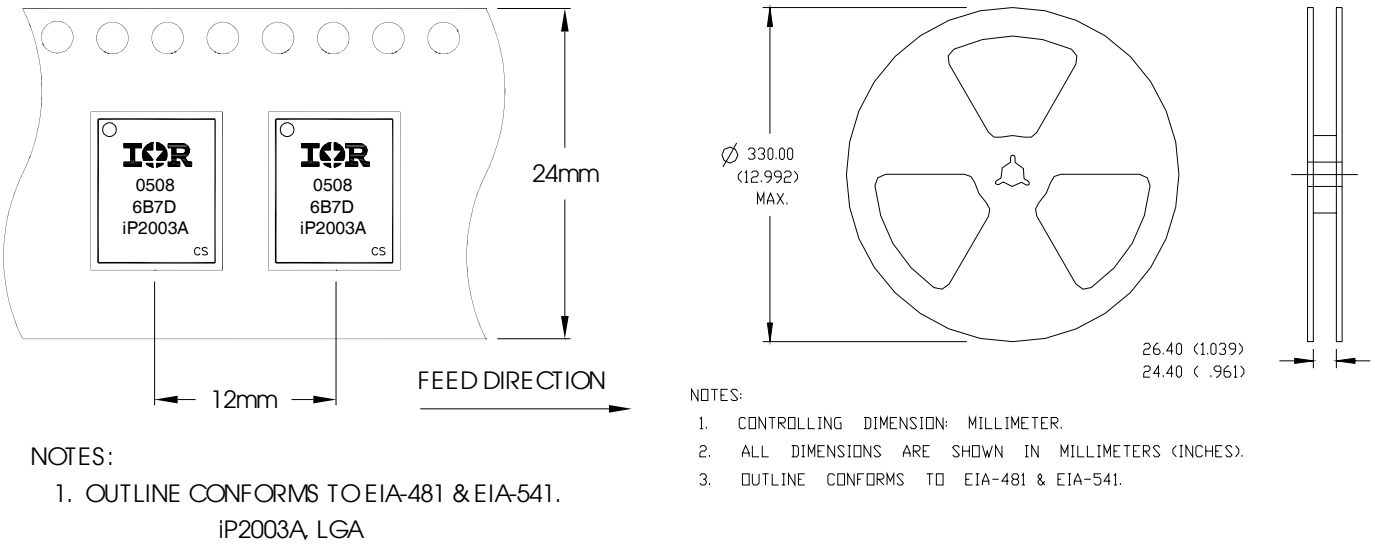


Fig. 12: Tape & Reel Information

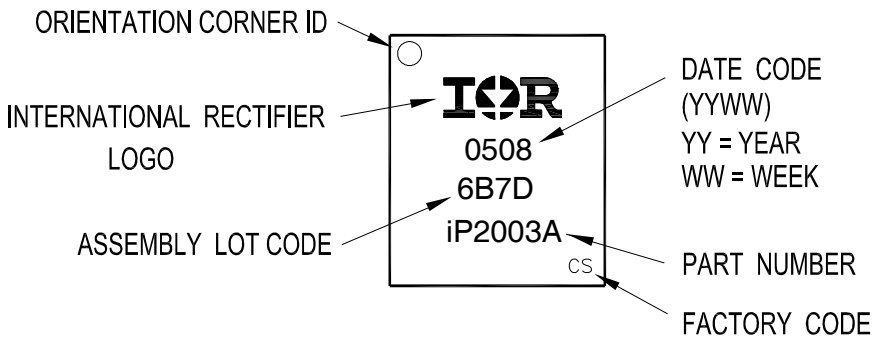
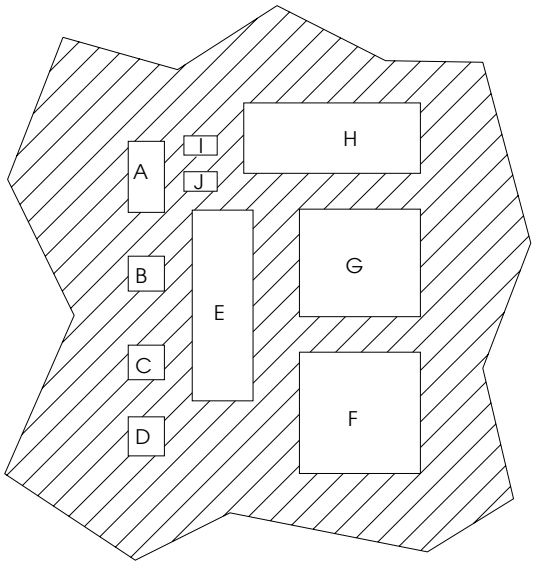


Fig. 13: Part Marking



STENCIL DESIGN

DIMENSION		NOMINAL	DIMENSION		NOMINAL
A	X	0.9906	F	X	3.3274
	Y	1.9492		Y	3.3274
B,C	X	0.9906	G	X	3.3274
	Y	0.9492		Y	2.9464
D	X	0.9906	H	X	4.8514
	Y	1.0668		Y	1.9304
E	X	1.6764	I,J	X	0.9144
	Y	5.2324		Y	0.5334

NOTES:
1. THIS VIEW IS STENCIL SQUEEGEE VIEW
2. DIMENSIONS ARE SHOWN IN MILLIMETERS.
3. THIS OPENING IS BASED ON USING 150 MICRON STENCIL. IF USING DIFFERENT THICKNESS STENCIL, THIS OPENING NEEDS TO BE ADJUSTED ACCORDINGLY

The recommended reflow peak temperature is 220°C to 225°C. The total furnance time is approximately 5 minutes with approximately 10 seconds at the peak temperature.

Fig.14: Recommended solder profile and stencil design

International
IOR Rectifier

Data and specifications subject to change without notice.

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