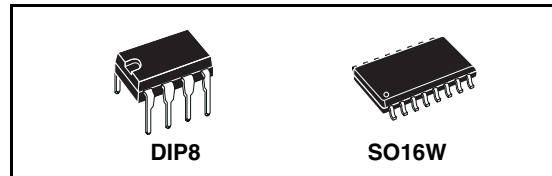


## 1A step down switching regulator

### Features

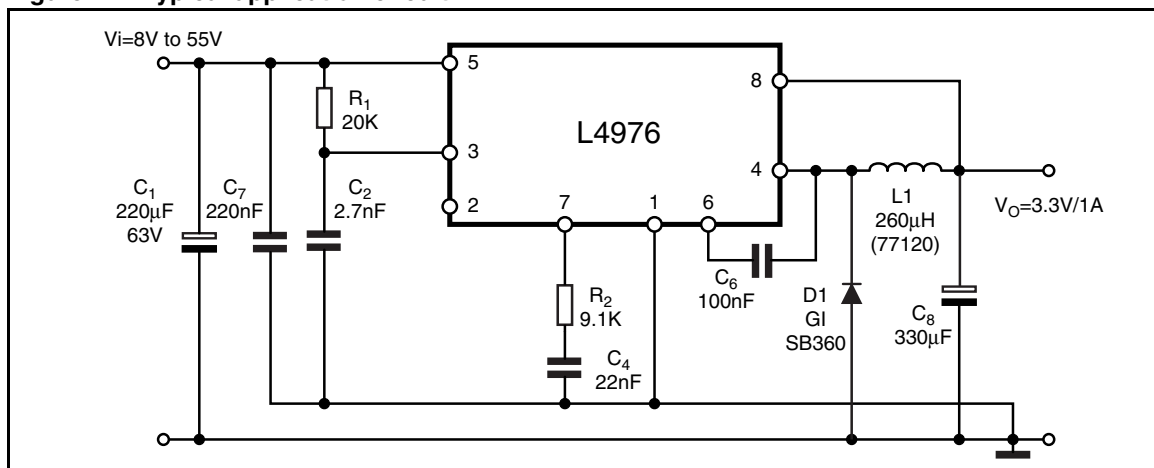
- Up to 1A step down converter
- Operating input voltage from 8v to 55v
- Precise 5.1V reference voltage
- Output voltage adjustable from 0.5V to 50V
- Switching frequency adjustable up to 300kHz
- Voltage feedforward
- Zero load current operation
- Internal current limiting (pulse-by-pulse and hiccup mode)
- Protection against feedback disconnection
- Thermal shutdown



### Description

The L4976 is a step down monolithic power switching regulator delivering 1A at a voltage between 3.3V and 50V (selected by a simple external divider). Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical  $R_{ds(ON)}$  of  $0.25\Omega$ ) to obtain very high efficiency and high switching speed. A switching frequency up to 300KHz is achievable (the maximum power dissipation of the packages must be observed). A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 40V cover the majority of today's applications. Features of this new generations of DC-DC converter include pulse-by-pulse current limit, hiccup mode for short circuit protection, voltage feedforward regulation, protection against feedback loop disconnection and thermal shutdown. The device is available in plastic dual in line, MINIDIP 8 for standard assembly, and SO16W for SMD assembly.

**Figure 1. Typical application circuit**

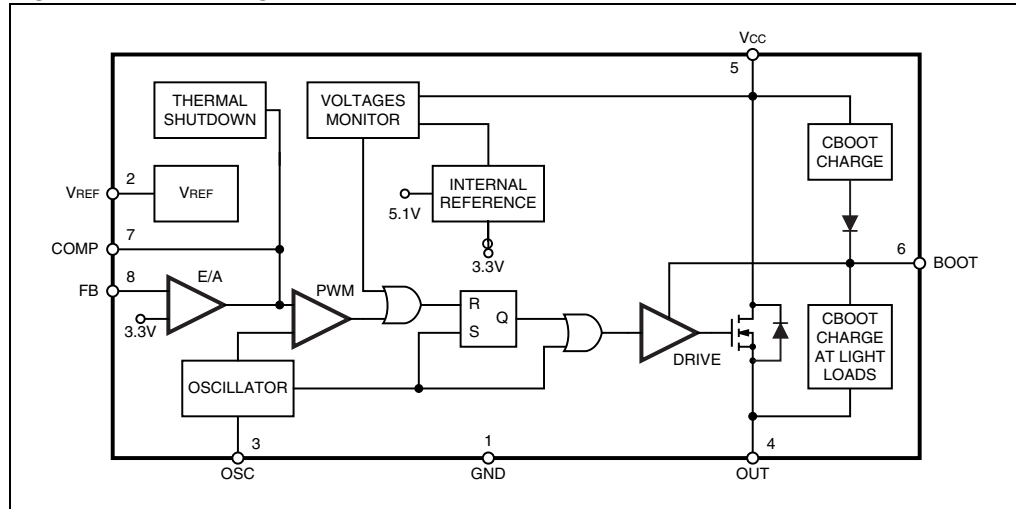


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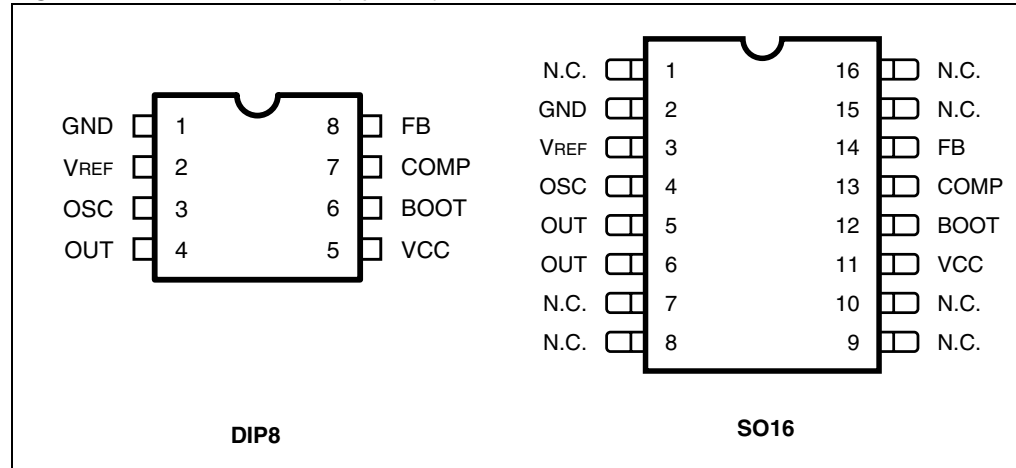
# 1 Block diagram

**Figure 2. Block diagram**

## 2 Pin settings

### 2.1 Pin connection

Figure 3. Pin connection (top view)



### 2.2 Pin description

Table 1. Pin description

N° Pin		Name	Description
DIP8	SO16W <sup>(1)</sup>		
1	2	GND	Ground
2	3	VREF	5.1V Reference voltage with 20mA current capability.
3	4	OSC	An external resistor connected between the unregulated input voltage and this pin and a capacitor connected from this pin to ground fix the switching frequency. (Line feed forward is automatically obtained)
4	5, 6	OUT	Stepdown regulator output.
5	11	VCC	Unregulated DC input voltage.
6	12	BOOT	A capacitor connected between this pin and OUT allows to drive the internal VDMOS.
7	13	COMP	E/A output to be used for frequency compensation.
8	14	FB	Stepdown feedback input. Connecting directly to this pin results in an output voltage of 3.3V. An external resistive divider is required for higher output voltages.

1. Pins 1, 7, 8, 9, 10, 15 and 16 are not internally, electrically connected to the die.

### 3 Electrical data

#### 3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol		Parameter	Value	Unit	
DIP8	S016W				
V5	V11	Input voltage	58	V	
V4	V5, V6	Output DC voltage	-1	V	
		Output peak voltage at $t = 0.1\mu\text{s}$ , $f = 200\text{kHz}$	-5	V	
I4	I5, I6	Maximum output current	internal limit		
V6-V5	V12-V11		14	V	
V6	V12	Bootstrap voltage	70	V	
V7	V13	Analogs input voltage ( $V_{CC} = 24\text{V}$ )	12	V	
V8	V14	$(V_{CC} = 20\text{V})$	6	V	
			-0.3	V	
$P_{TOT}$		Power dissipation a $T_A \leq 60^\circ\text{C}$	DIP8	1	W
			SO16	0.8	W
$T_J, T_{STG}$		Junction and storage temperature	-40 to 150	$^\circ\text{C}$	

#### 3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	DIP8	S016W	Unit
$R_{thJA}$	Maximum thermal resistance junction-ambient	90 <sup>(1)</sup>	110 <sup>(1)</sup>	$^\circ\text{C/W}$

1. Package mounted on board

#### 3.3 Operating temperature rating

Table 4. Operating temperature rating

Symbol	Parameter	Value	Unit
$T_J$	Junction temperature range	-40 to 150	$^\circ\text{C}$

## 4 Electrical characteristics

**Table 5. Electrical characteristics**

( $T_J = 25^\circ\text{C}$ ,  $C_{\text{OSC}} = 2.7\text{nF}$ ,  $R_{\text{OSC}} = 20\text{k}\Omega$ ,  $V_{\text{CC}} = 24\text{V}$ , unless otherwise specified.)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>Dynamic characteristic</b>						
$V_I$	Operating input voltage range	$V_O = 3.3$ to $50\text{V}$ ; $I_O = 1\text{A}$ <sup>(1)</sup>	8		55	V
$V_O$	Output voltage	$I_O = 0.5\text{A}$	3.33	3.36	3.39	V
		$I_O = 0.2$ to $1\text{A}$	3.292	3.36	3.427	V
		$V_{\text{CC}} = 8$ to $55\text{V}$ <sup>(1)</sup>	3.22	3.36	3.5	V
$V_d$	Dropout voltage	$V_{\text{CC}} = 10\text{V}$ ; $I_O = 1\text{A}$		0.29	0.367	V
		<sup>(1)</sup>			0.587	V
$I_l$	Maximum limiting current	$V_{\text{CC}} = 8$ to $55\text{V}$ <sup>(1)</sup>	1.5	2	2.5	A
	Efficiency	$V_O = 3.3\text{V}$ ; $I_O = 1\text{A}$		85		%
$f_s$	Switching frequency	<sup>(1)</sup>	90	100	110	KHz
SVRR	Supply voltage ripple rejection	$V_I = V_{\text{CC}} + 2V_{\text{RMS}}$ ; $V_O = V_{\text{ref}}$ ; $I_O = 1\text{A}$ ; $f_{\text{ripple}} = 100\text{Hz}$	60			dB
	Voltage stability of switching frequency	$V_{\text{CC}} = 8$ to $55\text{V}$		3	6	%
	Temp. stability of switching frequency	$T_J = 0$ to $125^\circ\text{C}$		4		%
<b>Reference section</b>						
	Reference voltage		5.0	5.1	5.2	V
		$I_{\text{ref}} = 0$ to $10\text{mA}$ ; <sup>(1)</sup>	4.950	5.1	5.250	V
		$V_{\text{CC}} = 8$ to $55\text{V}$				
	Line regulation	$I_{\text{ref}} = 0\text{mA}$ ;		5	10	mV
		$V_{\text{CC}} = 8$ to $55\text{V}$				
	Load regulation	$V_{\text{ref}} = 0$ to $5\text{mA}$ ;		2	10	mV
		$V_{\text{CC}} = 0$ to $20\text{mA}$		6	25	mV
	Short circuit current		30	65	100	mA

Table 5. Electrical characteristics (continued)

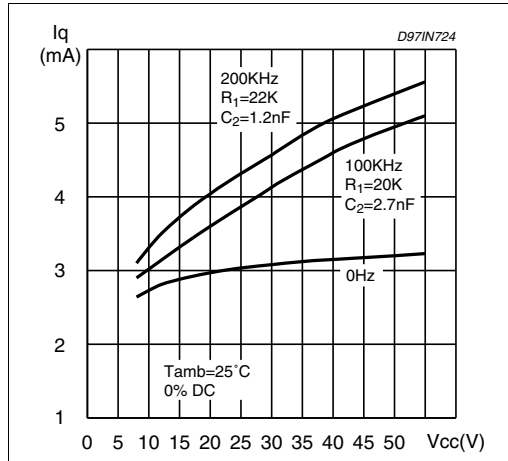
(T<sub>J</sub> = 25°C, C<sub>OSC</sub> = 2.7nF, R<sub>OSC</sub> = 20kΩ, V<sub>CC</sub> = 24V, unless otherwise specified.)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>DC Characteristics</b>						
I <sub>qop</sub>	Total operating quiescent current			4	6	mA
I <sub>q</sub>	Quiescent current	Duty Cycle = 0; V <sub>FB</sub> = 3.8V		2.5	3.5	mA
<b>Error Amplifier</b>						
V <sub>FB</sub>	Voltage feedback input		3.33	3.36	3.39	V
R <sub>L</sub>	Line regulation	V <sub>CC</sub> = 8 to 55V		5	10	mV
	Ref. voltage stability vs temperature	(1)		0.4		mV/°C
V <sub>oH</sub>	High level output voltage	V <sub>FB</sub> = 2.5V	10.3			V
V <sub>oL</sub>	Low level output voltage	V <sub>FB</sub> = 3.8V			0.65	V
I <sub>O source</sub>	Source output current	V <sub>comp</sub> = 6V; V <sub>FB</sub> = 2.5V	180	220		μA
I <sub>O sink</sub>	Sink output current	V <sub>comp</sub> = 6V; V <sub>FB</sub> = 3.8V	200	300		μA
I <sub>b</sub>	Source bias current			2	3	μA
SVRR E/A	Supply voltage ripple rejection	V <sub>comp</sub> = Vfb; V <sub>CC</sub> = 8 to 55V	60	80		dB
	DC open loop gain	R <sub>L</sub> = ∞	50	57		dB
gm	Transconductance	I <sub>comp</sub> = -0.1 to 0.1mA V <sub>comp</sub> = 6V		2.5		ms
<b>Oscillator section</b>						
	Ramp valley		0.78	0.85	0.92	V
	Ramp peak	V <sub>CC</sub> = 8V	2	2.15	2.3	V
		V <sub>CC</sub> = 55V	9	9.6	10.2	V
	Maximum duty cycle		95	97		%
	Maximum frequency	Duty cycle = 0% R <sub>osc</sub> = 13kW, C <sub>osc</sub> = 820pF			300	kHz

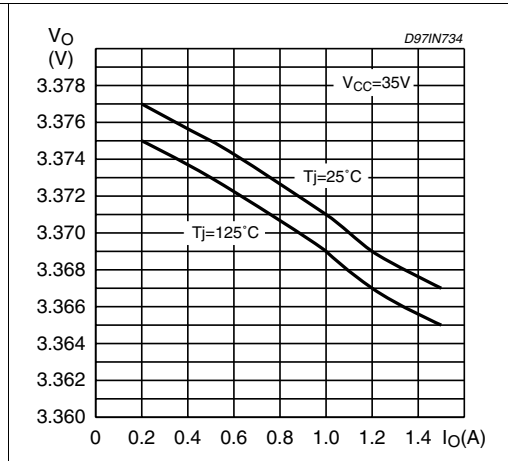
1. Specification referred to T<sub>J</sub> from 0 to 125°C

# 5 Typical characteristics

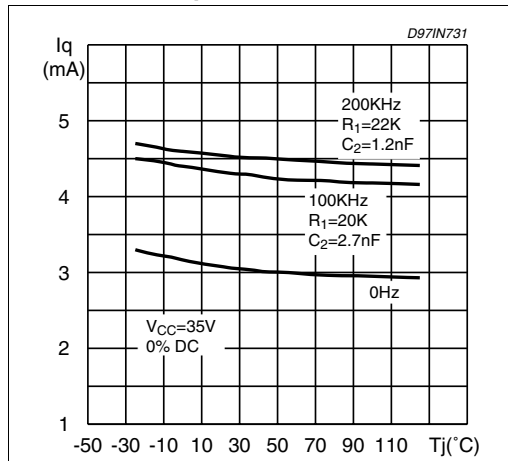
**Figure 4. Quiescent drain current vs. input voltage**



**Figure 5. Line regulation**



**Figure 6. Quiescent current vs. junction temperature**



**Figure 7. Switching frequency vs. R1 and C2**

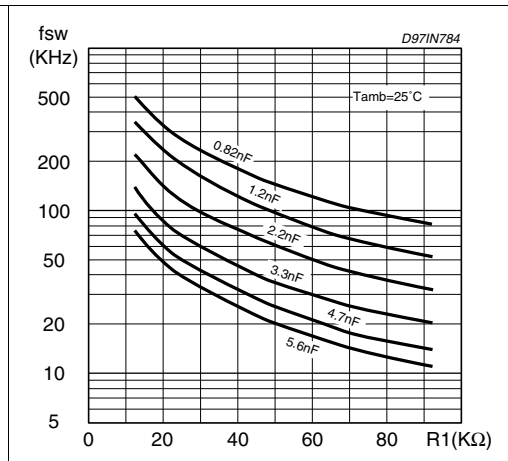




Figure 8. Load regulation

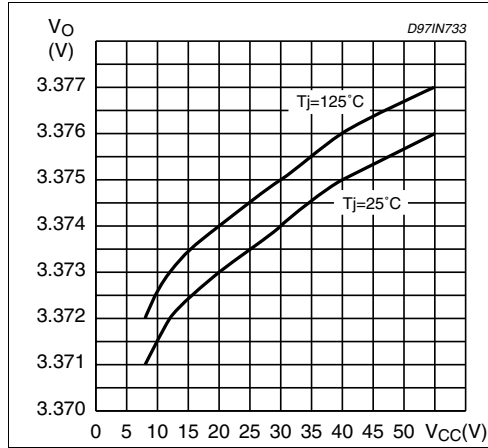


Figure 9. Switching frequency vs. input voltage

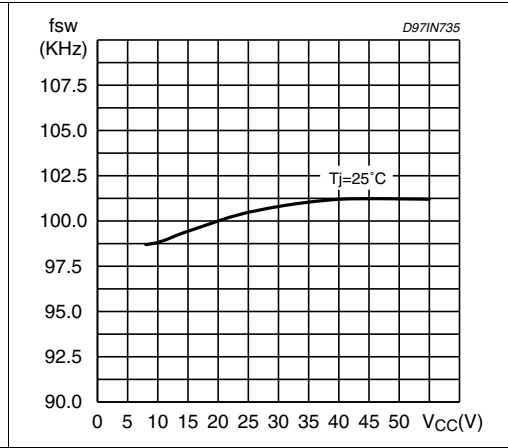


Figure 10. Switching frequency vs. junction temperature

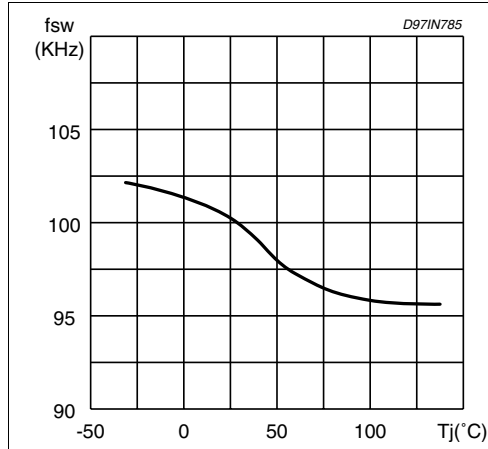


Figure 11. Efficiency vs. output current

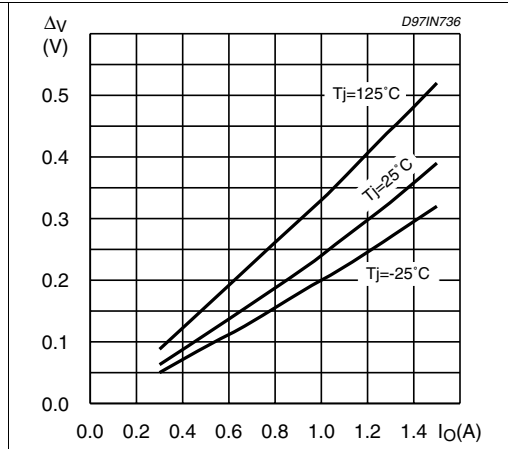


Figure 12. Dropout voltage between pin 5 and 4

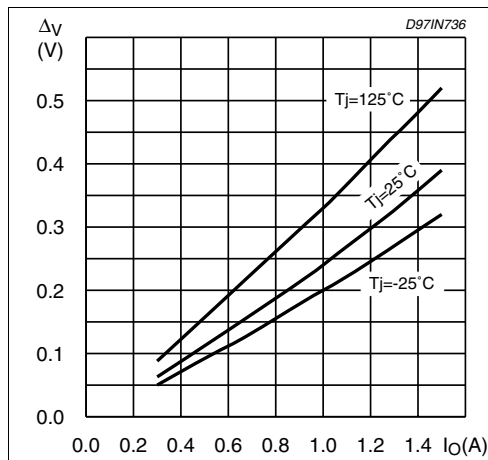


Figure 13. Efficiency vs. output current

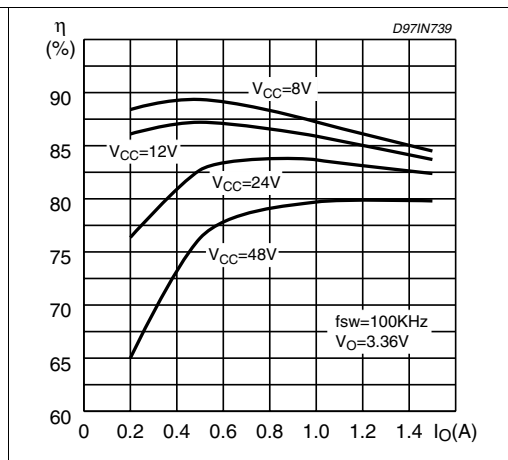


Figure 14. Efficiency vs output voltage

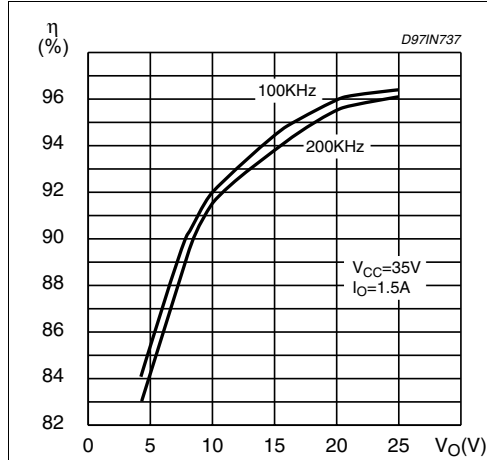


Figure 15. Efficiency vs. output current

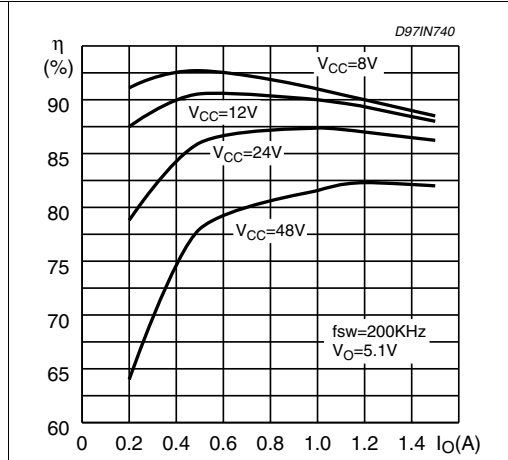


Figure 16. Efficiency vs. output current

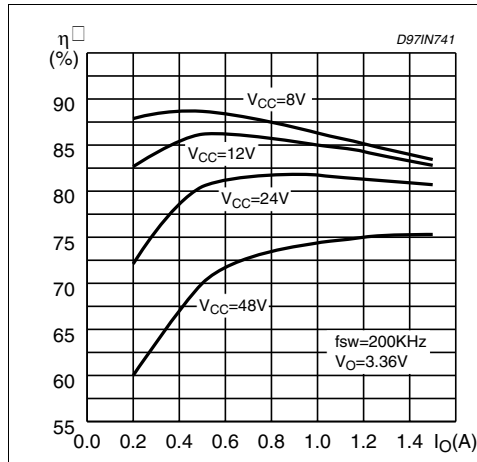


Figure 17. Efficiency vs. V\_o

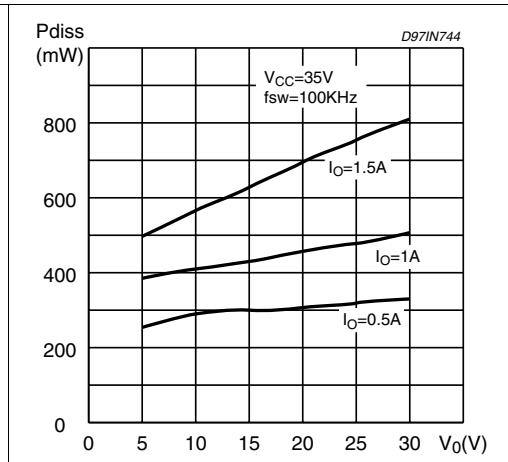


Figure 18. Efficiency vs. V<sub>CC</sub>

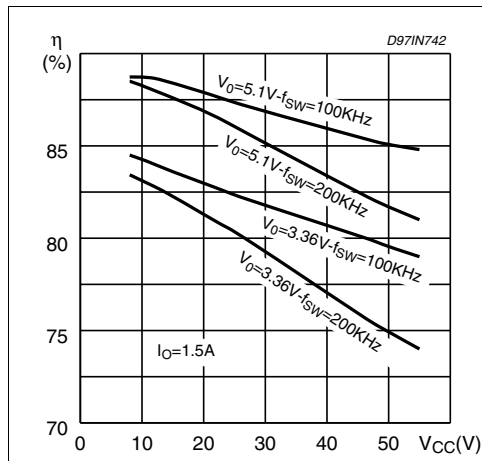


Figure 19. Pulse by pulse limiting current vs. junction temperature.

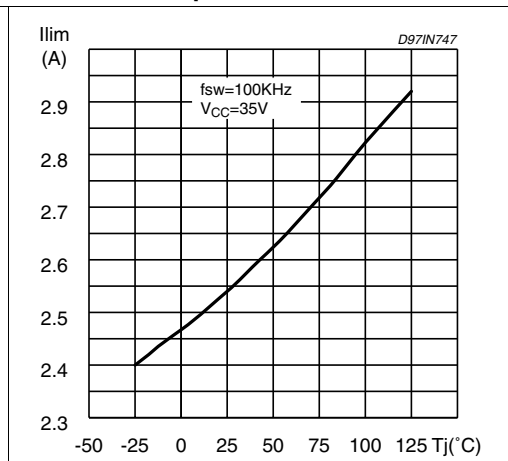


Figure 20. Power dissipation vs.  $V_{CC}$

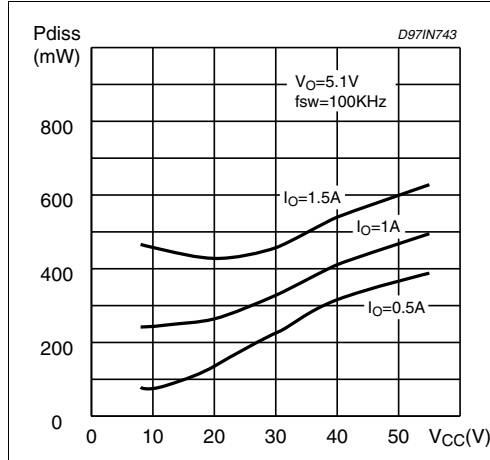


Figure 21. Load transient

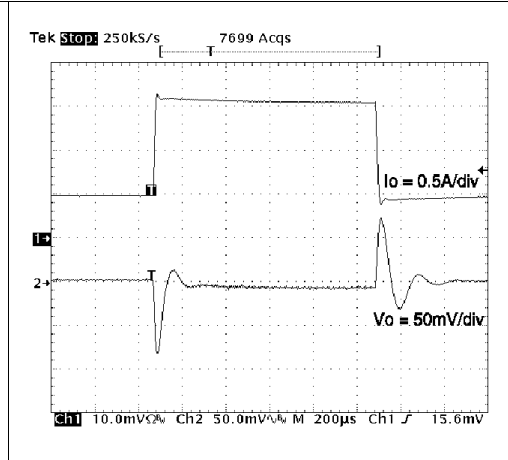


Figure 22. Line transient

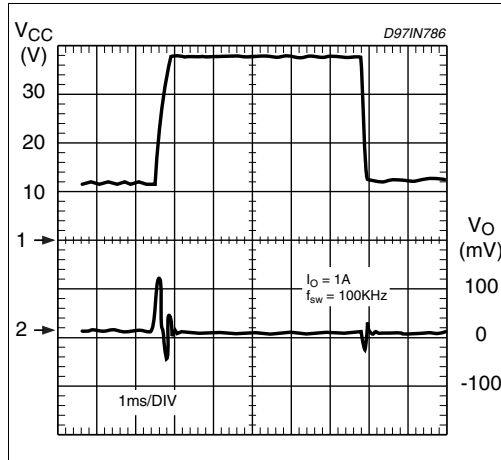
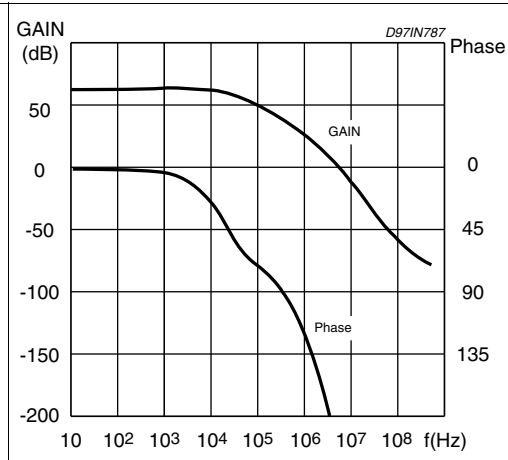


Figure 23. Open loop frequency and phase of error amplifier



## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Figure 24. DIP8 mechanical data &amp; package dimensions

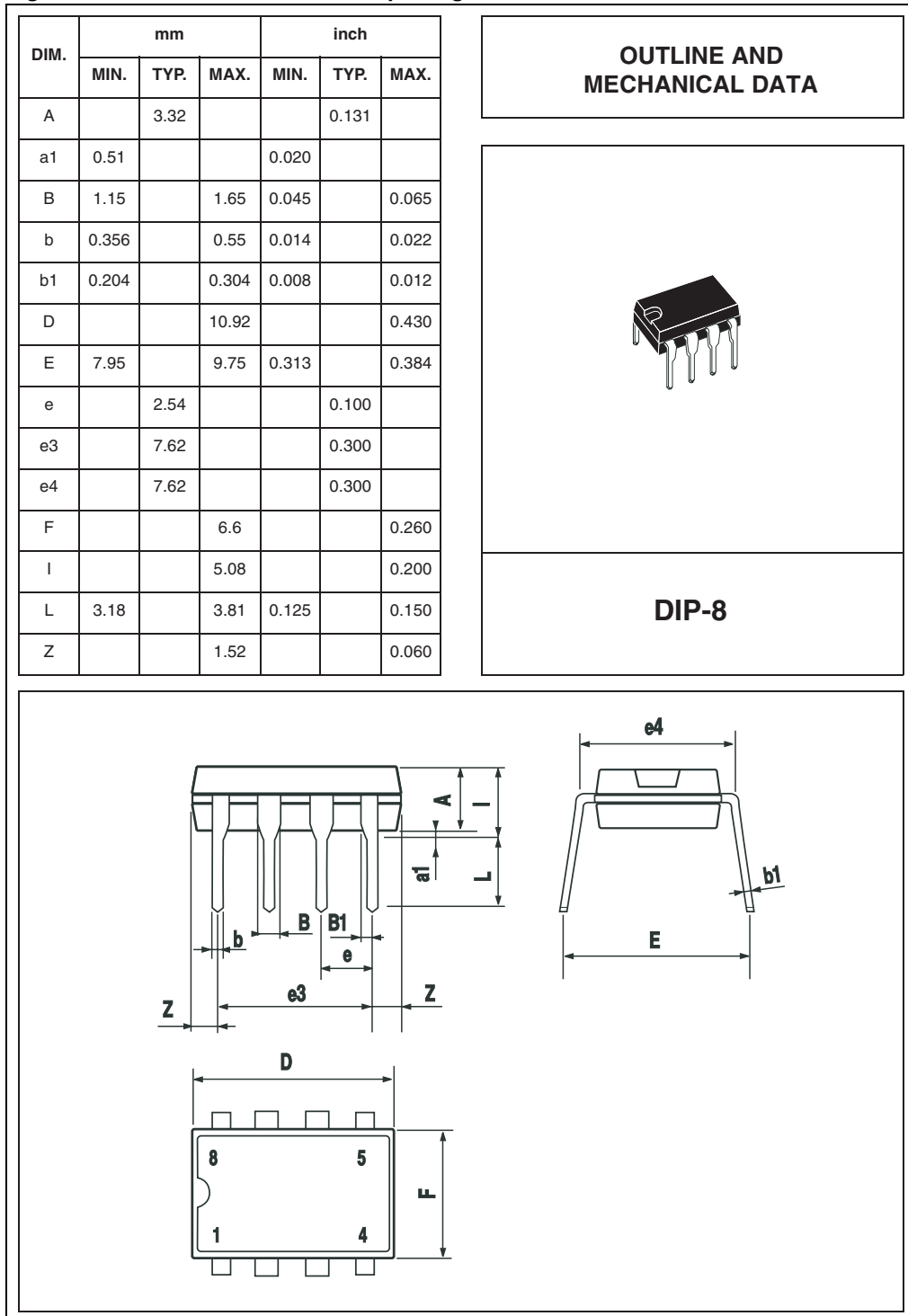
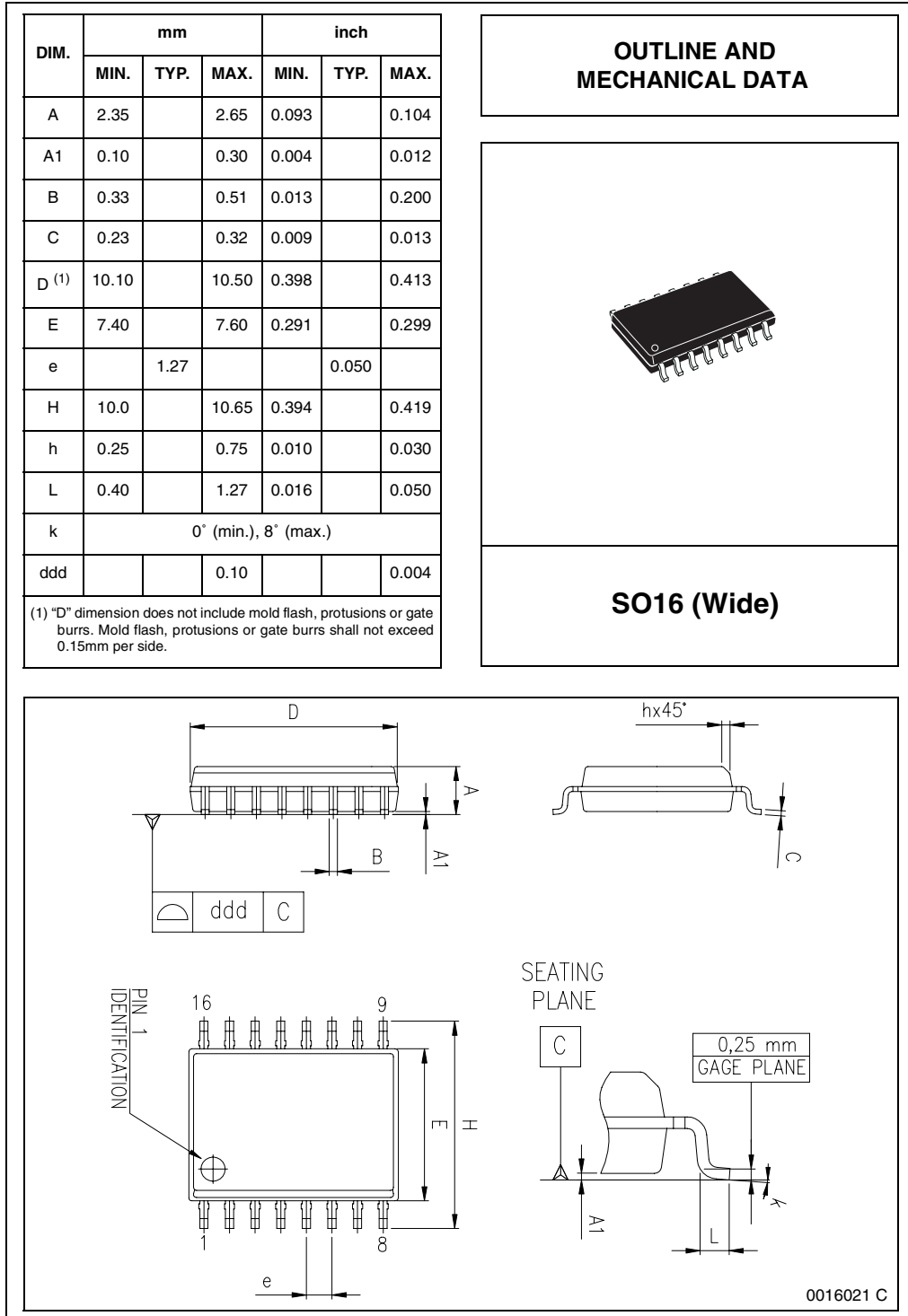


Figure 25. SO16Wide mechanical data & package dimensions



## 7 Order code

**Table 6. Order code**

Part number	Package	Packaging
L4976	DIP8	Tube
L4976D	SO16W	Tube
L4976D013TR	SO16W	Tape and reel

## 8 Revision history

**Table 7. Revision history**

Date	Revision	Changes
5-Aug-2001	6	First Issue
3-Apr-2007	7	Document reformatted, updated dropout voltage values in <a href="#">Table 5 on page 6</a>



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