# L6928

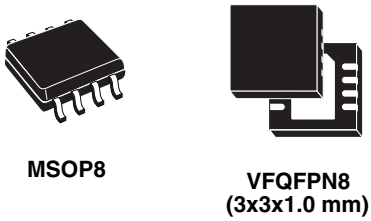
## High efficiency monolithic synchronous step down regulator

### Features

- 2 V to 5.5 V battery input range
- High efficiency: up to 95%
- Internal synchronous switch
- No external Schottky required
- Extremely low quiescent current
- 1 µA max shutdown supply current
- 800 mA max output current
- Adjustable output voltage from 0.6 V
- Low dropout operation: up to 100% duty cycle
- Selectable low noise/low consumption mode at light load
- Power Good signal
- ± 1% output voltage accuracy
- Current-mode control
- 1.4 MHz switching frequency
- Externally synchronizable from 1 MHz to 2 MHz
- OVP
- Short-circuit protection

### Applications

- Battery-powered equipment
- Portable instruments
- Cellular phones
- PDAs and hand held terminals

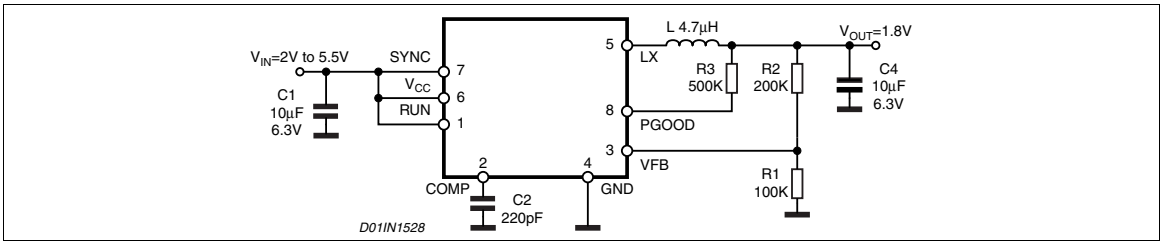



- DSC
- GPS

### Description

The device is DC-DC monolithic regulator specifically designed to provide extremely high efficiency. L6928 supply voltage can be as low as 2 V allowing its use in single Li-Ion cell supplied applications. Output voltage can be selected by an external divider down to 0.6 V. Duty cycle can saturate to 100% allowing low dropout operation. The device is based on a 1.4 MHz fixed frequency, current mode architecture. Low consumption mode operation can be selected at light load conditions, allowing switching losses to be reduced. L6928 is externally synchronizable with a clock which makes it useful in noise sensitive applications. Other features like Power Good, overvoltage protection, short-circuit protection and thermal shutdown (150 °C) are also present.

**Figure 1. Application test circuit**



# Contents

# 1 Pin settings

**Figure 2. Pin connection** (top view)

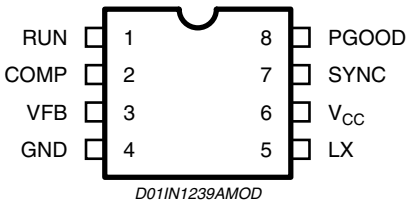



**Table 1. Pin description**

| Pin n° | Name | Description |
|---|---|---|
| 1 | RUN | Shutdown input. When connected to a low level (lower than 0.4 V) the device stops working. When high (higher than 1.3 V) the device is enabled. |
| 2 | COMP | Error amplifier output. A compensation network has to be connected to this pin. Usually a 220 pF capacitor is enough to guarantee the loop stability. |
| 3 | VFB | Error amplifier inverting input. The output voltage can be adjusted from 0.6 V up to the input voltage by connecting this pin to an external resistor divider. |
| 4 | GND | Ground. |
| 5 | LX | Switch output node. This pin is internally connected to the drain of the internal switches. |
| 6 | $V_{CC}$ | Input voltage. The start up input voltage is 2.2 V (typ) while the operating input voltage range is from 2 V to 5.5 V. An internal UVLO circuit realizes a 100 mV (typ.) hysteresis. |
| 7 | SYNC | Operating mode selector input. When high (higher than 1.3 V) the low consumption mode is selected. When low (lower than 0.5 V) the low noise mode is selected. If connected with an appropriate external synchronization signal (from 500 kHz up to 1.4 MHz) the internal synchronization circuit is activated and the device works at the same switching frequency. |
| 8 | PGOOD | Power good comparator output. It is an open drain output. A pull-up resistor should be connected between PGOOD and $V_{OUT}$ (or $V_{CC}$ depending on the requirements). The pin is forced low when the output voltage is lower than 90% of the regulated output voltage and goes high when the output voltage is greater than 90% of the regulated output voltage. If not used the pin can be left floating. |

# 2 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_6$ | Input voltage | -0.3 to 6 | V |
| $V_5$ | Output switching voltage | -1 to $V_{CC}$ | V |
| $V_1$ | Shutdown | -0.3 to $V_{CC}$ | V |
| $V_3$ | Feedback voltage | -0.3 to $V_{CC}$ | V |
| $V_2$ | Error amplifier output voltage | -0.3 to $V_{CC}$ | V |
| $V_8$ | PGOOD | -0.3 to $V_{CC}$ | V |
| $V_7$ | Synchronization mode selector | -0.3 to $V_{CC}$ | V |
| $P_{TOT}$ | Power dissipation at $T_A$ = 70 °C | 0.45 | W |
| $T_J$ | Junction operating temperature range | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| LX pin | Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “Human body model” acceptance criteria: “normal performance’ | ±1000 | V |
| Other pins | | ±2000 | V |

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Maximum thermal resistance junction-ambient for MSOP8 | 180 | °C/W |
| | Maximum thermal resistance junction-ambient for VFQFPN8 | 56 | °C/W |

# 3 Electrical characteristics

$T_J$ = 25 °C, $V_{IN}$ = 3.6 V unless otherwise specified.

**Table 4. Electrical characteristics (1)**

| Symbol | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{cc}$ | Operating input voltage | After turn on | (1) | 2 | | 5.5 | V |
| $V_{cc\ ON}$ | Turn On threshold | | | | 2.2 | | V |
| $V_{cc\ OFF}$ | Turn Off threshold | | | | | 2 | V |
| $V_{cc\ hys}$ | Hysteresis | | | | 100 | | mV |
| $R_p$ | High side $R_{ON}$ | $V_{cc}$ = 3.6 V, $I_{lx}$ =100 mA | | | 240 | 300 | mΩ |
| | | | (1) | | | 400 | |
| $R_n$ | Low side $R_{ON}$ | $V_{cc}$ = 3.6 V, $I_{lx}$ =100 mA | | | 215 | 300 | mΩ |
| | | | (1) | | | 400 | |
| $I_{lim}$ | Peak current limit | $V_{cc}$ = 3.6 V | | 1 | 1.2 | 1.5 | A |
| | | | (1) | 0.85 | | 1.65 | |
| | Valley current limit | $V_{cc}$ = 3.6 V | | 1 | 1.4 | 1.7 | A |
| | | | (1) | 0.9 | | 1.85 | |
| $V_{OUT}$ | Output voltage range | | | $V_{fb}$ | | $V_{CC}$ | V |
| $f_{osc}$ | Oscillator frequency | | | | 1.4 | | MHz |
| $f_{sync}$ | Sync mode clock (2) | | | 1 | | 2 | MHz |
| **DC characteristics** | | | | | | | |
| $I_q$ | Quiescent current (low noise mode) | $V_{sync}$ = 0 V, no load, $V_{FB}$ > 0.6 V | | | 230 | | µA |
| | Quiescent current (low consumption mode) | $V_{sync}$ = $V_{CC}$, no load, $V_{FB}$ > 0.6 V | (1) | | 25 | 50 | µA |
| $I_{sh}$ | Shutdown current | RUN to GND, $V_{CC}$ = 5.5 V | | | 0.2 | | µA |
| $I_{lx}$ | LX leakage current (2) | RUN to GND, $V_{LX}$ = 5.5 V, $V_{CC}$ = 5.5 V | | | 1 | | µA |
| | | RUN to GND, $V_{LX}$ = 0 V, $V_{CC}$ = 5.5 V | | | 1 | | µA |
| **Error amplifier characteristics** | | | | | | | |
| $V_{fb}$ | Voltage feedback | | | 0.593 | 0.600 | 0.607 | V |
| | | | (1) | 0.590 | 0.600 | 0.610 | V |
| $I_{fb}$ | Feedback input current (2) | $V_{FB}$ = 0.6 V | | | 25 | | nA |
| **Run** | | | | | | | |
| $V_{run\_H}$ | RUN threshold high | | | | | 1.3 | V |
| $V_{run\_L}$ | RUN threshold low | | | 0.4 | | | V |

**Table 4. Electrical characteristics (continued)(1)**

| Symbol | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{run}$ | RUN input current (2) | | | | 25 | | nA |
| **SYNC/MODE function** | | | | | | | |
| $V_{sync\_H}$ | Sync mode threshold high | | | | | 1.3 | V |
| $V_{sync\_L}$ | Sync mode threshold low | | | 0.5 | | | V |
| **PGOOD section** | | | | | | | |
| $V_{PGOOD}$ | Power Good Threshold | $V_{OUT} = V_{fb}$ | | | 90 | | $\%V_{OUT}$ |
| $\Delta V_{PGOOD}$ | Power Good Hysteresis | $V_{OUT} = V_{fb}$ | | | 4 | | $\%V_{OUT}$ |
| $V_{Pgood(low)}$ | Power Good Low Voltage | Run to GND | | | | 0.4 | V |
| $I_{LK-PGOOD}$ | Power Good Leakage Current (2) | $V_{PGOOD}$ = 3.6 V | | | 50 | | nA |
| **Protections** | | | | | | | |
| HOVP | Hard overvoltage threshold | $V_{OUT} = V_{fb}$ | | | 10 | | $\%V_{OUT}$ |

1. Specification referred to $T_J$ from -40°C to +125°C. Specification over the -40 to +125°C $T_J$ temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

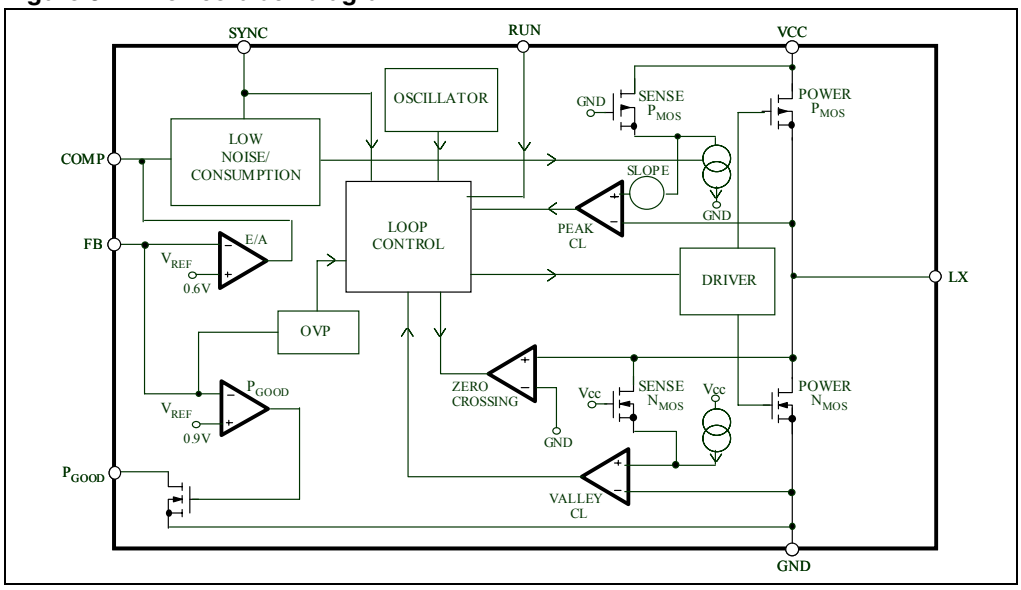
# 4 Operation description

The main loop uses slope compensated PWM current mode architecture. Each cycle the high side MOSFET is turned on, triggered by the oscillator, so that the current flowing through it (the same as the inductor current) increases. When this current reaches the threshold (set by the output of the error amplifier E/A), the peak current limit comparator PEAK_CL turns off the high side MOSFET and turns on the low side one until the next clock cycle begins or the current flowing through it goes down to zero (ZERO CROSSING comparator). The peak inductor current required to trigger PEAK_CL depends on the slope compensation signal and on the output of the error amplifier.

In particular, the error amplifier output depends on the VFB pin voltage. When the output current increases, the output capacitor is discharged and so the VFB pin decreases. This produces increase of the error amplifier output, so allowing a higher value for the peak inductor current. For the same reason, when due to a load transient the output current decreases, the error amplifier output goes low, so reducing the peak inductor current to meet the new load requirements.

The slope compensation signal allows the loop stability also in high duty cycle conditions (see related section).

**Figure 3. Device block diagram**




## 4.1 Modes of operation

Depending on the SYNC pin value the device can operate in low consumption or low noise mode. If the SYNC pin is high (higher than 1.3 V) the low consumption mode is selected while the low noise mode is selected if the SYNC pin is low (lower than 0.5 V).

### 4.1.1 Low consumption mode

In this mode of operation, at light load, the device operates discontinuously based on the COMP pin voltage, in order to keep the efficiency very high also in these conditions. While the device is not switching the load discharges the output capacitor and the output voltage goes down. When the feedback voltage goes lower than the internal reference, the COMP pin voltage increases and when an internal threshold is reached, the device starts to switch. In these conditions the peak current limit is set approximately in the range of 200 mA - 400 mA, depending on the slope compensation (see related section).

Once the device starts to switch the output capacitor is recharged. The feedback pin increases and, when it reaches a value slightly higher than the reference voltage, the output of the error amplifier goes down until a clamp is activated. At this point, the device stops to switch. In this phase, most of the internal circuitries are off, so reducing the device consumption down to a typical value of 25 µA.

### 4.1.2 Low noise mode

If for noise reasons, the very low frequencies of the low consumption mode are undesirable, the low noise mode can be selected. In low noise mode, the efficiency is a little bit lower compared with the low consumption mode in very light load conditions but for medium-high load currents the efficiency values are very similar.

Basically, the device switches with its internal free running frequency of 1.4 MHz. Obviously, in very light load conditions, the device could skip some cycles in order to keep the output voltage in regulation.

### 4.1.3 Synchronization

The device can also be synchronized with an external signal from 1 MHz up to 2 MHz.

In this case the low noise mode is automatically selected. The device will eventually skip some cycles in very light load conditions. The internal synchronization circuit is inhibited in short-circuit and overvoltage conditions in order to keep the protections effective (see relative sections).

## 4.2 Short circuit protection

During the device operation, the inductor current increases during the high side turn ON phase and decrease during the high side turn off phase based on the following equations:

**Equation 1**

$$\Delta I_{ON} = \frac{(V_{IN} - V_{OUT})}{L} \cdot T_{ON}$$

**Equation 2**

$$\Delta I_{OFF} = \frac{(V_{OUT})}{L} \cdot T_{OFF}$$

In strong overcurrent or short-circuit conditions the $V_{OUT}$ can be very close to zero. In this case $\Delta I_{ON}$ increases and $\Delta I_{OFF}$ decreases. When the inductor peak current reaches the

current limit, the high side MOSFET turns off and so the $T_{ON}$ is reduced down to the minimum value (250 ns typ.) in order to reduce as much as possible $\Delta I_{ON}$.

Anyway, if $V_{OUT}$ is low enough it can be that the inductor peak current further increases because during the $T_{OFF}$ the current decays very slowly.

Due to this reason a second protection that fixes the maximum inductor valley current has been introduced. This protection doesn't allow the high side MOSFET to turn on if the current flowing through the inductor is higher that a specified threshold (valley current limit). Basically the $T_{OFF}$ is increased as much as required to bring the inductor current down to this threshold. So, the maximum peak current in worst case conditions will be:

**Equation 3**

$$I_{PEAK} = I_{VALLEY} + \frac{V_{IN}}{L} \cdot T_{ON\_MIN}$$

Where $I_{PEAK}$ is the valley current limit (1.4 A typ.) and $T_{ON\_MIN}$ is the minimum $T_{ON}$ of the high side MOSFET.

## 4.3 Slope compensation

In current mode architectures, when the duty cycle of the application is higher than approximately 50%, a pulse-by-pulse instability (the so called sub harmonic oscillation) can occur. To allow loop stability also in these conditions a slope compensation is present. This is realized by reducing the current flowing through the inductor necessary to trigger the COMP comparator (with a fixed value for the COMP pin voltage). With a given duty cycle higher than 50%, the stability problem is particularly present with an higher input voltage (due to the increased current ripple across the inductor), so the slope compensation effect increases as the input voltage increases. From an application point of view, the final effect is that the peak current limit depends both on the duty cycle (if higher than approximately 40%) and on the input voltage.

## 4.4 Loop stability

Since the device is realized with a current mode architecture, the loop stability is usually not a big issue. For most of the application a 220 pF connected between the COMP pin and ground is enough to guarantee the stability. In case very low ESR capacitors are used for the output filter, such as multilayer ceramic capacitors, the zero introduced by the capacitor itself can shift at very high frequency and the transient loop response could be affected. Adding a series resistor to the 220 pF capacitor can solve this problem.

The right value for the resistor (in the range of 50 K) can be determined by checking the load transient response of the device. Basically, the output voltage has to be checked at the scope after the load steps required by the application. In case of stability problems, the output voltage could oscillates before to reach the regulated value after a load step.

# 5 Additional features and protections

## 5.1 DROPOUT operation

The Li-Ion battery voltage ranges from approximately 3 V and 4.1 V - 4.2 V (depending on the anode material). In case the regulated output voltage is from 2.5 V and 3.3 V, it can be that, close to the end of the battery life, the battery voltage goes down to the regulated one. In this case the device stops to switch, working at 100% of duty cycle, so minimizing the dropout voltage and the device losses.

## 5.2 PGOOD (Power Good output)

A power good output signal is available. The $V_{FB}$ pin is internally connected to a comparator with a threshold set at 90% of the of reference voltage (0.6 V). Since the output voltage is connected to the $V_{FB}$ pin by a resistor divider, when the output voltage goes lower than the regulated value, the $V_{FB}$ pin voltage goes lower than 90% of the internal reference value. The internal comparator is triggered and the PGOOD pin is pulled down.

The pin is an open drain output and so, a pull up resistor should be connected to him.

If the feature is not required, the pin can be left floating.

## 5.3 Adjustable output voltage

The output voltage can be adjusted by an external resistor divider from a minimum value of 0.6 V up to the input voltage. The output voltage value is given by:

**Equation 4**

$$V_{OUT} = 0.6 \cdot \left(1 + \frac{R_2}{R_1}\right)$$

## 5.4 OVP (Overvoltage protection)

The device has an internal overvoltage protection circuit to protect the load.

If the voltage at the feedback pin goes higher than an internal threshold set 10% (typ) higher than the reference voltage, the low side power MOSFET is turned on until the feedback voltage goes lower than the reference one.

During the overvoltage circuit intervention, the zero crossing comparator is disabled so that the device is also able to sink current.

## 5.5 Thermal shutdown

The device has also a thermal shutdown protection activated when the junction temperature reaches 150 °C. In this case both the high side MOSFET and the low side one are turned off. Once the junction temperature goes back lower than 95 °C, the device restarts the normal operation.

# 6 Package mechanical data

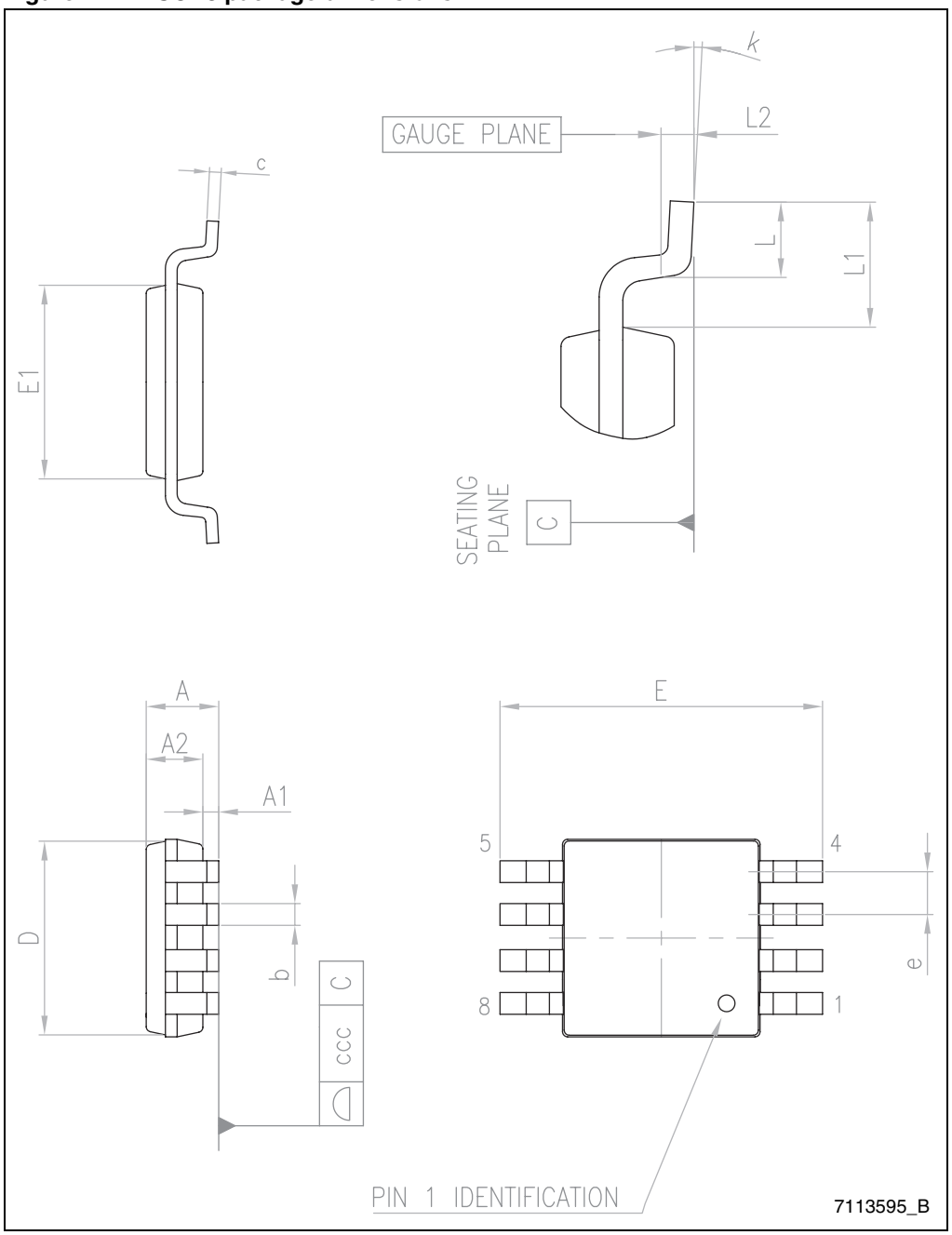
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Table 5. MSOP8 mechanical data**

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.10 |
| A1 | 0 | | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.22 | | 0.40 |
| c | 0.08 | | 0.23 |
| D (1) | 2.80 | 3.00 | 3.20 |
| E | 4.65 | 4.90 | 5.15 |
| E1 (1) | 2.80 | 3.00 | 3.10 |
| e | | 0.65 | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 0.95 | |
| L2 | | 0.25 | |
| k | 0 | | 8 |
| ccc | | | 0.10 |

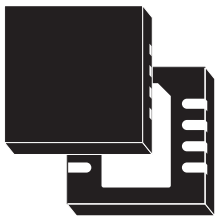
1. Dimension “D” and “E1” does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

**Figure 4. MSOP8 package dimensions**

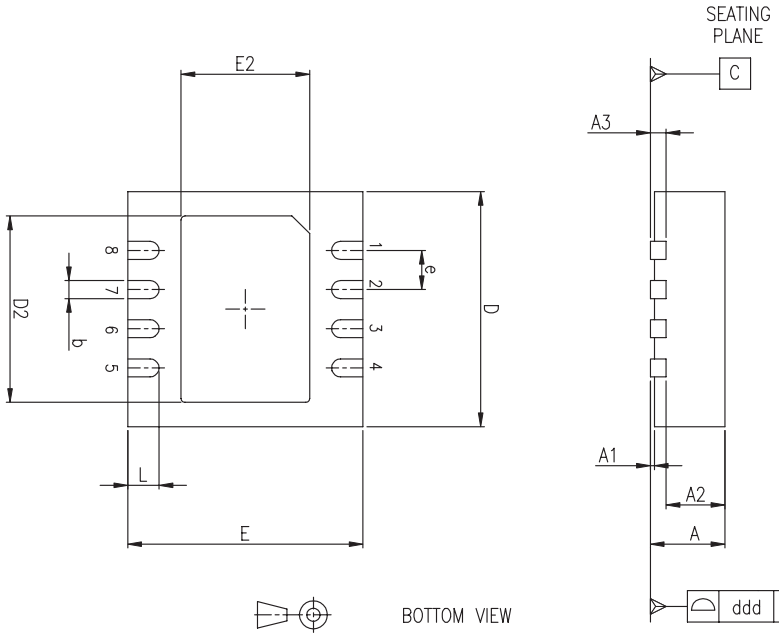


| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.02 | 0.05 | | 0.0008 | 0.0020 |
| A2 | | 0.70 | | | 0.0276 | |
| A3 | | 0.20 | | | 0.0079 | |
| b | 0.18 | 0.23 | 0.30 | 0.0071 | 0.0091 | 0.0118 |
| D | | 3.00 | | | 0.1181 | |
| D2 | 2.23 | 2.38 | 2.48 | 0.0878 | 0.0937 | 0.0976 |
| E | | 3.00 | | | 0.1181 | |
| E2 | 1.49 | 1.64 | 1.74 | 0.0587 | 0.0646 | 0.0685 |
| e | | 0.50 | | | 0.0197 | |
| L | 0.30 | 0.40 | 0.50 | 0.0118 | 0.0157 | 0.0197 |
| ddd | | | 0.08 | | | 0.0031 |

## OUTLINE AND MECHANICAL DATA



**VFQFPN8 (3x3x1.0 8mm)**
**V**ery thin **F**ine pitch **Q**uad **P**ackages **N**o lead



# 7 Order codes

**Table 1. Order codes**

| Order codes | Package | Packaging |
|---|---|---|
| L6928D | MSOP8 | Tube |
| L6928D013TR | MSOP8 | Tape and reel |
| L6928Q1 | VFQFPN8 | Tube |
| L6928Q1TR | VFQFPN8 | Tape and reel |

# 8 Revision history

**Table 6. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| Oct-2004 | 1 | First Issue. |
| Feb-2005 | 2 | Changed from product preview to final datasheet. |
| Nov-2005 | 3 | Updated Table 5. Electrical characteristics.<br>Added VFQFPN8 package and new part numbers. |
| 27-Oct-2006 | 4 | Added $R_{thJA}$ for VFQFPN8 in *Table 3.* |
| 22-Aug-2007 | 5 | Updated *Table 1: Order codes on page 14*. |
| 11-Apr-2011 | 6 | Updated MSOP8 package mechanical data *Table 5 on page 11* and *Figure 4 on page 12*. |