Switching Regulator (VIN=20V / Io=6A)

BD95500MUV

●Description

BD95500MUV is a switching regulator with high output current (up to 6A) which can achieve low output voltage (0.7V to 5.0V) from a wide input voltage range (3V to 20V). High efficiency for the switching regulator can be realized by utilizing an internal N-MOSFET power transistor. A new technology called H^4Reg^{TM} is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For protection and ease of use, the soft start function, variable frequency function, short circuit protection function with timer latch, over voltage protection function, and power good function are all built in. This switching regulator is specially designed for sets of various kinds.

●Features

1) Integrated low ON resistance N-MOSFET (TYP. 50mΩ)
2) H^4Reg^{TM} DC/DC converter controller
3) Adjustable Simple Light Load Mode (SLLM), and forced continuous mode
4) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO), Adjustable Over Current Protection (OCP), Over Voltage Protection (OVP), Short Circuit Protection(SCP) built-in
5) Soft start function to minimize rush current during startup
6) Adjustable switching frequency (f=200KHz～1000KHz)
7) Built-in output discharge function
8) VQFN040-V6060 Package
9) Tracking Function
10) Integrated boot strap diode
11) Power Good function

●Applications

Mobile PC, Desktop PC, LCD-TV, Digital Components, etc

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●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage 1	VCC	7 *1	V
Input Voltage 2	VDD	7 *1	V
Input Voltage 3	VIN	24 *1	V
BOOT Voltage	BOOT	30	V
BOOT-SW Voltage	BOOT-SW	7	V
LG Voltage	LG	VDD	V
REF Voltage	REF	VCC	V
Output Voltage	VOUT/Is+/Is-	VCC	V
ILIM/SS/FS/MODE Voltage	ILIM/SS/FS/MODE	VCC	V
VREG Voltage	VREG	VCC	V
EN Input Voltage	EN	7	V
Output Current (Average)	Isw	6	A
Power Dissipation 1	Pd1	0.54 *2	W
Power Dissipation 2	Pd2	1.00 *3	W
Power Dissipation 3	Pd3	3.77 *4	W
Power Dissipation 4	Pd4	4.66 *5	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd, ASO, and Tjmax=150℃.
*2 Reduced by 4.3mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*3 Reduced by 8.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 0mm^2))
*4 Reduced by 30.1mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm^2, 2nd and 3rd copper foil area : 5505mm^2))
*5 Reduced by 37.3mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm^2))

●Operating Conditions (Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	VCC	4.5	5.5	V
Input Voltage 2	VDD	4.5	5.5	V
Input Voltage 3	VIN	3.0	20	V
BOOT Voltage	BOOT	4.5	25	V
SW Voltage	SW	-0.7	20	V
BOOT-SW Voltage	BOOT-SW	4.5	5.5	V
MODE Input Voltage	MODE	0	5.5	V
EN Input Voltage	EN	0	5.5	V
Output Adjustable Voltage	REF	0.7	2.0	V
Is Input Voltage	Is+/Is-	0.7	2.7	V
MIN ON Time	Tonmin	-	200	nsec

★This product should not be used in a radioactive environment.

●ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, Ta=25℃, VCC=5V, VDD=5V, EN / MODE=5V, VIN=12V, REF=1.8V, R_{FS}=68kΩ)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Whole Device]						
VCC Bias Current	Icc	-	1200	2000	μA	
VIN Bias Current	Iin	-	100	200	μA	
VCC Standby Current	Iccstb	-	0	10	μA	EN＝0V
VIN Standby Current	Iinstb	-	0	10	μA	EN＝0V
EN Low Voltage	Enlow	GND	-	0.8	V	
EN High Voltage	Enhigh	2.3	-	5.5	V	
EN Bias Current	Ien	-	7	10	μA	
VREG Voltage	Vreg	2.475	2.500	2.525	V	Ireg=0 to 500uA Ta=-10°C to 100°C*
[Under Voltage Locked Out]						
VCC Threshold Voltage	Vcc_UVLO	4.1	4.3	4.5	V	VCC:Sweep up
VCC Hysteresis Voltage	dVcc_UVLO	100	160	220	mV	VCC:Sweep down
VIN Threshold Voltage	Vin_UVLO	2.4	2.6	2.8	V	VIN:Sweep up
VIN Hysteresis	dVin_UVLO	100	160	220	mV	VIN:Sweep down
VREG Threshold Voltage	Vreg_UVLO	2.0	2.2	2.4	V	VREG:Sweep up
VREG Hysteresis Voltage	dVreg_UVLO	100	160	220	mV	VREG:Sweep down
[H^4REG^{TM} Control Block]						
ON Time	Ton	400	500	600	nsec	
MAX ON Time	Tonmax	-	3	6.0	μsec	
MIN OFF Time	Toffmin	-	450	550	nsec	
[FET Block]						
High Side ON Resistance	HGhon	-	50	80	mΩ	
Low Side ON Resistance	HGlon	-	50	80	mΩ	
[SCP Block]						
SCP Start up Voltage	Vscp	REF×0.60	REF×0.70	REF×0.80	V	
Delay Time	Tscp	-	1.0	2.0	ms	
[OVP Block]						
OVP Detect Voltage	Vovp	REF×1.16	REF×1.2	REF×1.24	V	
[Soft Start Block]						
Charge Current	Iss	2	4	6	μA	
Discharge Current	Idis	0.5	1.0	2.0	μA	
Standby Voltage	Vss_stb	-	-	50	mV	
[Over Current Protection Block]						
Current Limit Threshold 1	Ilim1	40	50	60	mV	ILIM=0.5V Ta=-10°C to 100°C
Current Limit Threshold2	Ilim2	160	200	240	mV	ILIM=2.0V
[Vout Setting]						
VOUT Offset Voltage 1	Voutoff1	REF-10m	REF	REF+10m	V	Ta=-10°C to 100°C
VOUT Bias Current	Ivout	-100	0	100	nA	
REF Bias Current	Iref	-100	0	100	nA	
Is+ Input Current	IIs+	-1	0	1	μA	Is+=1.8V
Is- Input Current	IIs-	-1	0	1	μA	Is-=1.8V
[MODE Block]						
SLLM Threshold	VthSLLM	VCC-0.5	-	VCC	V	
Forced Continuous Mode	VthCONT	GND	-	0.5	V	
Input Impedance	RMODE	-	400	-	kΩ	
[Power Good Block]						
VOUT Power Good Low Voltage	VoutPL	REF×0.85	REF×0.90	REF×0.95	V	
VOUT Power Good High Voltage	VoutPH	REF×1.05	REF×1.10	REF×1.15	V	

●Reference Data

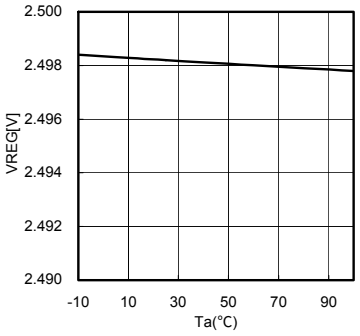


Fig.1 Ta vs VREG

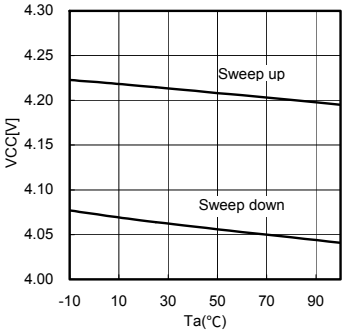


Fig.2 Ta vs UVLO (VCC)

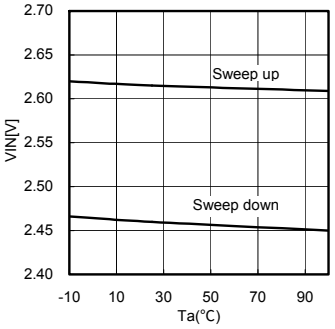


Fig.3 Ta vs UVLO (VIN)

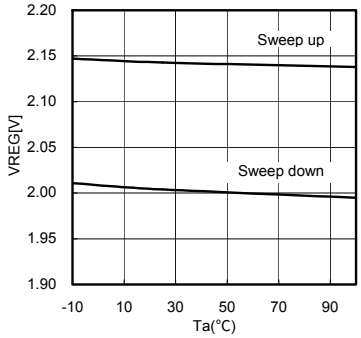


Fig.4 Ta vs UVLO (VREG)

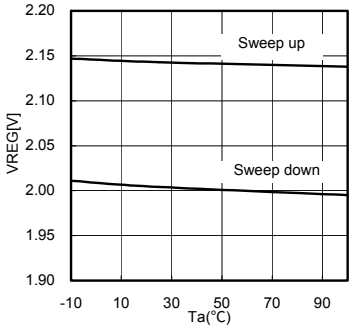


Fig.5 Ta vs EN Threshold

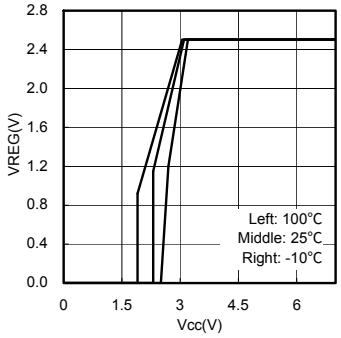


Fig.6 Vcc vs VREG

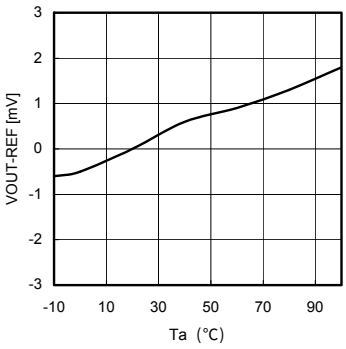


Fig.7 Ta vs VOUT Offset

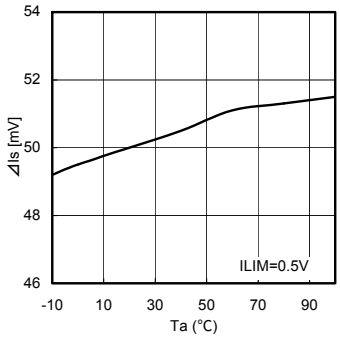


Fig.8 Ta vs Current Limit Threshold

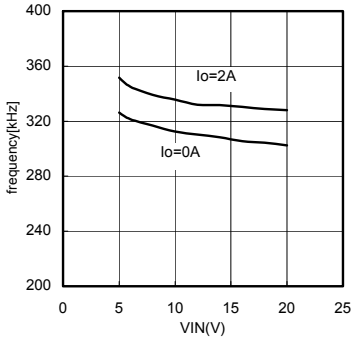


Fig.9 VIN vs f

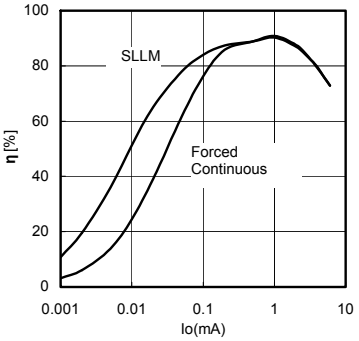


Fig.10 Io vs Efficiency
(VIN=7V, VOUT=1.5V)

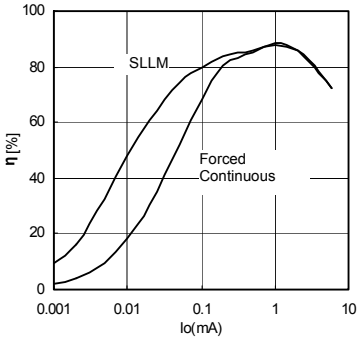


Fig.11 Io vs Efficiency
(VIN=12V, VOUT=1.5V)

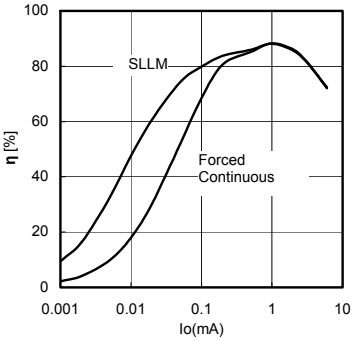


Fig.12 Io vs Efficiency
(VIN=19V, VOUT=1.5V)

●Reference Data

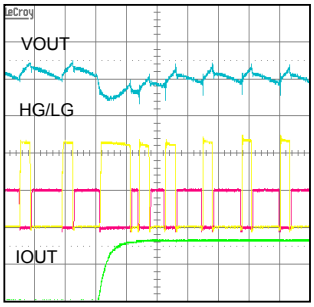


Fig.13 Transient Response
(VIN=7V)

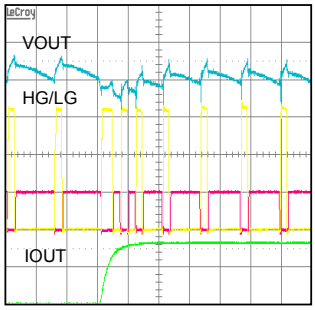


Fig.14 Transient Response
(VIN=12V)

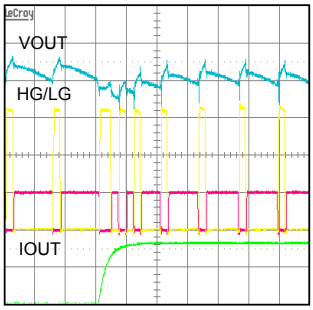


Fig.15 Transient Response
(VIN=19V)

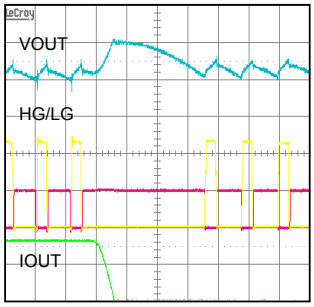


Fig.16 Transient Response
(VIN=7V)

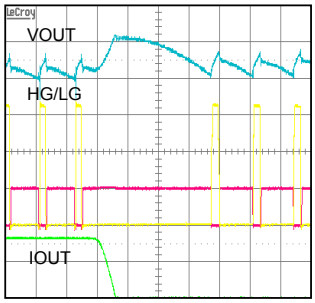


Fig.17 Transient Response
(VIN=12V)

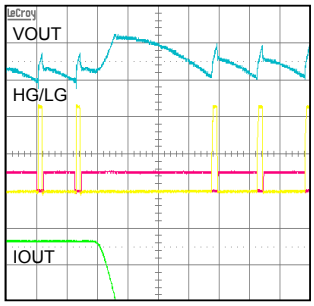


Fig.18 Transient Response
(VIN=19V)

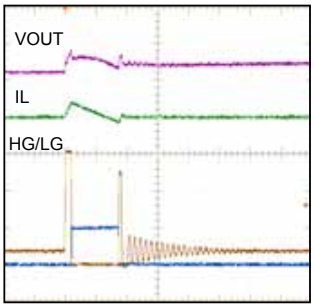


Fig.19 SLLM Mode
(IOUT=0A)

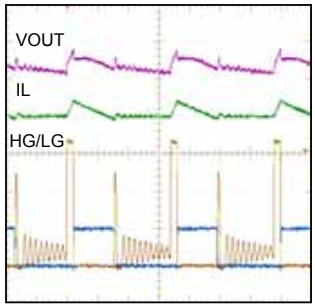


Fig.20 SLLM Mode
(IOUT=0.4A)

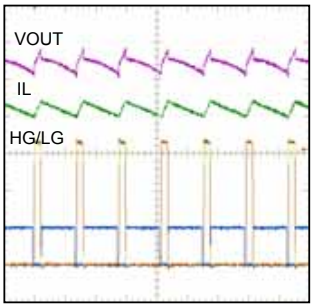


Fig.21 SLLM Mode
(IOUT=1A)

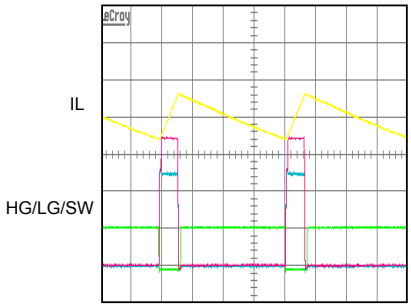


Fig.22 Continuous Mode
(Io=0A)

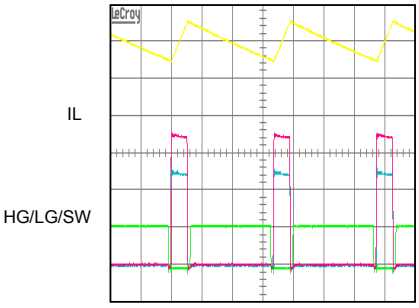


Fig.23 Continuous Mode
(Io=4A)

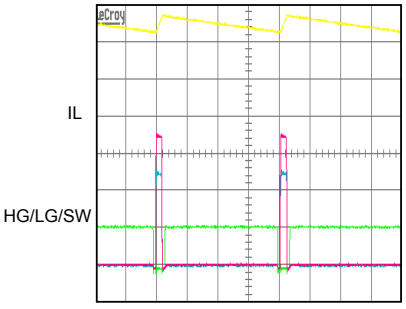


Fig.24 OCP Status
(Io=5A)

●Reference Data

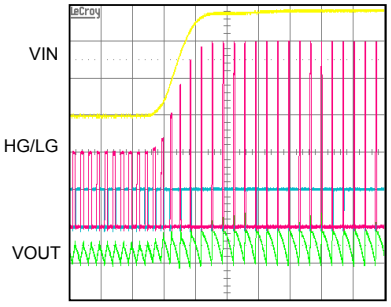


Fig.25 VIN change
(5→19V)

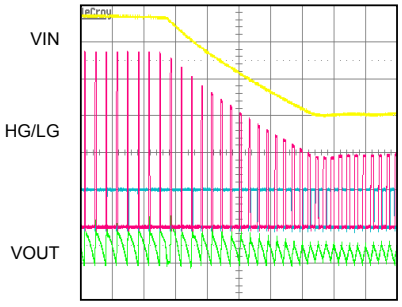


Fig.26 VIN change
(19→5V)

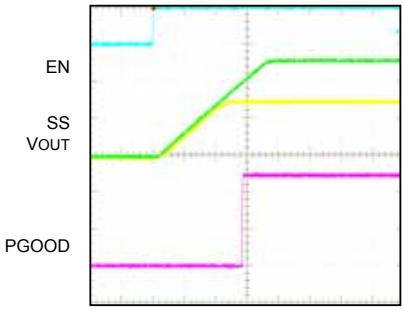


Fig.27 EN wake up

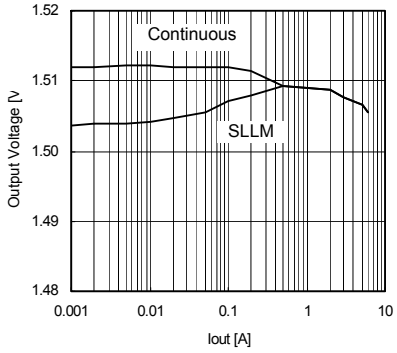


Fig.28 IOUT vs VOUT

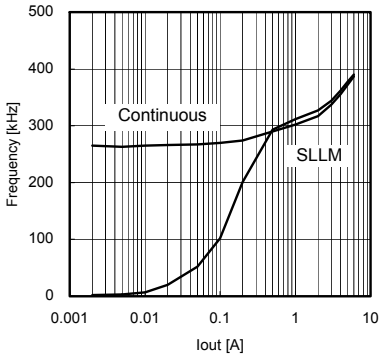


Fig.29 IOUT vs f

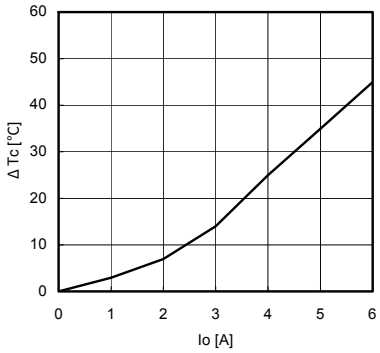
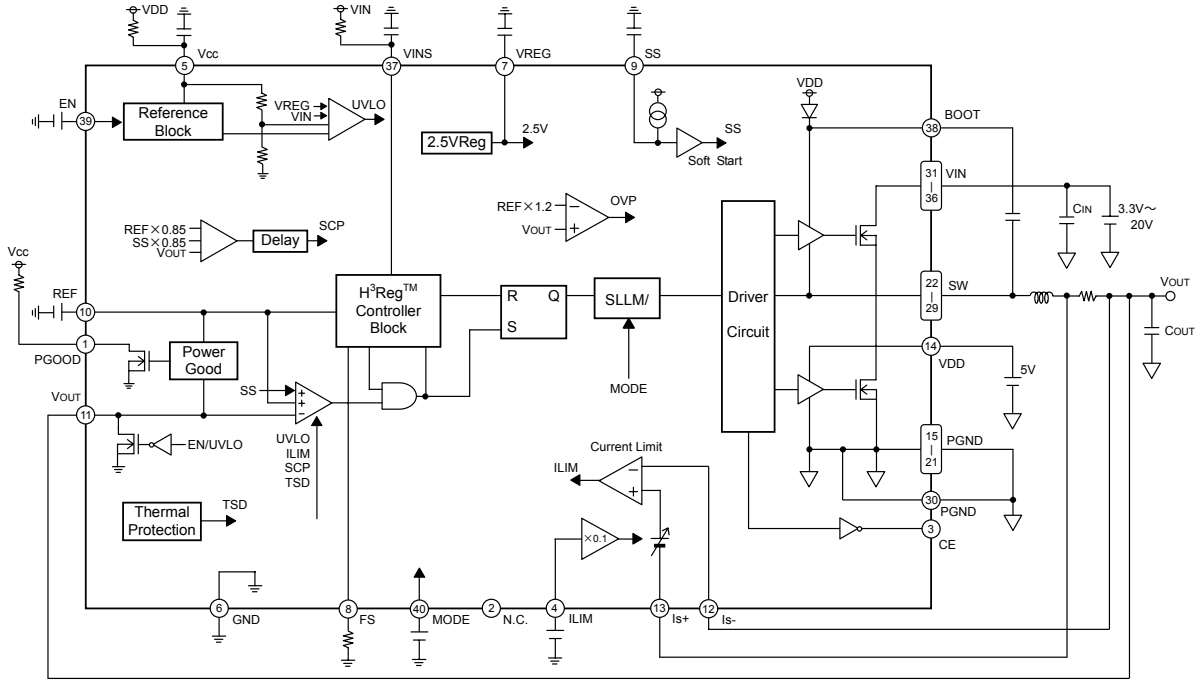
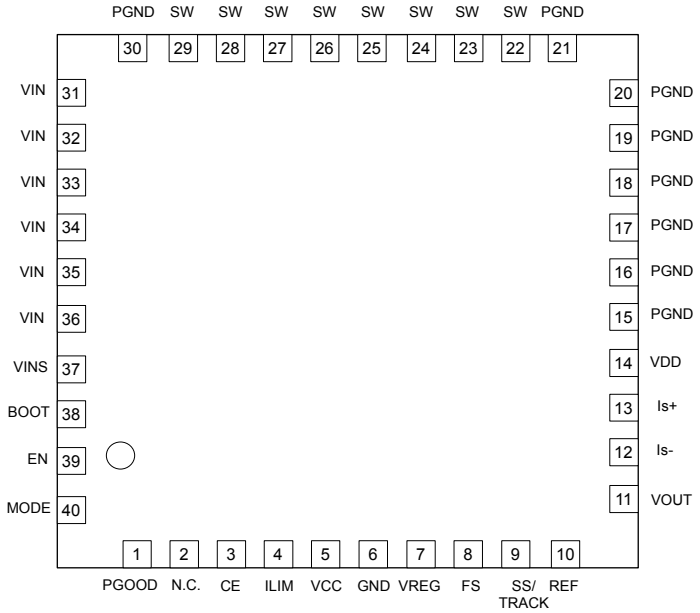


Fig.30 IOUT vs Δ Tc

●Block Diagram



●Pin Configuration



*Connect the bottom side (FIN) to the ground terminal

●Pin Function Table

PIN No.	PIN name	PIN function
1	PGOOD	Power Good Output Pin (+/-10% Window)
2	N.C.	-
3	CE	Ceramic Capacitor Reactive Pin
4	ILIM	Current Limit Setting Pin
5	VCC	Power Supply Input pin (Control Block)
6	GND	Sense GND
7	VREG	IC Reference Voltage (2.5V/500uA)
8	FS	Switching Frequency Adjustable Pin (30k～100kΩ)
9	SS/ TRACK	Soft Start Setting Pin (w/ Capacitor)/ Tracking Voltage Input Pin
10	REF	Vo Setting Pin
11	VOUT	Output Voltage Sense Pin
12	Is-	Current Sense Pin -
13	Is+	Current Sense Pin +
14	VDD	FET Driver Power Supply Pin (5V Input)
15-21	PGND	Power GND Pin
22-29	SW	High Side FET Source Pin
30	PGND	Power GND Pin
31-36	VIN	Battery Voltage Input pin (3.3~20V Input)
37	VINS	Battery Voltage Sense pin
38	BOOT	HG Driver Power Supply Pin
39	EN	Enable Input pin (IC ON when High)
40	MODE	Control Mode Adjustment Pin Low: Continuous High: SLLM
bottom	FIN	Substrate connection

●Pin Descriptions

- VCC (5 Pin)

  This is the power supply pin for IC internal circuits, except the FET driver. The input supply voltage range is 4.5V to 5.5V. It is recommended that a 10Ω/0.1uF C-R filter be put in this pin from VDD rail.

- EN (39 Pin)

  When EN pin voltage is at least 2.3V, the status of this switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V and circuit current becomes 0uA.

- VDD (14 Pin)

  This is the power supply pin to drive the LOW side FET and for Boot-strap diode. It is recommended that a 1~10uF bypass capacitor be established to compensate for rush current during the FET ON/OFF transition.

- VREG (7 Pin)

  This is the reference voltage output pin. The voltage is 2.5V, with 500uA current ability. It is recommended that a 0.22~1uF capacitor (X5R or X7R) be established between VREG and GND (6 Pin). When REF is not adjusted from the external voltage supply, the REF voltage can be adjusted using the external resistor divider of VREG.

- REF (10 Pin)

  This is the output voltage adjustment pin by resistor divider network from VREG pin (0.7~2.0V). It is also very convenient for synchronizing external voltage supply. The IC controls the output voltage (REF　VOUT).

- ILIM (4 Pin)

  BD95500MUV detects the voltage between Is+ pin and Is- pin and limits the output current (OCP). Voltage equivalent to 1/10 of the ILIM voltage is the voltage drop of external current sense resistor. A very low current sense resistor or inductor DCR can also be used for this platform.

- SS/TRACK (9 Pin)

  This is the adjustment pin to set the soft start time. SS voltage is low during standby status. When EN is ON, the soft start time can be determined by the SS charge current and capacitor between SS-GND. Until SS reaches REF voltage, the output voltage is equivalent to SS voltage. And also this pin enables to operate tracking function. The output voltage keeps track of a power supply rail by connecting 10kΩ resistance between the power supply rail and SS/TRACK pin.

- VINS (37 Pin)

  The duty cycle is determined by input voltage and controls output voltage. In other words, the output voltage is affected by input voltage. Therefore, when VINS voltage fluctuates, the output voltage becomes also unstable. Since the VINS line is also the input voltage of the switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish a bypass capacitor or CR filter suitable for the actual application.

- FS (8 Pin)

  This is the pin to adjust the switching frequency with the resistor. It is recommended that a resistor be established to GND (6 pin).The frequency range is from 200kHz to 1000kHz.

- Is+ (13 pin)、Is- (12 pin)

  These pins are connected to both sides of the current sense resistor to detect output current. The voltage drop between Is+ and Is- is compared with the voltage equivalent to 1/10 of ILIM voltage. When this voltage drop hits the specified voltage level, the output voltage is OFF. Since the maximum input voltage is 2.7V, set the output voltage by the resistance division value in case the output voltage is 2.7V or more.

- BOOT (38 pin)

  This is the voltage supply to drive the high side FET and a Diode for BOOT strap function is built in. The maximum absolute ratings are 30V (from GND) and 7V (from SW). BOOT voltage swings between (VIN+Vcc) and Vcc during active operation.

- PGOOD (1 pin)

  This pin is output pin for Power Good. It is open drain pin and recommended to connect to other power supply through the pull-up resistance (about 100kΩ).

- CE (3 pin)

  This pin is for the ceramic capacitor. It is useful to utilize low ESR capacitor for output capacitor.

- MODE (40 pin)

  This is the control mode changeable pin. The status is Low : continuous mode, the status is High : SLLM™.

- VOUT (11 pin)

  This is the monitor pin for output voltage. This IC controls the voltage in the status of REF　VOUT. When output voltage is required 2V or more, set the output voltage by the resistance division value.

- SW (22-29 pin)

  This is connected pin for coil. SW voltage swings between VIN and GND. It is recommended to connect by heavy and short pattern to coil.

- VIN (31-36 pin)

  This is input power supply pin. Recommend input voltage is 3.3V to 20V. Connect the input capacitor against PGND directly.

- PGND (15-21, 30 pin)

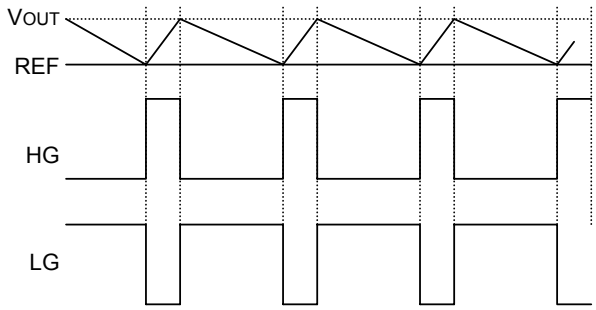
  This is power ground pin. It is recommended to connect by heavy and short pattern. Connect in reverse side of IC when connecting to GND (6 pin).

●Explanation of Operation

The BD95500MUV is a switching regulator controller incorporating ROHM's proprietary H^{3}REG CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the tON time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM) control when the load is light, to further increase efficiency.

H^{3}Reg^{TM} control

(Normal operation)

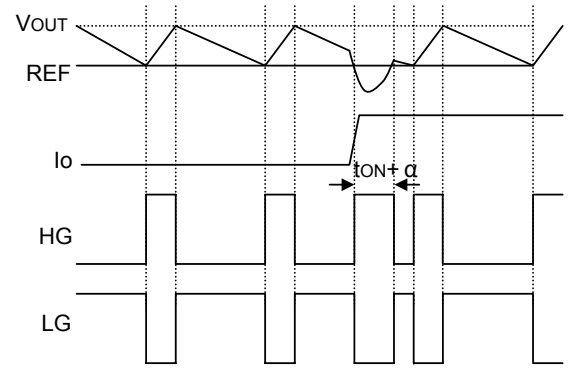


When VOUT falls to a threshold voltage (REF), the drop is detected, activating the H^{3}REG CONTROLLA system.

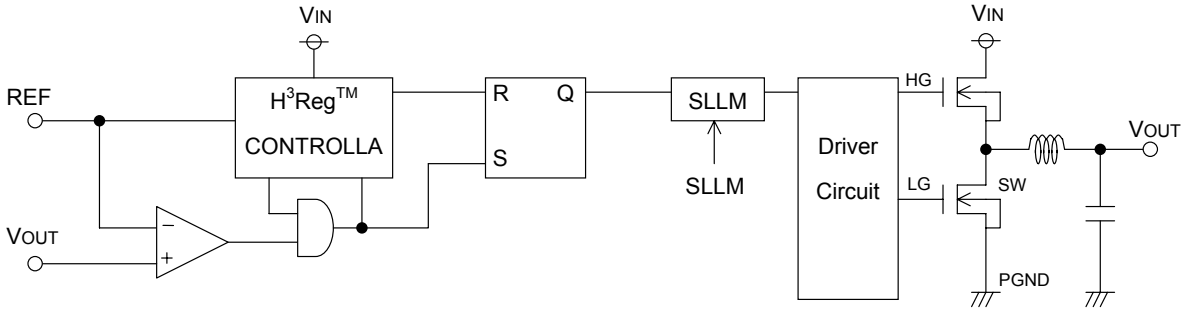
$$T_{ON} = \frac{REF}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

HG output is determined by the formula above.

(VOUT drops due to a rapid load change)

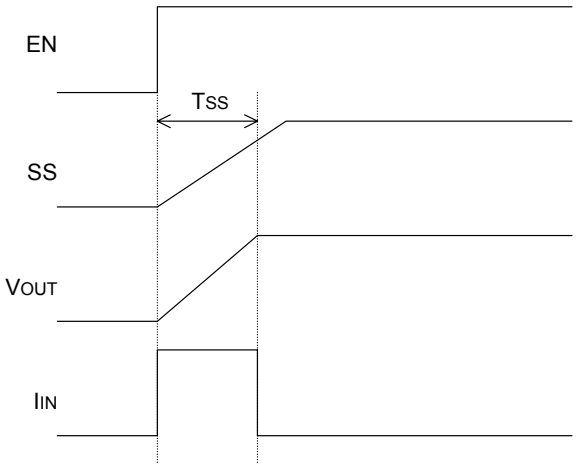


When VOUT drops due to a rapid load change, and the voltage remains below VREF after the programmed tON time interval has elapsed, the system quickly restores VOUT by extending the tON time, improving the transient response.



●Timing Chart

・Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage “ramping start.” Soft start timing and incoming current are calculated with formulas (2) and (3) below.

Soft start time

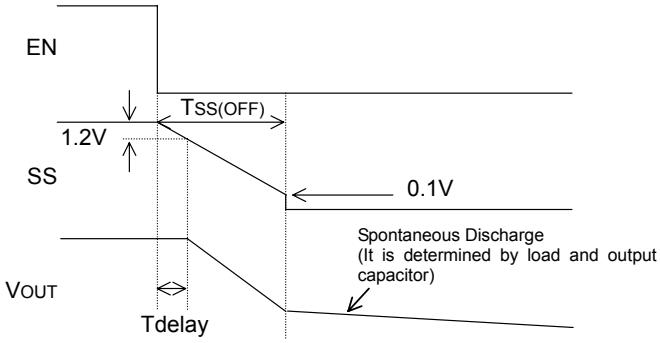
$$Tss = \frac{REF \times Css}{4\,\mu A(typ)} \quad [sec] \quad \cdot\cdot\cdot (2)$$

Rush current

$$I_{IN}(ON) = \frac{Co \times V_{OUT}}{Tss} \quad [A] \quad \cdot\cdot\cdot (3)$$

(Css: Soft start capacitor; Co: Output capacitor)

・Soft Stop Function



Soft stop is exercised with the EN pin set low. Current control takes effect at startup, enabling a moderate output voltage. Soft start timing and incoming current are calculated with formulas (4) below.

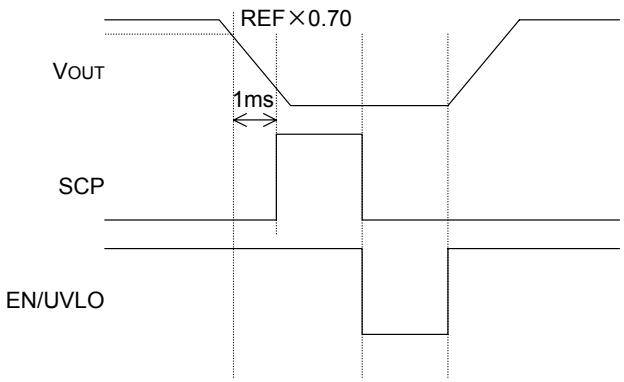
Soft stop time

$$T_{SS(OFF)} = \frac{(REF + 2V_{BE}) \times Css}{1\,\mu A\,(typ)} \quad [sec] \quad \cdot\cdot\cdot (4)$$

$$\Delta V_{SS} = 1.2[V]\ (typ)$$

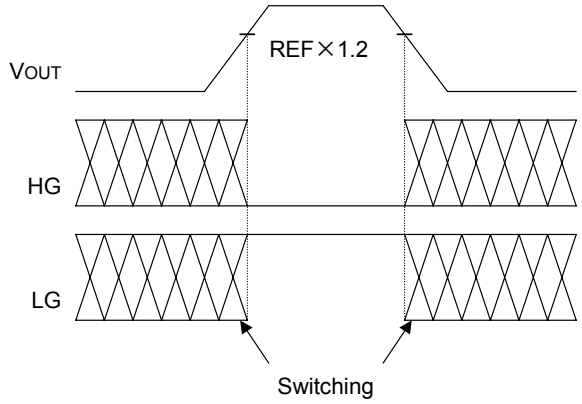
$$Tdelay = \frac{Css}{1\,\mu A(typ)} \quad [sec] \quad \cdot\cdot\cdot (5)$$

・Timer Latch Type Short Circuit Protection



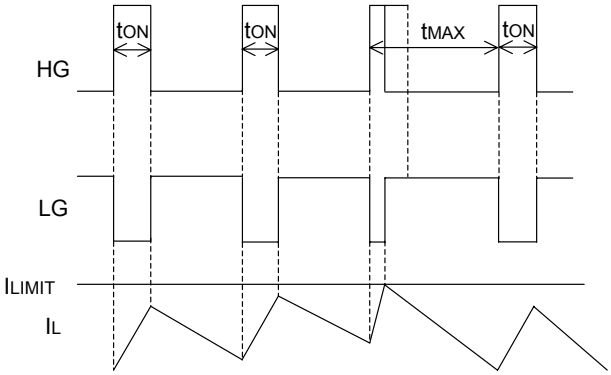
When output voltage (Is-) falls to REF×0.7 or less, SCP comparator inside IC is exercised.
If the status of High is continued 1ms or more (programmed time inside IC), the IC goes OFF. It can be restored either by reconnecting the EN pin or disabling UVLO.

・Output Over Voltage Protection



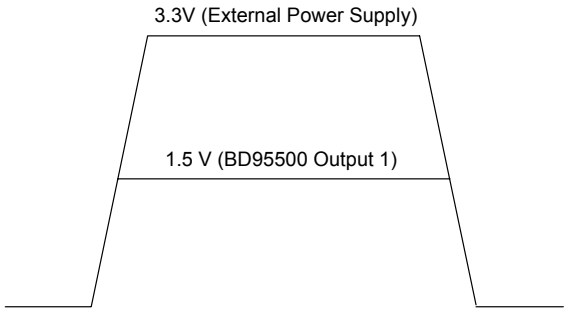
When output rise to or above REF×1.2, output over voltage protection is exercised, and low side FET goes up maximum for reducing output. (LG=High, HG=Low). When output falls, it returns to the standard mode.

・Over current protection circuit



During the normal operation, when VOUT becomes less than REF Voltage, HG becomes High during the time tON (P9). However, when inductor current exceeds I_{LIMIT} threshold, HG becomes OFF.
After MAX ON TIME, HG becomes ON again if the output voltage is lower than the specific voltage level and I_L is lower than I_{LIMIT} level.

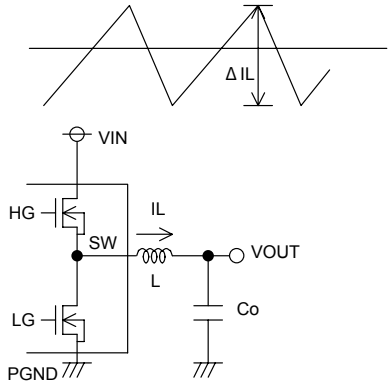
・Synchronous operation with external power supply



These power supply sequences are realized to connect SS pin to other power supply output through the resistance (10kΩ).

●External Component Selection

1. Inductor (L) selection



Output Ripple Current

The inductor value is a major influence on the output ripple current. As formula (5) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times V_{IN}\times f} \quad [A] \cdots (4)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3\times I_{OUT}\text{max.} \quad [A] \cdots (5)$$

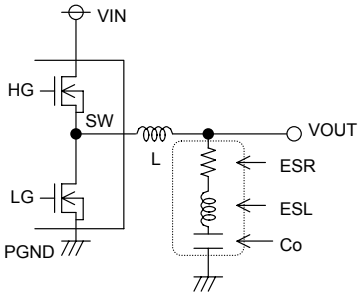
$$L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times V_{IN}\times f} \quad [H] \cdots (6)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (Co) Selection



Output Capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance and equivalent series inductance required to set the output ripple voltage 20mV or more.

In selecting the limit of inductor, be sure to allow enough margin for output voltage. Output ripple voltage is determined as in formula (7) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / T_{ON} \cdots (7)$$

(ΔI_L: Output ripple current; ESR: Co equivalent series resistance, ESL: equivalent series inductance)

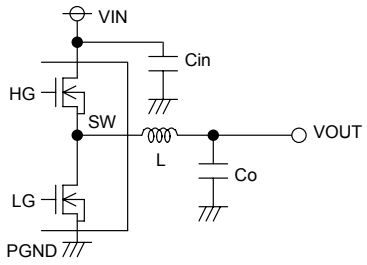
Please give due consideration to the conditions in formula (8) below for output capacity, bear in mind that output rise time must be established within the soft start time frame.

$$Co \leqq \frac{TSS\times(Limit-I_{OUT})}{V_{OUT}} \quad \cdots (8)$$

Tss: Soft start time (See formula (2) in P10)
Limit: Over current detection (See formula (10)(11) in P13)

Note: Improper capacitor may cause startup malfunctions

3. Input Capacitor (Cin) Selection



Input Capacitor

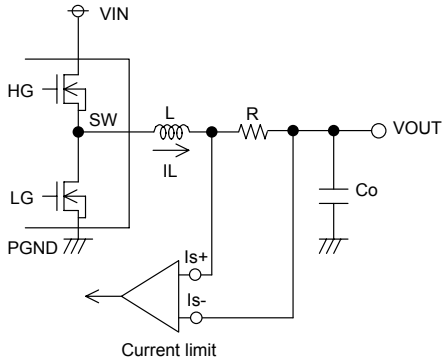
The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (9) below.

$$I_{RMS} = I_{OUT}\times \frac{\sqrt{V_{IN}\,(V_{IN}-V_{OUT})}}{V_{IN}} \quad [A] \cdots (9)$$

Where $V_{IN}=2\times V_{OUT}$, $I_{RMS}=\frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

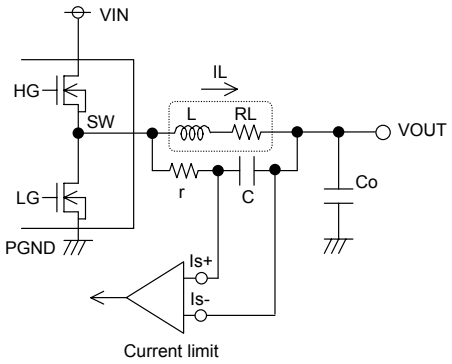
4. Setting Detection Resistance



The over current protection function detects the output ripple current peak value. This parameter (setting value) is determined as in formula (10) below.

$$I_{LMIT}=\frac{V_{ILIM}\times 0.1}{R}\ [A]\ \cdot\ \cdot\ \cdot\ (10)$$

(V_{ILIM}: ILIM voltage, R: Detection resistance)

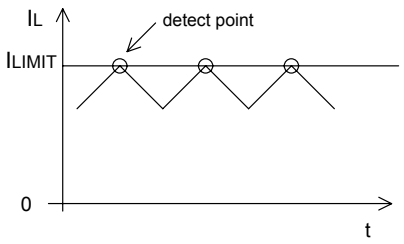


When the over current protection is detected by DCR of coil L, this parameter (setting value) is determined as in formula (11) below.

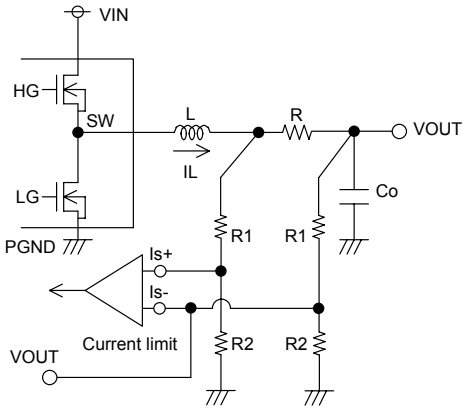
$$I_{LMIT}=V_{ILIM}\times 0.1\times\frac{r\times C}{L}\ [A]\ \cdot\ \cdot\ \cdot\ (11)$$

$$(RL=\frac{L}{r\times C})$$

(V_{ILIM}:ILIM voltage, RL: the DCR value of coil)



As soon as the voltage drop between Is+ and Is- generated by the inductor current becomes specific threshold, the gate voltage of the high side MOSFET becomes low.
Since the peak voltage of the inductor ripple current is detected, this operation can sense high current ripple operation caused by inductance saturated rated current and lead to high reliable systems.

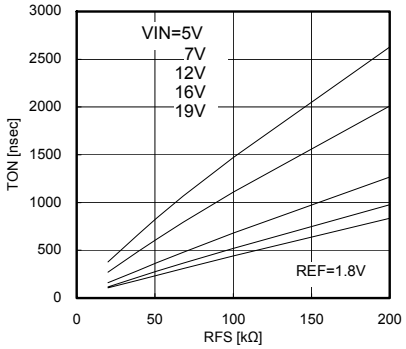


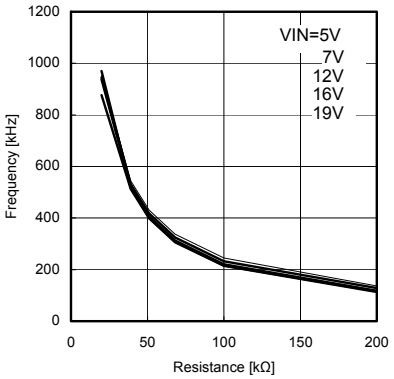
When the output voltage is 2.7V or more, use the resistance for setting output voltage like left figure, for Is+ and Is-.
According to the setting value above, I_{LIMIT} setting current is in proportion to the divided ratio.

$$I_{LMIT}=\frac{R1+R2}{R1}\times\frac{V_{LIMIT}\times 0.1}{R}\ [A]\ \cdot\ \cdot\ \cdot\ (12)$$

(V_{ILIM}: ILIM voltage R: Detection resistance)

5.Setting frequency



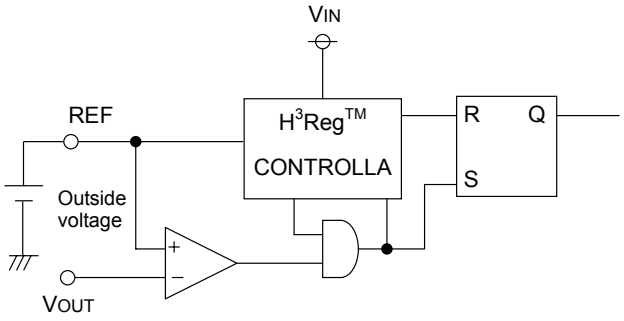


The On Time (t_{ON}) at steady state is determined by resistance value connected to FS pin.
But actually SW rising time and falling time come up due to influence of the external MOSFET gate capacity or switching speed and t_{ON} is increased.
The frequency is determined by the following formula after t_{ON}, input current and the REF voltage are fixed.

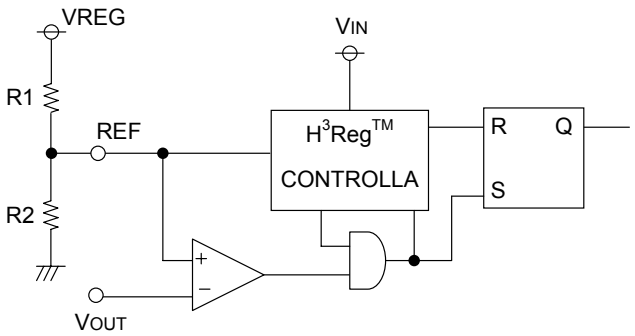
$$F = \frac{REF}{V_{IN} \times t_{ON}} \quad \cdots (13)$$

Consequently, total frequency becomes lower than the formula above.
T_{ON} is also influenced by Dead Time around the output current 0A area in continuous mode.
This frequency becomes lower than setting frequency.
It is recommended to check the steady frequency in large current area (at the point where the coil current doesn't back up).

6. Setting standard voltage (REF)



It is available to synchronize setting the reference voltage (REF) with outside supply voltage [V] by using outside power supply voltage.



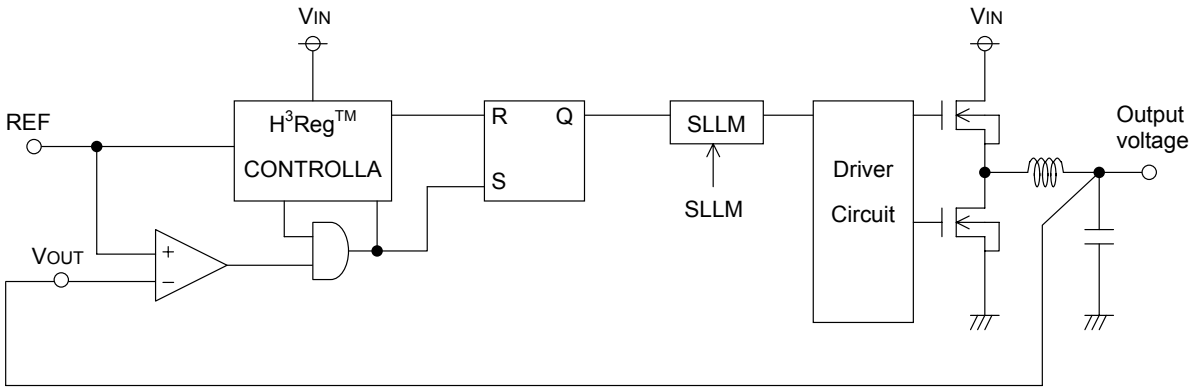
It is available to set the reference voltage (REF) by the resistance division value from VREG in case it is not set REF from an external power supply.

$$REF = \frac{R2}{R1+R2} \times VREG\ [V] \quad \cdots (14)$$

7. Setting output voltage

This IC is operated that output voltage is REF　VOUT.

And it is operated that output voltage is feed back to FB pin in case the output voltage is 0.7V to 2.0V.



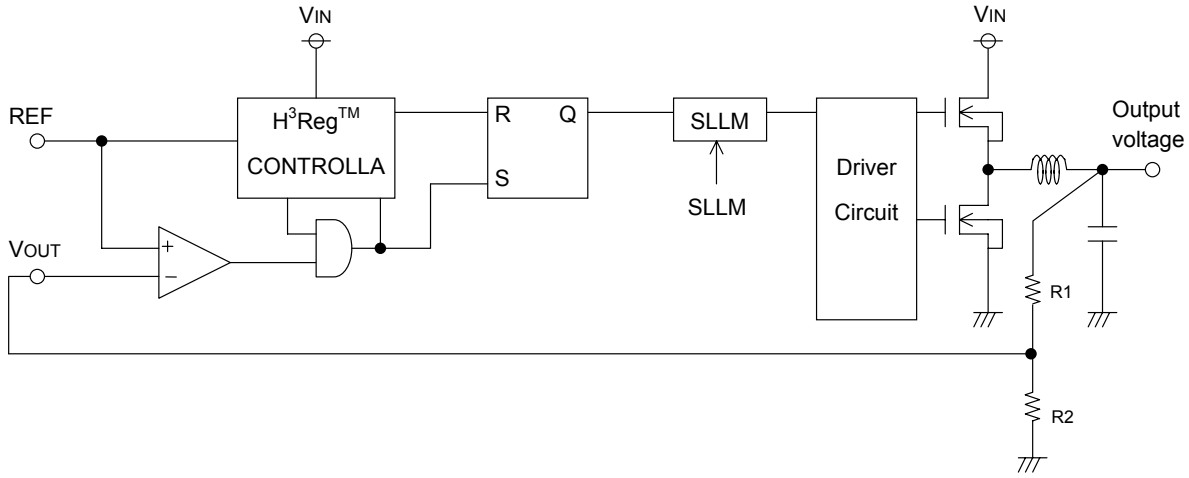
In case the output voltage range is 0.7V to 2.0V.

It is operated that the resistance division value of the output voltage is feed back to VOUT pin in case the output voltage is more than 2.0V.

$$\text{output voltage} \quad \frac{R1+R2}{R2} \times \text{REF [V]} \cdot \cdot \cdot (15)$$

And then the frequency is also in proportion to the divided ratio.

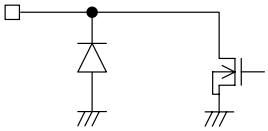
$$F= \frac{R2}{R1+R2} \times \frac{REF}{VIN \times tON} \cdot \cdot \cdot (16)$$



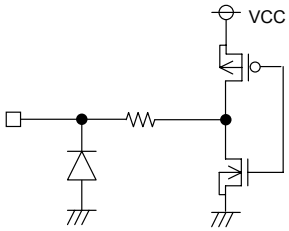
In case the output voltage is more than 2.0V.

●I/O Equivalent Circuit

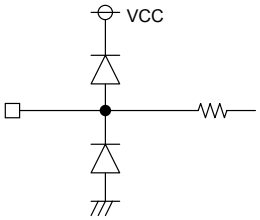
1pin (PGOOD)



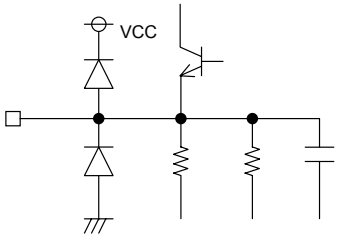
3pin (CE)



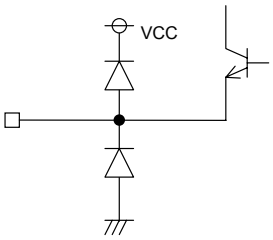
4pin (ILIM)



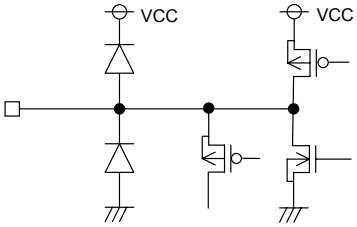
7pin (VREG)



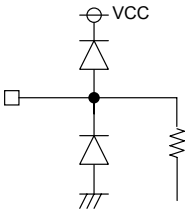
8pin (FS)



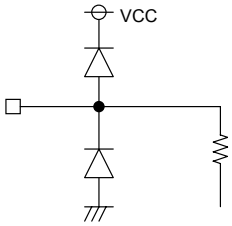
9pin (SS/TRACK)



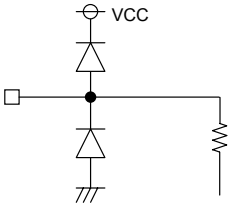
10pin (REF)



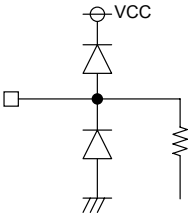
11pin (VOUT)



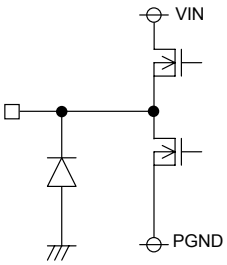
12pin (Is-)



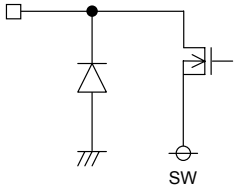
13pin (Is+)



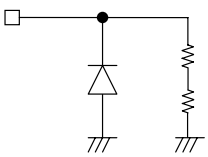
22-29pin (SW)



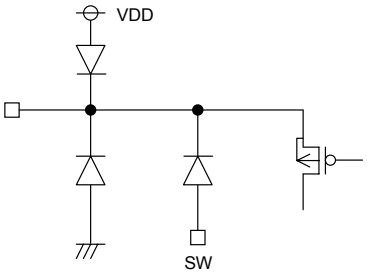
31-36pin (VIN)



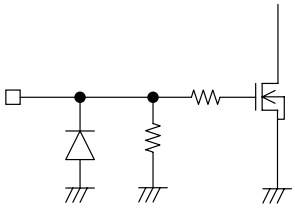
37pin (VINS)



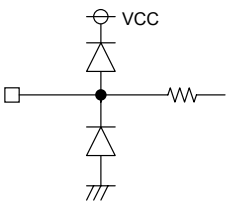
38pin (BOOT)



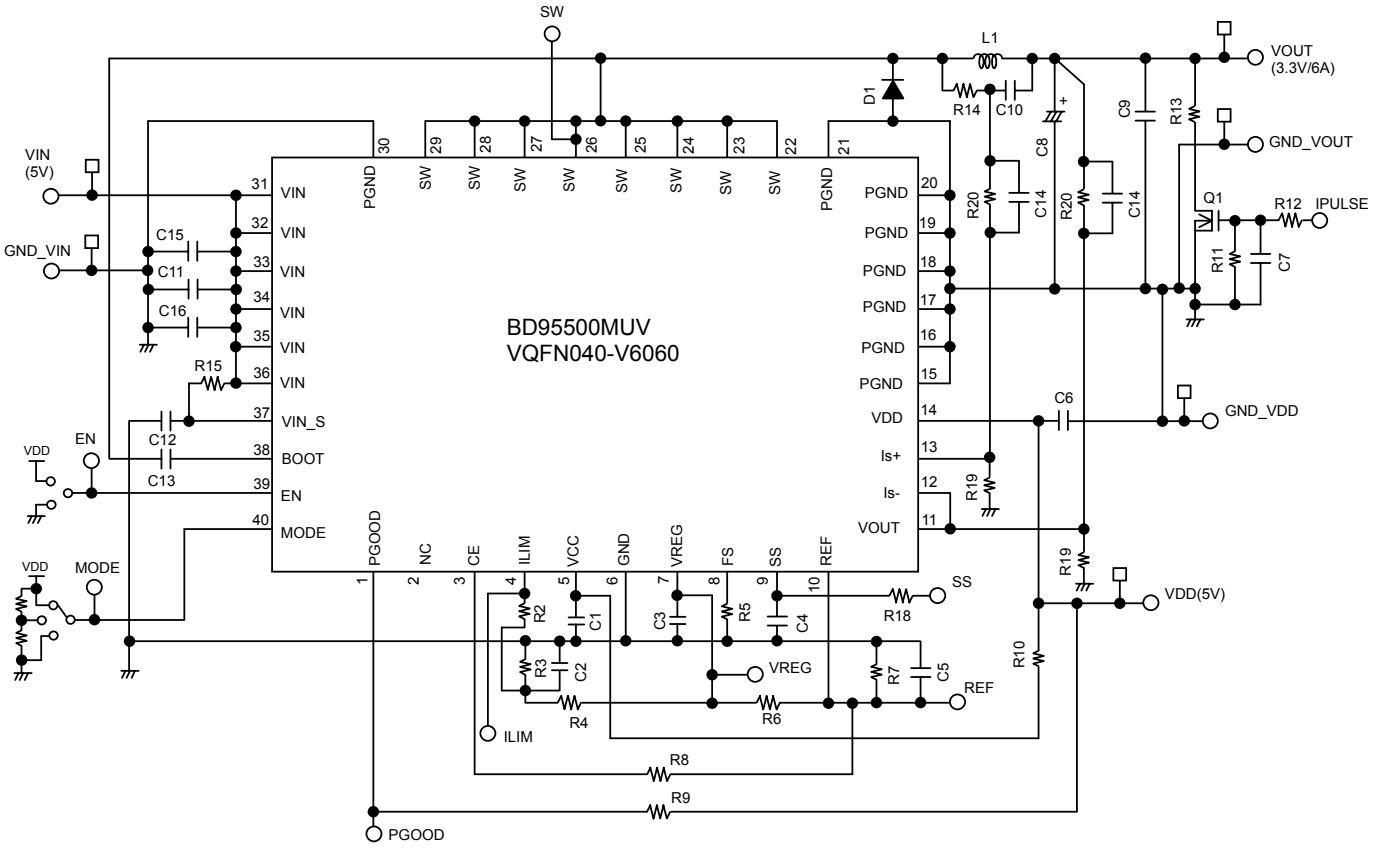
39pin (EN)



40pin (MODE)



●Evaluation Board Circuit (Frequency=300kHz Continuous/SLLM Circuit Example)



●Evaluation Board Parts List

Part No	Value	Company	Part name
U1	-	ROHM	BD95500MUV
D1	-	ROHM	RB051L-40
L1	4.3uH	Sumida	CDEP105NP-4R3MC-88
Q1	-	-	-
R1	0Ω	ROHM	MCR03
R2	0Ω	ROHM	MCR03
R3	100kΩ	ROHM	MCR03
R4	150kΩ	ROHM	MCR03
R5	68kΩ	ROHM	MCR03
R6	100kΩ	ROHM	MCR03
R7	150kΩ	ROHM	MCR03
R8	-	ROHM	MCR03
R9	100kΩ	ROHM	MCR03
R10	10Ω	ROHM	MCR03
R11	-	ROHM	MCR03
R12	10Ω	ROHM	MCR03
R13		ROHM	MCR100
R14	1kΩ	ROHM	MCR03
R15	1kΩ	ROHM	MCR03
R16	100kΩ	ROHM	MCR03

Part No	Value	Company	Part name
R17	100kΩ	ROHM	MCR03
R18	1kΩ	ROHM	MCR03
R19	10kΩ	ROHM	MCR03
R20	12kΩ	ROHM	MCR03
C1	0.1uF	ROHM	MCH18
C2	100pF	ROHM	MCH18
C3	0.47uF	ROHM	MCH18
C4	1000pF	ROHM	MCH18
C5	1000pF	ROHM	MCH18
C6	10uF	ROHM	MCH218
C7	-	ROHM	MCH18
C8	220uF	SANYO or something	functional high polymer
C9	10uF	ROHM	MCH218
C10	0.1uF	ROHM	MCH18
C11	10uF	KYOSERA or something	CM316B106M25A
C12	0.1uF	ROHM	MCH18
C13	0.1uF	ROHM	MCH18
C14	100pF	ROHM	MCH18
C15	10uF	KYOSERA or something	CM316B106M25A
C16	0.1uF	ROHM	MCH182CN104K

●Operation Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

(7) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9) Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD ON Temp. [°C] (typ.)	Hysteresis Temp. [°C] (typ.)
BD95500MUV	175	15

(10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

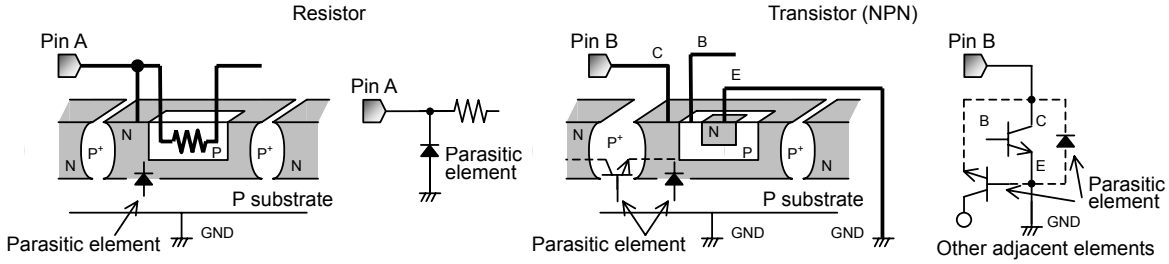
(11) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

◯When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

◯When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

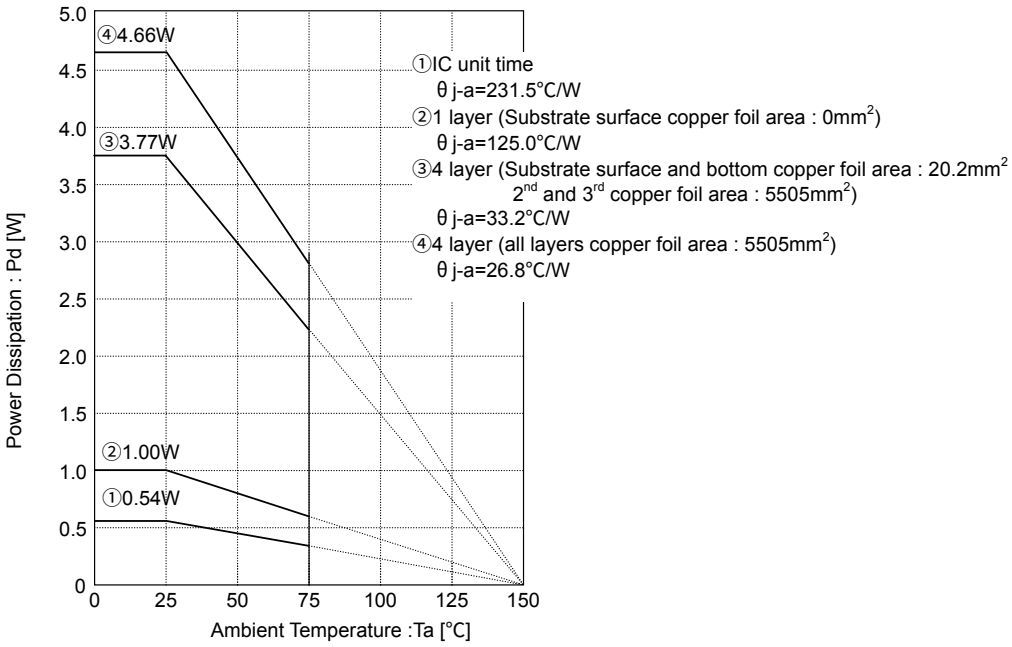


Example of IC structure

(12) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Power Dissipation



VQFN040-V6060

●Type Designations (Selections) for Ordering

B	D	9	5	5	0	0	M	U	V	–	E	2

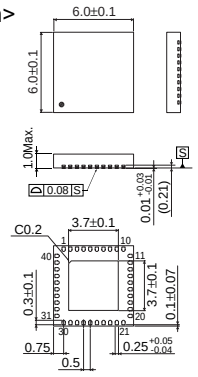
• **BD95500**

Package Type
• **MUV : VQFN040-V6060**

E1 Emboss tape reel pin1 on draw-out side
E2 Emboss tape reel pin1 opposite draw-out side
TL Emboss tape reel pin1 on draw-out side
TR Emboss tape reel pin1 opposite draw-out side

VQFN040-V6060

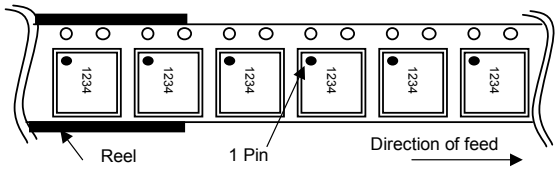
<Dimension>



(Unit:mm)

<Tape and Reel Information>

Tape	Embossed Carrier Tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When ordering, please order in times the amount of package quantity