512K × 8 CMOS FLASH MEMORY WITH FWH INTERFACE

Table of Contents-

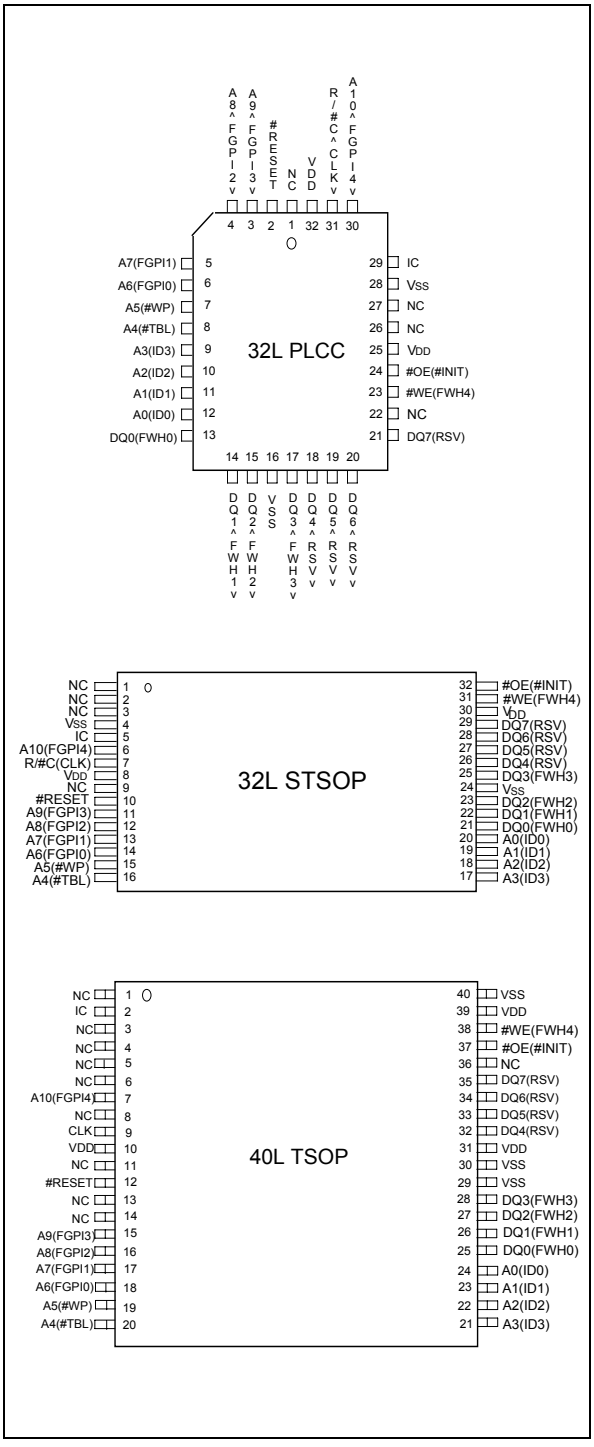
1. GENERAL DESCRIPTION

The W39V040FA is a 4-megabit, 3.3-volt only CMOS flash memory organized as 512K × 8 bits. For flexible erase capability, the 4Mbits of data are divided into 8 uniform sectors of 64 Kbytes, which are composed of 16 smaller even pages with 4 Kbytes. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the W39V040FA results in fast program/erase operations with extremely low current consumption. This device can operate at two modes, Programmer bus interface mode and FWH bus interface mode. As in the Programmer interface mode, it acts like the traditional flash but with a multiplexed address inputs. But in the FWH interface mode, this device complies with the Intel FWH specification. The device can also be programmed and erased using standard EPROM programmers.

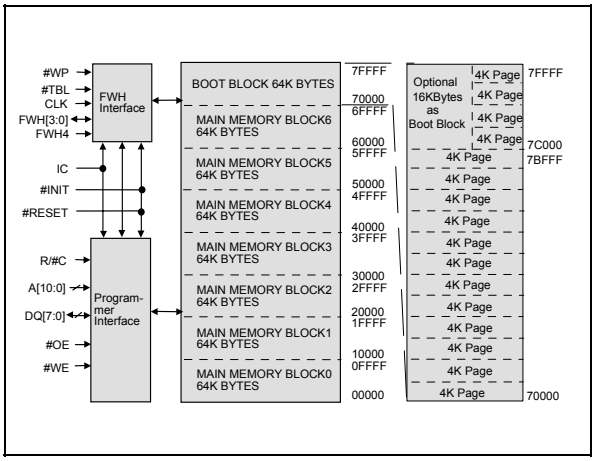
2. FEATURES

- Single 3.3-volt operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast Program operation:
  - Byte-by-Byte programming: 35 μS (typ.)
- Fast Erase operation:
  - Chip erase 100 mS (max.)
  - Sector erase 25 mS (max.)
  - Page erase 25 mS (max.)
- Fast Read access time: Tkq 11 nS
- Endurance: 10K cycles (typ.)
- Twenty-year data retention
- 8 Even sectors with 64K bytes each, which is composed of 16 flexible pages with 4K bytes
- Any individual sector or page can be erased
- Hardware protection:
  - Optional 16K byte or 64K byte Top Boot Block with lockout protection
  - #TBL & #WP support the whole chip hardware protection
- Flexible 4K-page size can be used as Parameter Blocks
- Low power consumption
  - Active current: 12.5 mA (typ. for FWH mode)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32L PLCC, 32L STSOP, 40L TSOP (10 x 20 mm), 32L PLCC Lead free, 32L STSOP Lead free and 40L TSOP (10 x 20 mm) Lead free

3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYM.	INTERFACE		PIN NAME
	PGM	FWH	
IC	*	*	Interface Mode Selection
#RESET	*	*	Reset
#INIT		*	Initialize
#TBL		*	Top Boot Block Lock
#WP		*	Write Protect
CLK		*	CLK Input
FGPI[4:0]		*	General Purpose Inputs
ID[3:0]		*	Identification Inputs They Are Internal Pull Down to Vss
FWH[3:0]		*	Address/Data Inputs
FWH4		*	FWH Cycle Initial
R/#C	*		Row/Column Select
A[10:0]	*		Address Inputs
DQ[7:0]	*		Data Inputs/Outputs
#OE	*		Output Enable
#WE	*		Write Enable
VDD	*	*	Power Supply
VSS	*	*	Ground
RSV	*	*	Reserved Pins
NC	*	*	No Connection

6. FUNCTIONAL DESCRIPTION

6.1 Interface Mode Selection and Description

This device can operate in two interface modes, one is Programmer interface mode, and the other is FWH interface mode. The IC pin of the device provides the control between these two interface modes. These interface modes need to be configured before power up or return from #RESET. When IC pin is set to V_{DD}, the device will be in the Programmer mode; while the IC pin is set to low state (or leaved no connection), it will be in the FWH mode. In Programmer mode, this device just behaves like traditional flash parts with 8 data lines. But the row and column address inputs are multiplexed. The row address are mapped to the higher internal address A[18:11]. And the column address are mapped to the lower internal address A[10:0]. For FWH mode, it complies with the FWH Interface Specification. Through the FWH[3:0] and FWH4 to communicate with the system chipset .

6.2 Read (Write) Mode

In Programmer interface mode, the read (write) operation of the W39V040FA is controlled by #OE (#WE). The #OE (#WE) is held low for the host to obtain (write) data from (to) the outputs (inputs). #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when #OE is high. As for in the FWH interface mode, the read or write is determined by the "bit 0 & bit 1 of START CYCLE ". Refer to the FWH cycle definition and timing waveforms for further details.

6.3 Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is at low state, it will halt the device and all outputs will be at high impedance state. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals.

6.4 Boot Block Operation and Hardware Protection at Initial- #TBL & #WP

There are two alternatives to set the boot block. Either 16K-byte or 64K-byte in the top location of this device can be locked as boot block, which can be used to store boot codes. It is located in the last 16K/64K bytes of the memory with the address range from 7C000(hex)/70000(hex) to 7FFFF(hex).

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout), other memory locations can be changed by the regular programming method.

Besides the software method, there is a hardware method to protect the top boot block and other sectors. Before power on programmer, tie the #TBL pin to low state and then the top boot block will not be programmed/erased. If #WP pin is tied to low state before power on, the other sectors will not be programmed/erased.

In order to detect whether the boot block feature is set on or not, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address 7FFF2(hex). If the DQ0/DQ1 output data is "1," the 64Kbytes/16Kbytes boot block programming lockout feature will be activated; if the DQ0/DQ1 output data is "0," the lockout feature will be inactivated and the boot block can be erased/programmed. But the hardware protection will override the software lock setting, i.e., while the #TBL pin is trapped at low state, the top boot block cannot be programmed/erased whether the output data, DQ0/DQ1 at the address 7FFF2, is "0" or "1". The #TBL will lock the whole 64Kbytes top boot block, it will not partially lock the 16Kbytes boot block. You can

check the DQ2/DQ3 at the address 7FFF2 to see whether the #TBL/#WP pin is in low or high state. If the DQ2 is "0", it means the #TBL pin is tied to high state. In such condition, whether boot block can be programmed/erased or not will depend on software setting. On the other hand, if the DQ2 is "1", it means the #TBL pin is tied to low state, then boot block is locked no matter how the software is set. Like the DQ2, the DQ3 inversely mirrors the #WP state. If the DQ3 is "0", it means the #WP pin is in high state, then all the sectors except the boot block can be programmed/erased. On the other hand, if the DQ3 is "1", then all the sectors except the boot block are programmed/erased inhibited.

To return to normal operation, perform a three-byte command sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

6.5 Chip Erase Operation

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed within fast 100 mS (max). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the other memory sectors will be erased to FF(hex) while the data in the boot block will not be erased (remains as the same state before the chip erase operation). The entire memory array will be erased to FF(hex) by the chip erase operation if the boot block programming lockout feature is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

6.6 Sector/Page Erase Command

Sector/page erase is a six bus cycles operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the sector/page erase command. The sector/page address (any address location within the desired sector/page) is latched on the falling edge of #WE, while the command (30H/50H) is latched on the rising edge of #WE.

Sector/page erase does not require the user to program the device prior to erase. When erasing a sector/page or sectors/pages the remaining unselected sectors/pages are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector/page erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last sector/page erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors/pages being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

6.7 Program Operation

The W39V040FA is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0." The erase operation, which changed entire data in main memory and/or boot block from "0" to "1", is needed before programming.

The program operation is initiated by a 4-byte command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (50 μS max. - T_{BP}) once it is completed and then return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

6.8 Hardware Data Protection

The integrity of the data stored in the W39V040FA is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming and read operation are inhibited when V_{DD} is less than 1.5V typical.

(3) Write Inhibit Mode: Forcing #OE low or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

6.9 Data Polling (DQ_7)- Write Status Detection

The W39V040FA includes a data polling feature to indicate the end of a program or erase cycle. When the W39V040FA is in the internal program or erase cycle, any attempts to read DQ_7 of the last byte loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that DQ_7 will show logical "0" during the erase cycle, and when erase cycle has been completed it becomes logical "1" or true data.

6.10 Toggle Bit (DQ_6)- Write Status Detection

In addition to data polling, the W39V040FA provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

6.11 Register

There are three kinds of registers on this device, the General Purpose Input Registers, the Block Lock Control Registers and Product Identification Registers. Users can access these registers through respective address in the 4Gbytes memory map. There are detail descriptions in the sections below.

6.11.1 General Purpose Inputs Register

This register reads the FGPI[4:0] pins on the W39V040FA.This is a pass-through register which can read via memory address FFBC0100(hex). Since it is pass-through register, there is no default value.

GPI Register Table

BIT	FUNCTION
7 – 5	Reserved
4	Read FGPI4 pin status
3	Read FGPI3 pin status
2	Read FGPI2 pin status
1	Read FGPI1 pin status
0	Read FGPI0 pin status

6.12 Block Locking Registers

This part provides 8 even 64Kbytes blocks, and each block can be locked by register control. These control registers can be set or clear through memory address. Below is the detail description.

Block Locking Registers type and access memory map Table

REGISTERS	REGISTERS TYPE	CONTROL BLOCK	DEVICE PHYSICAL ADDRESS	4GBYTES SYSTEM MEMORY ADDRESS
BLR7	R/W	7	7FFFFh – 70000h	FFBF0002h
BLR6	R/W	6	6FFFFh – 60000h	FFBE0002h
BLR5	R/W	5	5FFFFh – 50000h	FFBD0002h
BLR4	R/W	4	4FFFFh – 40000h	FFBC0002h
BLR3	R/W	3	3FFFFh – 30000h	FFBB0002h
BLR2	R/W	2	2FFFFh – 20000h	FFBA0002h
BLR1	R/W	1	1FFFFh – 10000h	FFB90002h
BLR0	R/W	0	0FFFFh – 00000h	FFB80002h

Block Locking Register Bits Function Table

BIT	FUNCTION
7 – 3	Reserved
2	Read Lock 1: Prohibit to read in the block where set 0: Normal read operation in the block where clear. This is default state.
1	Lock Down 1: Prohibit further to set or clear the Read Lock or Write Lock bits. This Lock Down Bit can only be set not clear. Only the device is reset or re-powered, the Lock Down Bit is cleared. 0: Normal operation for Read Lock or Write Lock. This is the default state.
0	Write Lock 1: Prohibited to write in the block where set. This is default state. 0: Normal programming/erase operation in the block where clear.

Register Based Block Locking Value Definitions Table

BIT [7:3]	BIT 2	BIT 1	BIT 0	RESULT
00000	0	0	0	Full Access.
00000	0	0	1	Write Lock. Default State.
00000	0	1	0	Locked Open (Full Access, Lock Down).
00000	0	1	1	Write Locked, Locked Down.
00000	1	0	0	Read Locked.
00000	1	0	1	Read & Write Locked.
00000	1	1	0	Read Locked, Locked Down.
00000	1	1	1	Read & Write Locked, Locked Down.

6.13 Read Lock

Any attempt to read the data of read locked block will result in “00.” The default state of any block is unlocked upon power up. User can clear or set the write lock bit anytime as long as the lock down bit is not set.

6.14 Write Lock

This is the default state of blocks upon power up. Before any program or erase to the specified block, user should clear the write lock bit first. User can clear or set the write lock bit anytime as long as the lock down bit is not set. The write lock function is in conjunction with the hardware protect pins, #WP & TBL. When hardware protect pins are enabled, it will override the register block locking functions and write lock the blocks no matter how the status of the register bits. Reading the register bit will not reflect the status of the #WP or #TBL pins.

6.15 Lock Down

The default state of lock down bit for any block is unlocked. This bit can be set only once; any further attempt to set or clear is ignored. Only the reset from #RESET or #INIT can clear the lock down bit. Once the lock down bit is set for a block, then the write lock bit & read lock bit of that block will not be set or cleared, and keep its current state.

6.16 Product Identification Registers

In the FWH interface mode, a read from FFBC, 0000(hex) can output the manufacturer code, DA(hex). A read from FFBC,0001(hex) can output the device code 34(hex).

There is an alternative software method (six commands bytes) to read out the Product Identification in both the Programmer interface mode and the FWH interface mode. Thus, the programming equipment can automatically matches the device with its proper erase and programming algorithms.

In the software access mode, a six-byte (or JEDEC 3-byte) command sequence can be used to access the product ID for programmer interface mode. A read from address 0000(hex) outputs the manufacturer code, DA(hex). A read from address 0001(hex) outputs the device code, 34(hex).” The product ID operation can be terminated by a three-byte command sequence or an alternate one-byte command sequence (see Command Definition table for detail).

6.17 Table of Operating Mode

6.17.1 Operating Mode Selection - Programmer Mode

MODE	PINS				
	#OE	#WE	#RESET	ADDRESS	DQ.
Read	V_{IL}	V_{IH}	V_{IH}	AIN	Dout
Write	V_{IH}	V_{IL}	V_{IH}	AIN	Din
Standby	X	X	V_{IL}	X	High Z
Write Inhibit	V_{IL}	X	V_{IH}	X	High Z/DOUT
	X	V_{IH}	V_{IH}	X	High Z/DOUT
Output Disable	V_{IH}	X	V_{IH}	X	High Z

6.17.2 Operating Mode Selection - FWH Mode

Operation modes in FWH interface mode are determined by "START Cycle" when it is selected. When it is not selected, its outputs (FWH[3:0]) will be disable. Please reference to the "FWH Cycle Definition".

6.18 Table of Command Definition

COMMAND DESCRIPTION	NO. OF Cycles (1)	1ST CYCLE Addr. Data	2ND CYCLE Addr. Data	3RD CYCLE Addr. Data	4TH CYCLE Addr. Data	5TH CYCLE Addr. Data	6TH CYCLE Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Sector Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA(5) 30
Page Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	PA(6) 50
Byte Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Top Boot Block Lockout – 64K/16KByte	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40/70
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (4)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (4)	1	XXXX F0					

Notes:

1. The cycle means the write command cycle not the FWH clock cycle.
2. The Column Address / Row Address are mapped to the Low / High order Internal Address. i.e. Column Address A[10:0] are mapped to the internal A[10:0], Row Address A[7:0] are mapped to the internal A[18:11]
3. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
4. Either one of the two Product ID Exit commands can be used.
5. SA: Sector Address

SA = 7XXXXh for Unique Sector7 (Boot Sector)	SA = 3XXXXh for Unique Sector3
SA = 6XXXXh for Unique Sector6	SA = 2XXXXh for Unique Sector2
SA = 5XXXXh for Unique Sector5	SA = 1XXXXh for Unique Sector1
SA = 4XXXXh for Unique Sector4	SA = 0XXXXh for Unique Sector0

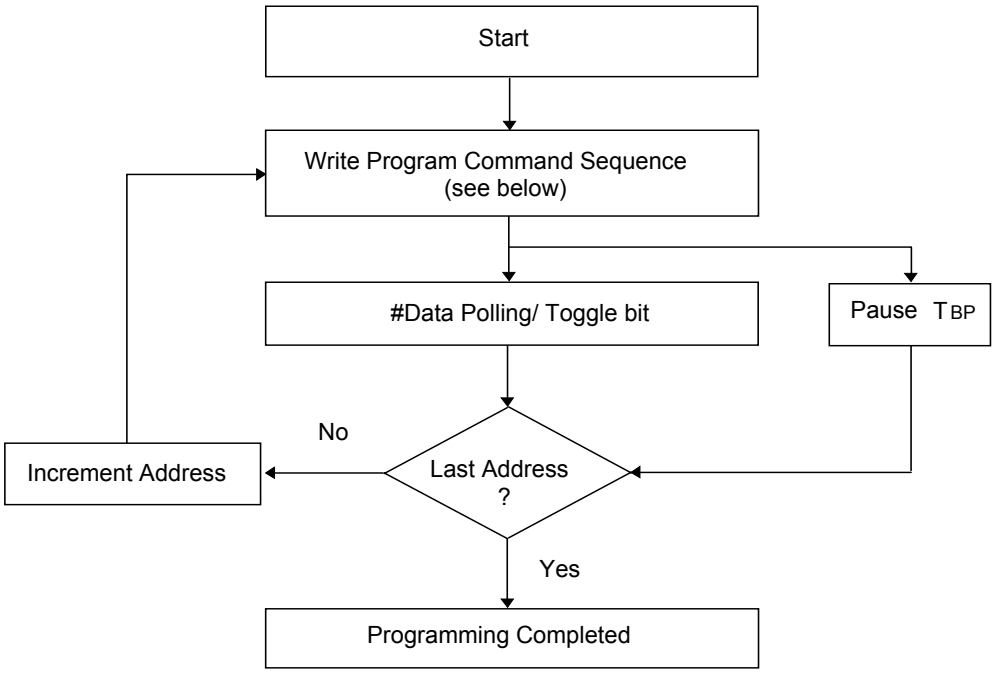
6. PA: Page Address

PA = 7FXXXh for Page 15 in Sector 7	PA = 6FXXXh to 60XXXh for Page 15 to Page 0 In Sector 6 (Reference to the first column)	PA = 5FXXXh to 50XXXh for Page 15 to Page 0 In Sector 5 (Reference to the first column)	PA = 4FXXXh to 40XXXh for Page 15 to Page 0 In Sector 4 (Reference to the first column)	PA = 3FXXXh to 30XXXh for Page 15 to Page 0 In Sector 3 (Reference to the first column)	PA = 2FXXXh to 20XXXh for Page 15 to Page 0 In Sector 2 (Reference to the first column)	PA = 1FXXXh to 10XXXh for Page 15 to Page 0 In Sector 1 (Reference to the first column)	PA = 0FXXXh to 00XXXh for Page 15 to Page 0 In Sector 0 (Reference to the first column)
PA = 7EXXXh for Page 14 in Sector 7							
PA = 7DXXXh for Page 13 in Sector 7							
PA = 7CXXXh for Page 12 in Sector 7							
PA = 7BXXXh for Page 11 in Sector 7							
PA = 7AXXXh for Page 10 in Sector 7							
PA = 79XXXh for Page 9 in Sector 7							
PA = 78XXXh for Page 8 in Sector 7							
PA = 77XXXh for Page 7 in Sector 7							
PA = 76XXXh for Page 6 in Sector 7							
PA = 75XXXh for Page 5 in Sector 7							
PA = 74XXXh for Page 4 in Sector 7							
PA = 73XXXh for Page 3 in Sector 7							
PA = 72XXXh for Page 2 in Sector 7							
PA = 71XXXh for Page 1 in Sector 7							
PA = 70XXXh for Page 0 in Sector 7							

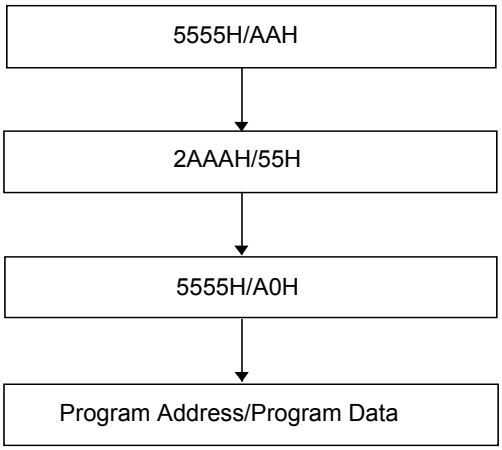
6.19 FWH Cycle Definition

FIELD	NO. OF CLOCKS	DESCRIPTION
START	1	"1101b" indicates FWH Memory Read cycle; while "1110b" indicates FWH Memory Write cycle. 0000b" appears on FWH bus to indicate the initial
IDSEL	1	This one clock field indicates which FWH component is being selected.
MSIZE	1	Memory Size. There is always show “0000b” for single byte access.
TAR	2	Turned Around Time
ADDR	7	Address Phase for Memory Cycle. FWH supports the 28 bits address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e. Address[27:24] on FWH[3:0] first, and Address[3:0] on FWH[3:0] last.)
SYNC	N	Synchronous to add wait state. "0000b" means Ready, "0101b" means Short Wait, "0110b" means Long Wait, "1001b" for DMA only, "1010b" means error, and other values are reserved.
DATA	2	Data Phase for Memory Cycle. The data transfer least significant nibble first and most significant nibble last. (i.e. DQ[3:0] on FWH[3:0] first, then DQ[7:4] on FWH[3:0] last.)

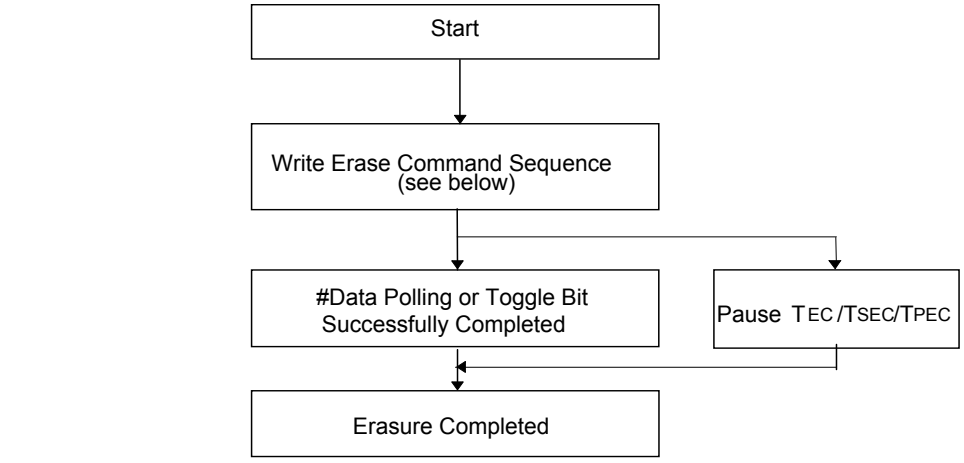
6.20 Embedded Programming Algorithm



Program Command Sequence (Address/Command):

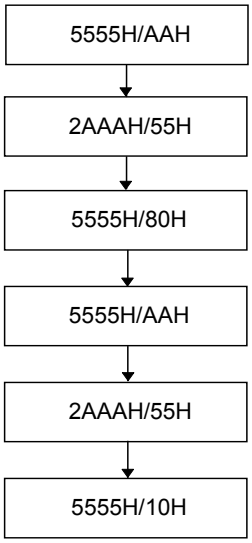


6.21 Embedded Erase Algorithm

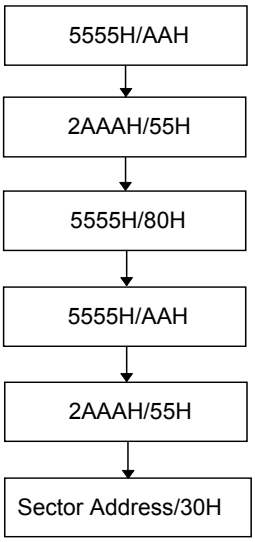


Chip Erase Command Sequence

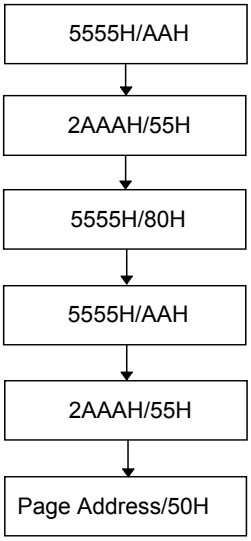
(Address/Command):



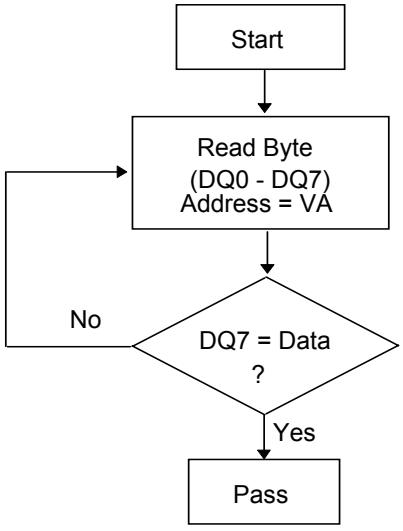
Individual Sector Erase Command Sequence (Address/Command):



Individual Page Erase Command Sequence (Address/Command):

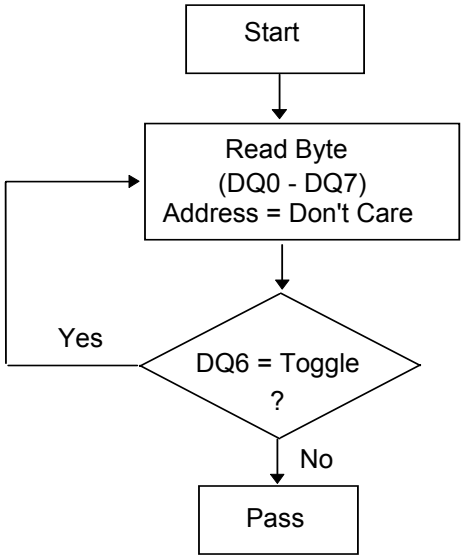


6.22 Embedded #Data Polling Algorithm

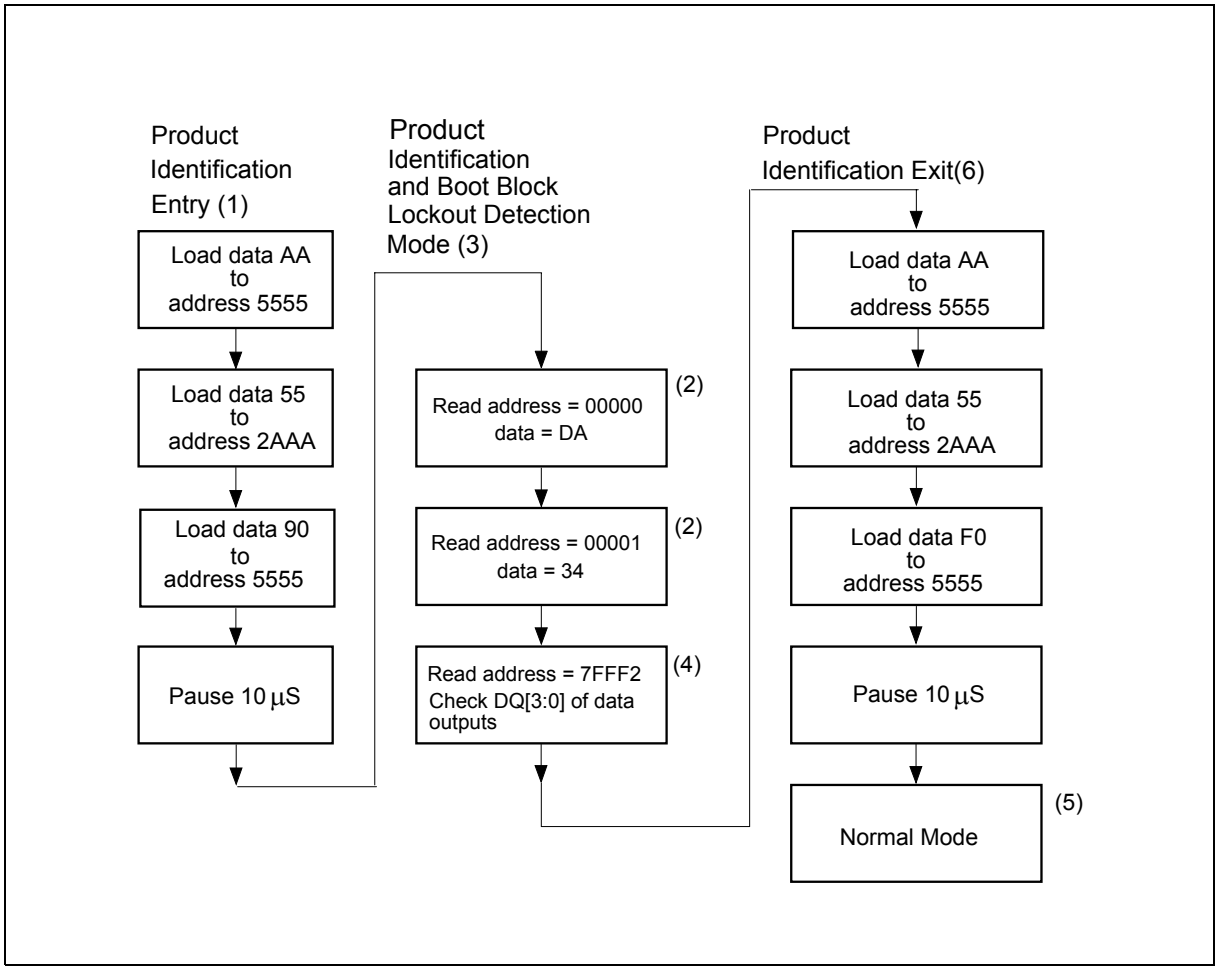


VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= Any of the page addresses within the page being erased during page erase operation
= Any of the device addresses being erased during chip erase operation

6.23 Embedded Toggle Bit Algorithm



6.24 Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7 – DQ0 (Hex); Address Format: A14 – A0 (Hex)

(2) A1 – A18 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

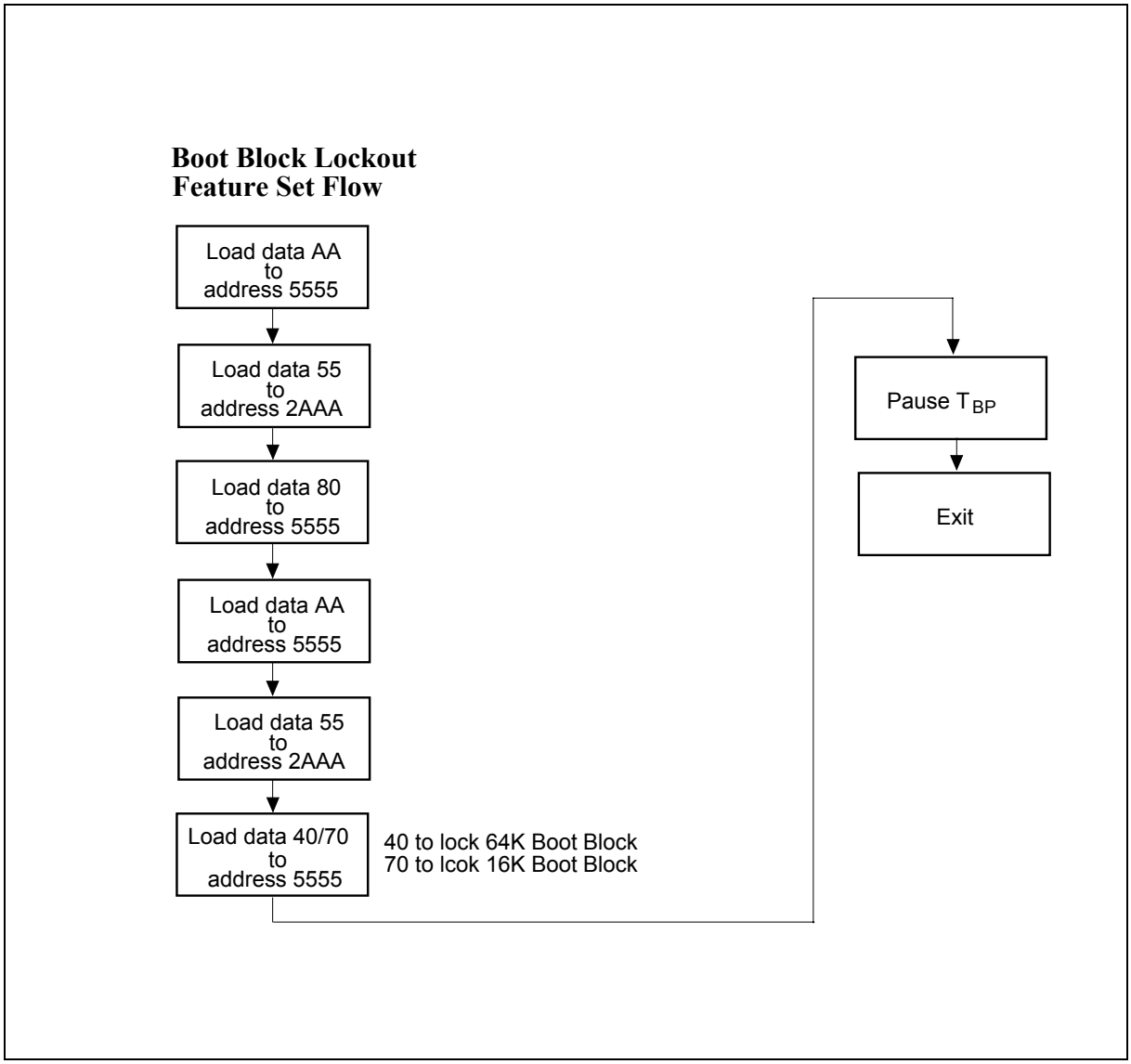
(4) The DQ[3:0] to indicate the sectors protect status as below:

	DQ0	DQ1	DQ2	DQ3
0	64K Boot Block Unlocked by Software	16Kbytes Boot Block Unlocked by Software	64Kbytes Boot Block Unlocked by #TBL hardware trapping	Whole Chip Unlocked by #WP hardware trapping Except Boot Block
1	64K Boot Block Locked by Software	16Kbytes Boot Block Locked by Software	64Kbytes Boot Block Locked by #TBL hardware trapping	Whole Chip Locked by #WP hardware trapping Except Boot Block

(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 (hex.) at XXXX address) can be used to exit the product identification/boot block lockout detection.

6.25 Boot Block Lockout Enable Acquisition Flow



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential	-0.5 to V_{DD} +0.5	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +0.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings May adversely affect the life and reliability of the device.

7.2 Programmer interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ±0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz	-	10	20	mA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	90	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	90	µA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	2.4	-	-	V

7.3 FWH Interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	All I_{out} = 0A, CLK = 33 MHz, in FWH mode operation.	-	12.5	20	mA
Standby Current 1	Isb1	FWH4 = 0.9 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} / 0.1 V_{DD} no internal operation	-	5	25	uA
Standby Current 2	Isb2	FWH4 = 0.1 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} /0.1 V_{DD} no internal operation.	-	3	10	mA
Input Low Voltage	V_{IL}	-	-0.5	-	0.3 V_{DD}	V
Input Low Voltage of #INIT	V_{ILI}	-	-0.5	-	0.2 V_{DD}	V
Input High Voltage	V_{IH}	-	0.5 V_{DD}	-	V_{DD} +0.5	V
Input High Voltage of #INIT Pin	V_{IHI}	-	1.35 V	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA	-	-	0.1 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.9 V_{DD}	-	-	V

7.4 Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

7.5 Capacitance

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

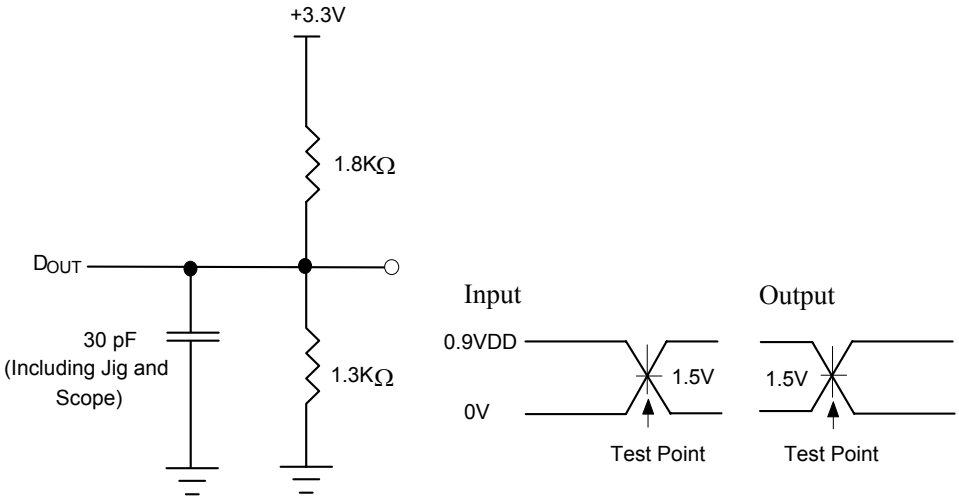
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

8. PROGRAMMER INTERFACE MODE AC CHARACTERISTICS

8.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 0.9 V_{DD}
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

8.2 AC Test Load and Waveform



8.3 Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V040FA		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	300	-	nS
Row / Column Address Set Up Time	T_{AS}	50	-	nS
Row / Column Address Hold Time	T_{AH}	50	-	nS
Address Access Time	T_{AA}	-	150	nS
Output Enable Access Time	T_{OE}	-	75	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#OE High to High-Z Output	T_{OHZ}	-	35	nS
Output Hold from Address Change	T_{OH}	0	-	nS

8.4 Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reset Time	T_{RST}	1	-	-	μS
Address Setup Time	T_{AS}	50	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
R/#C to Write Enable High Time	T_{CWH}	50	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	50	-	-	nS
#OE Hold Time	T_{OEH}	0	-	-	nS
Byte programming Time	T_{BP}	-	35	50	μS
Sector/Page Erase Cycle Time	T_{PEC}	-	20	25	mS
Chip Erase Cycle Time	T_{EC}	-	75	100	mS

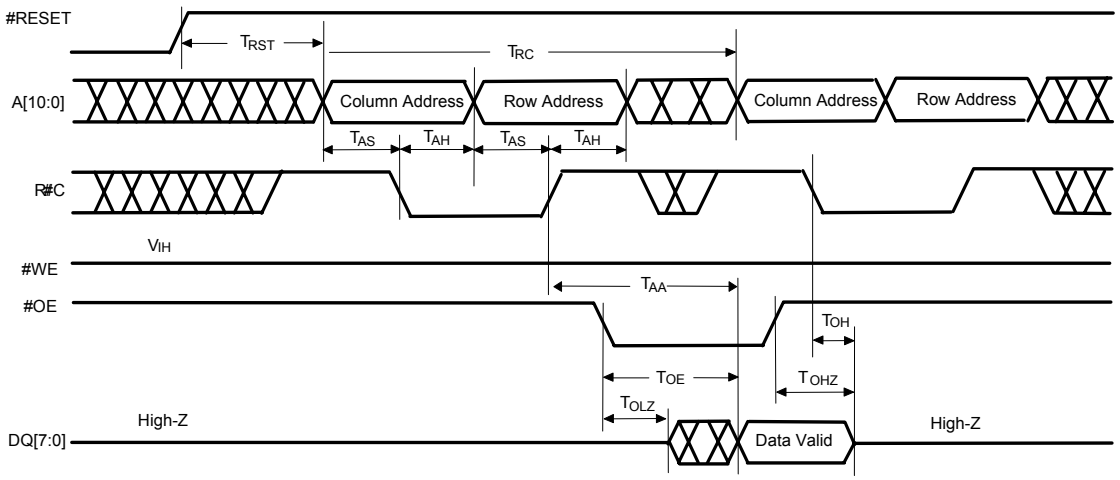
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.
Ref. to the AC testing condition.

8.5 Data Polling and Toggle Bit Timing Parameters

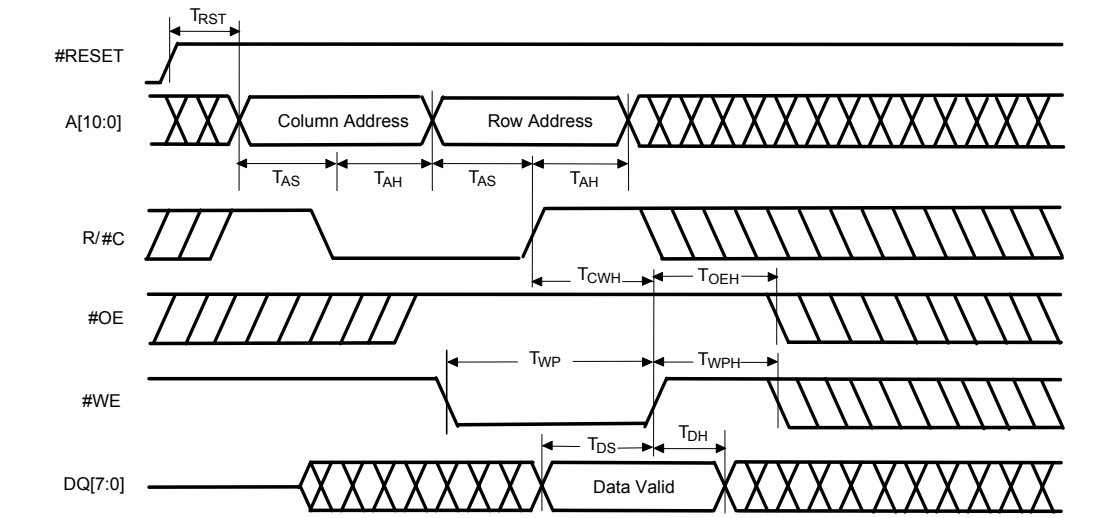
PARAMETER	SYMBOL	W39V040FA		UNIT
		MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	40	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	40	nS

9. TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE

9.1 Read Cycle Timing Diagram

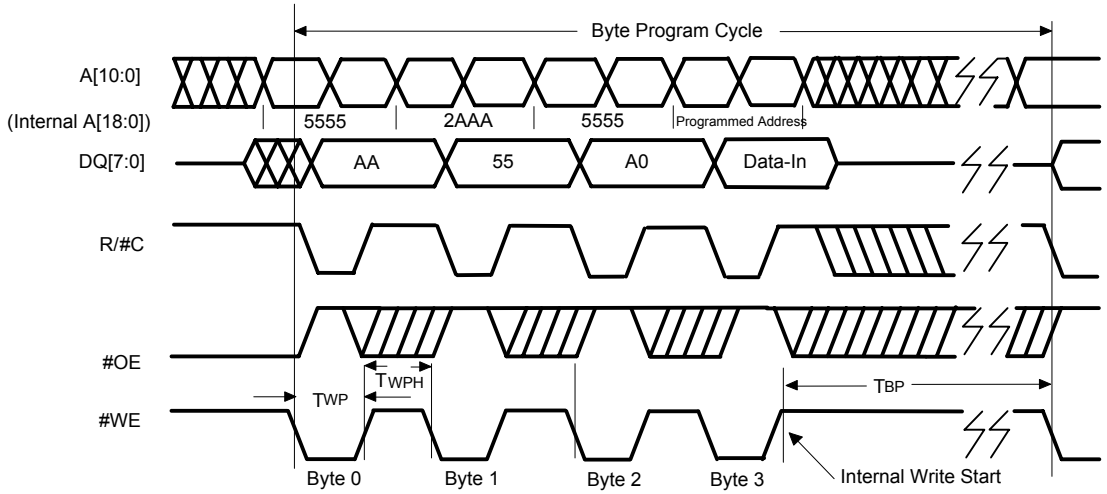


9.2 Write Cycle Timing Diagram



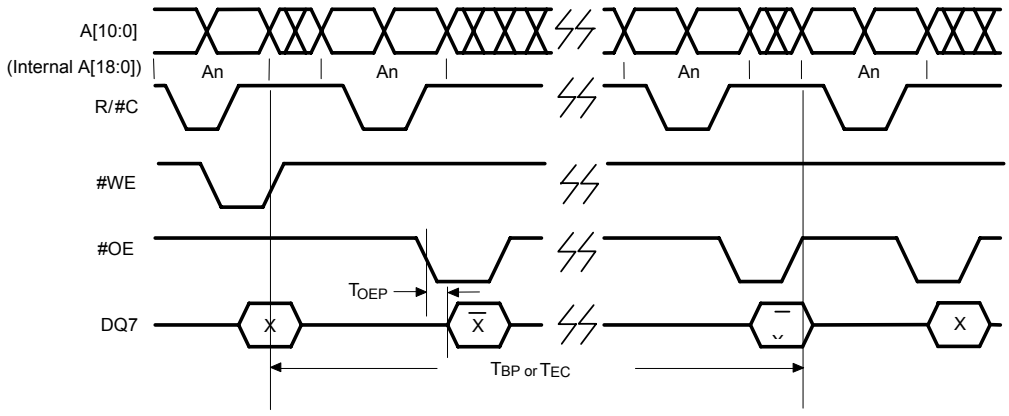
Timing Waveforms for Programmer Interface Mode, continued

9.3 Program Cycle Timing Diagram



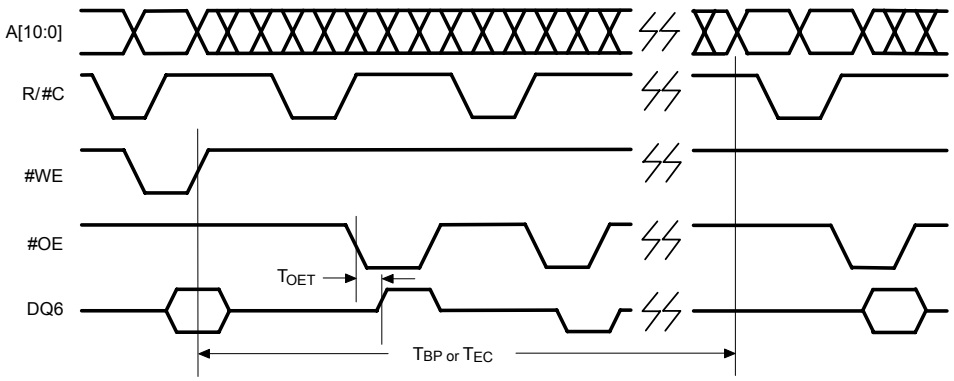
Note: The internal address A[18:0] are converted from external Column/Row address
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[7:0] are mapped to the internal A[18:11].

9.4 #DATA Polling Timing Diagram

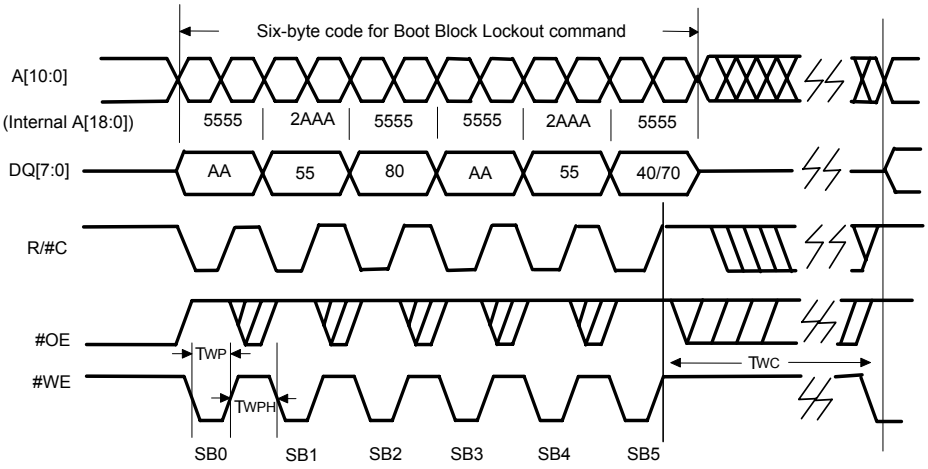


Timing Waveforms for Programmer Interface Mode, continued

9.5 Toggle Bit Timing Diagram



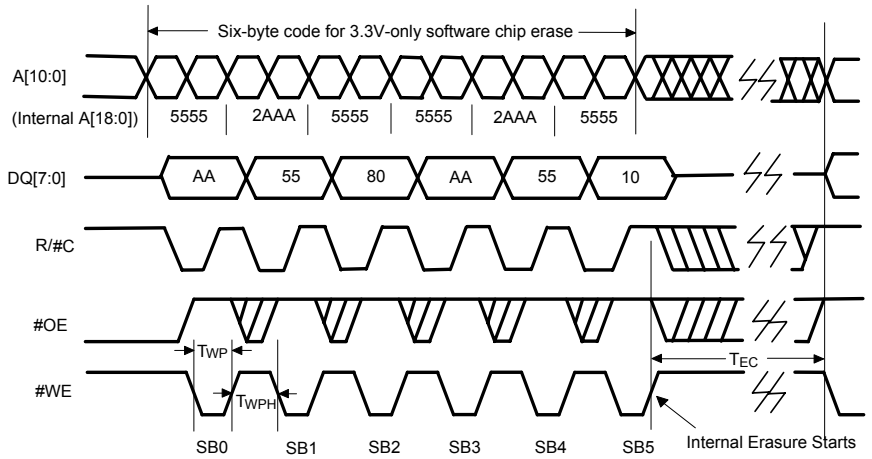
9.6 Boot Block Lockout Enable Timing Diagram



Note: The internal address A[18:0] are converted from external Column/Row ad
Column/Row Address are mapped to the Low/High order internal addr
i.e. Column Address A[10:0] are mapped to the internal A[10:
Row Address A[7:0] are mapped to the internal A[18:1
When 40(hex) is loaded, the 64KByte are locked; while 70(hex) is loaded, the 16KByte is lo

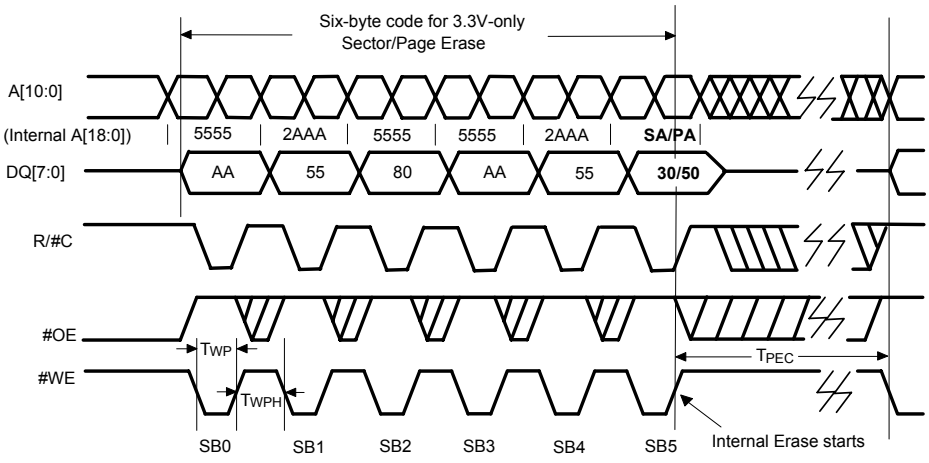
Timing Waveforms for Programmer Interface Mode, continued

9.7 Chip Erase Timing Diagram



Note: The internal address A[18:0] are converted from external Column/Row addr
Column/Row Address are mapped to the Low/High order internal addre
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[7:0] are mapped to the internal A[18:11].

9.8 Sector/Page Erase Timing Diagram



Note: The internal address A[18:0] are converted from external Column/Row address
Column/Row Address are mapped to the Low/High order internal address
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[7:0] are mapped to the internal A[18:11].
SA = Sector Address and PA = Page Address, Please ref. to the "Table of Command Definition'

10. FWH INTERFACE MODE AC CHARACTERISTICS

10.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6 V_{DD} to 0.2 V_{DD}
Input Rise/Fall Slew Rate	1 V/nS
Input/Output Timing Level	0.4V_{DD} / 0.4V_{DD}
Output Load	1 TTL Gate and C_L = 10 pF

10.2 Read/Write Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V040FA		UNIT
		MIN.	MAX.	
Clock Cycle Time	T_{CYC}	30	-	nS
Input Set Up Time	T_{SU}	7	-	nS
Input Hold Time	T_{HD}	0	-	nS
Clock to Data Valid	T_{KQ}	2	11	nS

Note: Minimum and Maximum time has different loads. Please refer to PCI specification.

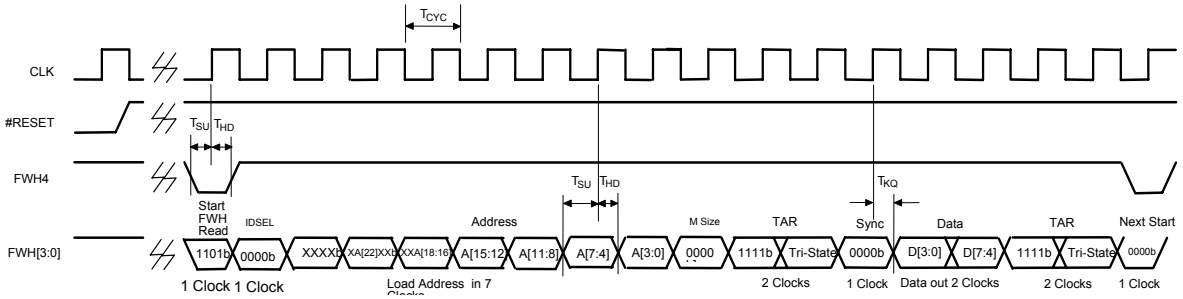
10.3 Reset Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{DD} stable to Reset Active	T_{PRST}	1	-	-	mS
Clock Stable to Reset Active	T_{KRST}	100	-	-	µS
Reset Pulse Width	T_{RSTP}	100	-	-	nS
Reset Active to Output Float	T_{RSTF}	-	-	50	nS
Reset Inactive to Input Active	T_{RST}	10	-	-	µS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.
Ref. to the AC testing condition.

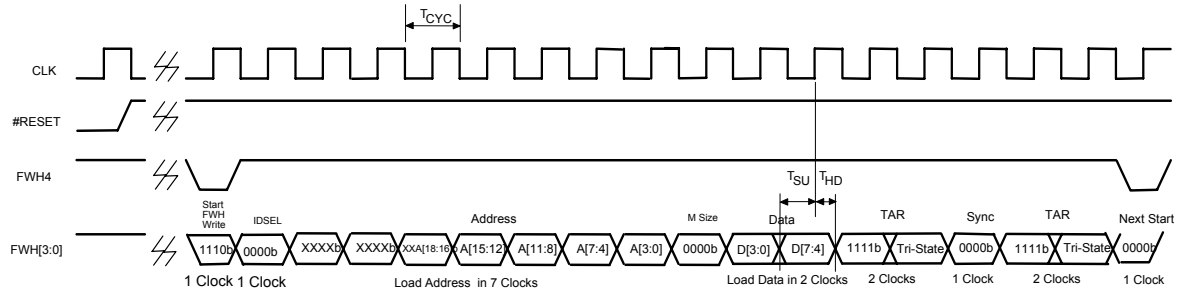
11. TIMING WAVEFORMS FOR FWH INTERFACE MODE

11.1 Read Cycle Timing Diagram



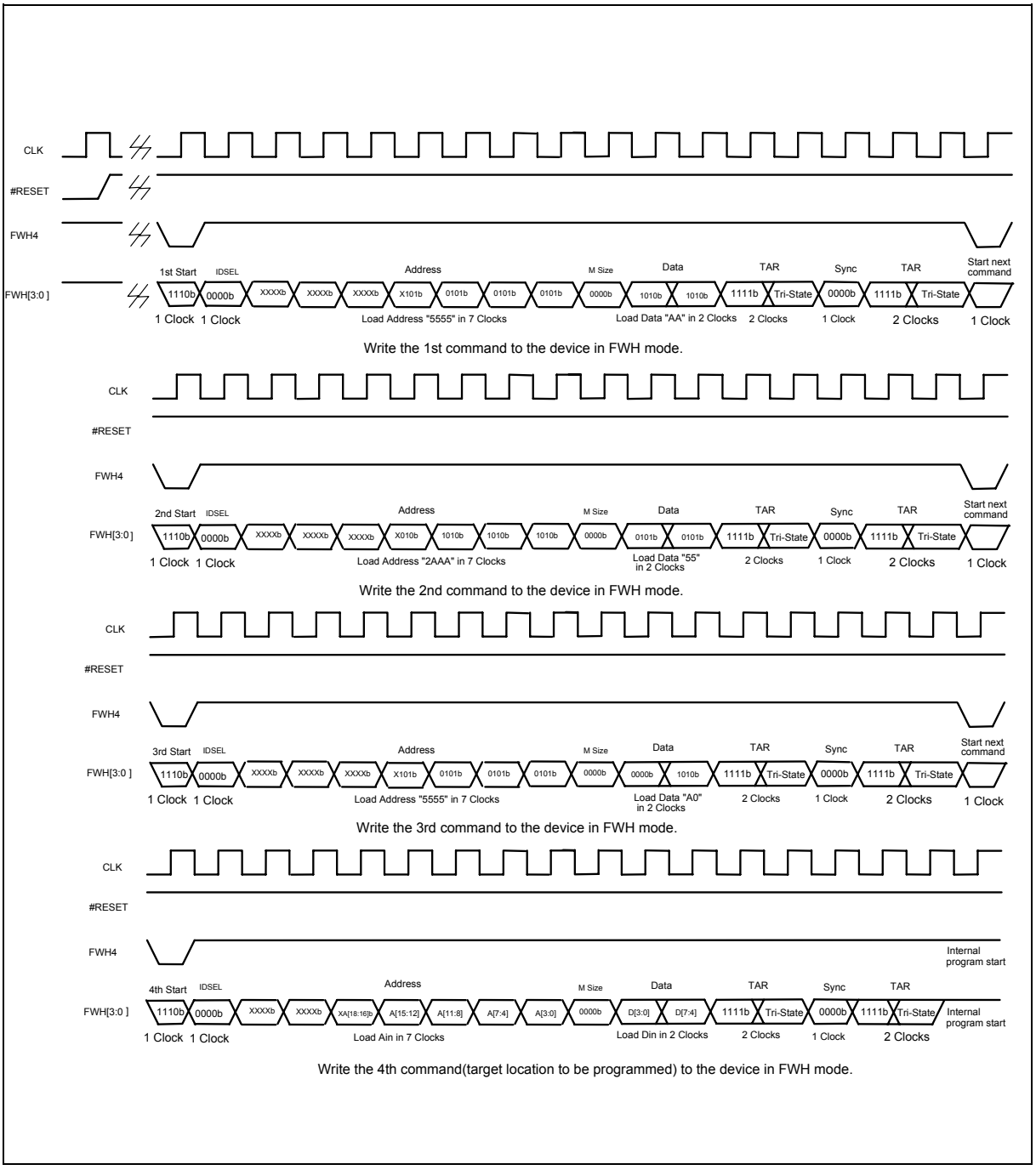
Note: When A22 = high, the host will read the BIOS code from the FWH d
While A22 = low, the host will read the GPI (Add = FFBC010(
Product ID (Add = FFBC0000/FFBC0001) from the FWH dev

11.2 Write Cycle Timing Diagram



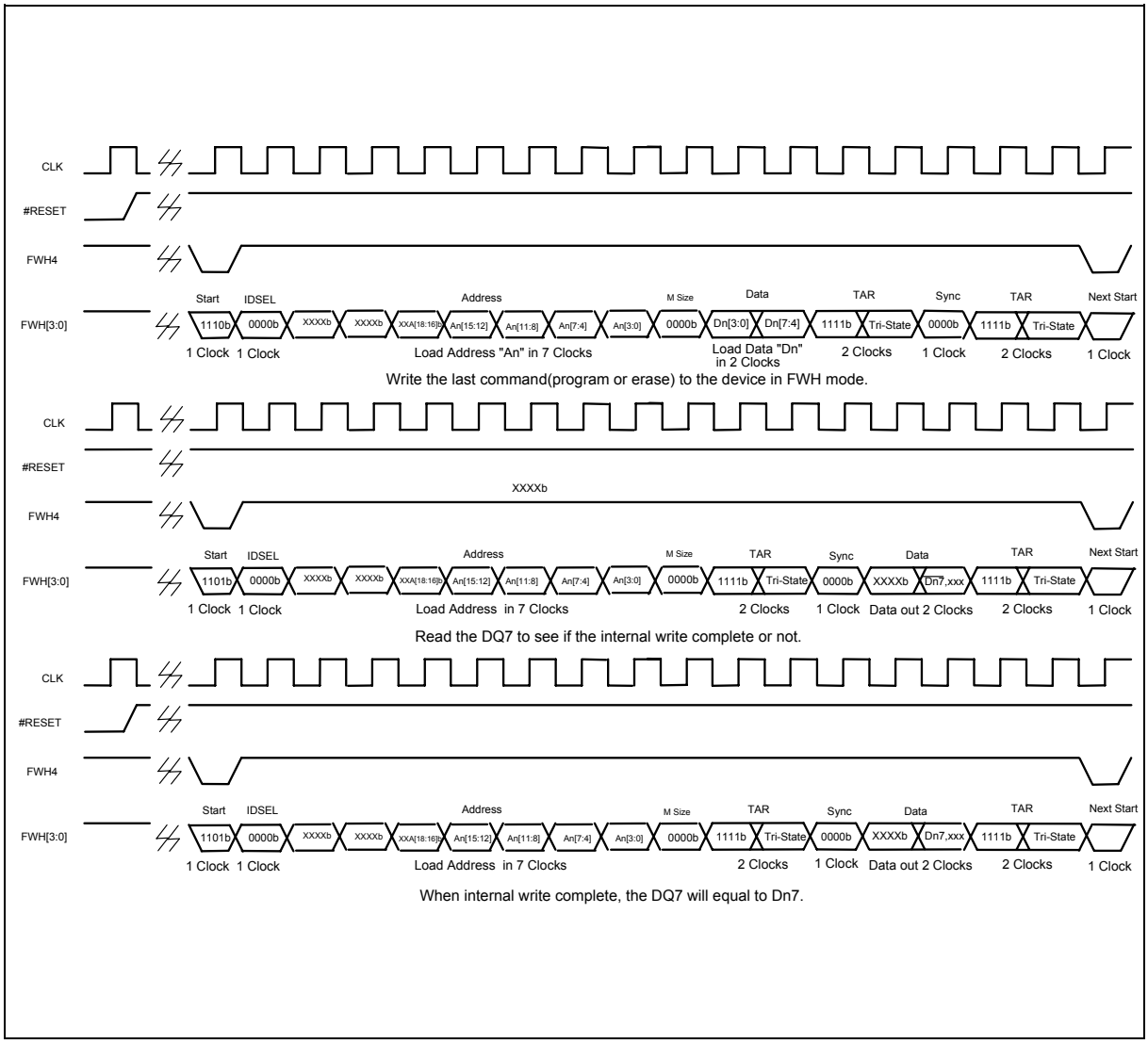
Timing Waveforms, for FWH Interface Mode, continued

11.3 Program Cycle Timing Diagram



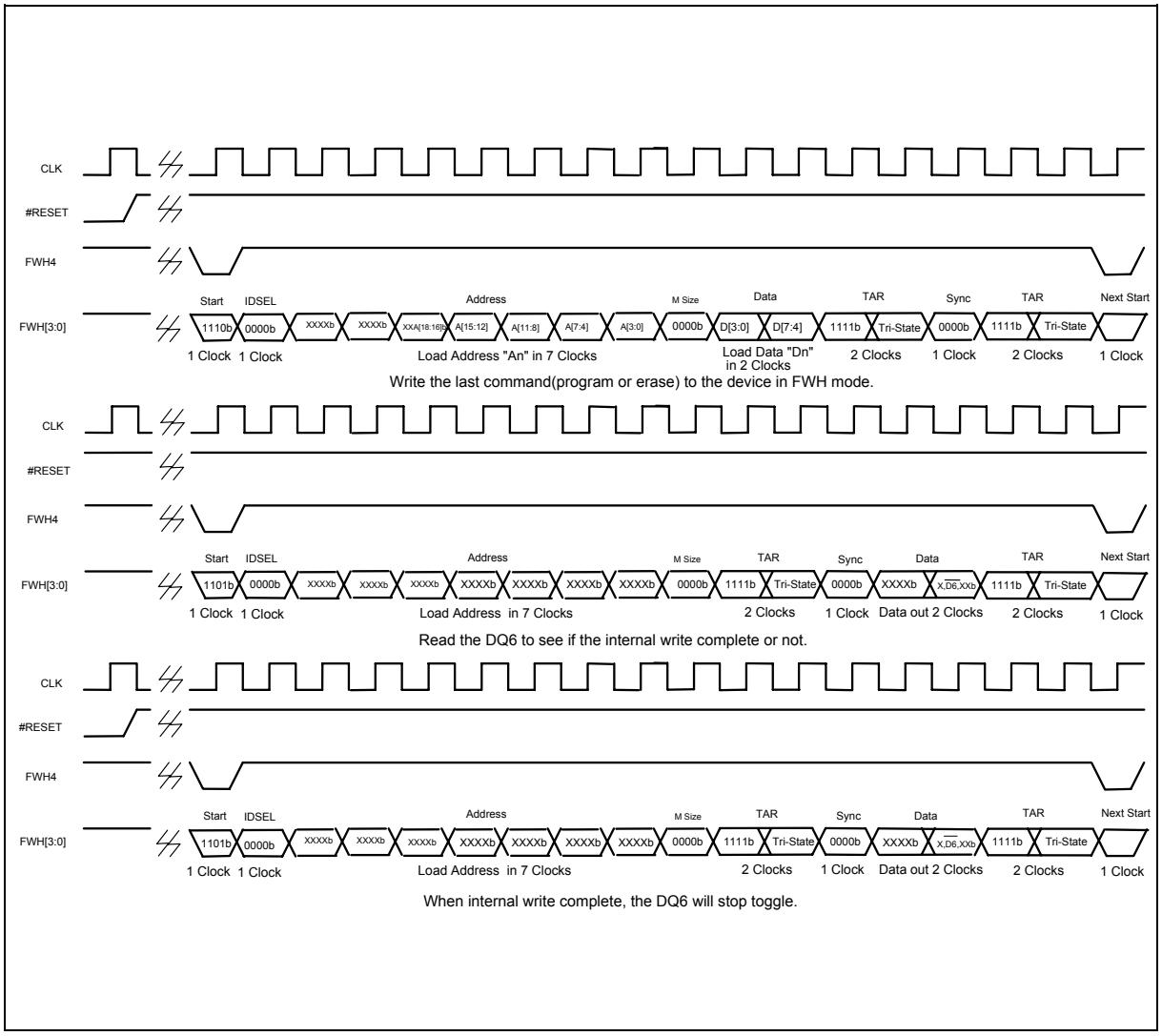
Timing Waveforms for FWH Interface Mode, continued

11.4 #DATA Polling Timing Diagram



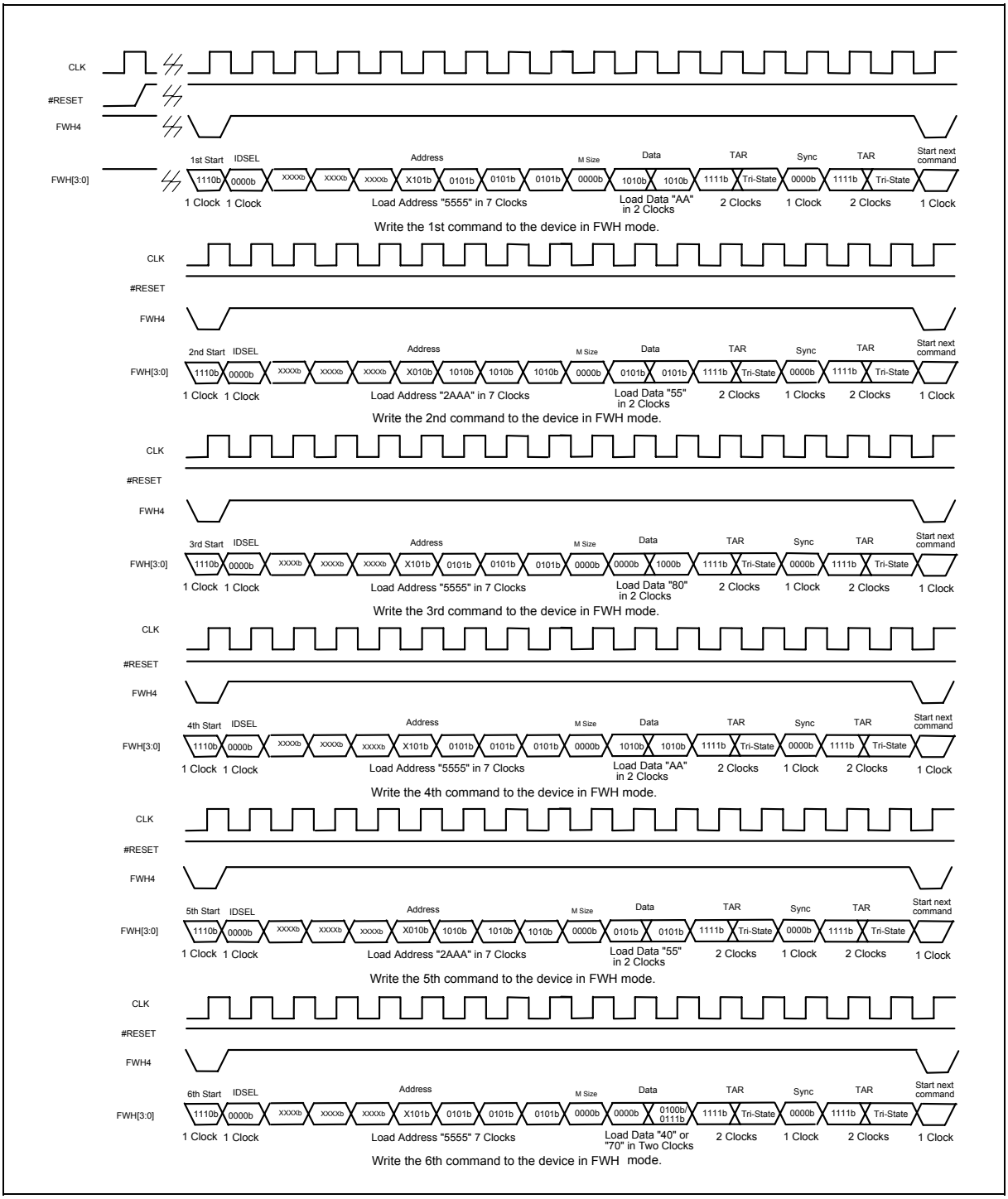
Timing Waveforms for FWH Interface Mode, continued

11.5 Toggle Bit Timing Diagram



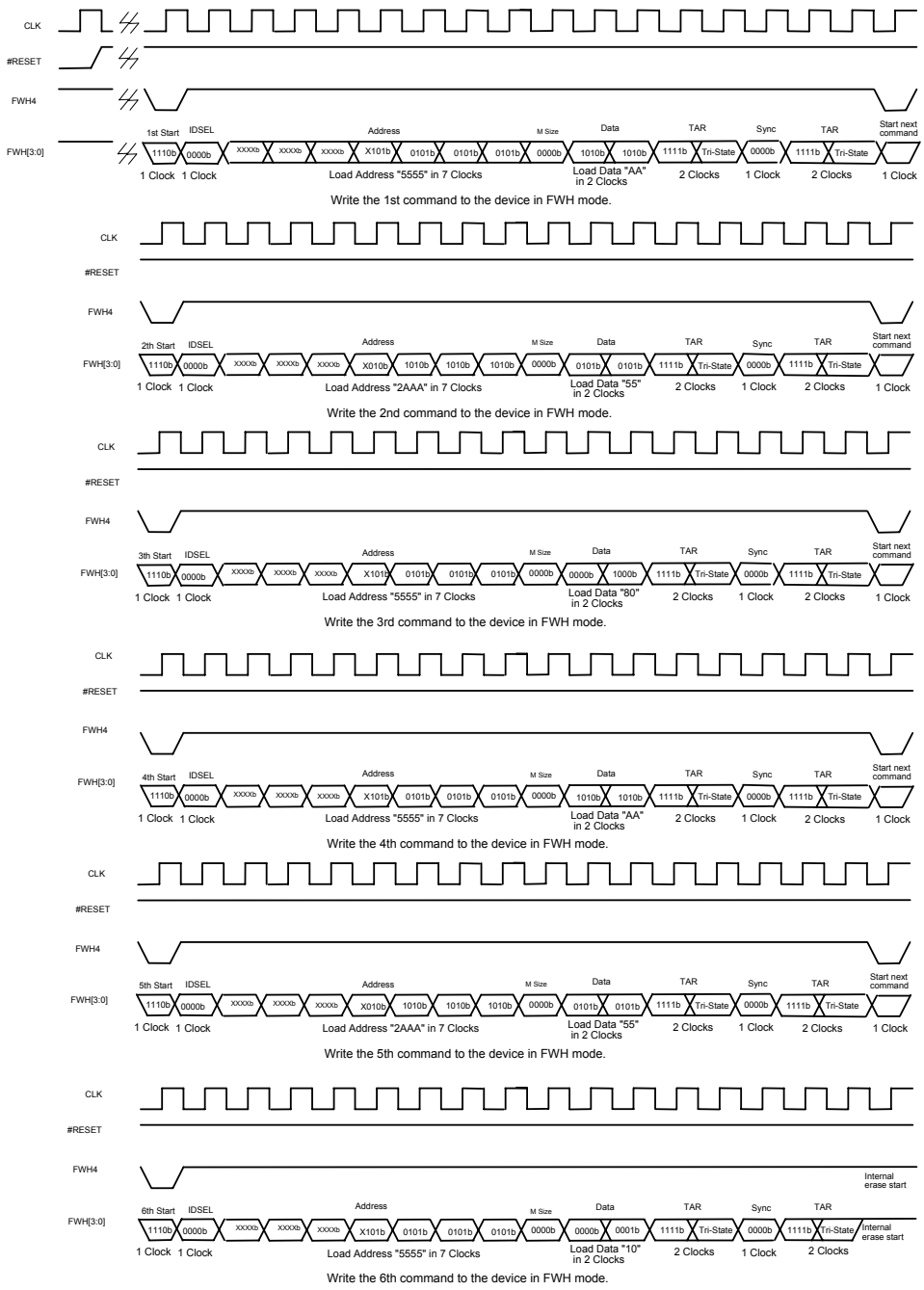
Timing Waveforms for FWH Interface Mode, continued

11.6 Boot Block Lockout Enable Timing Diagram



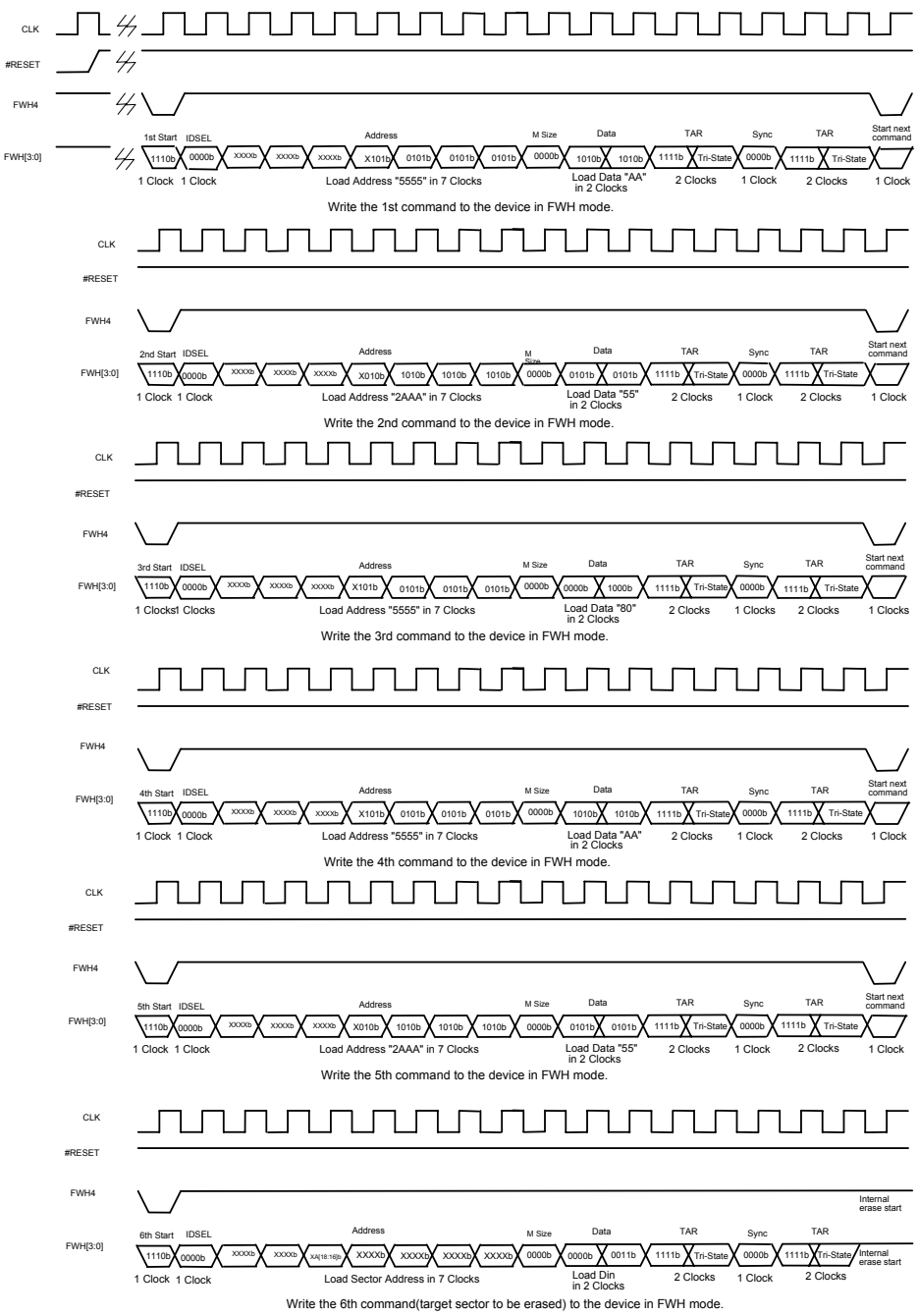
Timing Waveforms for FWH Interface Mode, continued

11.7 Chip Erase Timing Diagram



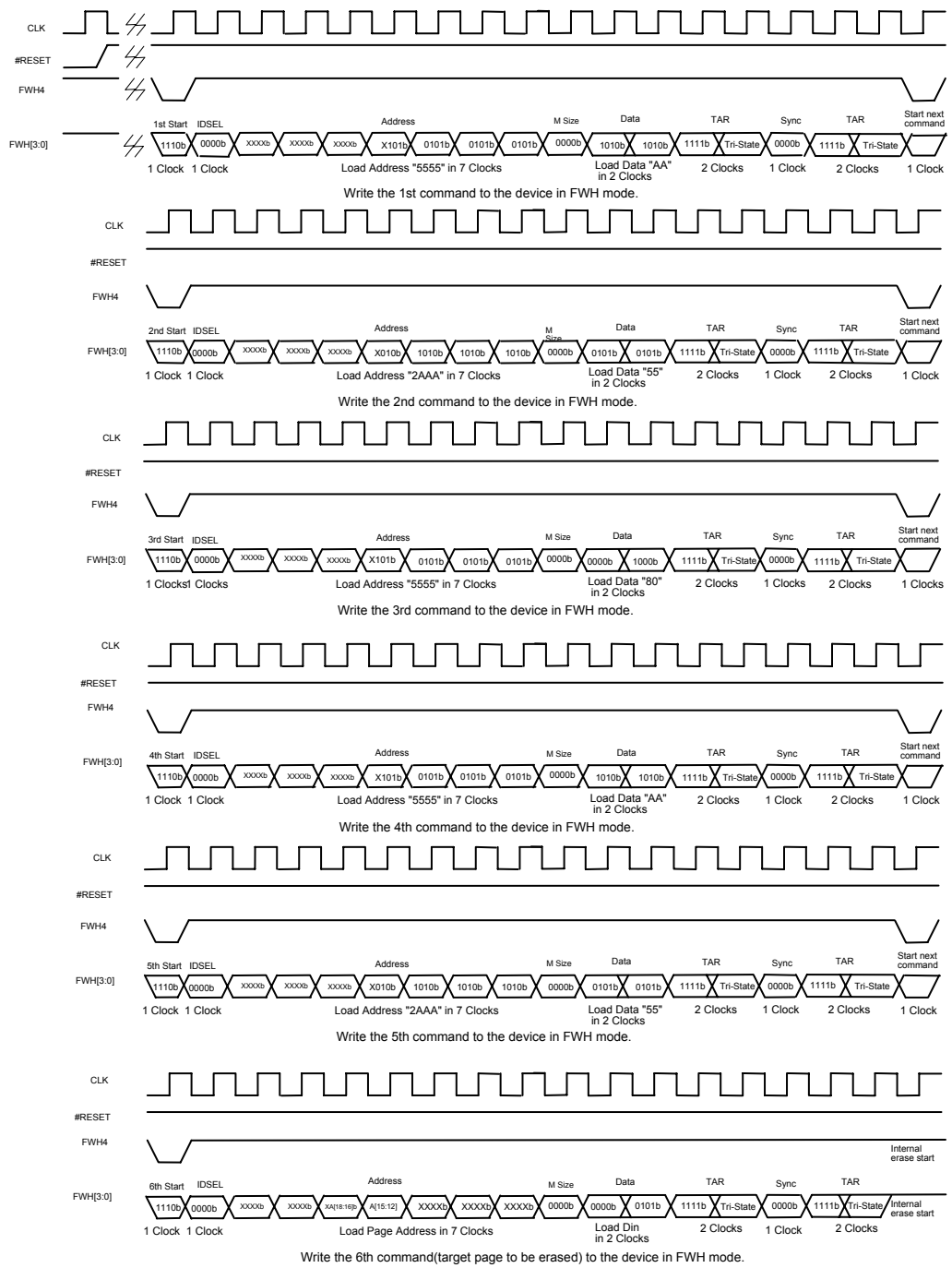
Timing Waveforms for FWH Interface Mode, continued

11.8 Sector Erase Timing Diagram



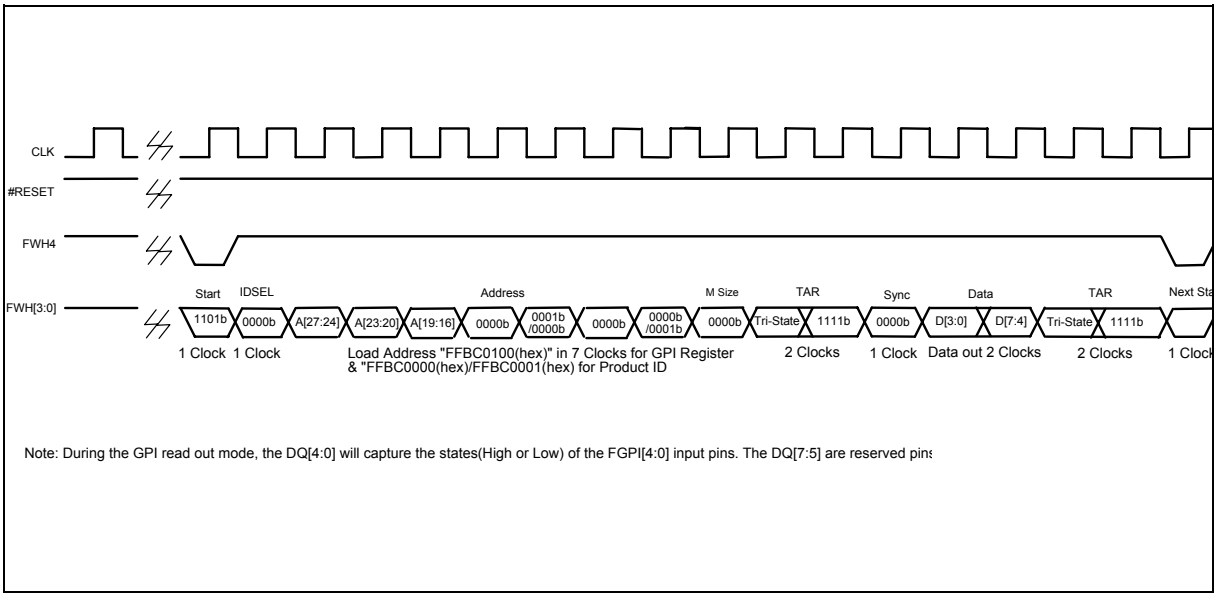
Timing Waveforms for FWH Interface Mode, continued

11.9 Page Erase Timing Diagram



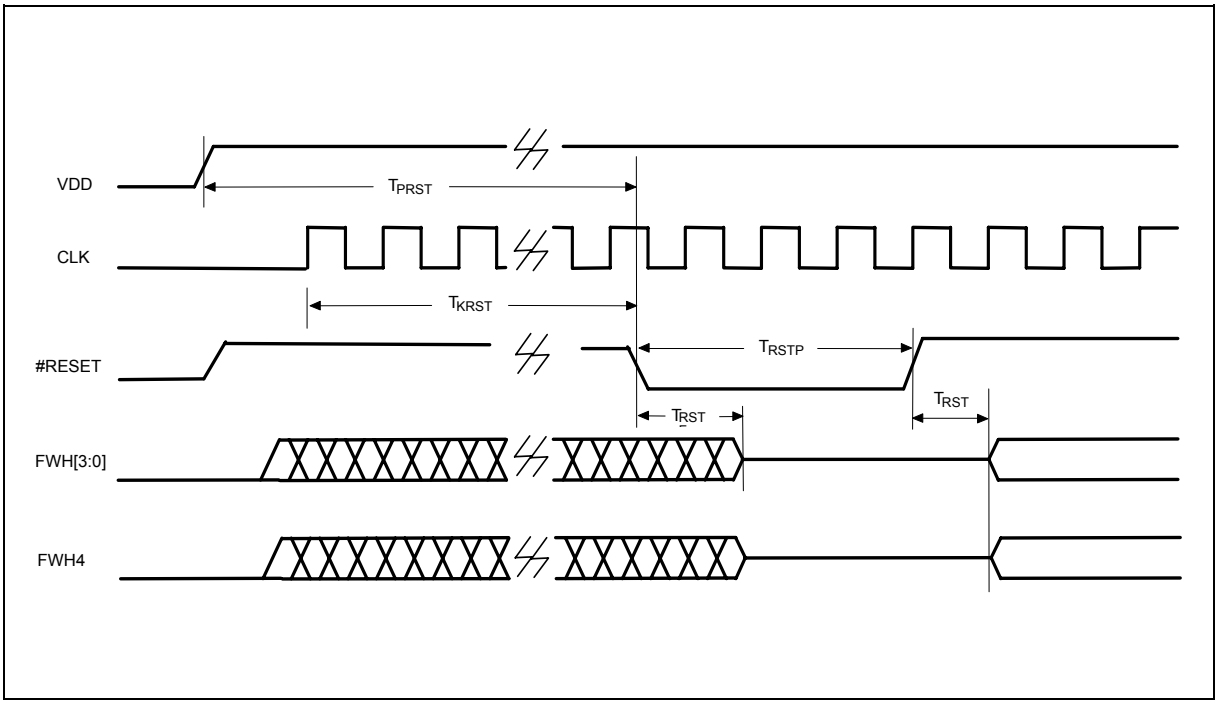
Timing Waveforms for FWH Interface Mode, continued

11.10 FGPI Register/Product ID Readout Timing Diagram



Note: During the GPI read out mode, the DQ[4:0] will capture the states(High or Low) of the FGPI[4:0] input pins. The DQ[7:5] are reserved pins

11.11 Reset Timing Diagram



12. 13. ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (mA)	PACKAGE
W39V040FAP	11	20	10	32L PLCC
W39V040FAQ	11	20	10	32L STSOP
W39V040FAT	11	20	10	40L TSOP
W39V040FAPZ	11	20	10	32L PLCC lead free
W39V040FAQZ	11	20	10	32L STSOP lead free
W39V040FATZ	11	20	10	40L TSOP lead free

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

13. HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin STSOP W39V040FAQ

1st line: Winbond logo

2nd line: the part number: W39V040FAQ

3rd line: the lot number

4th line: the tracking code: 149 O B SA

149: Packages made in '01, week 49

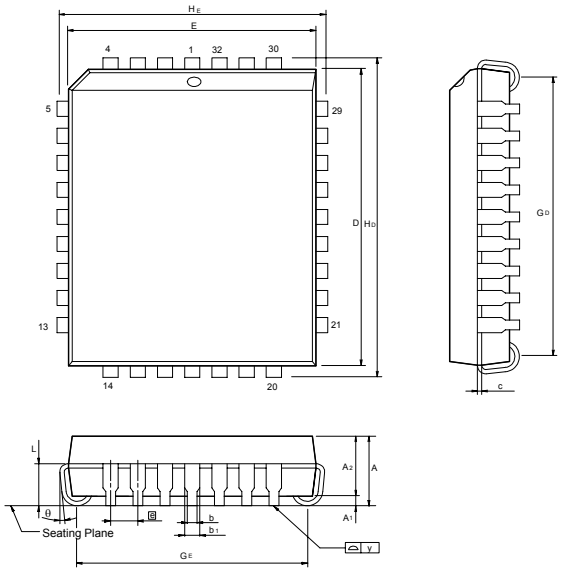
O: Assembly house ID: A means ASE, O means OSE, ...etc.

B: IC revision; A means version A, B means version B, ...etc.

SA: Process code

14. PACKAGE DIMENSIONS

14.1 32L PLCC

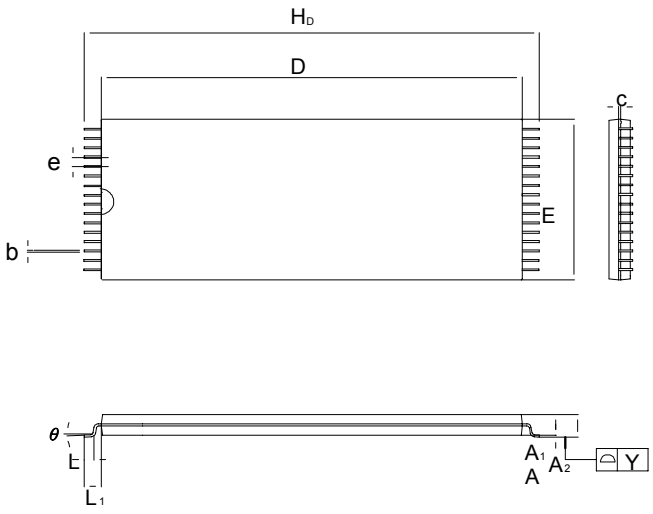


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusio
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

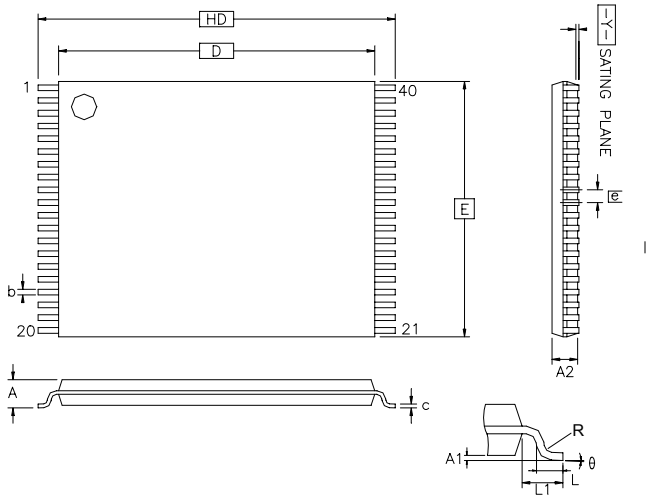
14.2 32L STSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0°	3°	5°	0°	3°	5°

Package Dimensions, continued

14.3 40L TSOP (10 mm x 20 mm)



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.007	0.009	0.011
c	0.10	—	0.20	0.004	—	0.008
D	18.30	18.40	18.50	0.720	0.724	0.728
E	9.90	10.00	10.10	0.390	0.394	0.398
HD	19.80	20.00	20.20	0.780	0.787	0.795
e	0.50 BASIC			0.020 BASIC		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
θ	0°	3°	5°	0°	3°	5°
Y	—	—	0.10	—	—	0.004
R	0.08	—	0.02	0.003	—	0.008

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 19, 2002	-	Initial Issued
A2	Dec. 16, 2002	23	Delete AC Test Load and Waveform.
			Add a note below Read/Write Cycle Timing Parameter
		15	Modify PGM mode power supply current (Icc) parameter from 20mA(typ.) to 10mA(typ.) and 30mA(max.) to 20mA(max.)
		1, 16, 33	Modify FWH mode power supply current (Icc) parameter from 40mA(typ.) to 12.5mA(typ.) and 60mA(max.) to 20mA(max.)
		16	Modify Standby current (Isb1) parameter from 20μA(typ.) to 5μA (typ.) and 100μA (max.) to 25μA (max.)
A3	Nov. 18, 2003	3	Modify the description of Interface Mode Selection: When IC pin is set to VDD, the device will be in the Programmer mode. (VDD is changed from High State)
A4	Aug. 20 , 2004	1 , 33	Add Lead free part
A5	Nov. 25, 2004	33	Add lead free word in package table

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