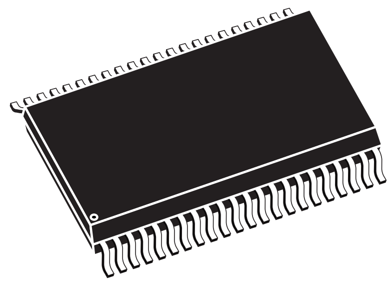
M29F800DT
M29F800DB

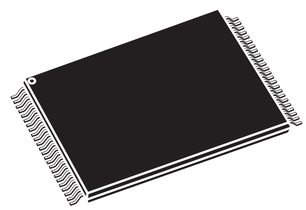
8 Mbit (1Mb x8 or 512Kb x16, Boot Block) 5V Supply Flash Memory

Feature summary

- Supply voltage
  - V_{CC} = 5V ±10% for Program, Erase and Read
- Access time: 55, 70, 90ns
- Programming time
  - 10µs per Byte/Word typical
- 19 Memory Blocks
  - 1 Boot Block (Top or Bottom location)
  - 2 Parameter and 16 Main Blocks
- Program/Erase controller
  - Embedded Byte/Word Program algorithms
- Erase Suspend and Resume modes
  - Read and Program another Block during Erase Suspend
- Unlock Bypass Program command
  - Faster Production/batch Programming
- Temporary Block Unprotection mode
- Common Flash Interface
  - 64 bit Security Code
- Low power consumption
  - Standby and Automatic Standby
- 100,000 Program/Erase cycles per Block
- Electronic Signature
  - Manufacturer Code: 0020h
  - Top Device Code M29F800DT: 22ECh
  - Bottom Device Code M29F800DB: 2258h



SO44 (M)



TSOP48 (N)
12 x 20mm

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1 Summary description

The M29F800D is a 8 Mbit (1Mb x8 or 512Kb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (5V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see *Figure 4: Block addresses (x8)*, and *Figure 5: Block addresses (x16)*. The first or last 64 Kbytes have been divided into four additional blocks. The 16 Kbyte Boot Block can be used for small initialization code to start the microprocessor, the two 8 Kbyte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in SO44 and TSOP48 (12 x 20mm) packages. The memory is supplied with all the bits erased (set to ’1’).

Figure 1. Logic diagram

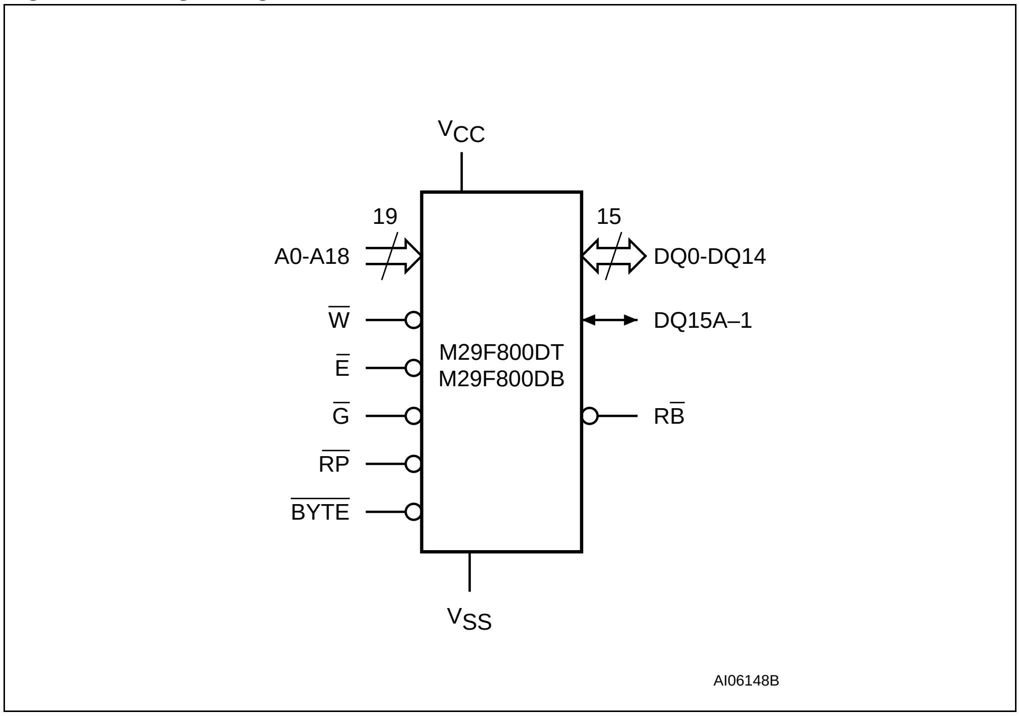


Table 1. Signal names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
R$\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 2. SO connections

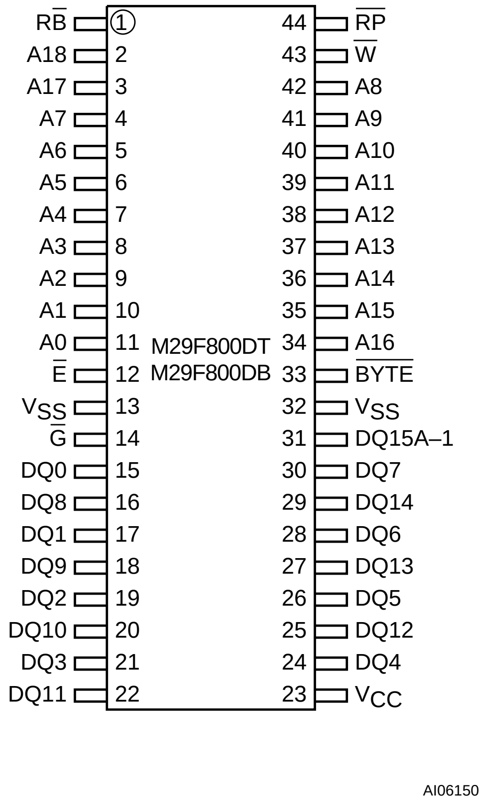


Figure 3. TSOP connections

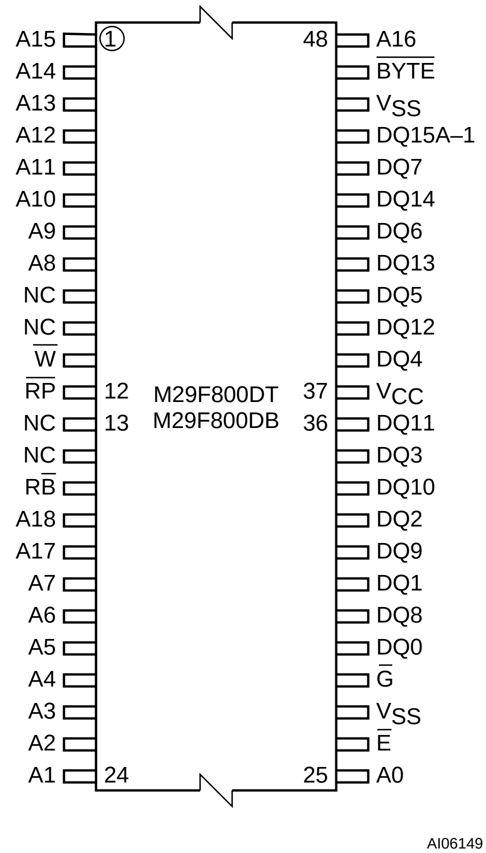
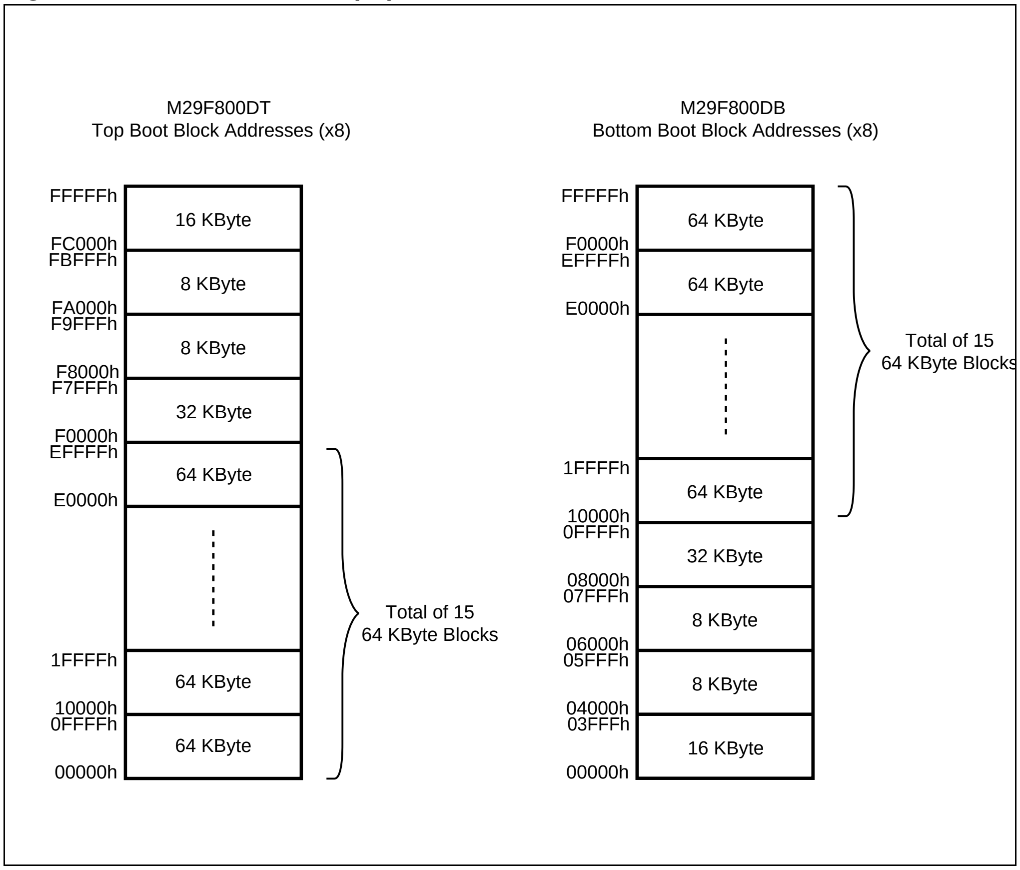
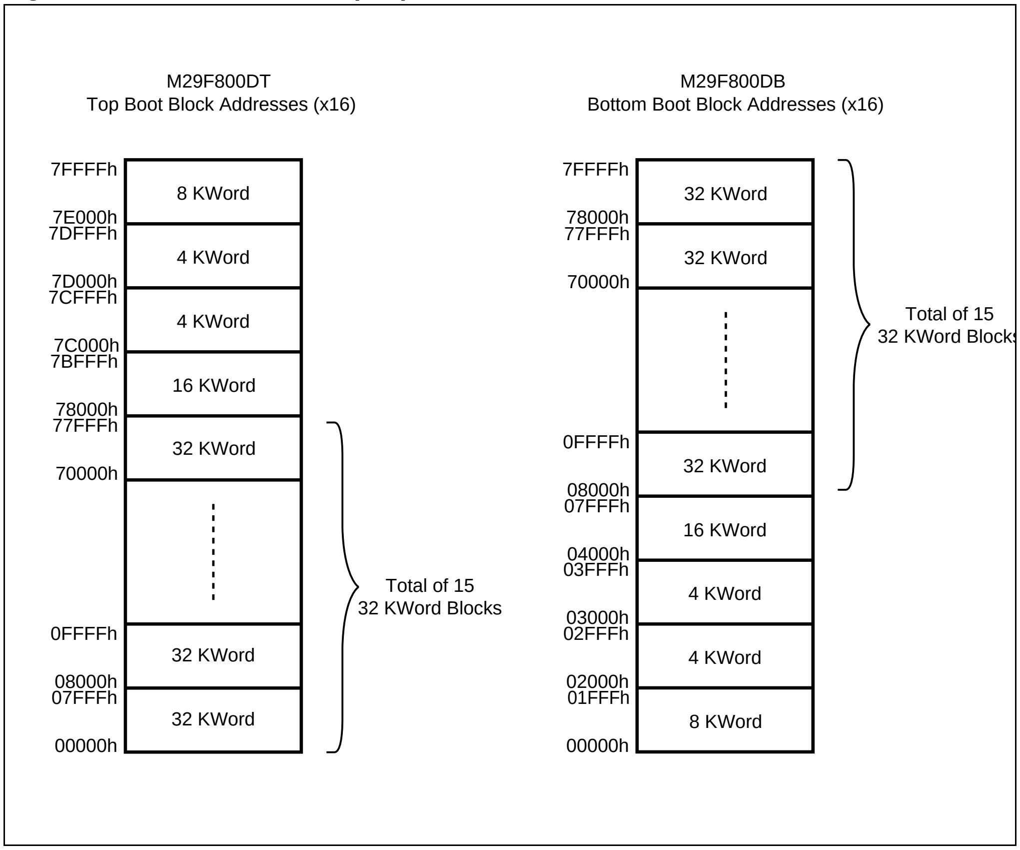


Figure 4. Block addresses (x8)



1. Also see *Appendix A*, *Table 19*, and *Table 20* for a full listing of the Block addresses.

Figure 5. Block addresses (x16)



1. Also see *Appendix A*, *Table 19*, and *Table 20* for a full listing of the Block addresses.

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.0.1 Address Inputs (A0-A18)

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

2.0.2 Data Inputs/Outputs (DQ0-DQ7)

The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

2.0.3 Data Inputs/Outputs (DQ8-DQ14)

The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

2.0.4 Data Input/Output or Address Input (DQ15A-1)

When $\overline{BYTE}$ is High, V_{IH}, this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When $\overline{BYTE}$ is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the Word on the other addresses, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when $\overline{BYTE}$ is High and references to the Address Inputs to include this pin when $\overline{BYTE}$ is Low except when stated explicitly otherwise.

2.0.5 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.0.6 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

2.0.7 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

2.0.8 Reset/Block Temporary Unprotect ($\overline{RP}$)

The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.0.9: Ready/Busy output (RB)*, *Table 15: Reset/Block Temporary Unprotect AC characteristics*, and *Figure 13: Reset/Block Temporary Unprotect AC waveforms* for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

2.0.9 Ready/Busy output (R$\overline{B}$)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 15: Reset/Block Temporary Unprotect AC characteristics*, and *Figure 13: Reset/Block Temporary Unprotect AC waveforms*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.0.10 Byte/Word Organization Select ($\overline{BYTE}$)

The Byte/Word Organization Select pin is used to switch between the 8-bit and 16-bit Bus modes of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in 8-bit mode, when it is High, V_{IH}, the memory is in 16-bit mode.

2.0.11 V_{CC} Supply Voltage

The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

2.0.12 V_{SS} Ground

The V_{SS} Ground is the reference for all voltage measurements.

3 Bus operations

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See *Table 2: Bus operations, BYTE = VIL*, and *Table 3: Bus operations, BYTE = VIH* for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.0.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see *Figure 10: Read Mode AC waveforms*, and *Table 12: Read AC characteristics* for details of when the output becomes valid.

3.0.2 Bus Write

Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 11: Write AC waveforms, Write Enable controlled*, *Figure 12: Write AC waveforms, Chip Enable controlled*, *Table 13: Write AC characteristics, Write Enable controlled*, and *Table 14: Write AC characteristics, Chip Enable controlled*, for details of the timing requirements.

3.0.3 Output Disable

The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.0.4 Standby

When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see *Table 11: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

3.0.5 Automatic Standby

If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

3.0.6 Special bus operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.0.7 Electronic Signature

The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in *Table 2: Bus operations, BYTE = VIL*, and *Table 3: Bus operations, BYTE = VIH*.

3.0.8 Block Protection and Blocks Unprotection

Each block can be separately protected against accidental Program or Erase. Protected blocks can be unprotected to allow data to be changed.

There are two methods available for protecting and unprotecting the blocks, one for use on programming equipment and the other for in-system use. Block Protect and Chip Unprotect operations are described in *Appendix C*.

Table 2. Bus operations, $\overline{BYTE}$ = V_{IL}(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs DQ15A–1, A0-A18	Data Inputs/Outputs	
					DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell address	Hi-Z	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command address	Hi-Z	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	20h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	ECh (M29F800DT) 58h (M29F800DB)

1. X = V_{IL} or V_{IH}.

Table 3. Bus operations, $\overline{BYTE}$ = V_{IH}(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A18	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	22ECh (M29F800DT) 2258h (M29F800DB)

1. X = V_{IL} or V_{IH}.

4 Command Interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode. See either *Table 4*, or *Table 5*, depending on the configuration that is being used, for a summary of the commands.

4.0.1 Read/Reset command

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset Command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. Once the program or erase operation has started the Read/Reset command is no longer accepted. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

4.0.2 Auto Select command

The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued. Read CFI Query and Read/Reset commands are accepted in Auto Select mode, all other commands are ignored.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Manufacturer Code for STMicroelectronics is 0020h.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A12-A18 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

4.0.3 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in *Table 6: Program, Erase times and Program, Erase Endurance cycles*. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See *Section 5: Status Register*, for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at ’0’ back to ’1’. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

4.0.4 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

4.0.5 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

4.0.6 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass Mode.

4.0.7 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 6*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See *Section 5: Status Register*, for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

4.0.8 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command. Typical block erase times are given in *Table 6*. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See *Section 5: Status Register*, for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

4.0.9 Erase Suspend command

The Erase Suspend command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within the Erase Suspend Latency Time (refer to *Table 6* for value) of the Erase Suspend command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

4.0.10 Erase Resume command

The Erase Resume command must be used to restart the Program/Erase Controller from Erase Suspend. An erase can be suspended and resumed more than once.

4.0.11 Read CFI Query command

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. This command is valid when the device is ready to read the array data or when the device is in autoselected mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. The Read/Reset command must be issued to return the device to Read Array mode. See *Appendix B*, *Table 21*, *Table 22*, *Table 23*, *Table 24*, *Table 25*, and *Appendix B: Common Flash Interface (CFI)*, for details on the information contained in the Common Flash Interface (CFI) memory area.

4.0.12 Block Protect and Chip Unprotect commands

Each block can be separately protected against accidental Program or Erase. The whole chip can be unprotected to allow the data inside the blocks to be changed.

Block Protect and Chip Unprotect operations are described in *Appendix C*.

Table 4. Commands, 16-bit mode, $\overline{BYTE} = V_{IH}$[(1)]

Command	Length	Bus Write operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	X	B0										
Erase Resume	1	X	30										
Read CFI Query	1	55	98										

1. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A18, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 5. Commands, 8-bit mode, $\overline{BYTE}$ = V_{IL} (1)

Command	Length	1st Addr	1st Data	2nd Addr	2nd Data	3rd Addr	3rd Data	4th Addr	4th Data	5th Addr	5th Data	6th Addr	6th Data
Read/Reset	1	X	F0										
	3	AAA	AA	555	55	X	F0						
Auto Select	3	AAA	AA	555	55	AAA	90						
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase	6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BA	30
Erase Suspend	1	X	B0										
Erase Resume	1	X	30										
Read CFI Query	1	AA	98										

1. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A18, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 6. Program, Erase times and Program, Erase Endurance cycles

Parameter	Min	Typ(1)(2)	Max(2)	Unit
Chip Erase		12	60(3)	s
Block Erase (64 Kbytes)		0.8	6(4)	s
Erase Suspend Latency time		30		µs
Program (Byte or Word)		10	200(3)	µs
Chip Program (Byte by Byte)		12	60(3)	s
Chip Program (Word by Word)		6	30(3)	s
Program/Erase cycles (per Block)	100,000			cycles
Data Retention	20			years

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,00 program/erase cycles.
4. Maximum value measured at worst case conditions for both temperature and V_{CC}.

5 Status Register

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 7: Status Register Bits*.

5.0.1 Data Polling Bit (DQ7)

The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a ’1’ during a Bus Read operation within a block being erased. The Data Polling Bit will change from a ’0’ to a ’1’ when the Program/Erase Controller has suspended the Erase operation.

Figure 6: Data Polling flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

5.0.2 Toggle Bit (DQ6)

The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 1µs.

Figure 7: Data Toggle flowchart, gives an example of how to use the Data Toggle Bit.

5.0.3 Error Bit (DQ5)

The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'

5.0.4 Erase Timer Bit (DQ3)

The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

5.0.5 Alternative Toggle Bit (DQ2)

The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 7. Status Register Bits[(1)]

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	$R\overline{B}$
Program	Any address	$\overline{DQ7}$	Toggle	0	–	–	0
Program during Erase Suspend	Any address	$\overline{DQ7}$	Toggle	0	–	–	0
Program Error	Any address	$\overline{DQ7}$	Toggle	1	–	–	0
Chip Erase	Any address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	1
	Non-Erasing Block	Data read as normal					1
Erase Error	Good Block address	0	Toggle	1	1	No Toggle	0
	Faulty Block address	0	Toggle	1	1	Toggle	0

1. Unspecified data bits should be ignored.

Figure 6. Data Polling flowchart

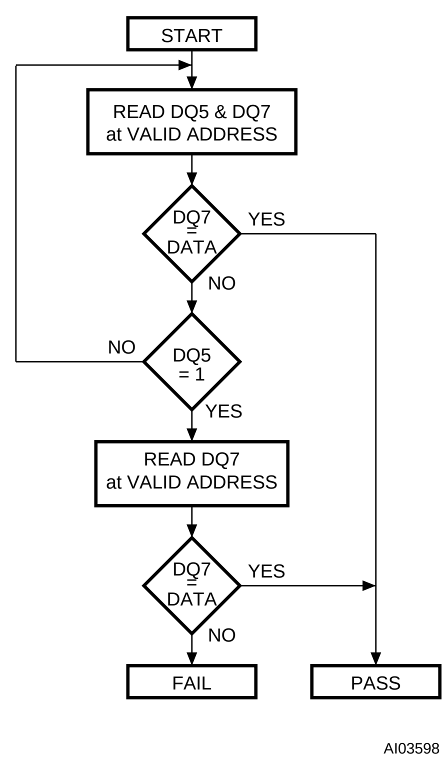
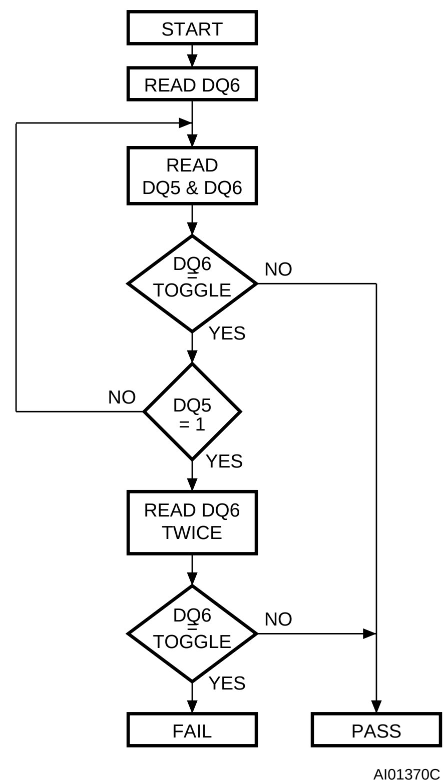


Figure 7. Data Toggle flowchart



6 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature under bias	–50	125	°C
T_{STG}	Storage temperature	–65	150	°C
V_{IO}	Input or Output voltage(1)(2)	–0.6	V_{CC} +0.6	V
V_{CC}	Supply voltage	–0.6	6	V
V_{ID}	Identification voltage	–0.6	13.5	V

1. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 9: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 9. Operating and AC measurement conditions

Parameter	M29F800D				Unit
	55		70/ 90		
	Min	Max	Min	Max	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
Ambient Operating Temperature (range 1)	0	70	0	70	°C
Ambient Operating Temperature (range 6)	–40	85	–40	85	°C
Load capacitance (C_L)	30		100		pF
Input Rise and Fall times		10		10	ns
Input Pulse voltages	0 to 3		0.45 to 2.4		V
Input and Output Timing Ref. voltages	1.5		0.8 and 2.0		V

Figure 8. AC measurement I/O waveform

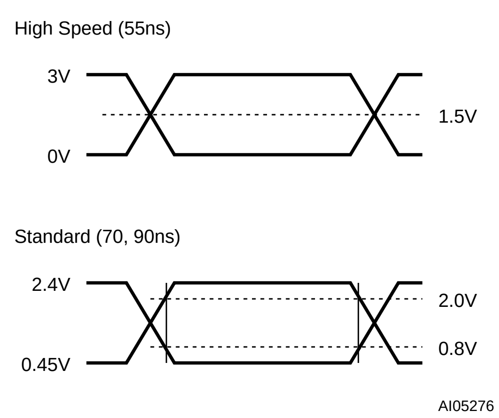


Figure 9. AC measurement Load Circuit

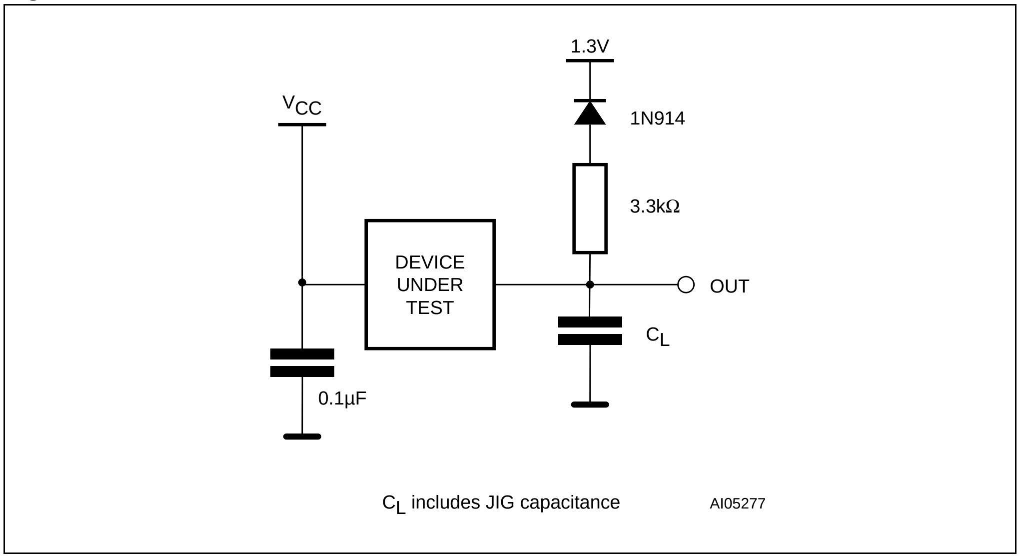


Table 10. Device capacitance[(1)]

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V		12	pF

1. Sampled only, not 100% tested.

Table 11. DC characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		20	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		2	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		150	µA
I_{CC4}(1)	Supply Current (Program/Erase)	Program/Erase Controller active		20	mA
V_{IL}	Input Low voltage		–0.5	0.8	V
V_{IH}	Input High voltage		2	$V_{CC} + 0.5$	V
V_{OL}	Output Low voltage	$I_{OL} = 5.8mA$		0.45	V
V_{OH}	Output High voltage TTL CMOS	$I_{OH} = –2.5mA$	2.4		V
V_{ID}	Identification voltage		11.5	12.5	V
I_{ID}	Identification Current	$A9 = V_{ID}$		100	µA
V_{LKO}	Program/Erase Lockout Supply voltage		3.2	4.2	V

1. Sampled only, not 100% tested.

Figure 10. Read Mode AC waveforms

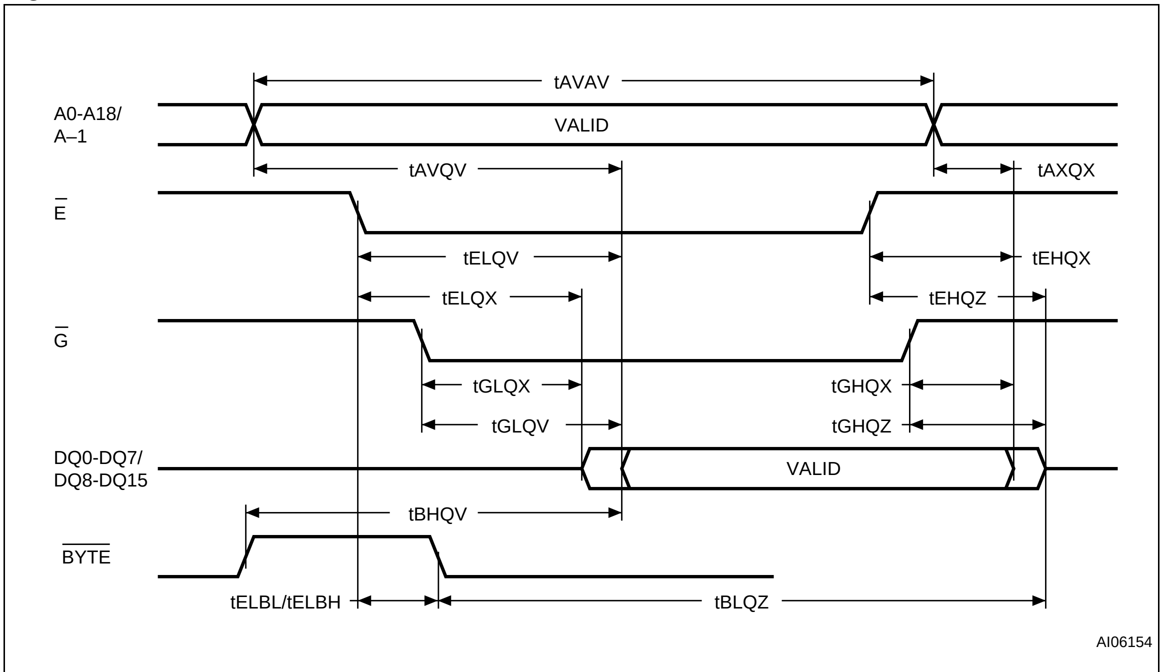


Table 12. Read AC characteristics

Symbol	Alt	Parameter	Test condition		M29F800D		Unit
					55	70/ 90	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	55	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	55	70	ns
t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	55	70	ns
t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	30	30	ns
t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	18	20	ns
t_{GHQZ}(1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	18	20	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	30	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	40	ns

1. Sampled only, not 100% tested.

Figure 11. Write AC waveforms, Write Enable controlled

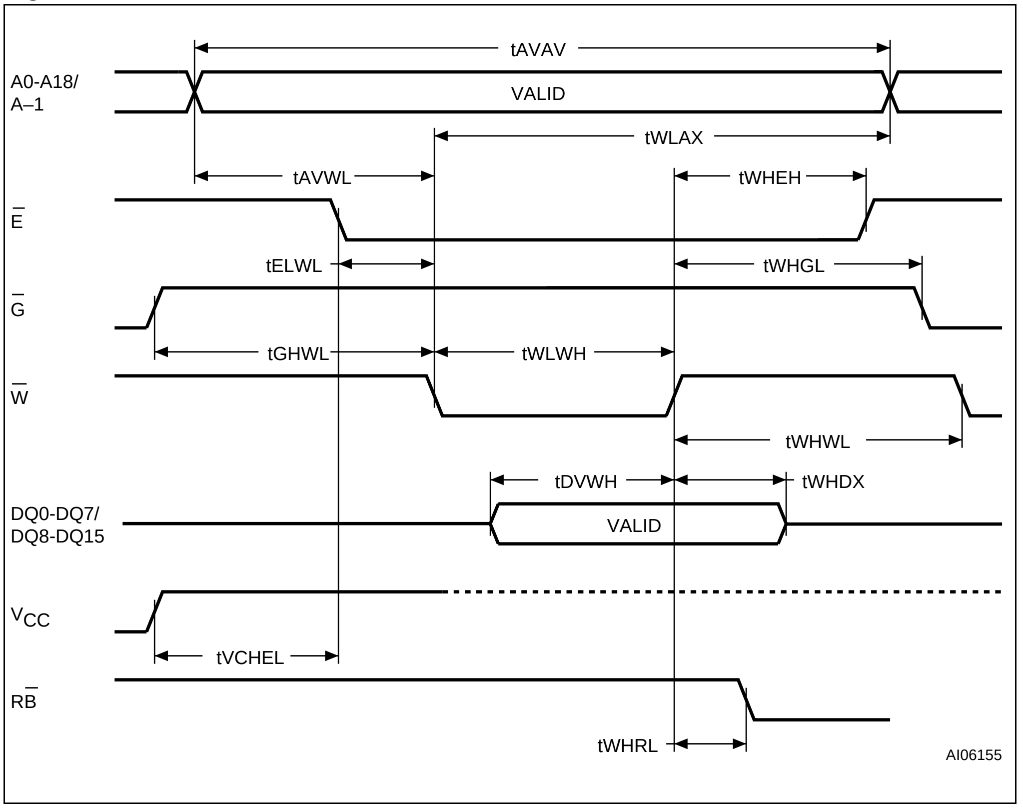


Table 13. Write AC characteristics, Write Enable controlled

Symbol	Alt	Parameter		M29F800D 55	M29F800D 70/ 90	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20	20	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to R$\overline{B}$ Low	Max	30	30	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 12. Write AC waveforms, Chip Enable controlled

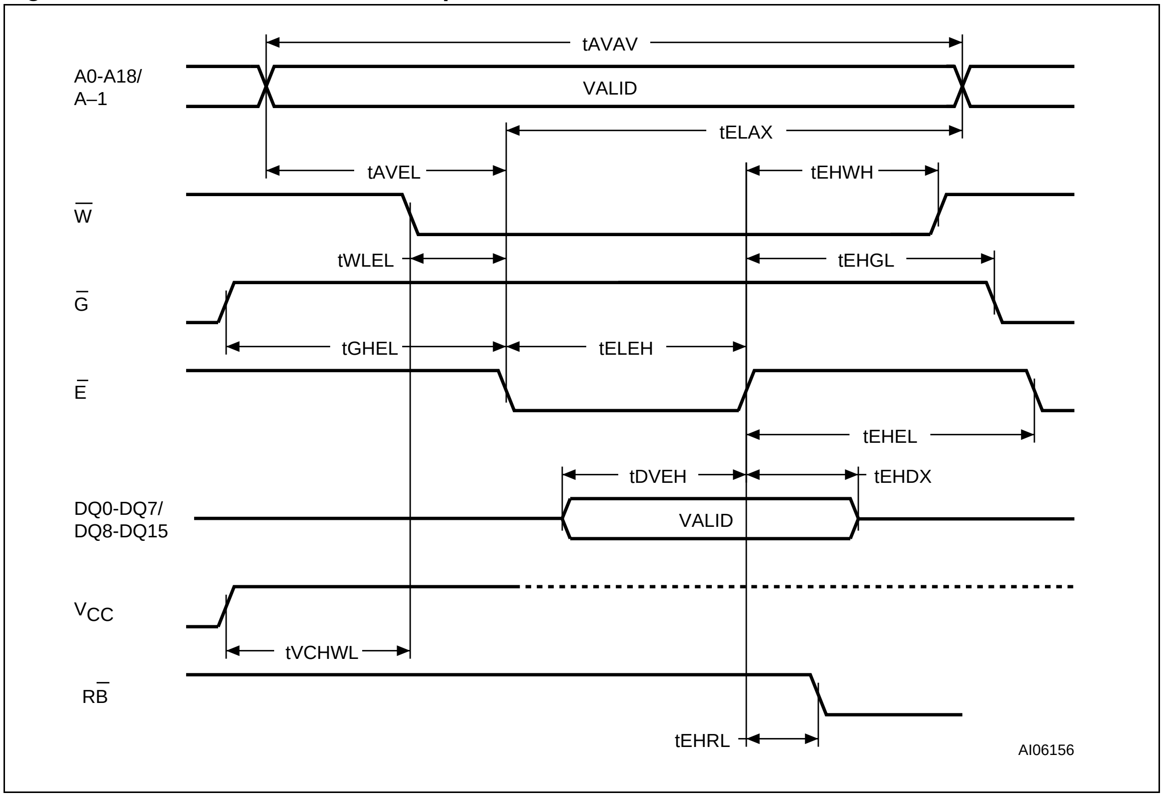


Table 14. Write AC characteristics, Chip Enable controlled

Symbol	Alt	Parameter		M29F800D 55	M29F800D 70/ 90	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	20	20	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $R\overline{B}$ Low	Max	30	30	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 13. Reset/Block Temporary Unprotect AC waveforms

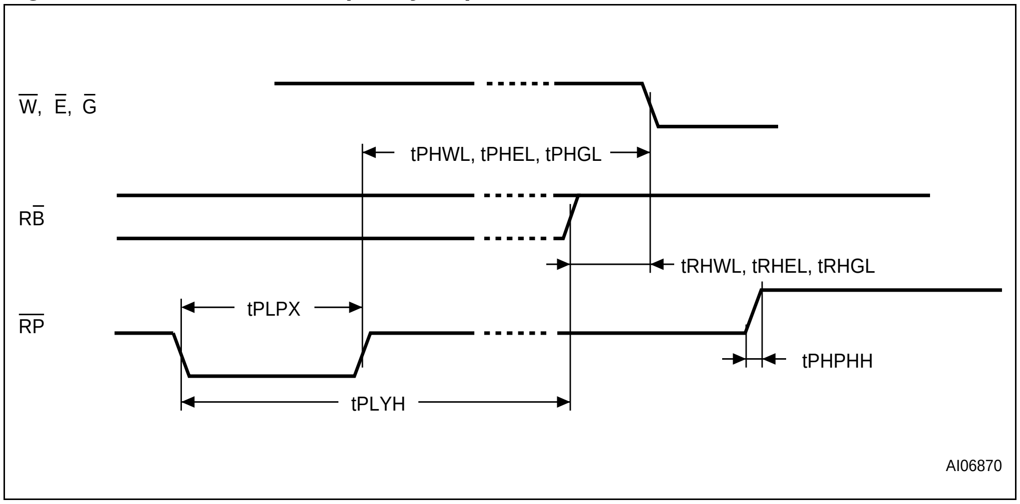


Table 15. Reset/Block Temporary Unprotect AC characteristics

Symbol	Alt	Parameter		M29F800D		Unit
				55	70/ 90	
t_{PHWL}(1) t_{PHEL} t_{PHGL}(1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL}(1) t_{RHEL}(1) t_{RHGL}(1)	t_{RB}	R$\overline{B}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	Min	500	500	ns
t_{PLYH}(1)	t_{READY}	$\overline{RP}$ Low to Read Mode	Max	10	10	µs
t_{PHPHH}(1)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	Min	500	500	ns

1. Sampled only, not 100% tested.

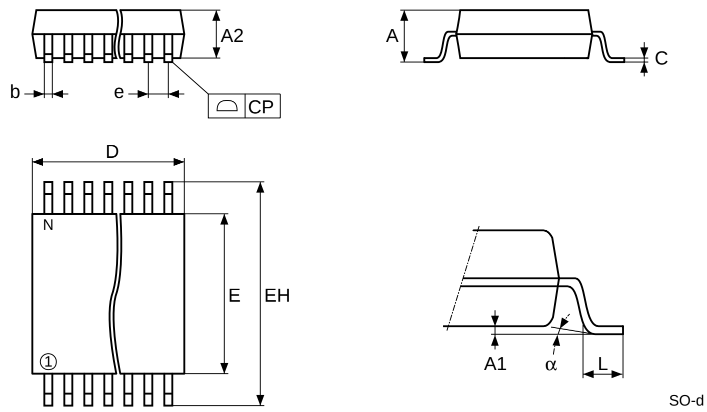
8 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. SO44 - 44 lead Plastic Small Outline, 525 mils body width, package outline

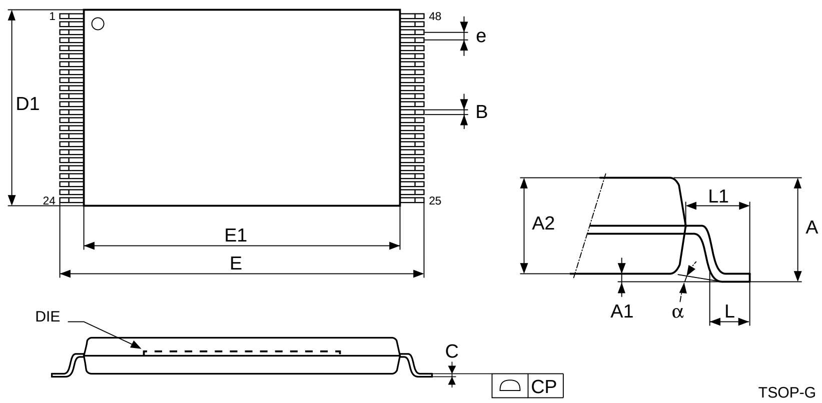


1. Drawing is not to scale.

Table 16. SO44 – 44 lead Plastic Small Outline, 525 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.80			0.1102
A1		0.10			0.0039	
A2	2.30	2.20	2.40	0.0906	0.0866	0.0945
b	0.40	0.35	0.50	0.0157	0.0138	0.0197
C	0.15	0.10	0.20	0.0059	0.0039	0.0079
CP			0.08			0.0030
D	28.20	28.00	28.40	1.1102	1.1024	1.1181
E	13.30	13.20	13.50	0.5236	0.5197	0.5315
EH	16.00	15.75	16.25	0.6299	0.6201	0.6398
e	1.27	–	–	0.0500	–	–
L	0.80			0.0315		
α			8°			8°
N	44			44		

Figure 15. TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package outline



1. Drawing is not to scale.

Table 17. TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
α	3°	0	5°	3°	0	5°

9 Part numbering

Table 18. Ordering information scheme

Example:	M29	F	800DB	55	N	6	T

Device Type

M29

Operating Voltage

F = V_{CC} = 5V ± 10%

Device Function

800D = 8 Mbit (x8/x16), Boot Block

Array Matrix

T = Top Boot

B = Bottom Boot

Speed

55 = 55 ns

70 = 70 ns

90 = 90 ns

Package

M = SO44

N = TSOP48: 12 x 20 mm

Temperature Range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

E = ECOPACK® package, standard package

F = ECOPACK® package, tape & reel 24mm packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Appendix A Block address table

Table 19. Top Boot Block addresses, M29F800D

#	Size (Kbytes)	Address range (x8)	Address range (x16)
18	16	FC000h-FFFFFh	7E000h-7FFFFh
17	8	FA000h-FBFFFh	7D000h-7DFFFh
16	8	F8000h-F9FFFh	7C000h-7CFFFh
15	32	F0000h-F7FFFh	78000h-7BFFFh
14	64	E0000h-EFFFFh	70000h-77FFFh
13	64	D0000h-DFFFFh	68000h-6FFFFh
12	64	C0000h-CFFFFh	60000h-67FFFh
11	64	B0000h-BFFFFh	58000h-5FFFFh
10	64	A0000h-AFFFFh	50000h-57FFFh
9	64	90000h-9FFFFh	48000h-4FFFFh
8	64	80000h-8FFFFh	40000h-47FFFh
7	64	70000h-7FFFFh	38000h-3FFFFh
6	64	60000h-6FFFFh	30000h-37FFFh
5	64	50000h-5FFFFh	28000h-2FFFFh
4	64	40000h-4FFFFh	20000h-27FFFh
3	64	30000h-3FFFFh	18000h-1FFFFh
2	64	20000h-2FFFFh	10000h-17FFFh
1	64	10000h-1FFFFh	08000h-0FFFFh
0	64	00000h-0FFFFh	00000h-07FFFh

Table 20. Bottom Boot Block addresses, M29F800DB

#	Size (Kbytes)	Address range (x8)	Address range (x16)
18	64	F0000h-FFFFFh	78000h-7FFFFh
17	64	E0000h-EFFFFh	70000h-77FFFh
16	64	D0000h-DFFFFh	68000h-6FFFFh
15	64	C0000h-CFFFFh	60000h-67FFFh
14	64	B0000h-BFFFFh	58000h-5FFFFh
13	64	A0000h-AFFFFh	50000h-57FFFh
12	64	90000h-9FFFFh	48000h-4FFFFh
11	64	80000h-8FFFFh	40000h-47FFFh
10	64	70000h-7FFFFh	38000h-3FFFFh
9	64	60000h-6FFFFh	30000h-37FFFh
8	64	50000h-5FFFFh	28000h-2FFFFh
7	64	40000h-4FFFFh	20000h-27FFFh
6	64	30000h-3FFFFh	18000h-1FFFFh
5	64	20000h-2FFFFh	10000h-17FFFh
4	64	10000h-1FFFFh	08000h-0FFFFh
3	32	08000h-0FFFFh	04000h-07FFFh
2	8	06000h-07FFFh	03000h-03FFFh
1	8	04000h-05FFFh	02000h-02FFFh
0	16	00000h-03FFFh	00000h-01FFFh

Appendix B Common Flash Interface (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. *Table 21*, *Table 22*, *Table 23*, *Table 24*, *Table 25*, and *Table 26* show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see *Table 26: Security Code Area*). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 21. Query structure overview(1)

Address		Sub-section name	Description
x16	x8		
10h	20h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	36h	System Interface Information	Device timing & voltage information
27h	4Eh	Device Geometry Definition	Flash device layout
40h	80h	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
61h	C2h	Security Code Area	64 bit unique device number

1. Query data are always presented on the lowest order data outputs.

Table 22. CFI Query Identification String[(1)]

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	22h	0052h		"R"
12h	24h	0059h		"Y"
13h	26h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for Primary Algorithm extended Query table (see *Table 24*)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for Alternate Algorithm extended Query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 23. CFI Query System Interface Information

Address		Data	Description	Value
x16	x8			
1Bh	36h	0045h	V_{CC} Logic Supply Minimum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	4.5V
1Ch	38h	0055h	V_{CC} Logic Supply Maximum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	5.5V
1Dh	3Ah	0000h	V_{PP} [Programming] Supply Minimum Program/Erase voltage	NA
1Eh	3Ch	0000h	V_{PP} [Programming] Supply Maximum Program/Erase voltage	NA
1Fh	3Eh	0004h	Typical timeout per single byte/word program = 2^n µs	16µs
20h	40h	0000h	Typical timeout for minimum size write buffer program = 2^n µs	NA
21h	42h	000Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	44h	0000h	Typical timeout for full chip erase = 2^n ms	see note[(1)]
23h	46h	0004h	Maximum timeout for byte/word program = 2^n times typical	256µs
24h	48h	0000h	Maximum timeout for write buffer program = 2^n times typical	NA
25h	4Ah	0003h	Maximum timeout per individual block erase = 2^n times typical	8s
26h	4Ch	0000h	Maximum timeout for chip erase = 2^n times typical	see note[(1)]

1. Not supported in the CFI

Table 24. Device Geometry Definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0014h	Device Size = 2^n in number of bytes	1 MByte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface Code description	x8, x16 Async.
2Ah 2Bh	54h 56h	0000h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	NA
2Ch	58h	0004h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	4
2Dh 2Eh	5Ah 5Ch	0000h 0000h	Region 1 Information Number of identical size erase block = 0000h+1	1
2Fh 30h	5Eh 60h	0040h 0000h	Region 1 Information Block size in Region 1 = 0040h * 256 byte	16 Kbyte
31h 32h	62h 64h	0001h 0000h	Region 2 Information Number of identical size erase block = 0001h+1	2
33h 34h	66h 68h	0020h 0000h	Region 2 Information Block size in Region 2 = 0020h * 256 byte	8 Kbyte
35h 36h	6Ah 6Ch	0000h 0000h	Region 3 Information Number of identical size erase block = 0000h+1	1
37h 38h	6Eh 70h	0080h 0000h	Region 3 Information Block size in Region 3 = 0080h * 256 byte	32 Kbyte
39h 3Ah	72h 74h	000Eh 0000h	Region 4 Information Number of identical-size erase block = 000Eh+1	15
3Bh 3Ch	76h 78h	0000h 0001h	Region 4 Information Block size in Region 4 = 0100h * 256 byte	64 Kbyte

Table 25. Primary Algorithm-specific Extended Query table

Address		Data	Description	Value
x16	x8			
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Primary Algorithm Extended Query table unique ASCII string “PRI”	"P" "R" "I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0030h	Minor version number, ASCII	"0"
45h	8Ah	0000h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	8Eh	0001h	Block Protection 00 = not supported, x = number of sectors in per group	1
48h	90h	0001h	Temporary Block Unprotect 00 = not supported, 01 = supported	Yes
49h	92h	0004h	Block Protect /Unprotect 04 = M29W400B	4
4Ah	94h	0000h	Simultaneous Operations, 00 = not supported	No
4Bh	96h	0000h	Burst Mode, 00 = not supported, 01 = supported	No
4Ch	98h	0000h	Page Mode, 00 = not supported, 01 = 4 page word, 02 = 8 page word	No

Table 26. Security Code Area

Address		Data	Description
x16	x8		
61h	C3h, C2h	XXXX	64 bit: unique device number
62h	C5h, C4h	XXXX	
63h	C7h, C6h	XXXX	
64h	C9h, C8h	XXXX	

Appendix C Block protection

Block protection can be used to prevent any operation from modifying the data stored in the Flash. Each Block can be protected individually. Once protected, Program and Erase operations on the block fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

Unlike the Command Interface of the Program/Erase Controller, the techniques for protecting and unprotecting blocks change between different Flash memory suppliers. For example, the techniques for AMD parts will not work on STMicroelectronics parts. Care should be taken when changing drivers for one part to work on another.

9.1 Programmer technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a block follow the flowchart in *Figure 16: Programmer Equipment Block Protect flowchart*. To unprotect the whole chip it is necessary to protect all of the blocks first, then all blocks can be unprotected at the same time. To unprotect the chip follow *Figure 17: Programmer Equipment Chip Unprotect flowchart*. *Table 27: Programmer technique bus operations, BYTE = VIH or VIL*, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

9.2 In-System technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the Flash has been fitted to the system.

To protect a block follow the flowchart in *Figure 18: In-System Equipment Block Protect flowchart*. To unprotect the whole chip it is necessary to protect all of the blocks first, then all the blocks can be unprotected at the same time. To unprotect the chip follow *Figure 19: In-System Equipment Chip Unprotect flowchart*.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 27. Programmer technique bus operations, $\overline{BYTE}$ = V_{IH} or V_{IL}

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A18	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Block Protect	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-A18 Block address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others = X	X
Block Protection verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A12-A18 Block address Others = X	Pass = XX01h Retry = XX00h
Block Unprotection verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A12-A18 Block address Others = X	Retry = XX01h Pass = XX00h

Figure 16. Programmer Equipment Block Protect flowchart

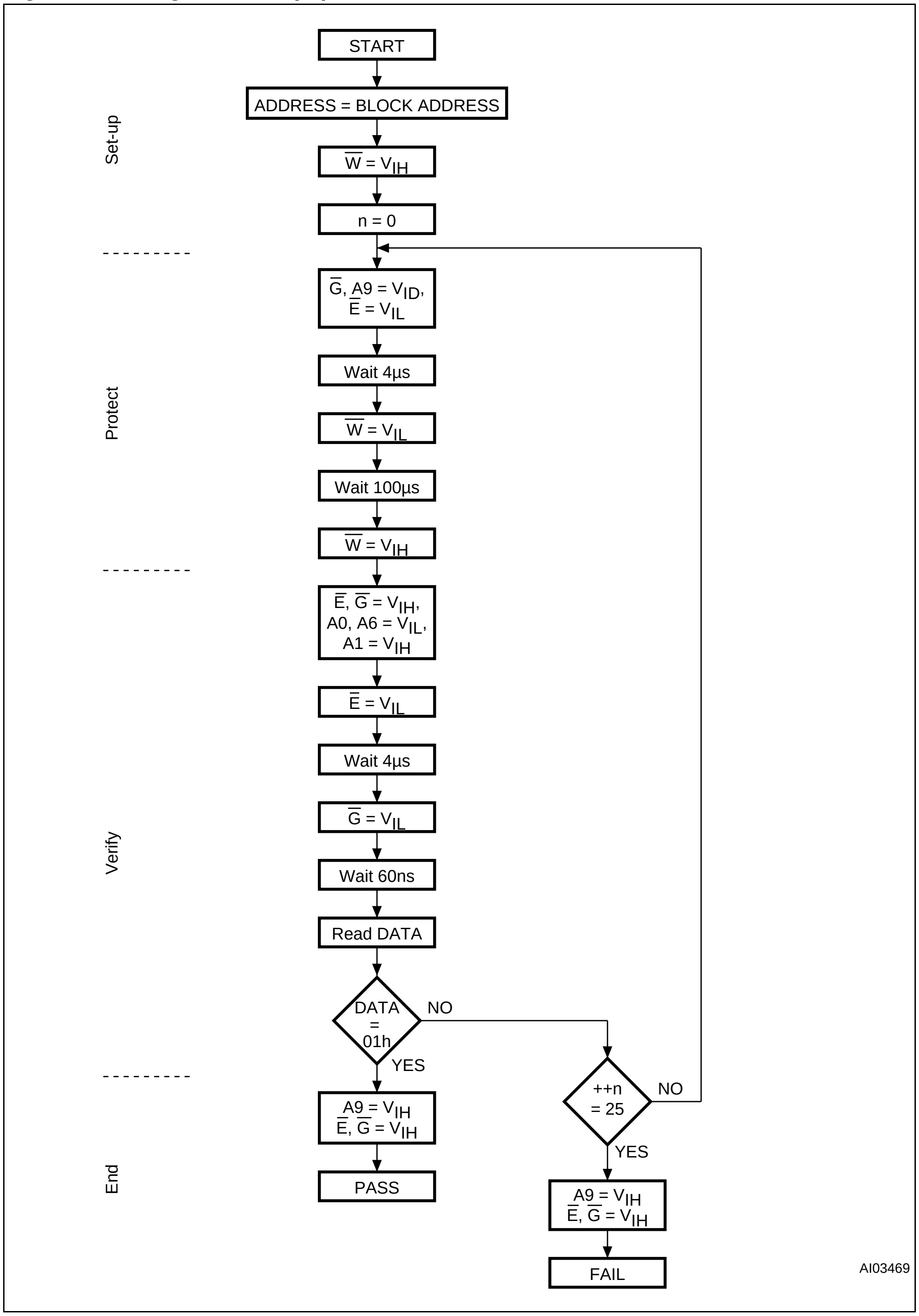


Figure 17. Programmer Equipment Chip Unprotect flowchart

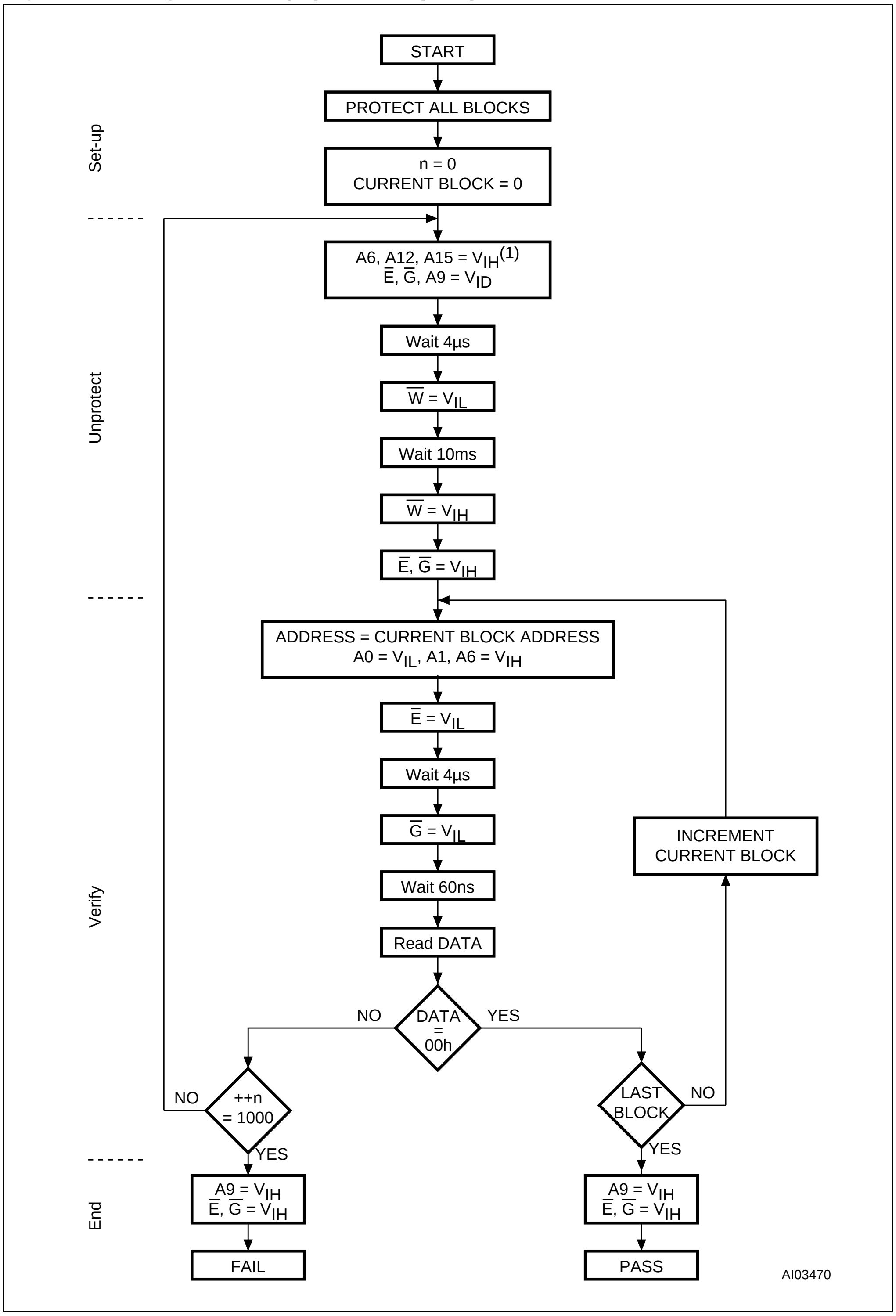


Figure 18. In-System Equipment Block Protect flowchart

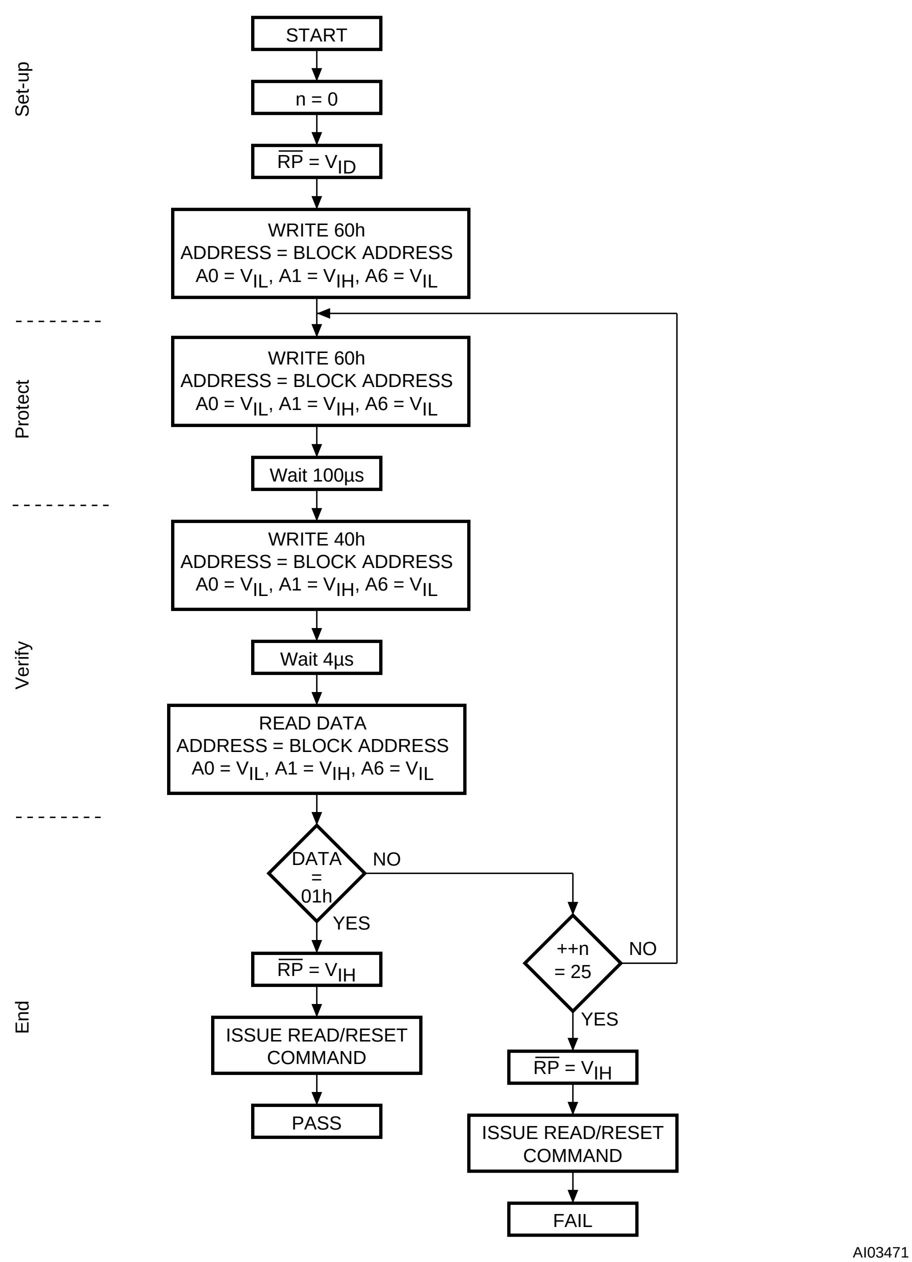
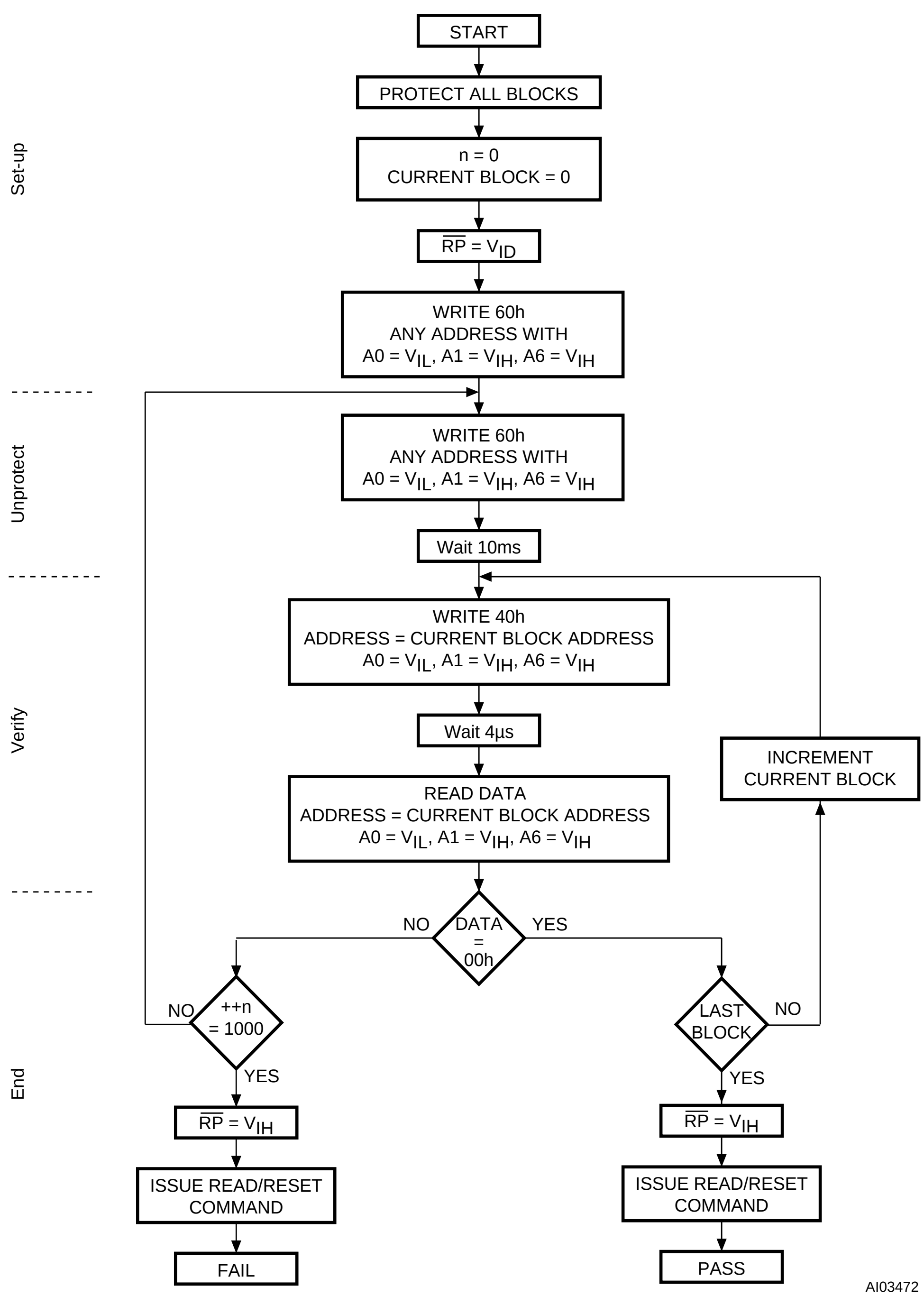


Figure 19. In-System Equipment Chip Unprotect flowchart



Revision history

Table 28. Document revision history

Date	Revision	Revision details
13-Dec-2001	-01	First Issue
21-Jan-2002	-02	V_{IH}(max) value corrected
01-Mar-2002	-03	Description of Ready/Busy signal clarified (and *Figure 13: Reset/Block Temporary Unprotect AC waveforms* modified) Clarified allowable commands during block erase Clarified the mode the device returns to in the CFI Read Query command section
17-Feb-2003	4.0	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 03 equals 3.0). Erase Suspend Latency Time (typical) and Data Retention parameters added to *Table 6: Program, Erase times and Program, Erase Endurance cycles*, and notes added to the table. *Figure 1: Logic diagram*, and *Figure 7: Data Toggle flowchart* corrected. Lead-free package options E and F added to *Table 18: Ordering information scheme*. Document promoted to full datasheet.
08-Jul-2003	4.1	TSOP48 package information updated (see *Figure 15: TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package outline* and *Table 17: TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package mechanical data*). Cross-references updated in *Appendix B: Common Flash Interface (CFI) on page 42*. Temperature range 3 added.
24-Aug-2006	5	Changed document to new template; indicated that Ready/Busy Output now available for both SO44 and TSOP48 packages (see *Table 1.: Signal names*); removed temperature range 3 from *Table 9* and *Table 18*; ecopack compliant

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