FAIRCHILD SEMICONDUCTOR®

November 2007

FDMF8704V

High Efficiency / High Frequency FET plus Driver Multi-chip Module with Internal Voltage Regulator

Benefits

- Fully optimized system efficiency. Higher efficiency levels are achievable compared with conventional discrete components.
- Space savings of up to 50% PCB versus discrete solutions.
- Higher frequency of operation.
- Simpler system design and board layout. Reduced time in component selection and optimization.

Features

- 7V to 20V Input Voltage Range
- Output current to 32A
- 1MHz switching frequency capable
- Internal adaptive gate drive
- Low Side FET with Integrated Schottky Diode
- Peak Efficiency >90%
- Output disable for lost phase shutdown
- Integrated 5V regulator
- Low profile SMD package
- RoHS Compliant

General Description

The FDMF8704V is a fully optimized integrated Driver plus MOSFET power stage solution for high current synchronous buck DC-DC applications. The device integrates a driver IC and two Power MOSFETs into a space saving, MLP 8x8, 56-pin package. Fairchild Semiconductor's integrated approach optimizes the complete switching power stage with regards to driver to FET dynamic performance, system inductance and overall solution ON resistance. Package parasitics and problematical layouts associated with conventional discrete solutions are greatly reduced. This integrated approach results in significant board space saving, therefore maximizing footprint power density. This solution is based on the Intel™ DrMOS specification.

Applications

- Desktop and server VR11.x V-core and non V-core buck converters.
- CPU/GPU power train in game consoles and high end desktop systems.
- High-current DC-DC Point of Load (POL) converters.
- Networking and telecom microprocessor voltage regulators.
- Small form factor voltage regulator modules.

Powertrain Application Circuit

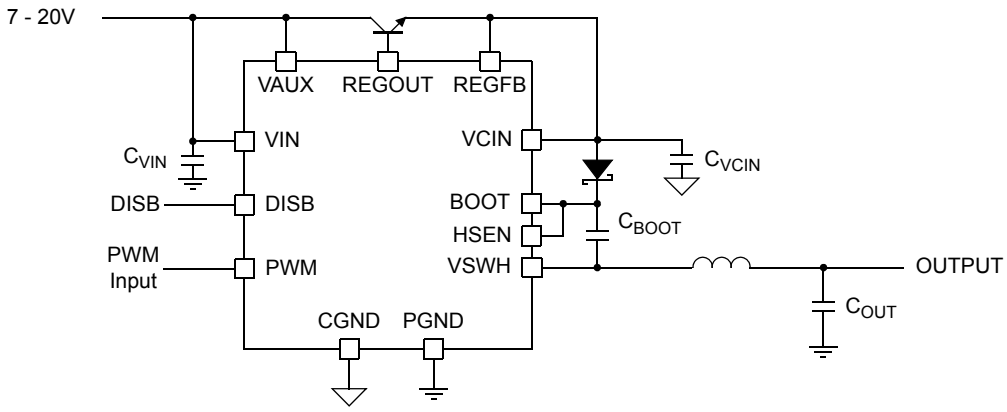


Figure 1. Powertrain Application Circuit

Ordering Information

Part	Current Rating Max [A]	Input Voltage Typical [V]	Frequency Max [KHz]	Device Marking
FDMF8704V	32	12-19	1000	FDMF8704V

Pin Configuration

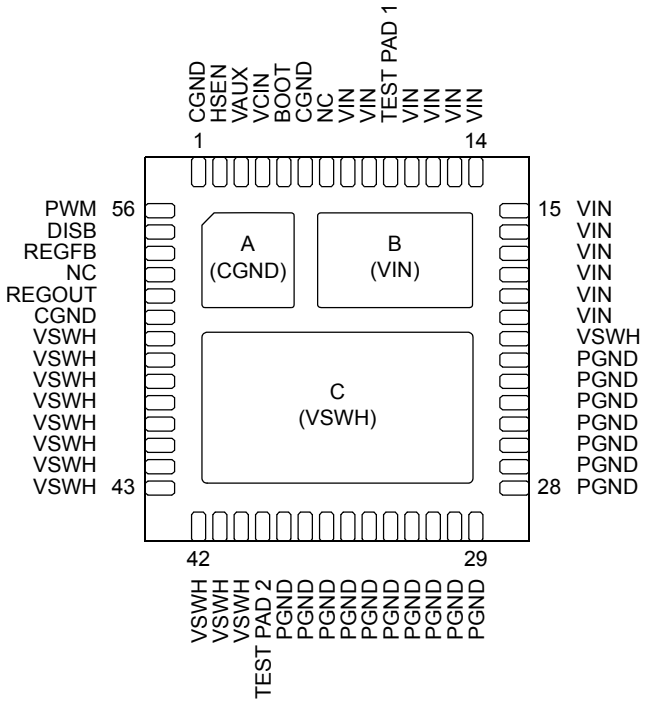


Figure 2. MLP 8x8 56L Bottom View

Pin Description

Pin	Name	Function
1, 6, 51, A	CGND	IC Ground. Ground return for driver IC.
2	HSEN	High Side FET Enable. Must be connected to BOOT pin.
3	VAUX	Auxiliary Power for 5V regulator Op-Amp.
4	VCIN	IC Supply. +5V chip bias power. Bypass with a 1µF ceramic capacitor.
5	BOOT	Bootstrap Supply Input. Provides voltage supply to high-side MOSFET driver. Connect to bootstrap capacitor.
7, 53	NC	No Connect.
21, 40-50, C	VSWH	Switch Node Input. SW Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
8, 9, 11-20, B	VIN	Power Input. Output stage supply voltage.
10	TEST PAD 1	For manufacturing test only. HDRV pin. This pin must be floated. Must not be connected to any pin.
22-38	PGND	Power Ground. Output stage ground. Source pin of low side MOSFET(s).
39	TEST PAD 2	For manufacturing test only. LDRV pin. This pin must be floated. Must not be connected to any pin.
52	REGOUT	Regulator Driver Output. An external NPN transistor is used to generate the 5V output voltage with internal controller.
54	REGFB	Regulation Sense Input. The internal resistor divider will set this voltage to be regulated at 5V.
55	DISB	Output Disable. When low, this pin disable FET switching (HDRV and LDRV are held low).
56	PWM	PWM Signal Input. This pin accepts a logic-level PWM signal from the controller.

Absolute Maximum Rating

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter		Min.	Max.	Units
V_{CIN}, PWM, DISB to PGND		-0.3	6	V
V_{IN} to PGND		-0.3	24	V
BOOT to VSWH		-0.3	6	V
VAUX to PGND		-0.3	20	V
VSWH to PGND		-1.0	24	V
BOOT to PGND		-0.3	30	V
$I_{O(AV)}$	V_{IN} = 12V, V_O = 1.3V, f_{sw} = 1MHz, T_{PCB} = 100°C		32	A
$I_{O(PK)}$	V_{IN} = 12V, t_{PULSE} = 10µs		65	A
$R_{\theta JPCB}$	Junction to PCB Thermal Resistance (note 1)		5	°C/W
P_D	T_{PCB} = 100°C (note 1)		10	W
Operating and Storage Junction Temperature Range		-55	150	°C

Note 1: Package power dissipation based on 4 layers, 2 square inch, 2 oz. copper pad. $R_{\theta JPCB}$ is the steady state junction to PCB thermal resistance with PCB temperature referenced at VSWH pin.

Recommended Operating Range

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Min.	Typ.	Max.	Units
V_{CIN}	Control Circuit Supply Voltage	4.5	5	5.5	V
V_{IN}	Output Stage Supply Voltage	7	12	20	V
V_{OUT}	Output Voltage	0.8	1.3	3.2	V

Electrical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage Range	V_{CC}		4.5	5	5.5	V
Control Circuit Supply Current	I_{CC}	f_{SW} = 0Hz, V_{DISB} = 5V		1	3	mA
		f_{SW} = 1MHz, V_{DISB} = 5V		50		
PWM Input High Voltage	$V_{IH(PWM)}$		2.4			V
PWM Input Low Voltage	$V_{IL(PWM)}$				0.8	V
PWM Input Current	$I_{IL(PWM)}$		-2		2	µA
DISB Input High Voltage	$V_{IHDISB)}$		2.4			V
DISB Input Low Voltage	$V_{IL(DISB)}$				0.8	V
DISB Input Current	I_{DISB}		-2		2	µA
Auxiliary Input Voltage Operating Range	V_{AUX}		7		20	V
Regulator Output Voltage	V_{REGOUT}		4.75	5	5.25	V
Propagation Delay	$t_{PDL(DISB-LDRV)}$ [2]	V_{IN} = 12V, V_{OUT} = 1.3V, f_{sw} = 1MHz, I_O = 30A		8		ns
	$t_{PDH(DISB-LDRV)}$ [2]			6		ns
	$t_{PDL(LDRV)}$ [2]			9		ns
	$t_{PDL(HDRV)}$ [2]			22		ns
	$t_{PDH(LDRV)}$ [2]			12		ns
	$t_{PDH(HDRV)}$ [2]			20		ns

Note 2: $t_{PDL(LDRV/HRDV)}$ refers to HIGH-to-LOW transition, $t_{PDH(LDRV/HDRV)}$ refers to LOW-to-HIGH transition.

Functional Block Diagram

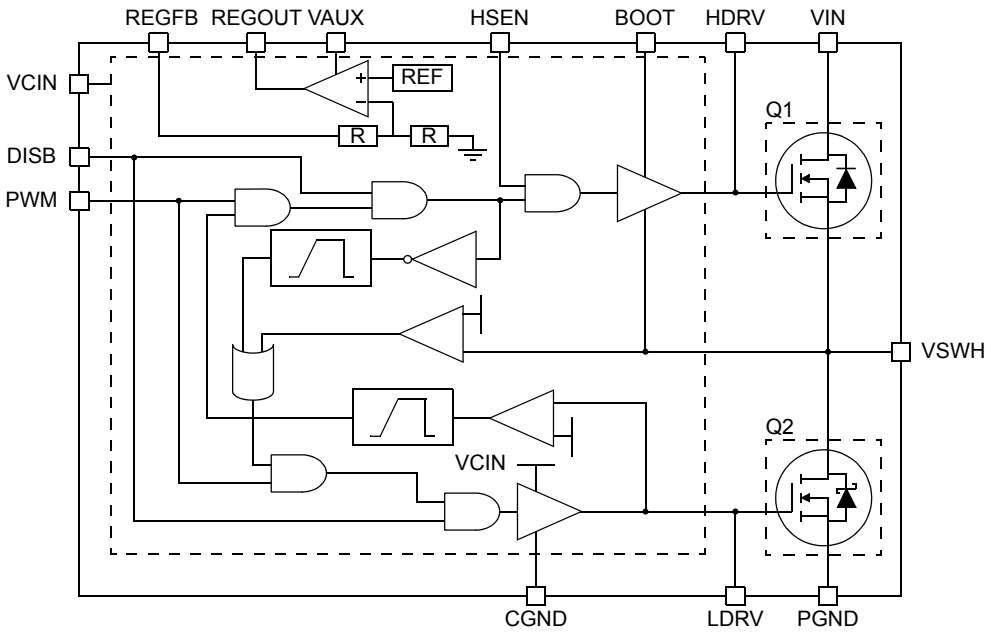


Figure 3. Functional Block Diagram

Functional Description

The FDMF8704V is a driver plus FET module optimized for synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1MHz.

Low-Side Driver

The low-side driver (LDRV) is designed to drive a ground referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for LDRV is internally connected between VCIN and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB = 0V), LDRV is held low.

High-Side Driver

The high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the external diode and external bootstrap capacitor (C_{BOOT}). During start-up, VSWH is held at PGND, allowing C_{BOOT} to charge to V_{CIN} through the internal diode. When the PWM input goes high, HDRV will begin to charge the high-side MOSFET's gate (Q1). During this transition, charge is removed from C_{BOOT} and delivered to Q1's gate. As Q1 turns on, VSWH rises to VIN, forcing the BOOT pin to VIN + $V_{C(BOOT)}$, which provide sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to VSWH. C_{BOOT} is then recharged to V_{CIN} when VSWH falls to PGND. HDRV output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Adaptive Gate Drive Circuit

The driver IC embodies an advanced design that ensures minimum MOSFET dead-time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to Figure 4 and 5 for the relevant timing waveforms. To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, Q2 will begin to turn OFF after some propagation delay ($t_{PDL(LDRV)}$). Once the LDRV pin is discharged below ~1.2V, Q1 begins to turn ON after adaptive delay $t_{PDH(HDRV)}$. To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, Q1 will begin to turn OFF after some propagation delay ($t_{PDL(HDRV)}$). Once the VSWH pin falls below ~2.2V, Q2 begins to turn ON after adaptive delay $t_{PDH(LDRV)}$. Additionally, V_{GS} of Q1 is monitored. When $V_{GS(Q1)}$ is discharged below ~1.2V, a secondary adaptive delay is initiated, which results in Q2 being driven ON after $t_{PDH(LDRV)}$, regardless of SW state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle, particularly for cases where the power converter is sinking current and SW voltage does not fall below the 2.2V adaptive threshold. Secondary delay $t_{PDH(HDRV)}$ is longer than $t_{PDH(LDRV)}$.

Timing Diagram

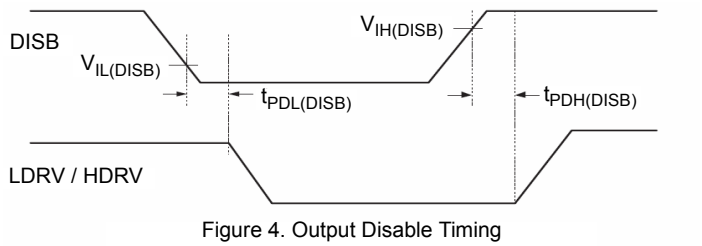


Figure 4. Output Disable Timing

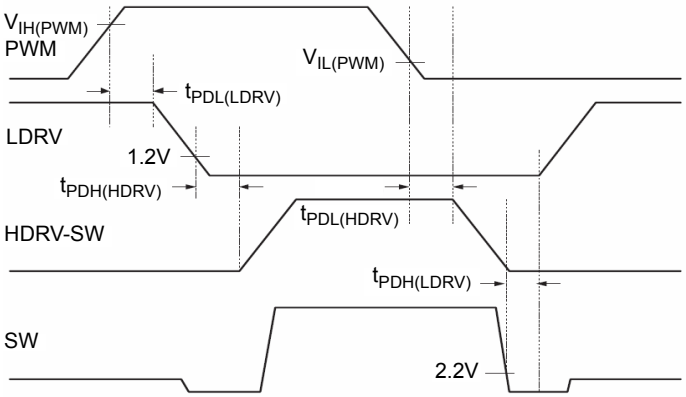


Figure 5. Adaptive Gate Drive Timing

Typical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

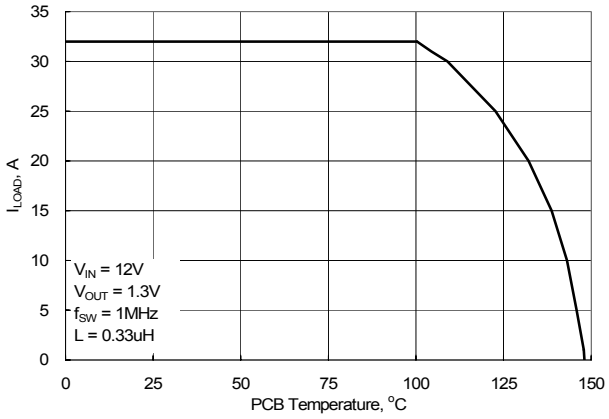


Figure 6. Safe Operating Area

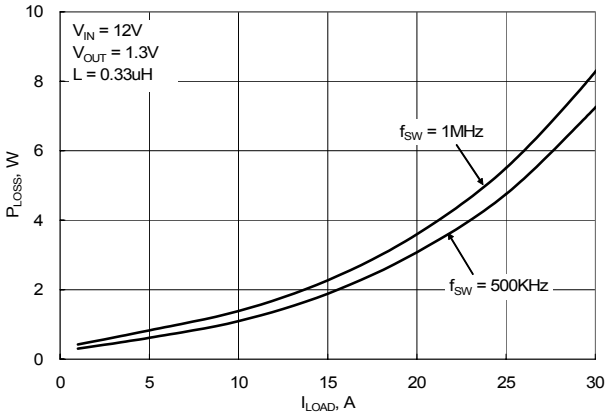


Figure 7. Module Power Loss vs. Output Current

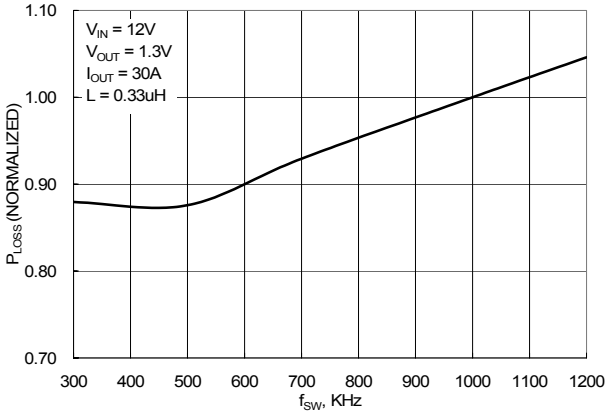


Figure 8. Power Loss vs. Switching Frequency

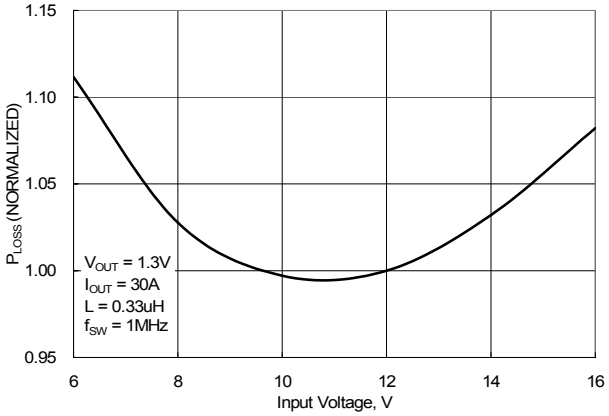


Figure 9. Power Loss vs. Input Voltage

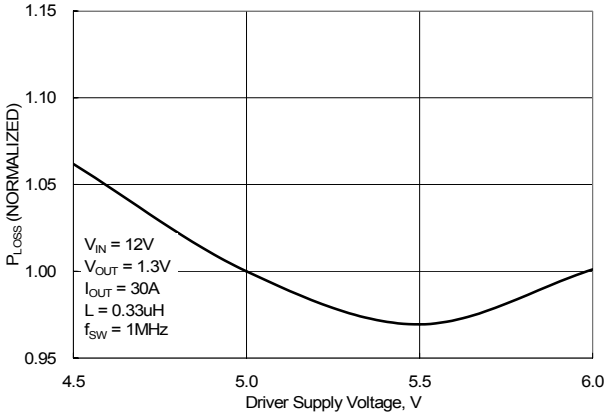


Figure 10. Power Loss vs. Driver Supply Voltage

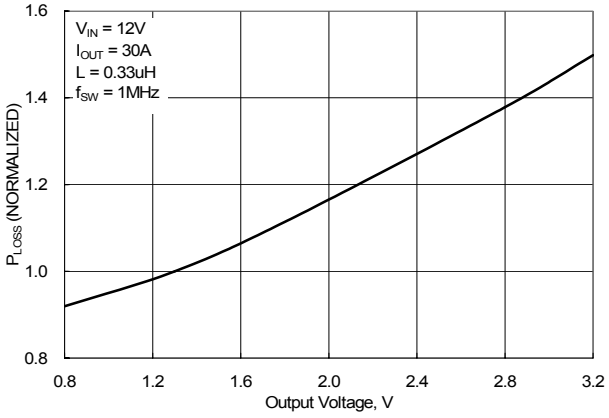


Figure 11. Power Loss vs. Output Voltage

Typical Characteristics

V_{IN} = 12V, V_{CIN} = 5V, T_A = 25°C unless otherwise noted.

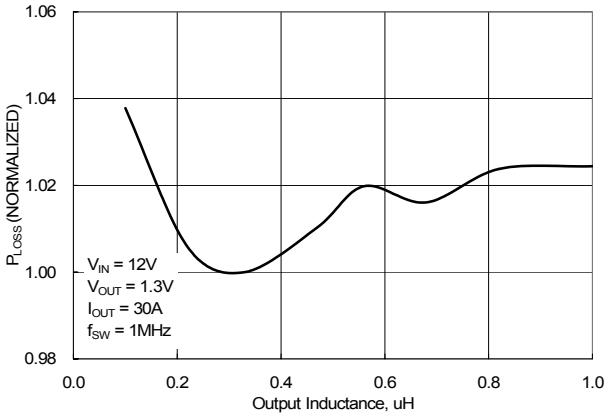


Figure 12. Power Loss vs. Output Inductance

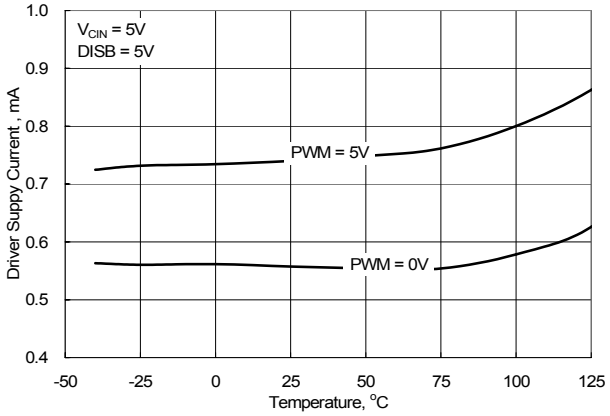


Figure 13. Driver Supply Current vs. Temperature

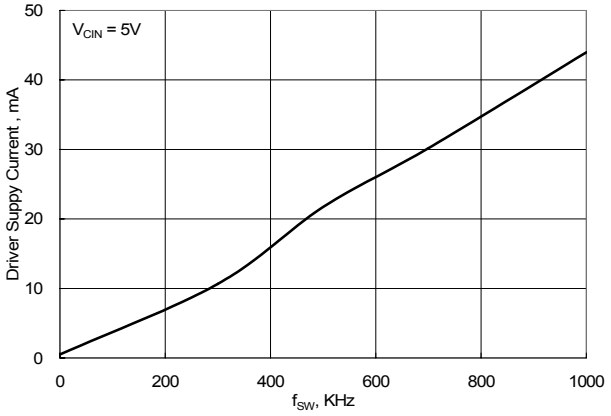


Figure 14. Driver Supply Current vs. Frequency

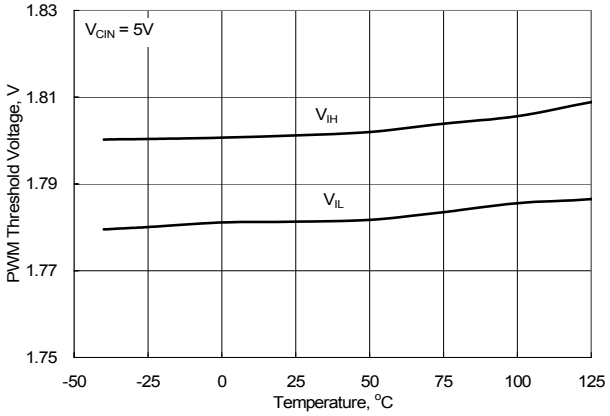


Figure 15. PWM Threshold Voltage vs. Temperature

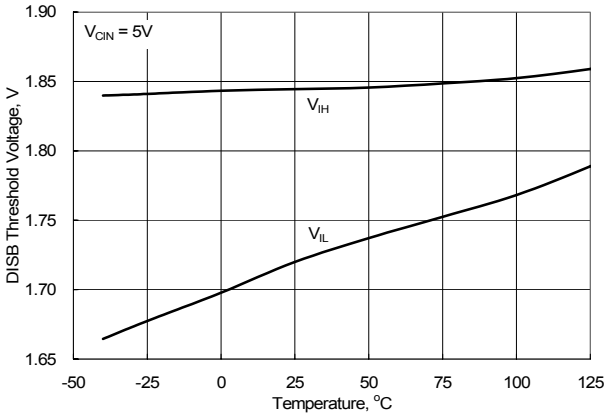


Figure 16. DISB Threshold Voltage vs. Temperature

Application Information

Supply Capacitor Selection

For the supply input (V_{CIN}) of the FDMF8704V, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FDMF8704V V_{CIN} and CGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and the external schottky diode, as shown in Figure 18. A bootstrap capacitance of 100nF, X7R or X5R capacitor is adequate.

The peak surge current rating of the boot diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces. Boot diode must be sized big enough to carry the forward charge current. Refer to Figure 14 for boot diode average forward current.

The bootstrap diode must have low V_F and low reverse current leakage. Breakdown voltage of the bootstrap diode must be greater than the BOOT to VSWH voltage.

Typical Application

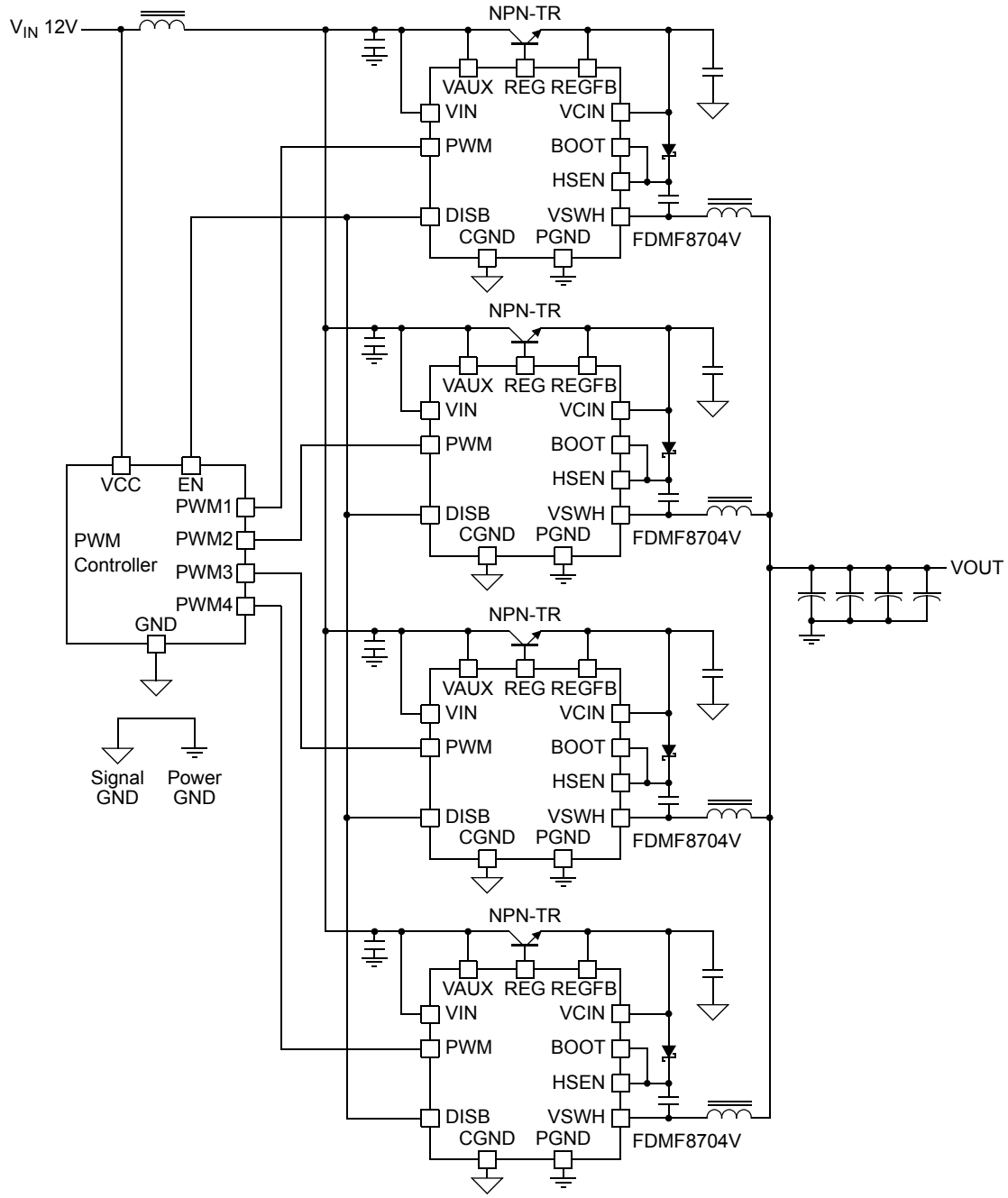


Figure 17. Typical Application

Module Power Loss Measurement and Calculation

Refer to Figure 18 for module power loss testing method. Power loss calculation are as follows:

(a) P_{IN} = $(V_{IN} \times I_{IN}) + (V_{CIN} \times I_{CIN})$ (W)
(b) P_{OUT} = $V_O \times I_{OUT}$ (W)
(c) P_{LOSS} = $P_{IN} - P_{OUT}$ (W)

PCB Layout Guideline

Figure 19. shows a proper layout example of FDMF8704V and critical parts. All of high current flow path, such as V_{IN}, VSWH, V_{OUT} and GND copper, should be short and wide for better and stable current flow, heat radiation and system performance.

Following is a guideline which the PCB designer should consider:

1. Input bypass capacitors should be close to V_{IN} and GND pin of FDMF8704V to help reduce input current ripple component induced by switching operation.

2. It is critical that the VSWH copper has minimum area for lower switching noise emission. VSWH copper trace should also be wide enough for high current flow. Other signal routing path, such as PWM IN and BOOT signal, should be considered with care to avoid noise pickup from VSWH copper area.

3. Output inductor location should be as close as possible to the FDMF8704V for lower power loss due to copper trace.

4. Snubber for suppressing ringing and spiking of VSWH voltage should be placed near the FDMF8704V. The resistor and capacitor need to be of proper size for power dissipation.

5. Place boot diode, ceramic bypass capacitor and boot capacitor as close to V_{CIN} and BOOT pin of FDMF8704V in order to supply stable power. Routing width and length should also be considered

6. Use multiple Vias on each copper area to interconnect each top, inner and bottom layer to help smooth current flow and heat conduction. Vias should be relatively large and of reasonable inductance.

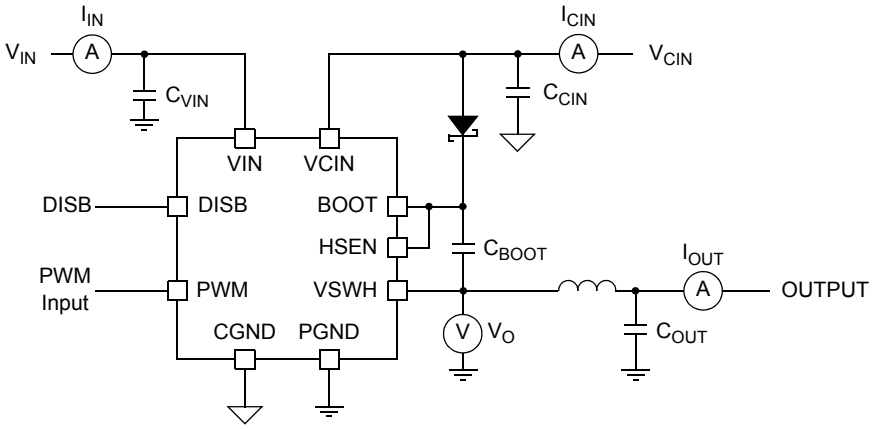


Figure 18. Power Loss Measurement Block Diagram

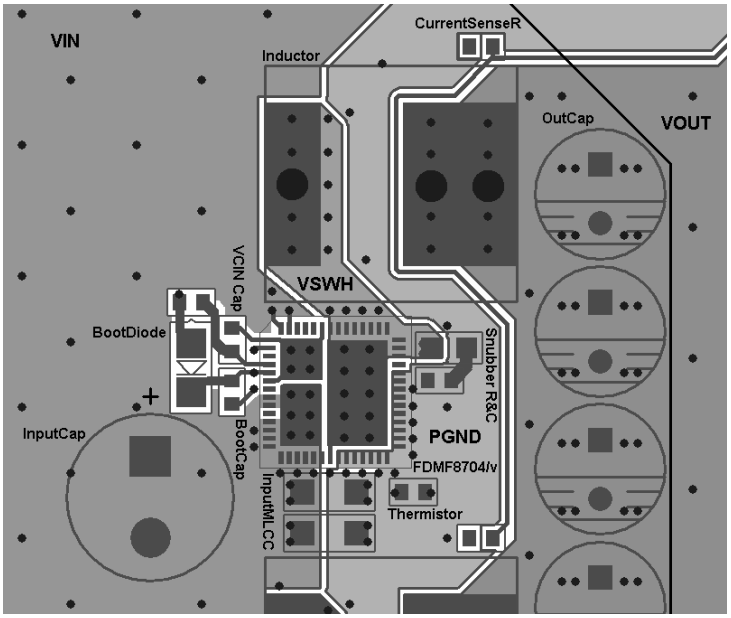
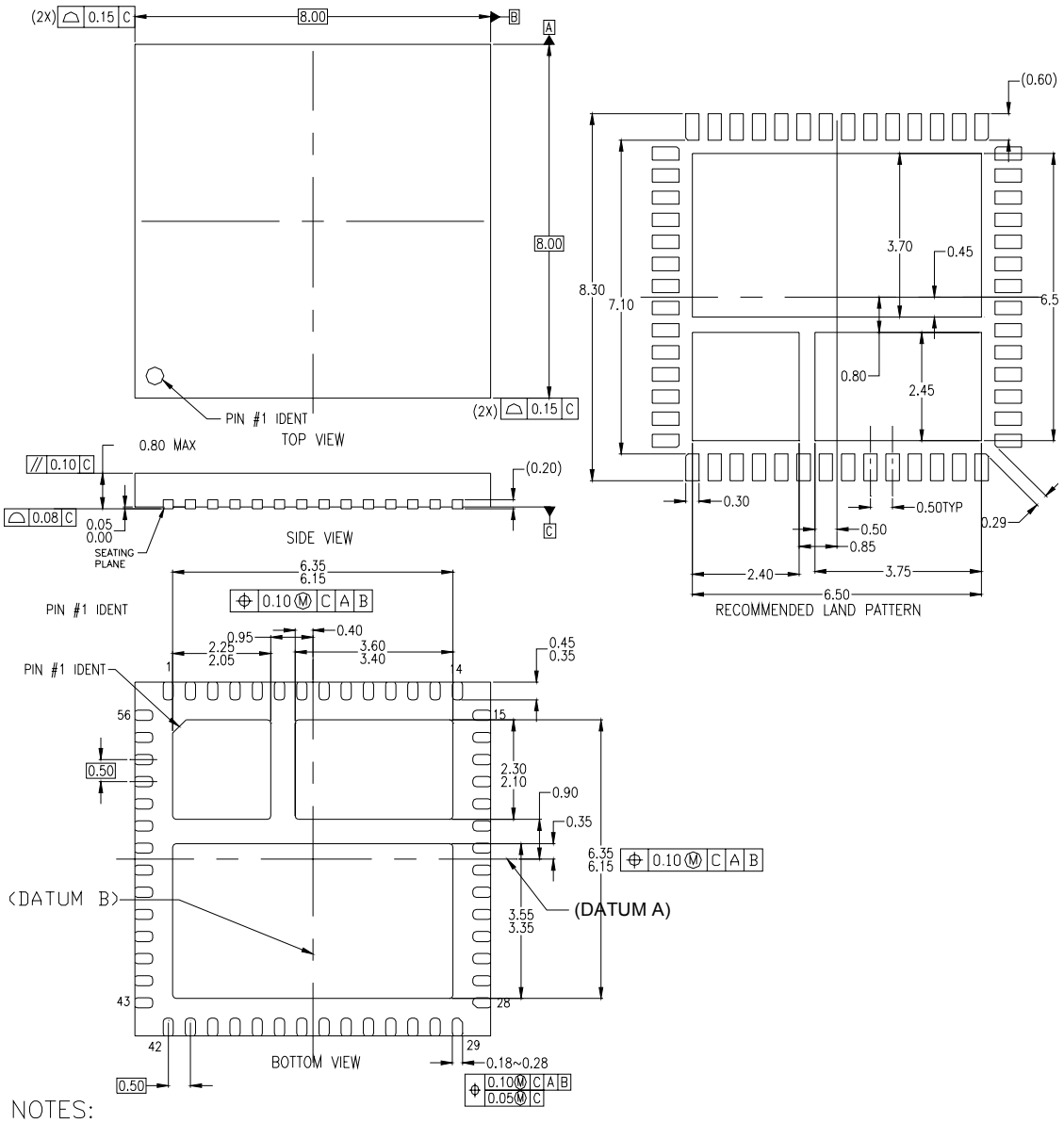


Figure 19. Typical PCB Layout Example (Top View)

Dimensional Outline and Pad layout



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SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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