19-3699; Rev 1; 9/05

EVALUATION KIT AVAILABLE

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

MAX8758

General Description

The MAX8758 includes a high-performance step-up regulator, a high-speed operational amplifier, and a logic-controlled, high-voltage switch-control block with programmable delay. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC regulator provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency (640kHz/1.2MHz), current-mode regulator with an integrated 14V n-channel power MOSFET. The high-switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides fast transient response to pulsed loads. The regulator achieves efficiencies over 85% by bootstrapping the supply rail of the internal gate driver from the step-up regulator output. The step-up regulator features undervoltage lockout (UVLO), soft-start, and internal current limit. The high-current operational amplifier is designed to drive the LCD backplane (VCOM). The amplifier features high output current (±150mA), fast slew rate (7.5V/µs), wide bandwidth (12MHz), and rail-to-rail inputs and outputs.

The MAX8758 is available in a 24-pin, 4mm x 4mm, thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels. The device operates over the -40°C to +85°C temperature range.

Applications

Notebook Displays

LCD Monitors

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8758ETG	-40°C to +85°C	24 Thin QFN-EP* 4mm x 4mm
MAX8758ETG+	-40°C to +85°C	24 Thin QFN-EP* 4mm x 4mm

*EP = Exposed pad.
+Denotes lead-free package.

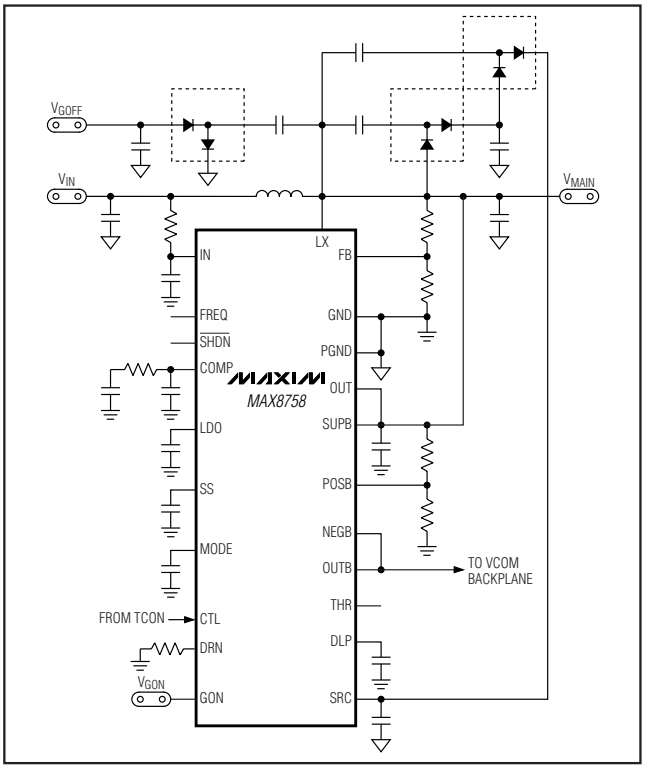
Pin Configuration appears at end of data sheet.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ **1.8V to 5.5V Input Voltage Range**
- ♦ **Input Undervoltage Lockout**
- ♦ **0.5mA Quiescent Current**
- ♦ **640kHz/1.2MHz Current-Mode Step-Up Regulator**
  - **Fast Transient Response**
  - **High-Accuracy Output Voltage (1.5%)**
  - **Built-In 14V, 2.5A, 115mΩ MOSFET**
  - **High Efficiency**
  - **Programmable Soft-Start**
  - **Current Limit with Lossless Sensing**
  - **Timer-Delay Fault Latch**
- ♦ **High-Speed Operational Amplifier**
  - **±150mA Output Current**
  - **7.5V/µs Slew Rate**
  - **12MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs/Outputs**
- ♦ **Dual Mode™, Logic-Controlled, High-Voltage Switch with Programmable Delay**
- ♦ **Thermal-Overload Protection**
- ♦ **24-Pin, 4mm x 4mm, Thin QFN Package**

Simplified Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, CTL, LDO to GND .....-0.3V to +6V
SUPB, LX, OUT to GND.....-0.3V to +14V
OUTB, NEGB, POSB to GND .....-0.3V to (SUPB + 0.3V)
THR, DLP, MODE, FREQ, COMP, FB,
SS to GND.....-0.3V to V_{LDO} + 0.3V
PGND to GND .....-0.3V to + 0.3V
SRC to GND .....-0.3V to + 30V
GON, DRN to GND .....-0.3V to V_{SRC} + 0.3V
GON RMS Current Rating.....± 50mA
OUTB RMS Current Rating .....± 60mA
LX RMS Current Rating 1.6A
Continuous Power Dissipation (T_A = +70°C)
24-Pin, 4mm x 4mm Thin QFN
(derate 16.9mW/°C above +70°C).....1349.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = +3V, OUT = +10V, FREQ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		1.8		5.5	V
IN Quiescent Current	V_{IN} = 3V, V_{FB} = 1.5V		27	40	µA
IN Undervoltage Lockout	IN rising, 200mV hysteresis, LX remains off below this level		1.3	1.75	V
LDO Output Voltage	6V ≤ V_{OUT} ≤ 13V, I_{LDO} = 12.5mA, V_{FB} = 1.5V (Note1)	4.8	5.0	5.2	V
LDO Undervoltage Lockout Voltage	LDO rising, 200mV hysteresis	2.4	2.7	3.0	V
OUT Supply Voltage Range	(Note 1)	4.5		13.0	V
OUT Overvoltage Fault Threshold		13.2	13.6	14.0	V
OUT Undervoltage Fault Threshold				1.4	V
OUT Supply Current	V_{FB} = 1.5V, no load		0.5	2.0	mA
	V_{FB} = 1.1V, no load		4	10.0	
Shutdown Supply Current (Total of IN, OUT, and SUPB)	V_{IN} = V_{OUT} = V_{SUPB} = 3V		4	10	µA
Thermal Shutdown	Temperature rising, 15°C hysteresis		+160		°C
STEP-UP REGULATOR					
Operating Frequency	FREQ = GND	512	600	768	kHz
	FREQ = IN	1020	1200	1380	
Oscillator Maximum Duty Cycle	FREQ = GND	91	95	99	%
	FREQ = IN	88	92	96	
FB Regulation Voltage		1.228	1.24	1.252	V
FB Fault Trip Level	Falling edge	0.96	1.0	1.04	V
Duration to Trigger Fault Condition	FREQ = GND	43	51	64	ms
	FREQ = IN	47	55	65	
FB Load Regulation	0 < I_{LOAD} < 200mA, transient only		-1		%
FB Line Regulation	V_{IN} = 1.8V to 5.5V	-0.15	-0.08	+0.15	%/V
FB Input Bias Current	V_{FB} = 1.3V		125	200	nA
FB Transconductance	ΔI = 5µA at COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		700		V/V
LX On-Resistance	I_{LX} = 200mA		115	200	mΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = +3V, OUT = +10V, FREQ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX Leakage Current	V_{LX} = 13V		0.01	20	µA
LX Current Limit	65% duty cycle	2.0	2.5	3.0	A
Current-Sense Transresistance		0.19	0.3	0.40	V/A
SS Source Current		3.0	4.0	5.5	µA
POSITIVE GATE DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage	V_{IN} = 1.8V to 5.5V			0.6	V
CTL Input High Voltage	V_{IN} = 1.8V to 2.4V	1.4			V
	V_{IN} = 2.4V to 5.5V	2.0			
CTL Input Leakage Current	V_{CTL} = 0 or V_{IN}	-1		+1	µA
CTL-to-SRC Propagation Delay	GON rising, V_{MODE} = 1.24V, V_{CTL} = 0 to 3V step, no load on GON		100		ns
	GON falling, V_{MODE} = 1.24V, V_{CTL} = 3V to 0 step, no load on GON		100		
SRC Input Voltage	V_{DLP} = 0, V_{IN} = 3V		2500		Ω
SRC Input Current	MODE = DLP = CTL = LDO		150	250	µA
DRN Input Current	MODE = DLP = LDO, V_{DRN} = 8V, V_{CTL} = 0		150	250	µA
SRC-to-GON Switch On-Resistance	DLP = CTL = LDO		15	30	Ω
DRN-to-GON Switch On-Resistance	DLP = LDO, V_{CTL} = 0		65	130	Ω
GON-to-PGND Switch On-Resistance	V_{DLP} = 0, V_{IN} = 3V		2500		Ω
MODE Switch On-Resistance	V_{DLP} = 0, V_{IN} = 3V		1000		Ω
MODE 1 Voltage Threshold	MODE rising		0.9 x V_{LDO}		V
MODE Capacitor Charge Current (MODE 2)	V_{MODE} = 1.5V	40	50	62	µA
MODE 2 Switch Transition Voltage Threshold	GON connected to DRN	2.3	2.5	2.7	V
MODE Current-Source Stop Threshold	MODE rising	3.3	3.5	3.7	V
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	4	5	6	µA
DLP Turn-On Threshold		2.375	2.500	2.625	V
THR-to-GON Voltage Gain	V_{GON} = 12V, V_{THR} = 1.2V	9.7	10.0	10.3	V/V
OPERATIONAL AMPLIFIER					
SUPB Supply Range		4.5		13.0	V
SUPB Supply Current	Buffer configuration, V_{POSB} = 4V, no load			1.0	mA
Input Offset Voltage	V_{NEGB}, V_{POSB} = V_{SUPB}/2, T_A = +25°C			12	mV
Input Bias Current	V_{NEGB}, V_{POSB} = V_{SUPB}/2	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{SUPB}	V

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = +3V, OUT = +10V, FREQ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing High	I_{OUTB} = 100µA	V_{SUPB} - 15			mV
	I_{OUTB} = 5mA	V_{SUPB} - 150			
Output Voltage Swing Low	I_{OUTB} = -100µA			15	mV
	I_{OUTB} = -5mA			150	
Slew Rate			7.5		V/µs
-3dB Bandwidth			12		MHz
Gain-Bandwidth Product			8		MHz
Short-Circuit Current	OUTB shorted to V_{SUPB}/2, sourcing	75	150		mA
	OUTB shorted to V_{SUPB}/2, sinking	75	150		
CONTROL INPUTS					
FREQ Input Low Voltage	V_{IN} = 1.8V to 5.5V			0.6	V
FREQ Input High Voltage	V_{IN} = 1.8V to 2.4V	1.4			V
	V_{IN} = 2.4V to 5.5V	2.0			
FREQ Pulldown Current	V_{FREQ} = 1.0V	3.5	5.0	6.0	µA
$\overline{SHDN}$ Input Low Voltage	V_{IN} = 1.8V to 5.5V			0.6	V
$\overline{SHDN}$ Input High Voltage	V_{IN} = 1.8V to 2.4V	1.4			V
	V_{IN} = 2.4V to 3.6V	2.0			
	V_{IN} = 3.6V to 5.5V	2.9			
$\overline{SHDN}$ Input Current			0.001	1.0	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = +3V, OUT = +10V, FREQ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		1.8		5.5	V
IN Quiescent Current	V_{IN} = 3V, V_{FB} = 1.5V			30	µA
IN Undervoltage Lockout	IN rising, 200mV hysteresis, LX remains off below this level			1.75	V
LDO Output Voltage	6V ≤ V_{OUT} ≤ 13V, I_{LDO} = 12.5mA, V_{FB} = 1.5V (Note 1)	4.8		5.2	V
LDO Undervoltage Lockout Voltage	LDO rising, 200mV hysteresis	2.4		3.0	V
OUT Supply Voltage Range	(Note 1)	4.5		13.0	V
OUT Supply Current	V_{FB} = 1.5V, no load			2.0	mA
	V_{FB} = 1.1V, no load			10.0	
STEP-UP REGULATOR					
Operating Frequency	FREQ = GND	512		768	kHz
	FREQ = IN	990		1380	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = +3V, OUT = +10V, FREQ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Maximum Duty Cycle	FREQ = GND	91		99	%
	FREQ = IN	88		96	
FB Regulation Voltage		1.220		1.252	V
FB Transconductance	ΔI = 5µA at COMP	75		280	µS
LX On-Resistance	I_{LX} = 200mA			200	mΩ
LX Current Limit	65% duty cycle	2.0		3.0	A
POSITIVE GATE DRIVER TIMING AND CONTROL SWITCHES					
SRC Input Voltage Range				28	V
SRC Input Current	MODE = DLP = CTL = LDO			250	µA
DRN Input Current	MODE = DLP = LDO, V_{DRN} = 8V, V_{CTL} = 0			250	µA
SRC-to-GON Switch On-Resistance	DLP = CTL = LDO			30	Ω
DRN-to-GON Switch On-Resistance	DLP = LDO, V_{CTL} = 0			130	Ω
THR-to-GON Voltage Gain	V_{GON} = 12V, V_{THR} = 1.2V	9.7		10.3	V/V
OPERATIONAL AMPLIFIER					
SUPB Supply Range		4.5		13.0	V
SUPB Supply Current	Buffer configuration, V_{POSB} = 4V, no load			1.0	mA
Input Offset Voltage	V_{NEGB}, V_{POSB} = V_{SUPB} / 2			18	mV
Input Common-Mode Voltage Range		0		V_{SUPB}	V
Output Voltage Swing High	I_{OUTB} = 100µA	V_{SUPB} - 15			mV
	I_{OUTB} = 5mA	V_{SUPB} - 150			
Output Voltage Swing Low	I_{OUTB} = -100µA			15	mV
	I_{OUTB} = -5mA			150	
Short-Circuit Current	OUTB shorted to V_{SUPB}/2, sourcing	75			mA
	OUTB shorted to V_{SUPB}/2, sinking	75			

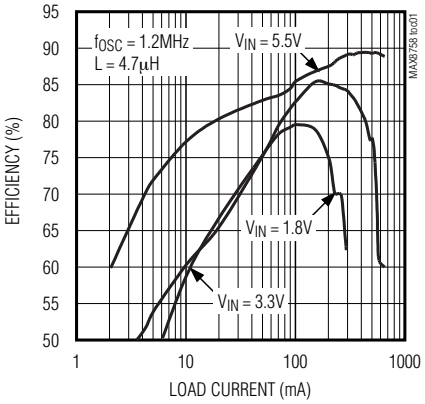
Note 1: OUT and SUP can operate down to 4.5V. LDO will be out of regulation, but IC will function correctly.
Note 2: -40°C specs are guaranteed by design, not production tested.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

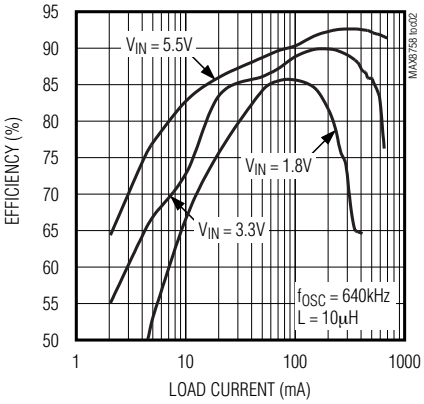
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 8.5V, FREQ = $\overline{SHDN}$ = IN, T_A = +25°C, unless otherwise noted.)

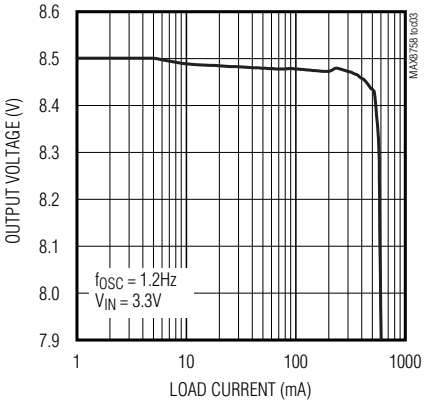
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 8.5V)



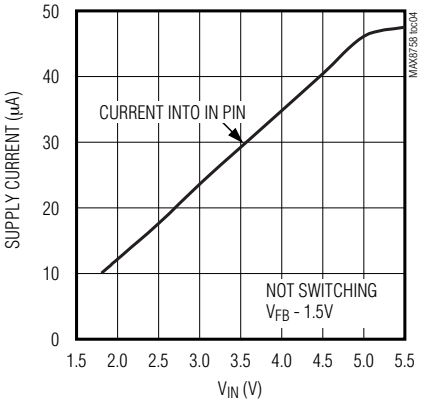
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 8.5V)



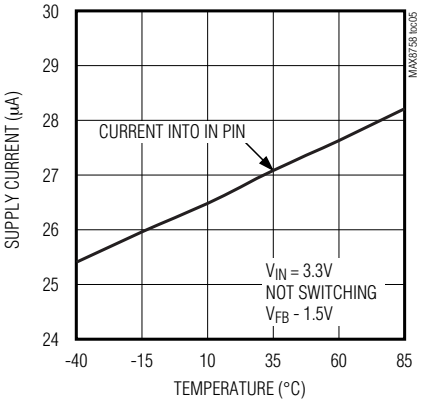
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (V_{MAIN} = 8.5V)



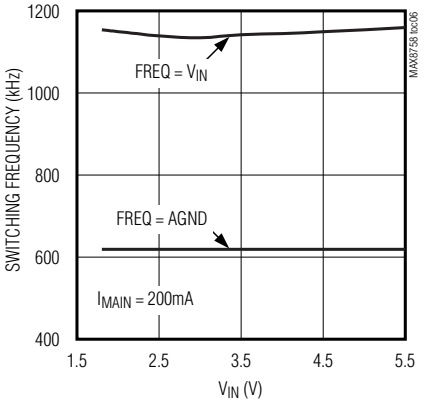
IN QUIESCENT CURRENT vs. SUPPLY VOLTAGE



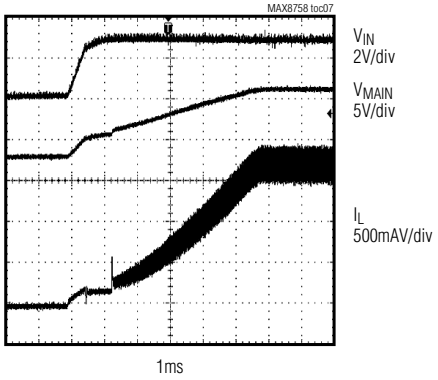
IN QUIESCENT CURRENT vs. TEMPERATURE



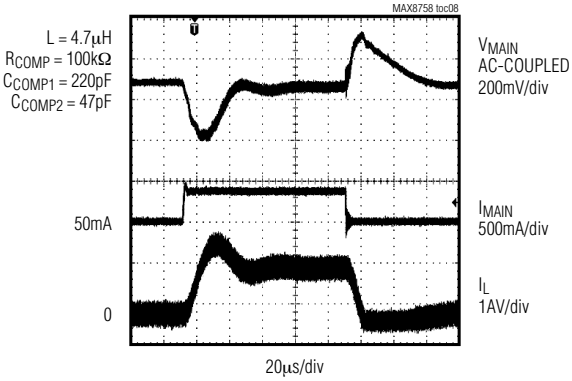
SWITCHING FREQUENCY vs. INPUT VOLTAGE



STEP-UP REGULATOR HEAVY-LOAD SOFT-START



STEP-UP REGULATOR LOAD TRANSIENT RESPONSE

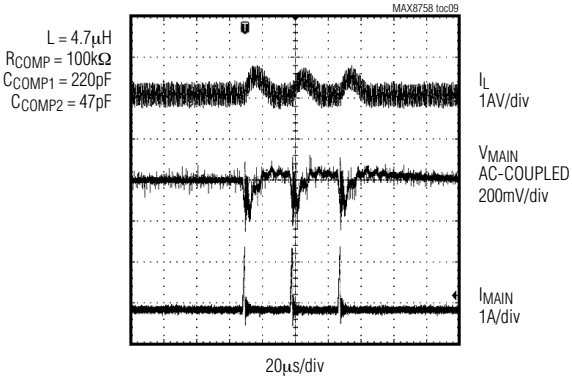


Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

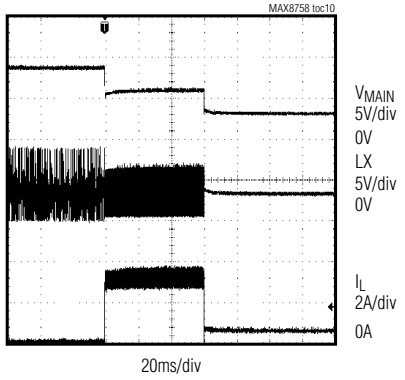
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 8.5V, FREQ = $\overline{SHDN}$ = IN, T_A = +25°C, unless otherwise noted.)

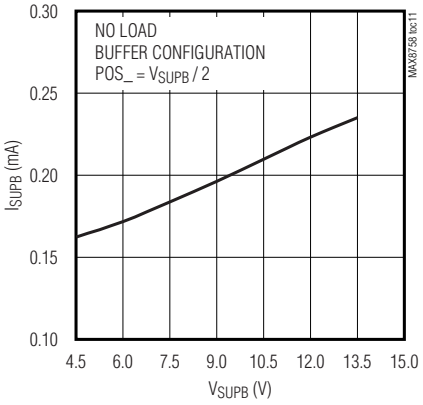
STEP-UP REGULATOR PULSED LOAD TRANSIENT RESPONSE



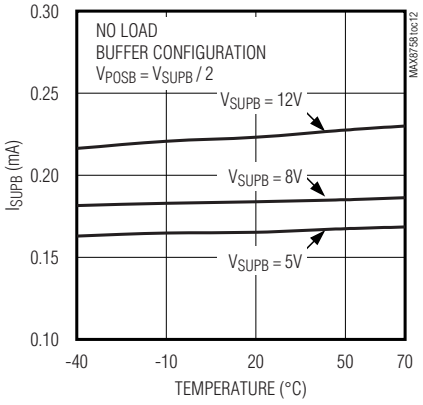
TIMER-DELAY LATCH RESPONSE TO OVERLOAD



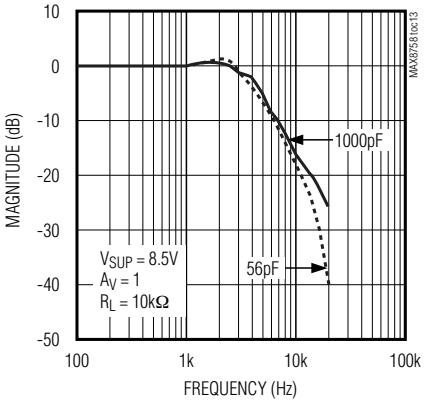
SUPB SUPPLY CURRENT vs. SUPB VOLTAGE



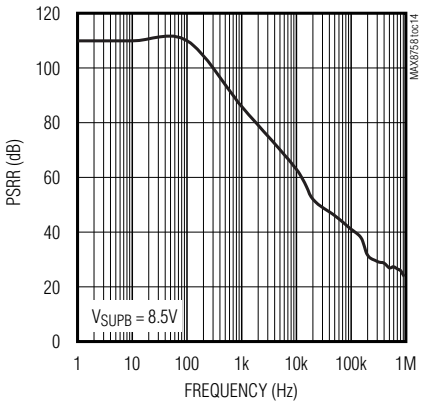
SUPB SUPPLY CURRENT vs. TEMPERATURE



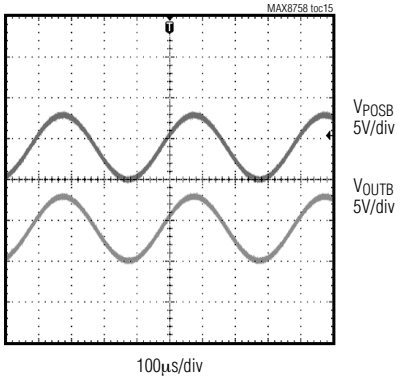
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE FOR VARIOUS C_{LOAD}



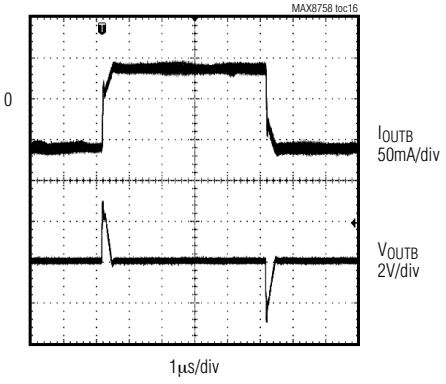
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OP-AMP RAIL-TO-RAIL INPUT/OUTPUT



OP-AMP LOAD TRANSIENT RESPONSE

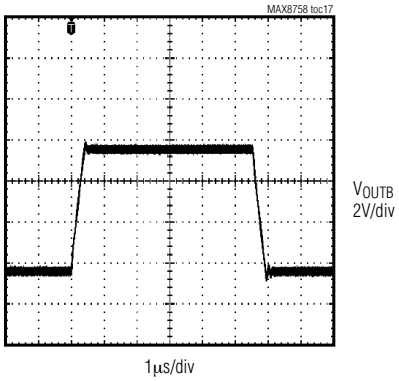


Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

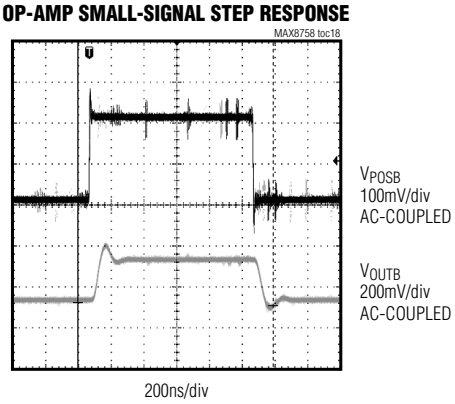
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 8.5V, FREQ = $\overline{SHDN}$ = IN, T_A = +25°C, unless otherwise noted.)

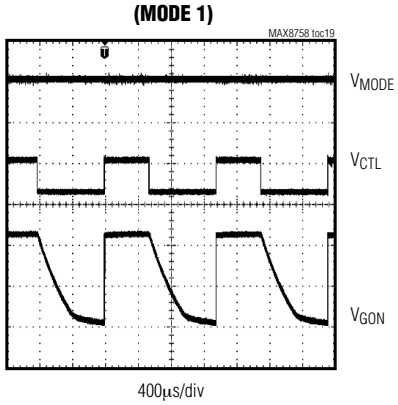
OP-AMP LARGE-SIGNAL STEP RESPONSE



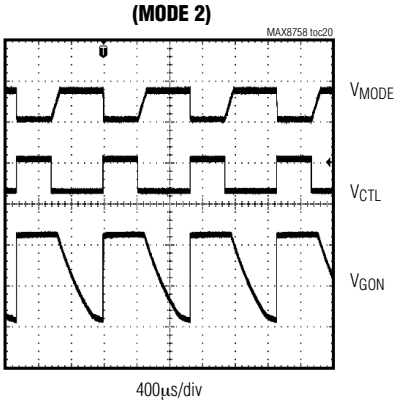
OP-AMP SMALL-SIGNAL STEP RESPONSE



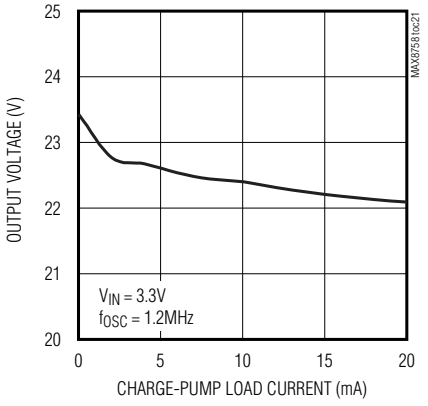
HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 1)



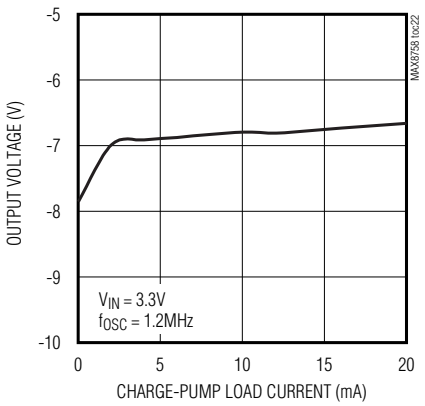
HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 2)



POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. CHARGE-PUMP LOAD CURRENT



NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



Pin Description

PIN	NAME	FUNCTION
1	GND	Analog Ground
2	GON	Internal High-Voltage-Switch Common Connection. GON is the output of the high-voltage-switch-control block. GON is internally pulled to PGND through a 1kΩ resistor in shutdown. See the *High-Voltage Switch Control* section for details.
3	CTL	High-Voltage, Switch-Control Block Timing Pin. See the *High-Voltage Switch Control* section for details.
4	DLP	High-Voltage, Switch-Control Block Delay Pin. Connect a capacitor from DLP to GND to set the delay time. A 5µA current source charges C_{DLP}. DLP is internally pulled to GND by a resistor in shutdown. See the *High-Voltage Switch Control* section for details.
5	THR	GON Falling Regulation Adjustment Pin. Connect THR to the center of a resistive voltage-divider between LDO or OUT and GND to adjust the V_{GON} falling regulation level. The actual regulation level is 10 x V_{THR}. See the *High-Voltage Switch Control* section for details.
6	SUPB	Operational Amplifier Supply Input. Bypass SUPB to GND with a 0.1µF capacitor.
7	OUTB	Operational Amplifier Output
8	NEGB	Operational Amplifier Inverting Input
9	POSB	Operational Amplifier Noninverting Input
10	N.C.	No Connection. Not internally connected.
11	LDO	5V Internal Linear Regulator Output. This regulator powers all internal circuitry except the operational amplifier. Bypass LDO to GND with a 0.22µF or greater ceramic capacitor.
12	OUT	Internal Linear Regulator Supply Pin. OUT is the supply input of the internal 5V linear regulator. Connect OUT directly to the output of the step-up regulator.
13	I.C.	Internally Connected. Make no connection to this pin.
14	SS	Soft-Start Control Pin. Connect a capacitor between SS and GND to set the soft-start period of the step-up regulator. See the *Bootstrapping and Soft-Start* section for details.
15	COMP	Error Amplifier Compensation Pin. See the *Step-Up Regulator Loop Compensation* section for details.
16	FREQ	Frequency-Select Pin. Connect FREQ to GND for 600kHz operation, and connect FREQ to IN for 1.2MHz operation.
17	IN	Supply Pin. Bypass IN to GND with a 1µF ceramic capacitor. Place the capacitor close to the IN pin.
18	LX	Switching Node. LX is the drain of the internal power MOSFET. Connect the inductor and the Schottky diode to LX and minimize trace area for low EMI.
19	$\overline{SHDN}$	Shutdown Control Pin. Pull $\overline{SHDN}$ low to turn off the step-up regulator, the operational amplifier, and the switch control block.
20	FB	Feedback Pin. The FB regulation point is 1.24V (typ). Connect FB to the center of a resistive voltage-divider between the step-up regulator output and GND to set the step-up regulator output voltage. Place the divider close to the FB pin.
21	PGND	Power Ground
22	MODE	High-Voltage, Switch-Control Block-Mode Selection Timing-Adjustment Pin. See the *High-Voltage Switch Control* section for details. MODE is high impedance when it is connected to LDO. MODE is internally pulled down by a 1kΩ resistor during UVLO, when V_{DLP} < 0.5 x V_{LDO}, or in shutdown.
23	DRN	High-Voltage, Switch-Control Input. DRN is the drain of the internal high-voltage p-channel MOSFET connected to GON.
24	SRC	High-Voltage Switch-Control Input. SRC is the source of the internal high-voltage p-channel MOSFET.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX8758 is a power-supply solution for TFT LCD panels in notebook computers. The circuit generates a +8.5V source driver supply, and approximately +22V and -7V gate driver supplies. The input voltage range for the IC is from +1.8V to +5.5V, but the Figure 1 circuit is designed to run from 2.7V to 3.6V. Table 1 lists some selected components and Table 2 lists the contact information of component suppliers.

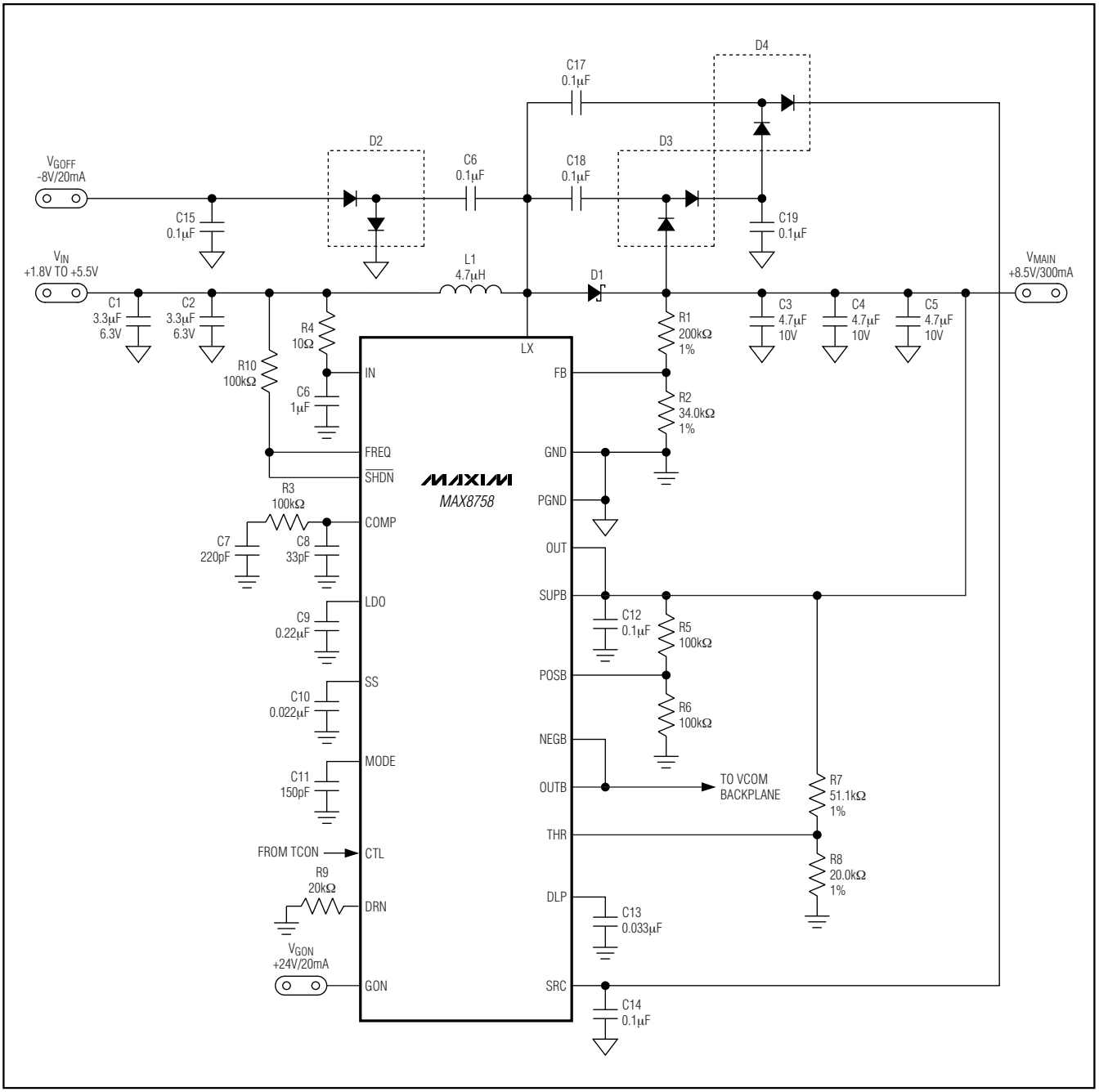


Figure 1. Typical Operating Circuit

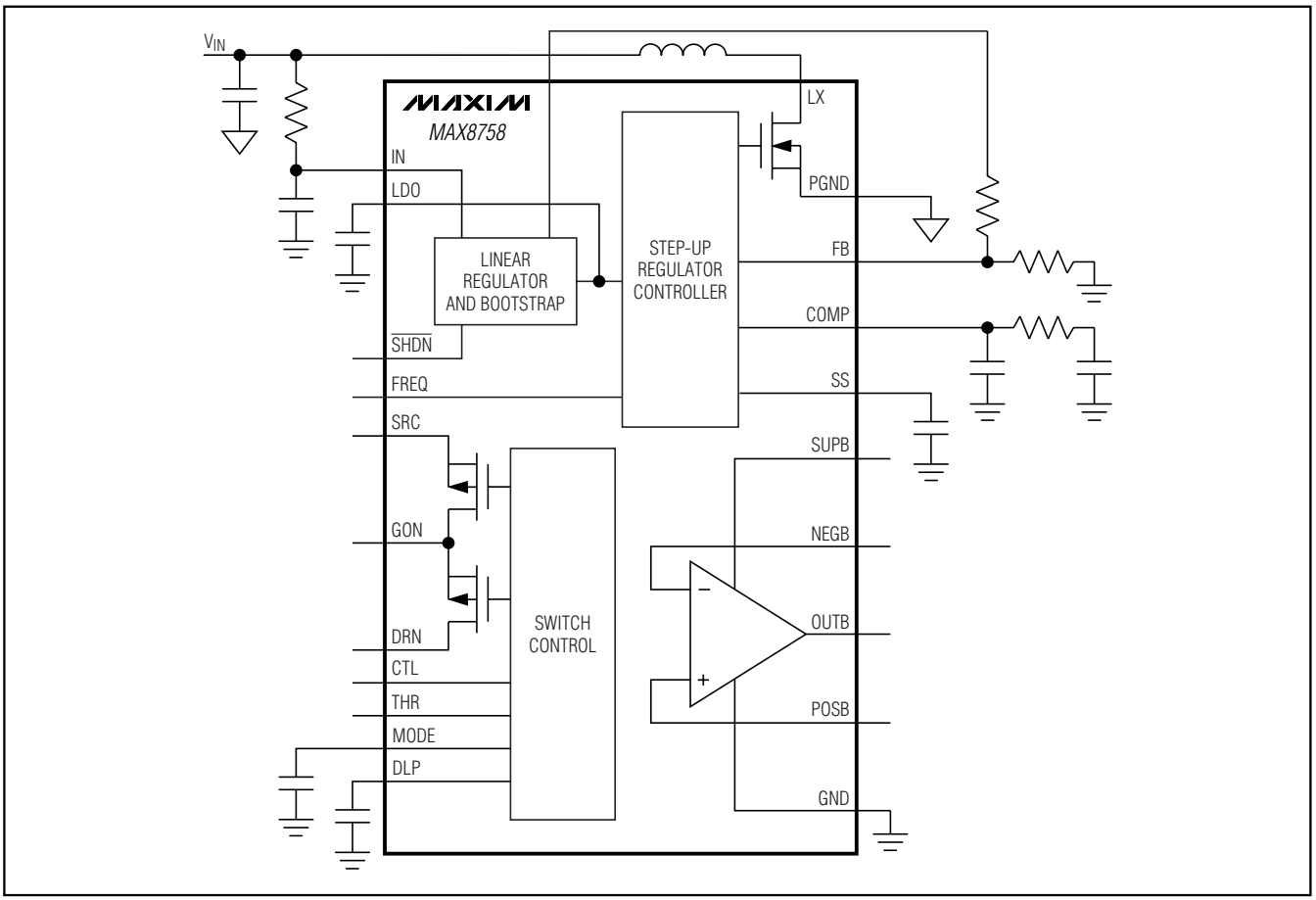


Figure 2. Functional Diagram

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	3.3µF ±10%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J335M
C3, C4, C5	4.7µF ±20%, 10V X5R ceramic capacitors (1206) TDK C3216X5R1A475M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02 (top mark S2)
D2, D3, D4	200mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE (top mark D4)
L1	4.2µH, 1.9A inductor Sumida CDRH6D12-4R2

Detailed Description

The MAX8758 is designed primarily for TFT LCD panels used in notebook computers. It contains a high-performance step-up regulator, a high-speed operational amplifier, a logic-controlled, high-voltage switch-control block with programmable delay, and an internal linear regulator for bootstrapping operation. Figure 2 shows the MAX8758 functional block diagram.

Step-Up Regulator

The step-up regulator is designed to generate the LCD source driver supply. It employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT LCD panel source drivers. The internal oscillator offers two pin-selectable frequency options (640kHz/1.2MHz), allowing users to optimize their designs based on the specific application requirements.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

The internal n-channel power MOSFET reduces the number of external components. The supply rail of the internal gate driver is bootstrapped to the internal linear regulator output to improve the efficiency at low-input voltages. The external-capacitor, soft-start function effectively controls inrush currents. The output voltage can be set from V_{IN} to 13V with an external resistive voltage-divider.

PWM Control Block

Figure 3 is the block diagram of the step-up regulator. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

where V_{OUT} is the output voltage of the step-up regulator.

On the rising edge of the internal oscillator clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. A transconductance error amplifier compares the FB voltage with a 1.24V (typ) reference voltage. The error amplifier changes the COMP voltage by charging or discharging the COMP capacitor. The COMP voltage is compared with a ramp, which is the sum of the current-sense signal and a slope compensation signal. Once the ramp signal exceeds the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the Schottky diode (D1 in Figure 1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

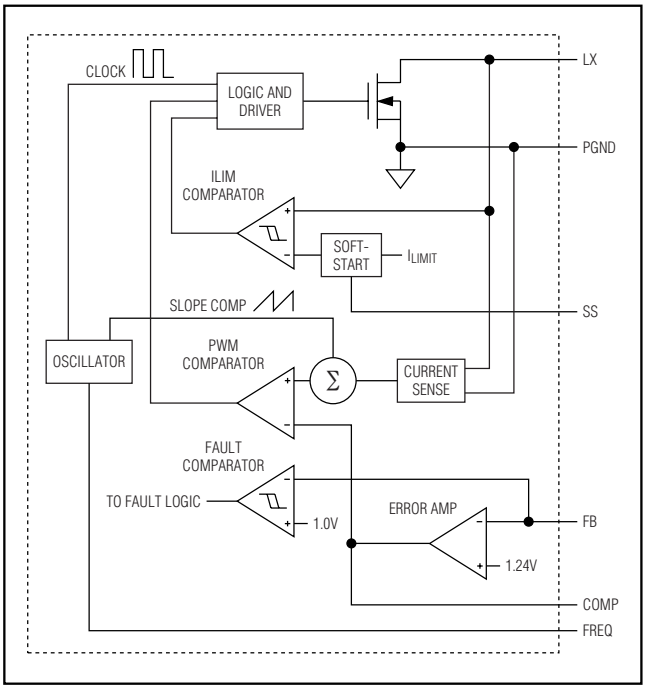


Figure 3. Step-Up Regulator Block Diagram

Bootstrapping and Soft-Start

The MAX8758 features bootstrapping operation. In normal operation, the internal linear regulator supplies power to the internal circuitry. The input of the linear regulator (OUT) should be directly connected to the output of the step-up regulator. The step-up regulator is enabled when the input voltage at OUT is above 1.75V, $\overline{SHDN}$ is high, and the fault latch is not set.

After being enabled, the regulator starts open-loop switching to generate the supply voltage for the linear regulator with a controlled duty cycle. The internal reference block turns on when the LDO voltage exceeds 2.7V (typ). When the reference voltage reaches regulation, the PWM controller and the current-limit circuit are enabled and the step-up regulator enters soft-start.

The soft-start timing can be adjusted with an external capacitor connected between SS and GND. After the step-up regulator is enabled, the SS pin is immediately charged to 0.5V. Then the capacitor is charged at a constant current of 4µA (typ). During this time, the SS voltage directly controls the peak inductor current, allowing a linear ramp from zero up to the full current limit. The maximum load current is available after the voltage on SS exceeds 1.5V. The soft-start capacitor is discharged to ground when $\overline{SHDN}$ is low. The soft-start routine minimizes inrush current and voltage overshoot and ensures a well-defined startup behavior (see the Step-Up Regulator Heavy Load Soft-Start waveform in the *Typical Operating Characteristics*).

Fault Protection

During steady-state operation, the MAX8758 monitors the FB voltage. If the FB voltage is below 1V (typ), the MAX8758 activates an internal fault timer. If there is a continuous fault for the fault-timer duration, the MAX8758 sets the fault latch, shutting down all the outputs. Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

The MAX8758 monitors the OUT voltage for undervoltage and overvoltage conditions. If the OUT voltage is below 1.4V (typ) or above 13.5V (typ), the MAX8758 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The OUT undervoltage and overvoltage conditions do not set the fault latch.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX8758. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which sets the fault latch and shuts down all the outputs, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage or toggle $\overline{SHDN}$ to clear the fault latch and restart the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Frequency Selection (FREQ)

The FREQ pin selects the switching frequency. Table 3 shows the switching frequency based on the FREQ connection. High-frequency (1.2MHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (600kHz) operation offers the best overall efficiency at the expense of component size and board space.

Table 3. Frequency Selection

FREQ	SWITCHING FREQUENCY (kHz)
GND	600
IN	1200

Operational Amplifier

The MAX8758's operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The operational amplifier features ±150mA output short-circuit current, 7.5V/µs slew rate, and 12MHz bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±150mA if the output is directly shorted to SUPB or to GND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled or $\overline{SHDN}$ is toggled.

Driving Pure Capacitive Load

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUTB and the capacitive load reduces peaking but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω and the typical value of the capacitor is 10pF.

High-Voltage Switch Control

The MAX8758's high-voltage switch-control block (Figure 5) consists of two high-voltage, p-channel MOSFETs: Q1, between SRC and GON and Q2, between GON and DRN. The switch-control block is enabled when V_{DLP} exceeds $V_{LDO}/2$ and then Q1 and Q2 are controlled by CTL and MODE. There are two different modes of operation (see the *Typical Operating Characteristics* section.)

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Activate the first mode by connecting MODE to LDO. When CTL is logic high, Q1 turns on and Q2 turns off, connecting GON to SRC. When CTL is logic low, Q1 turns off and Q2 turns on, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and PGND or AV_{DD}. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

When V_{MODE} is less than 0.9 x V_{LDO}, the switch control block works in the second mode. The rising edge of V_{CTL} turns on Q1 and turns off Q2, connecting GON to SRC. An internal n-channel MOSFET Q3 between MODE and GND is also turned on to discharge an external capacitor between MODE and GND. The falling edge of V_{CTL} turns off Q3, and an internal 50µA current source starts charging the MODE capacitor. Once V_{MODE} exceeds 0.5 x V_{REF}, the switch control block turns off Q1 and turns on Q2, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and GND or AV_{DD}. Q2 turns off and stops discharging GON when V_{GON} reaches 10 times the voltage on THR.

The timing of enabling the switch control block can be adjusted with an external capacitor connected between DLP and GND. An internal current source starts charging the DLP capacitor if the input voltage is above 1.75V (typ), $\overline{SHDN}$ is high, and the fault latch is not set. The voltage on DLP linearly rises because of the constant-charging current. When VDLP goes above 2.5V (typ), the switch control block is enabled. The switch control block is disabled and DLP is held low when the MAX8758 is shut down or in a fault state.

Linear Regulator (LDO)

The MAX8758 includes an internal 5V linear regulator. OUT is the input of the linear regulator and should be directly connected to the output of the step-up regulator. The input voltage range is between 4.5V and 13V. The output of the linear regulator (LDO) is set to 5V (typ). The regulator powers all the internal circuitry including the gate driver. This feature significantly improves the efficiency at low input voltages. Bypass the LDO pin to GND with a 0.22µF or greater ceramic capacitor.

Design Procedure

Step-Up Regulator

Step-Up Regulator Inductor Selection

The inductance value, peak-current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and, therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

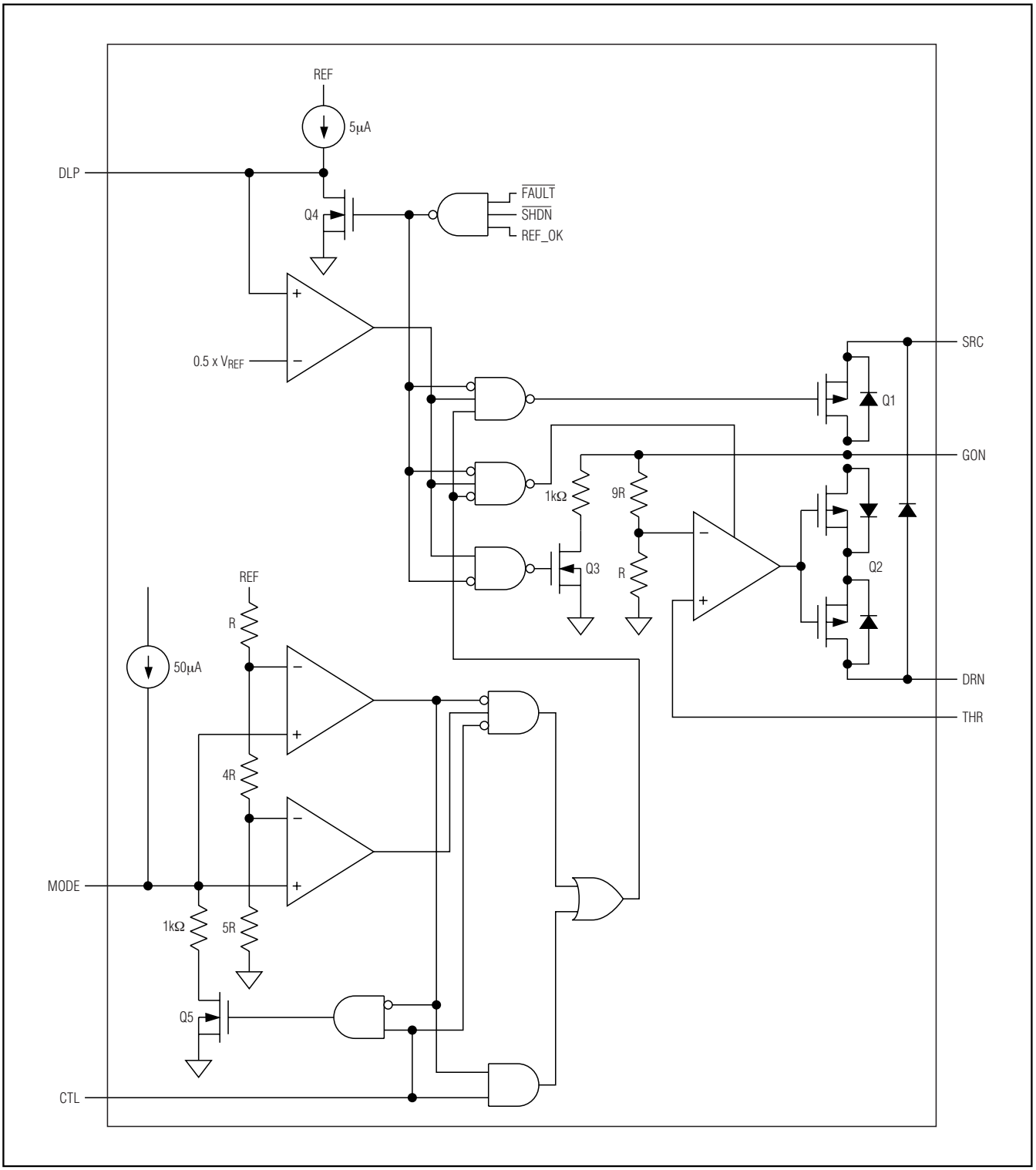


Figure 4. Switch Control

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

In Figure 1's *Typical Operating Circuit*, the LCD's gate-on and gate-off voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance calculation. The effective maximum output current $I_{MAIN(EFF)}$ becomes the sum of the maximum load current on the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{NEG} \times I_{NEG} + (n_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum output current, n_{NEG} is the number of negative charge-pump stages, n_{POS} is the number of positive charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current, assuming the pump source for I_{POS} is V_{MAIN}.

The required inductance can then be calculated as follows:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \times \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right) \times \left(\frac{\eta_{TYP}}{LIR}\right)$$

where V_{IN} is the typical input voltage and η_{TYP} is the expected efficiency obtained from the appropriate curve in the *Typical Operating Characteristics.*

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the guaranteed minimum value of the MAX8758's LX current limit (I_{LIM}) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the *Typical Operating Circuit*, the maximum load current ($I_{MAIN(MAX)}$) is 300mA for the step-up regulator, 20mA for the two-stage positive charge pump, and 20mA for the one-stage negative charge pump. Altogether, the effective maximum output current, $I_{MAIN(EFF)}$ is 360mA with an 8.5V output and a typical input voltage of 3.3V. The switching frequency is set to 1.2MHz. Choosing an LIR of 0.4 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{3.3V}{8.5V}\right)^2 \times \left(\frac{8.5V - 3.3V}{0.36A \times 1.2MHz}\right) \times \left(\frac{0.85}{0.4}\right) \approx 4.2\mu H$$

Using the circuit's minimum input voltage (3V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.36A \times 8.5V}{3V \times 0.8} \approx 1.28A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{3V \times (8.5V - 3V)}{4.2\mu H \times 8.5V \times 1.2MHz} \approx 0.4A$$

$$I_{PEAK} = 1.28A + \frac{0.4A}{2} \approx 1.48A$$

The peak-inductor current does not exceed the guaranteed minimum value of the LX current limit in the *Electrical Characteristics* table.

Step-Up Regulator Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{ARIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{MAIN}} \times \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{SW}}\right)$$

and

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times R_{ESR}$$

where I_{PEAK} is the peak inductor current (see the *Step-Up Regulator Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Step-Up Regulator Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the *Typical Applications Circuit* (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in the *Typical Applications Circuit*.

Step-Up Regulator Rectifier Diode

The MAX8758's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Step-Up Regulator Output Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{OUT}) to GND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.25V. Place R1 and R2 close to the IC.

Step-Up Regulator Loop Compensation

Choose R_{COMP} (R3 in Figure 1) to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} (C7 in Figure 1) to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{315 \times V_{IN} \times V_{MAIN} \times C_{MAIN}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{MAIN} \times C_{MAIN}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Place C_{COMP2} (C8 in Figure 1) from COMP to GND to add an additional high-frequency pole. Use C_{COMP2} between 10pF and 47pF.

Step-Up Regulator Soft-Start Capacitor

The soft-start capacitor should be large enough that it does not reach final value before the output has reached regulation. Calculate the soft-start capacitor (C_{SS}) value using:

$$C_{SS} = 21 \times 10^{-6} \times C_{MAIN} \times \left(\frac{V^2_{MAIN} - V_{IN} \times V_{MAIN}}{V_{IN} \times I_{INRUSH} - I_{MAIN} \times V_{MAIN}}\right)$$

where C_{MAIN} is the total output capacitance, V_{MAIN} is the maximum output voltage, and I_{INRUSH} is the peak inrush current allowed, I_{MAIN} is the maximum output current, and V_{IN} is the minimum input voltage.

The load must wait for the soft-start cycle to finish before drawing a significant amount of load current. The duration after which the load can begin to draw maximum load current is:

$$t_{MAX} = 6.77 \times 10^5 \times C_{SS}$$

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output voltage requirement.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GON} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

where n_{POS} is the number of positive-charge-pump stages, V_{GON} is the positive-charge-pump output, V_{MAIN} is the main step-up regulator output, and V_D is the forward voltage drop of the charge-pump diode.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF}}{V_{MAIN} - 2 \times V_D}$$

where n_{NEG} is the number of negative-charge-pump stages, V_{GOFF} is the negative charge-pump output, V_{MAIN} is the main step-up regulator output, and V_D is the forward voltage drop of the charge-pump diode.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Charge-Pump Flying Capacitors

Increasing the flying capacitor (C6, C17, C18) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the diode impedance places a lower limit on the source impedance. Ceramic capacitors of 0.1µF or greater work well in most applications that require output currents in the order of 10mA to 20mA.

The flying capacitor's voltage rating must exceed the following:

$$V_C > n \times V_{MAIN}$$

where n is the stage number in which the flying capacitor appears, and V_{MAIN} is the output voltage of the main step-up regulator.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output voltage ripple and the peak-to-peak voltage during load transients. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{MAIN\_CP} \geq \frac{I_{LOAD\_CP}}{2 \times f_{OSC} \times V_{RIPPLE\_CP}}$$

where C_{MAIN_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

The charge-pump output capacitor is typically also the input capacitor for a linear regulator. Often, its value must be increased to maintain the linear regulator's stability.

Charge-Pump Rectifier Diodes

Use low-cost, silicon-switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with equivalent current ratings.

PC Board Layout and Grounding

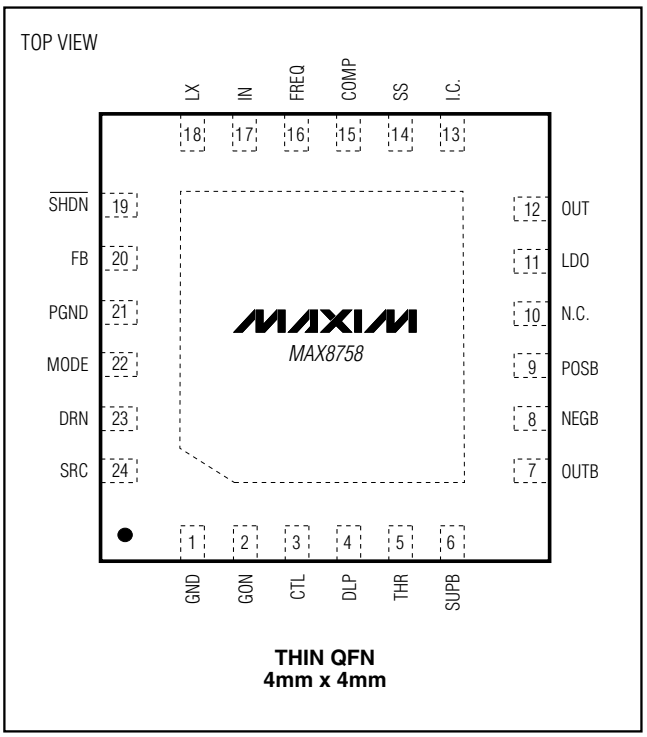
Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of high-current loops by placing the step-up regulator's inductor, diode, and output capacitors near its input capacitors, its LX, and PGND pin. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create a power ground island (PGND) for the step-up regulator, consisting of the input and output capacitor grounds and the PGND pin. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (GND) consisting of the GND pin, the feedback-divider ground connection, the COMP and DLP capacitor ground connections, and the device's exposed backside pad. Connect the PGND and GND islands by connecting the two ground pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
3) Place the feedback voltage-divider resistors as close to the feedback pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become antennas that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX.
4) Place the IN pin bypass capacitor as close to the device as possible. The ground connection of the IN bypass capacitor should be connected directly to the GND pin with a wide trace.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback node (FB) and analog ground. Use DC traces as shield if necessary.

Refer to the MAX8758 evaluation kit for an example of proper board layout.

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Pin Configuration



THIN QFN
4mm x 4mm

Chip Information

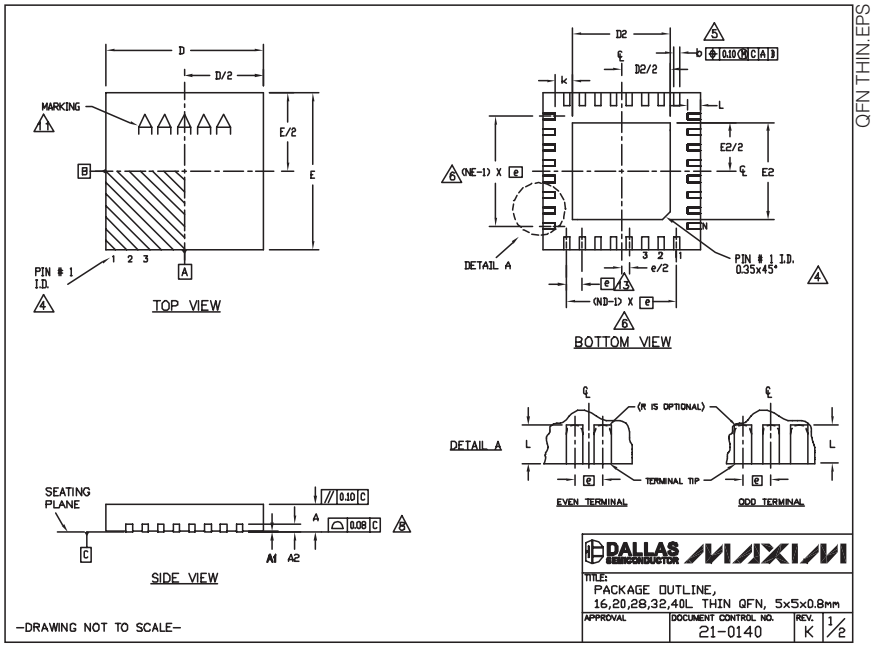
TRANSISTOR COUNT: 3208

PROCESS: BiCMOS

Step-Up Regulator with Switch Control and Operational Amplifier for TFT LCD

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1635-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. K
1/2
–DRAWING NOT TO SCALE–