19-2035; Rev 1; 11/02

MAXIM

150mA USB LDO Regulators with ±15kV TVS and µP Reset

General Description

The MAX5005/MAX5006/MAX5007 are low-dropout (LDO), micropower linear voltage regulators with an integrated microprocessor (µP) reset circuit for use with USB peripheral devices. Each device is available with a fixed +3.3V output voltage and can deliver up to 150mA load current. Each device features ±15kV transient voltage suppression (TVS) as well as precision 1.5kΩ data-line termination resistors for USB digital signals making them ideal for use with USB peripherals.

The MAX5005/MAX5006/MAX5007 include an internal reset circuit that enables the USB microcontroller 100ms after the LDO regulator output voltage reaches regulation. Reset outputs are available in push-pull (active-low or active-high) and open-drain (active-low) options.

The MAX5005/MAX5006/MAX5007 are optimized for use with a 1µF ceramic output capacitor. Each device includes thermal shutdown protection, output short-circuit protection, and output to input reverse leakage protection. These devices also include an active-low manual reset input.

The MAX5005 features an open-drain reset output, the MAX5006 features an active-low push-pull reset output, and the MAX5007 features an active-high push-pull reset output. Each device is available in a space-saving 10-pin µMAX package.

Applications

USB Peripherals

Hand-Held Instruments

Features

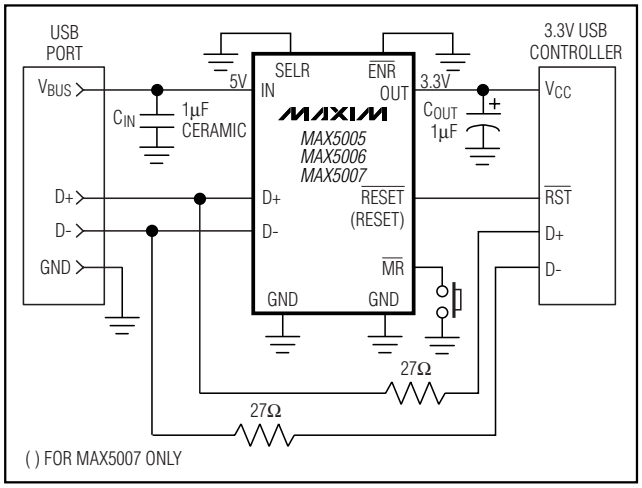
- ♦ **Integrated ±15kV Transient Voltage Suppressors for D+ and D- Data Lines**
- ♦ **Pin Selectable Internal D+ and D- Termination Resistors (1.5kΩ ±5%)**
- ♦ **Integrated Microprocessor Reset Circuit with 100ms (min) Timeout**
- ♦ **3.3V Output with ±3% Accuracy**
- ♦ **25µA Quiescent Current at Full Load**
- ♦ **Small 1µF Output Capacitor**
- ♦ **Output to Input Reverse Leakage Protection**
- ♦ **Thermal and Short-Circuit Protection**
- ♦ **10-Pin µMAX Package**

Ordering Information

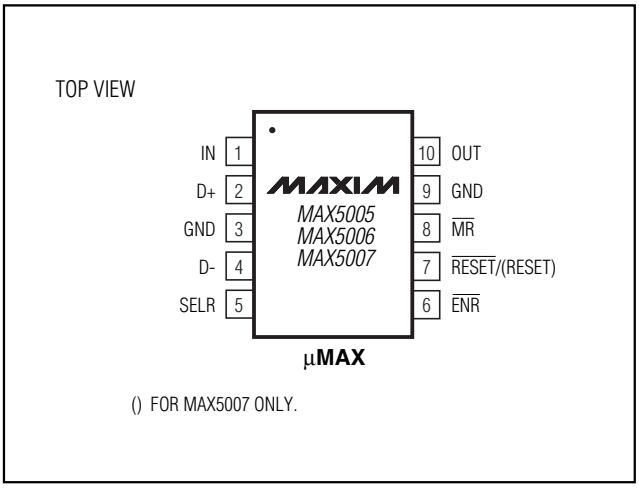
PART	TEMP RANGE	PIN-PACKAGE	RESET OUTPUT
MAX5005_CUB*	0°C to +70°C	10 µMAX	Open-Drain Low
MAX5006_CUB*	0°C to +70°C	10 µMAX	Push-Pull Low
MAX5007_CUB*	0°C to +70°C	10 µMAX	Push-Pull High

**Insert "A" for a 7.5% reset threshold and "B" for a 12.5% reset threshold.*

Typical Operating Circuit



Pin Configuration



150mA USB LDO Regulators with ±15kV TVS and µP Reset

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +6V
D+, D- to GND .....-0.3V to +6V
$\overline{MR}$ to GND .....-0.3V to (V_{OUT} + 0.3V)
RESET, $\overline{RESET}$ to GND, Push-Pull.....-0.3V to (V_{OUT} + 0.3V)
RESET to GND, Open-Drain.....-0.3V to +6V
OUT, SELR, $\overline{ENR}$ to GND .....-0.3V to +6V
Maximum Current to Any Pin
(except IN, OUT, D+, D-).....± 20mA

Short-Circuit Duration .....Indefinite
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Thermal Resistance (θ_{JA}).....180°C/W
Operating Temperature Range.....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2µF, T_A = 0°C to +70°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	I_{LOAD} = 100mA	4.0		5.5	V
Supply Current	I_{GND}	Measured at GND		25	50	µA
REGULATOR						
Guaranteed Output Current	I_{OUT}		150			mA
Output Voltage	V_{OUT}	V_{IN} = 4.0V to 5.5V, I_{OUT} = 0 to 100mA	3.2	3.3	3.4	V
Dropout Voltage (Note 2)	ΔV_{DO}	I_{LOAD} = 10mA		20	30	mV
		I_{LOAD} = 150mA		300	400	
Output Current Limit		V_{IN} = 5.5V	165	350		mA
Input Reverse Leakage Current		V_{IN} = 0, V_{OUT} = 5.5V		1		µA
Startup Response Time		Rising edge of V_{IN} to V_{OUT} R_L = 500Ω		500		µs
Thermal Shutdown Temperature	$T_{J\overline{SHDN}}$			160		°C
Thermal Shutdown Hysteresis	$\Delta T_{J\overline{SHDN}}$			20		°C
RESET CIRCUIT						
Reset Threshold (Note 3)	V_{TH}	MAX500_ACUB	2.92	3.05	3.18	V
		MAX500_BCUB	2.75	2.89	3.01	
Reset Timeout Period	t_{RP}		100	200	300	ms
V_{OUT} to Reset Delay	t_{RD}			75		µs
$\overline{MR}$ Input Voltage	V_{IL}				0.2 x V_{OUT}	V
	V_{IH}		0.8 x V_{OUT}			
$\overline{MR}$ Minimum Input Pulse Width			1			µs
$\overline{MR}$ Glitch Rejection				120		ns
$\overline{MR}$ to Reset Delay				500		ns
$\overline{MR}$ Pullup Resistance to OUT			10	25	45	kΩ
SELR Input Voltage	V_{IL}	Connects R_{TERM} to D-			0.2 x V_{OUT}	V
	V_{IH}	Connects R_{TERM} to D+	0.8 x V_{OUT}			

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2µF, T_A = 0°C to +70°C, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SELR Input Current		SELR = GND or OUT		-1		1	µA
$\overline{ENR}$ Input Voltage	V_{IL}	R_{TERM} enabled				0.2 x V_{OUT}	V
	V_{IH}	R_{TERM} disabled		0.8 x V_{OUT}			
$\overline{ENR}$ Input Current		$\overline{ENR}$ = GND or OUT		-1		1	µA
Open-Drain $\overline{RESET}$ Output Low Voltage (MAX5005)	V_{OL}	$V_{OUT} \geq$ 1.0V, I_{SINK} = 50µA, reset asserted				0.3	V
		$V_{OUT} \geq$ 2.7V, I_{SINK} = 3.2mA, reset asserted				0.4	
Open-Drain Reset Output Leakage Current (MAX5005)	I_{LKG}	Reset not asserted		-1.0		1.0	µA
Push-Pull $\overline{RESET}$ Output Voltage (MAX5006)	V_{OL}	V_{OUT} = 1.0V, I_{SINK} = 50µA, reset asserted				0.3	V
		$V_{OUT} > V_{TH(MIN)}$, I_{SINK} = 3.2mA, reset asserted				0.4	
	V_{OH}	$V_{OUT} > V_{TH(MAX)}$, I_{SOURCE} = 500µA, reset not asserted		0.8 x V_{OUT}			
Push-Pull RESET Output Voltage (MAX5007)	V_{OL}	$V_{OUT} > V_{TH(MAX)}$, I_{SINK} = 3.2mA, reset not asserted				0.4	V
	V_{OH}	V_{OUT} = 1.0V, I_{SOURCE} = 150µA, reset asserted		0.8 x V_{OUT}			
USB OPTIONS AND TRANSIENT SUPPRESSION							
D+/D- R_{TERM} Impedance		$\overline{ENR}$ = GND, SELR = GND or OUT		1425	1500	1575	Ω
D+/D- Input Leakage Current		$V_{\overline{ENR}} = V_{OUT}$ = 3.3V		-1		1	µA
D+ to D- Capacitance		1MHz, 100mVp-p signal applied at D+ and D-, V_{OUT} = 3.3V	$\overline{ENR}$ = OUT		5.5		pF
			Unpowered		24		
D+, D- Capacitance to GND		1MHz, 100mVp-p signal applied at D+ and D-, V_{OUT} = 3.3V	$\overline{ENR}$ = OUT		40		pF
			Unpowered		47		
ESD Trigger Voltage		dV/dt ≤ 1V/ns, V_{D+} or V_{D-} > 3.6V		3.6	5		V
Surge Trigger Voltage		dV/dt ≤ 2V/µs, V_{D+} or V_{D-} > 3.6V		3.6	16		V
Clamping Voltage		6A, pulse width = 200ns to 40µs			16		V
Surge Current		16V, pulse width = 200ns to 40µs			±6		A
D+/D- to GND ESD		Human Body Model MIL-STD-883			±16		kV
		Contact Discharge IEC1000-4-2 (EN61000-4-2)			±8		
		Air Discharge IEC1000-4-2 (EN61000-4-2)			±15		

Note 1: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by characterization and not production tested.

Note 2: Dropout voltage is defined as V_{IN} - V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for V_{IN} = V_{OUT} + 1V.

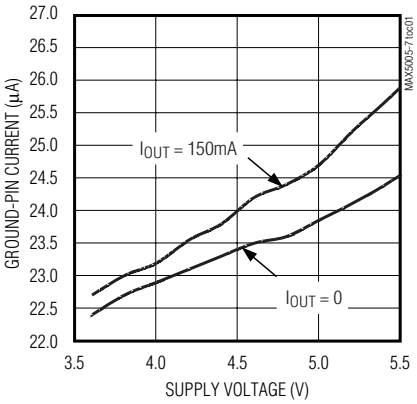
Note 3: Specification is guaranteed to ±4σ limit.

150mA USB LDO Regulators with ±15kV TVS and µP Reset

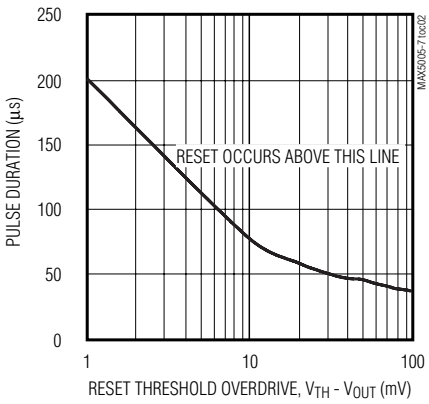
Typical Operating Characteristics

(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2µF, unless otherwise noted.)

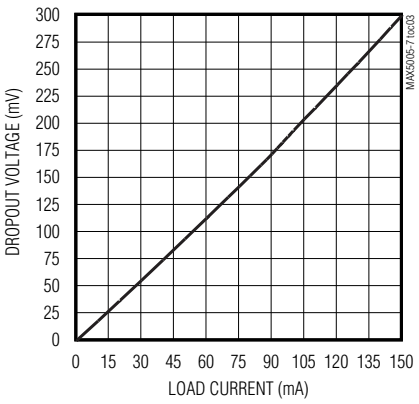
GROUND-PIN CURRENT vs. SUPPLY VOLTAGE



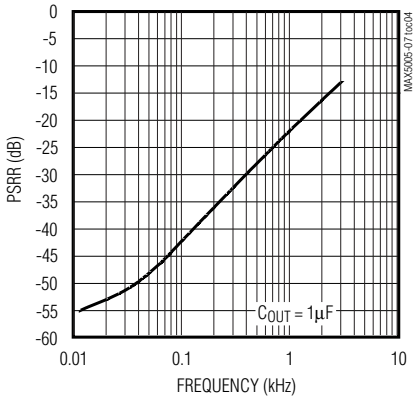
MAXIMUM PULSE DURATION vs. RESET THRESHOLD OVERDRIVE



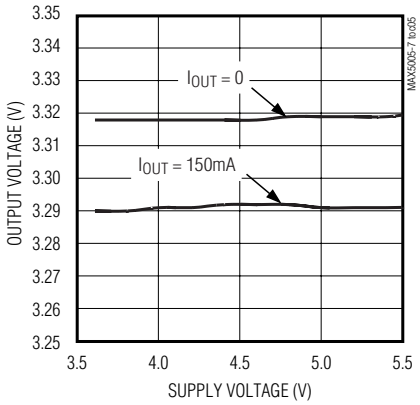
DROPOUT VOLTAGE vs. LOAD CURRENT



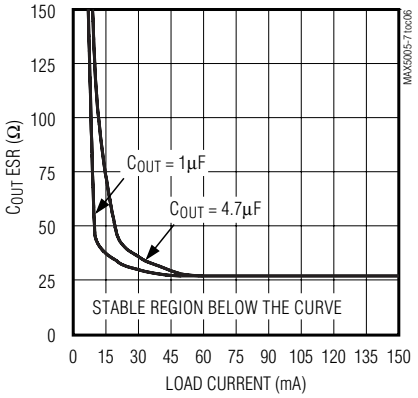
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



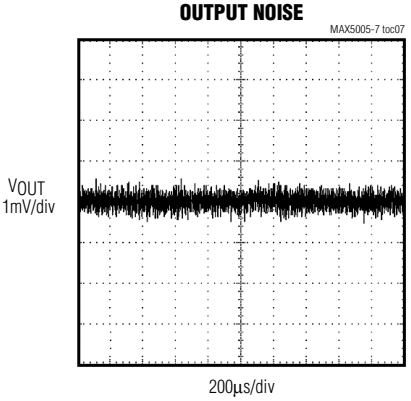
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



REGION OF STABLE C_{OUT} ESR vs. LOAD CURRENT



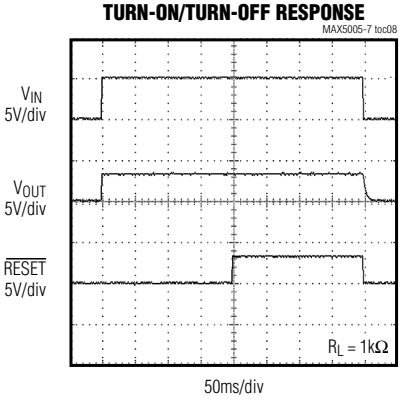
OUTPUT NOISE



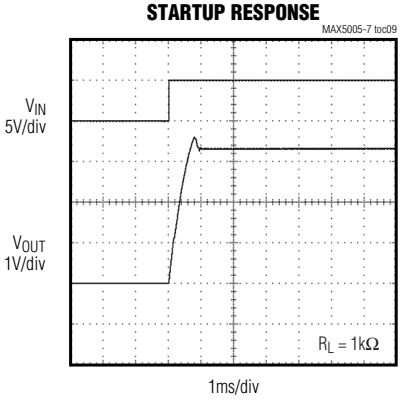
Typical Operating Characteristics (continued)

(V_{IN} = +5V, I_{OUT} = 0, C_{OUT} = 2.2µF, unless otherwise noted.)

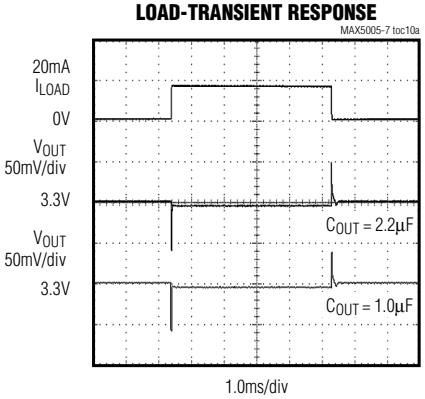
TURN-ON/TURN-OFF RESPONSE



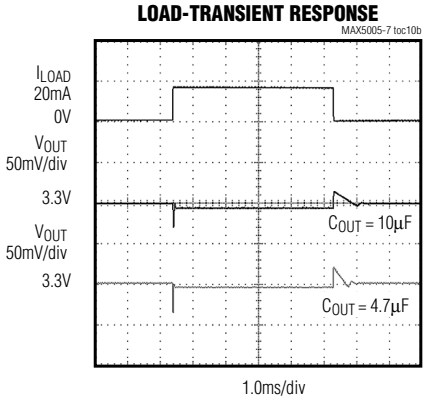
STARTUP RESPONSE



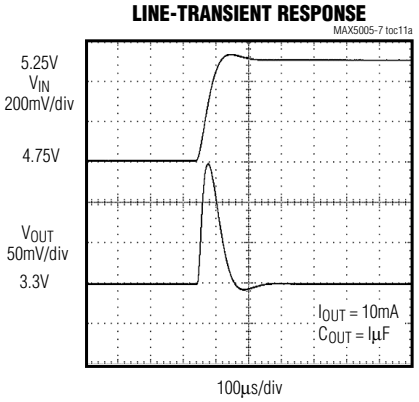
LOAD-TRANSIENT RESPONSE



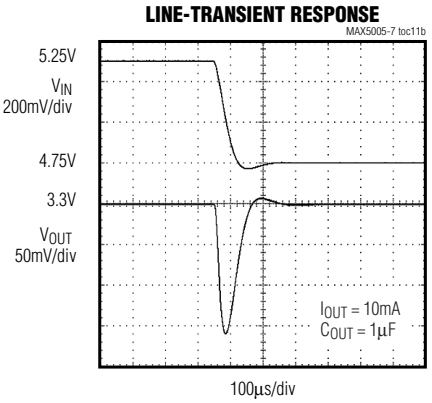
LOAD-TRANSIENT RESPONSE



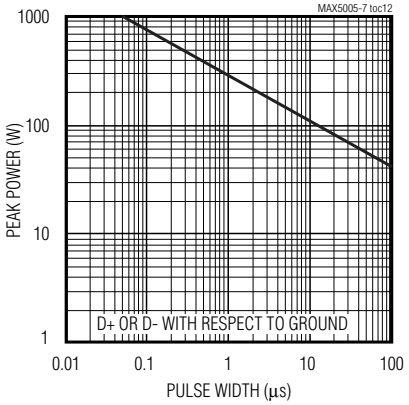
LINE-TRANSIENT RESPONSE



LINE-TRANSIENT RESPONSE



TVS PEAK POWER vs. PULSE WIDTH



150mA USB LDO Regulators with ±15kV TVS and µP Reset

Pin Description

PIN	NAME	DESCRIPTION
1	IN	Regulator Input. Supply voltage ranges from +4.0V to +5.5V. Bypass with a 1µF ceramic capacitor to ground.
2	D+	D+ ESD/Transient Suppression Input. Connect directly to USB port D+ data input. SELR high and $\overline{ENR}$ low connects D+ to OUT through a 1.5kΩ resistor.
3, 9	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
4	D-	D- ESD/Transient Suppression Input. Connect directly to USB port D- data input. SELR low and $\overline{ENR}$ low connects D- to OUT through a 1.5kΩ resistor.
5	SELR	USB Full-Speed/Low-Speed Termination Resistor Select. Logic high connects the termination resistor to D+ for full-speed peripherals. Logic low connects the termination resistor to D- for low-speed peripherals. An internal 1.5kΩ resistor connects to OUT when $\overline{ENR}$ is low.
6	$\overline{ENR}$	USB Termination Resistor Enable. When reset is not asserted, $\overline{ENR}$ low enables the termination resistor connection. $\overline{ENR}$ high or a reset disables the termination resistor connection.
7	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low while V_{OUT} is below the reset threshold or while $\overline{MR}$ is held low. $\overline{RESET}$ remains low for the duration of the reset timeout period after the reset conditions are terminated. **(MAX5005/MAX5006 ONLY)**
	RESET	Active-High Reset Output. RESET remains high while V_{OUT} is below the reset threshold or while $\overline{MR}$ is held low. RESET remains high for the duration of the reset timeout period after the reset conditions are terminated. **(MAX5007 ONLY)**
8	$\overline{MR}$	Active-Low Manual Reset Input. A logic low forces a reset. Reset remains asserted for the duration of the reset timeout period after $\overline{MR}$ transitions from low to high. Leave unconnected or connect to OUT if not used. $\overline{MR}$ has an internal pullup resistor of 25kΩ to OUT.
10	OUT	Voltage Regulator Output. Fixed +3.3V. Sources up to 150mA. Bypass with a 1µF (min) capacitor for full rated performance.

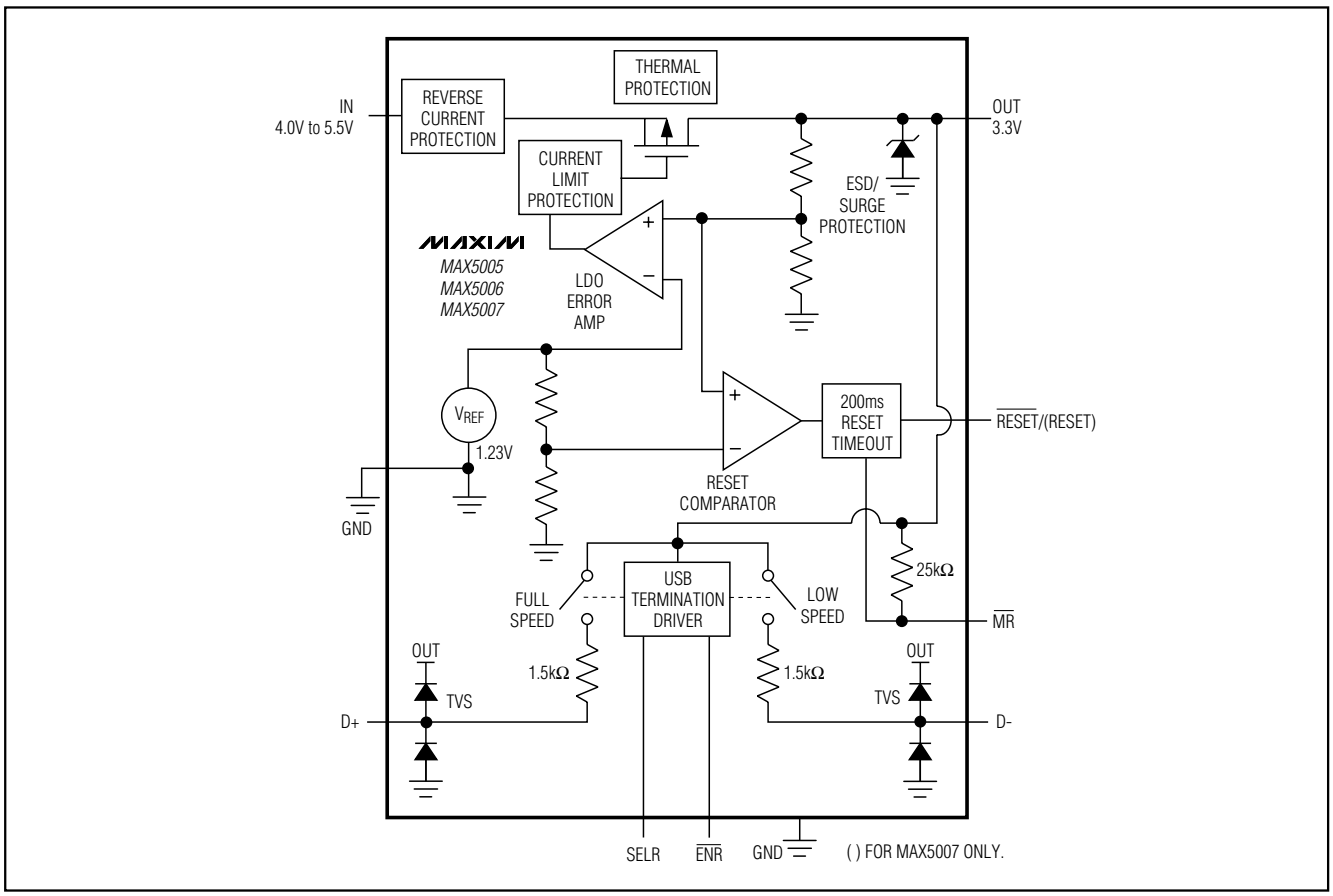


Figure 1. Functional Diagram

Detailed Description

The MAX5005/MAX5006/MAX5007 are USB application-specific, low-dropout, low-quiescent current linear regulators with an integrated µP reset circuit (see Figure 1). The devices drive loads up to 150mA and are available with a fixed output voltage of +3.3V. Features include 1.5kΩ D+ and D- termination resistors and ±15kV transient voltage suppression (TVS) in accordance with IEC1000-4-2 (EN61000-4-2) Air Discharge Method and MILSTD883C- Method 3015-6 making the MAX5005/MAX5006/MAX5007 ideal for use with USB peripheral devices. The internal reset circuit monitors the regulator output voltage and asserts a reset signal when the output is typically -7.5% out of regulation for MAX500_ACUB and -12.5% out of regulation for MAX500_BCUB.

Reset Circuit

The reset supervisor circuit is fully integrated in the MAX5005/MAX5006/MAX5007, and uses the same reference voltage as the regulator. Two supply tolerance reset thresholds, typically -7.5% and -12.5%, are available for each type of device.

7.5% reset: Reset does not assert until the regulator output voltage is at least -3.6% out of tolerance and always asserts before the regulator output voltage is -11.5% out of tolerance.

12.5% reset: Reset does not assert until the regulator output voltage is at least -8.8% out of tolerance and always asserts before the regulator output voltage is -16.7% out of tolerance.

Reset Output

The MAX5005/MAX5006/MAX5007 µP supervisory circuits assert a reset during power-up, power-down, and

150mA USB LDO Regulators with ±15kV TVS and µP Reset

brownout conditions. Reset is guaranteed to be logic high or low depending on the device chosen (see *Ordering Information*). RESET or $\overline{RESET}$ asserts when V_{OUT} is below the reset threshold and remains asserted for at least 100ms minimum after V_{OUT} rises above the reset threshold. RESET or $\overline{RESET}$ also asserts when $\overline{MR}$ is pulled low.

SELR and $\overline{ENR}$

When reset is not asserted a logic high to SELR connects a 1.5kΩ termination resistor from D+ to OUT for full speed USB peripherals and a logic low connects a 1.5kΩ termination resistor from D- to OUT for low-speed peripherals. Logic low on $\overline{ENR}$ enables the selected termination resistor connection and logic high disables the selected termination resistor connection. An asserted reset always disconnects the termination resistors.

D+ and D-

D+ and D- include transient voltage suppressors rated at ±15kV (see *USB ±15kV Transient Voltage Suppression* section).

The proprietary TVS shunt circuit passes no data through the MAX5005/MAX5006/MAX5007, thereby eliminating delays associated with series protection circuits. D+ and D- have only 1µA of leakage current and a typical input capacitance of 40pF at 1MHz.

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts a reset while the regulator output voltage is still within tolerance.

Reset remains asserted while $\overline{MR}$ is low and for the reset timeout period (100ms minimum) after $\overline{MR}$ returns high. The $\overline{MR}$ input has an internal pullup of 25kΩ (typ) to OUT. Drive this input with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity. For proper operation, ensure that the voltage on $\overline{MR}$ is not greater than a diode drop above V_{OUT}.

Output to Input Reverse Leakage Protection

An internal circuit monitors the input and output voltages. When the output voltage is greater than the input voltage, the internal pass transistor and parasitic diodes turn off, and OUT powers the device. There is no leakage path from OUT to IN. Therefore, the output can be powered from an auxiliary supply such as a backup battery without any need for additional blocking diodes.

Current Limit

The MAX5005/MAX5006/MAX5007 include a current limiter that monitors and controls the pass transistor's gate voltage, limiting the output current to 350mA (typ). For design purposes, consider the current limit to be 160mA (min) to 600mA (max). The output can be shorted to ground for an indefinite period without damaging the part.

Thermal Protection

When the junction temperature exceeds T_J = +160°C, an internal thermal sensor signals the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature decreases by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection is designed to protect the MAX5005/MAX5006/MAX5007 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

The MAX5005/MAX5006/MAX5007's maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / (\Theta_{JA})$$

where $T_J - T_A$ is the temperature difference between the die junction and the surrounding air, Θ_{JA} is the thermal resistance of the package from junction to ambient.

The MAX5005/MAX5006/MAX5007's ground pin (GND) performs the dual function of providing an electrical connection to the system ground and channeling heat away. Connect GND to the system ground using a large pad or ground plane. For optimum performance, minimize trace inductance to D+, D-, and GND.

Applications Information

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 150mA, use a 1µF (min) output capacitor. To reduce noise and improve load transient response, stability, and power-supply rejection, use large output capacitor values such as 10µF.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use 2.2µF or more to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1µF should be sufficient at all operating temperatures. Also, for high-ESR tantalum capacitors, 2.2µF or more may be needed to maintain stability. A graph of the Region of Stable C_{OUT} ESR vs. Load Current is shown in the *Typical Operating Characteristics*.

To improve power-supply rejection and transient response use a 1µF capacitor between IN and GND.

Negative-Going V_{OUT} Transients

These devices are relatively immune to short-duration, negative-going V_{OUT} transients. The *Typical Operating Characteristics* section shows a graph of the Maximum Pulse Duration vs. Reset Threshold Overdrive for which reset is not asserted. The graph was produced using negative going output transients starting at V_{OUT} and ending below the reset threshold by the magnitude indicated (Reset Threshold Overdrive). The graph shows the maximum pulse width that a negative going V_{OUT} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{OUT} transient that goes only 10mV below the reset threshold and lasts for 75µs will not trigger a reset pulse.

USB ±15kV Transient Voltage Suppression

The universal serial bus (USB) simplifies interconnectivity between peripheral devices and personal computers. USBs offer high-speed data communication rates (up to 12Mbps) using only two lines (D+ and D-). CMOS based USB peripherals that utilize deep submicron technologies are more susceptible to electrostatic discharge (ESD) failure due to shorter channel lengths, shallower drain/source junctions, and lightly doped drain structures. The MAX5005/MAX5006/MAX5007 incorporate a proprietary transient voltage suppression (TVS) circuit for use with submicron devices.

The TVS design complies with IEC-1000-4-2 level 4 (EN61000-4-2) ±15kV Air Discharge and ±8kV Contact Discharge as well as MIL STD 883C-Method 3015-6 level 3.

The TVS circuit handles up to 11A of surge current. The TVS/ESD structure is directly coupled to the output of the LDO regulator.

TVS Surge Test Information

Figure 2 shows the test circuit used to generate the 8/40µs short circuit waveform of Figure 3. Figures 4, 5, and 6 show the actual surge current I/V characteristics with various capacitive loads.

ESD Performance

The MAX5005/MAX5006/MAX5007 are characterized to the following limits on D+, D-, and IN:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge Method specified in IEC 1000-4-2 (EN61000-4-2)
- ±15kV using the Air-Gap Discharge Method specified in IEC 1000-4-2 (EN61000-4-2).

Note that in order to achieve the above ESD levels on IN, a ceramic 1µF ceramic capacitor should be connected from IN to GND.

ESD Test Conditions

ESD performance depends on several conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 7 shows the Human Body Model, and Figure 8 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

ESD Transmission Line Pulsing

Figure 9 shows the test circuit used for transmission line pulsing conditions. The 200ns pulsewidth has a rise time of 4ns. Figure 10 shows the Current vs. Voltage characteristics for various output capacitance values.

150mA USB LDO Regulators with ±15kV TVS and µP Reset

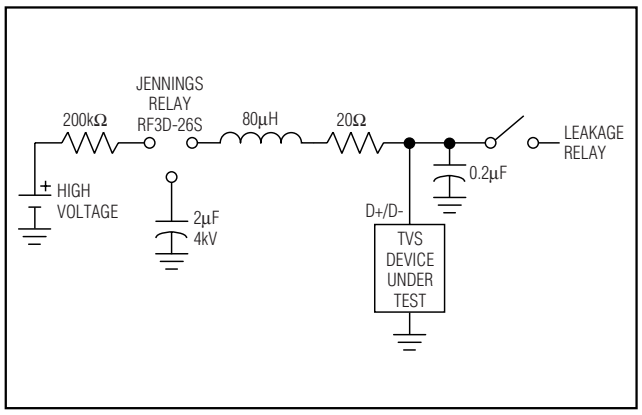


Figure 2. Surge Current Test Circut

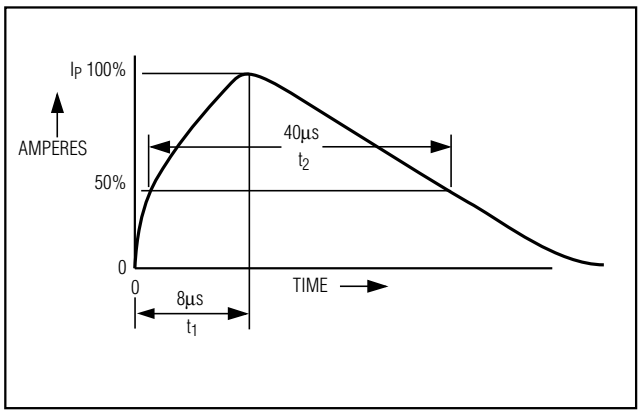


Figure 3. Test Circuit Surge Current Waveform (Short-Circuit Load)

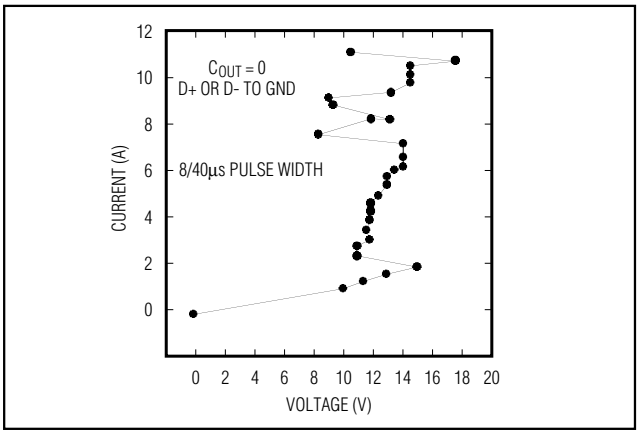


Figure 4. Surge Current I/V Characteristic (C_{OUT} = 0)

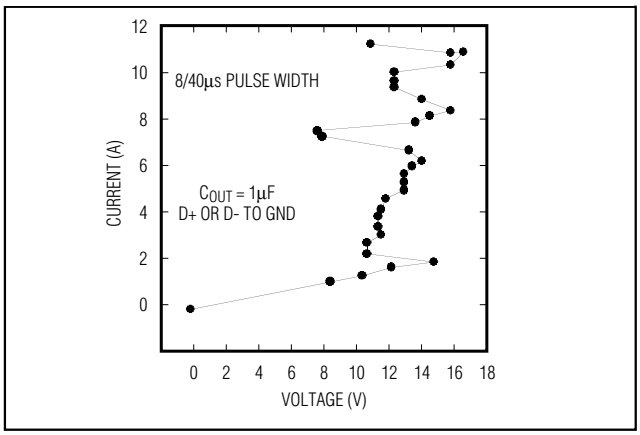


Figure 5. Surge Current I/V Characteristic (C_{OUT} = 1µF)

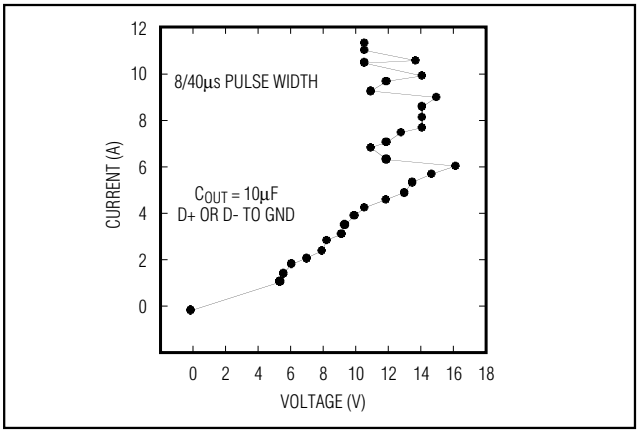


Figure 6. Surge Current I/V Characteristic (C_{OUT} = 10µF)

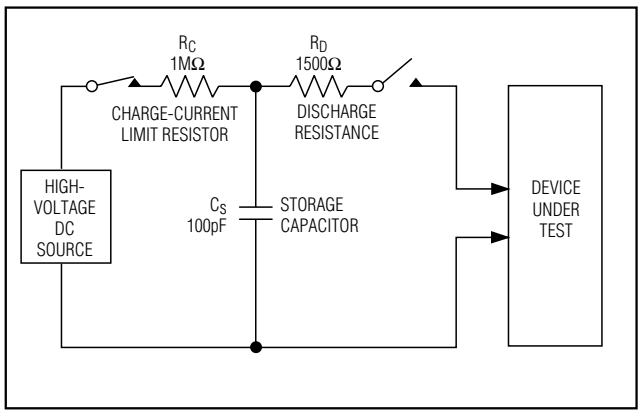


Figure 7. Human Body ESD Test Model

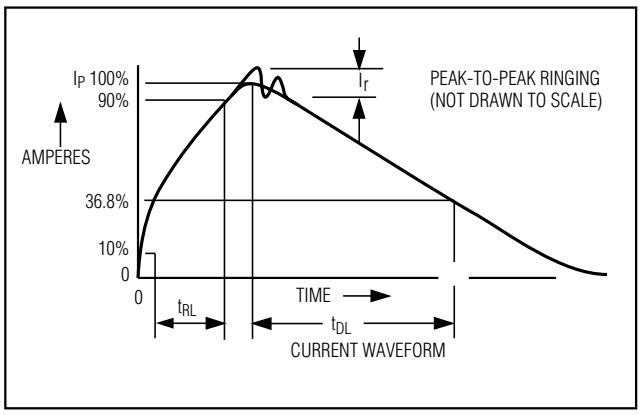


Figure 8. Human Body Model Current Waveform

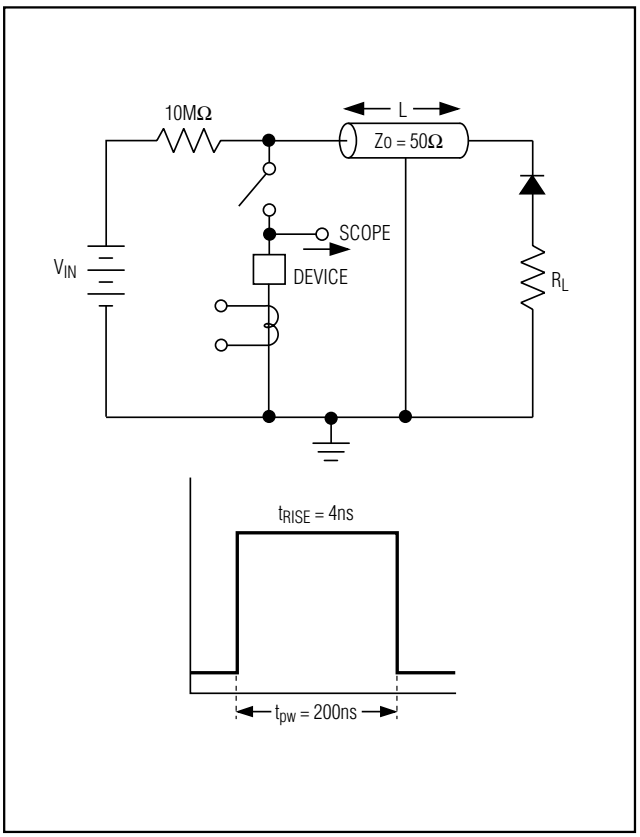


Figure 9. Transmission Line Pulsing Setup for ESD I/V Characteristics

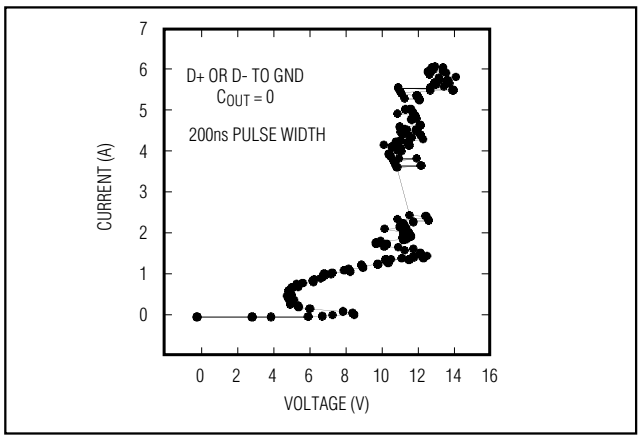


Figure 10. Transmission Line Pulsing I/V Characteristic (C_{OUT} = 0)

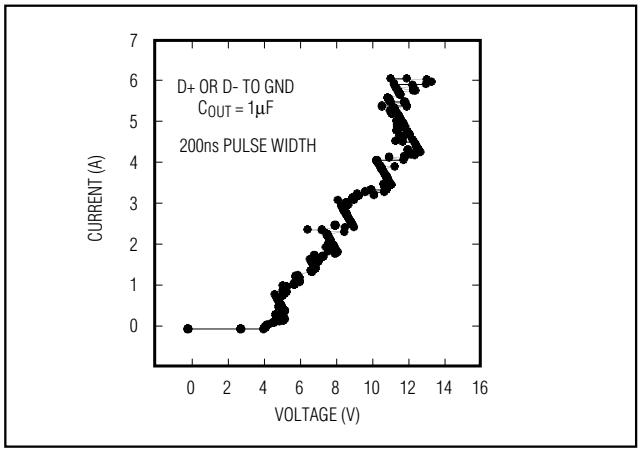


Figure 11. Transmission Line Pulsing I/V Characteristic (C_{OUT} = 1µF)

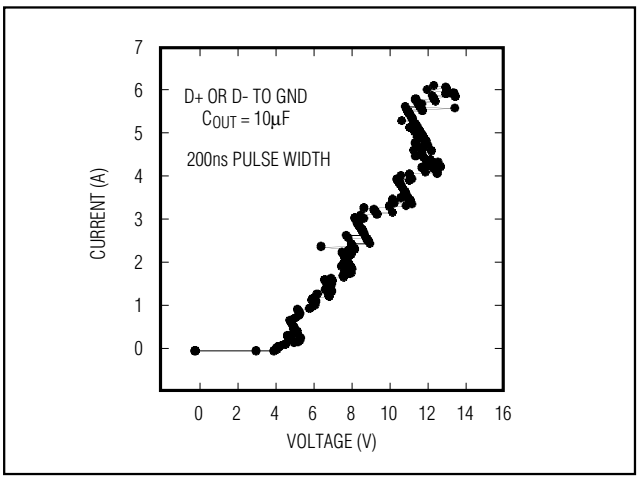


Figure 12. Transmission Line Pulsing I/V Characteristic (C_{OUT} = 10µF)

Chip Information

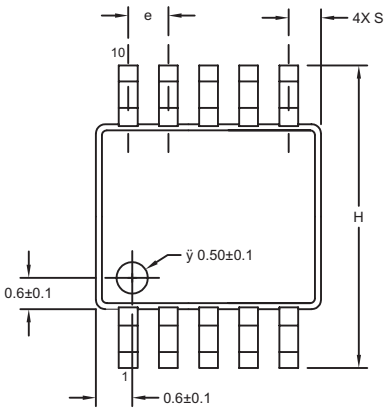
TRANSISTOR COUNT: 890

PROCESS: BiCMOS

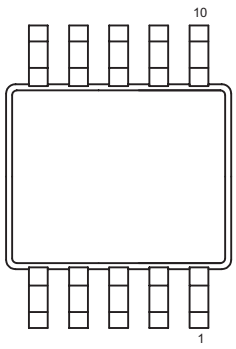
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

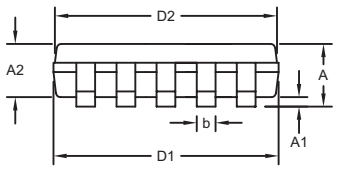


TOP VIEW

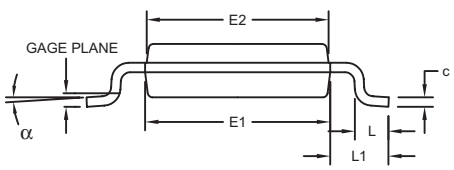


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1