# Winbond Bus Termination Regulator W83310DS/DG

#### W83310DS Datasheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		May/03	0.5	N.A.	All versions before 0.5 are only for internal use.
2	1	May/03	0.51	N.A.	Typo corrected.
3	5	May/03	0.60	N.A.	Electrical characteristics update.
4	5	Jul./03	0.61	N.A.	Electrical characteristics update.
5	10,11	Feb./04	0.70	N.A.	Package dimension outline and Thermal data.
6	11	Mar./04	0.71	N.A.	Thermal data update.
7	All	Sep./04	0.8	N.A.	Add Pb-free part W83310DG.
8	1	May/05	0.9	N.A.	Add DDR II support spec

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#### LIFE SUPPORT APPLICATIONS

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#### 1. General Description

The W83310DS/DG is a linear regulator provides a power achieves continuous 2.0Amp bi-directional sinking and driving capability for a high speed bus terminator application. The chip simply implements a stable power supply which tracks half of input power dynamically for bus terminator with a single chip; it's also can be fixed with the input of  $V_{REF1}$  and  $V_{REF2}$  pins following with setting of pin BOOT\_SEL. The W83310DS/DG is promoted with small footprint 8-SOP 150mil power package. With W83310DS/DG design, a high integration, high performance, and cost-effective solution is promoted.

#### 2. Features

- Regulates a bi-directional power with driving and sinking capability
- Provides achieve continuous 2.0Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- ❖ VCNTL Operates with +3.3V & 2.5 V power
- ❖ 8-SOP 150mil small power package
- Low cost and easy to use

#### 3. Applications

- DDR/DDRII Bus Termination Regulator
- Active Termination Bus
- ❖ Intel® Springdale GMCH-V<sub>TT</sub> Support
- ❖ SSTL-2
- ❖ SSTL-3



# 4. Pin Configuration and Description

#### - W83310DS/DG

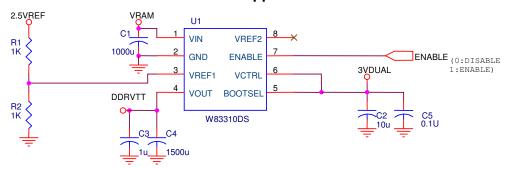


SYMBOL	PIN	FUNCTION			
V <sub>IN</sub>	1	Main power input pin.			
GND	2	Power ground.			
		Internal reference voltage source 1.			
$V_{REF1}$	3	Reference voltage on the pin will be referred with the value of pin BOOT_SEL set high.			
V <sub>OUT</sub> 4		Voltage output pin.			
BOOT_SEL	5	A signal for the chip reference voltage source selection. The function is designed for Intel® Springdale chipset GMCH_V <sub>TT</sub> application.			
$V_{CNTL}$	6	Power for internal control logic use			
ENABLE 7		Chip function enable pin. 1: Enable; 0: Disable			
V <sub>REF2</sub>	8	Internal reference voltage source 2.  Reference voltage of the pin will be referred with the value of pin BOOT_SEL set low.			

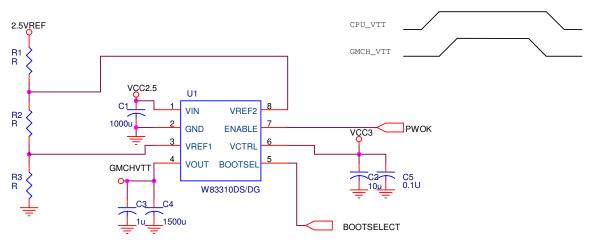


# 5. Application Circuit

#### - W83310DS/DG for DDR SDRAM Application



#### - W83310DS/DG for Intel® Springdale GMCH\_VTT Application



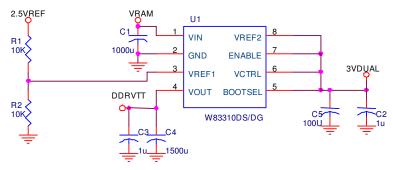
BOOTSELECT=0 GMCHVTT=1.45V for Intel® NORTHWOOD CPU BOOTSELECT=1 GMCHVTT=1.225V for Intel® PRESCOTT CPU

R1: R2: R3 = 4.66: 1.00: 5.44

Recommend resistor R1=23.2K  $\!\Omega$  , R2=4.99K  $\!\Omega$  , R3=27.4K  $\!\Omega$ 



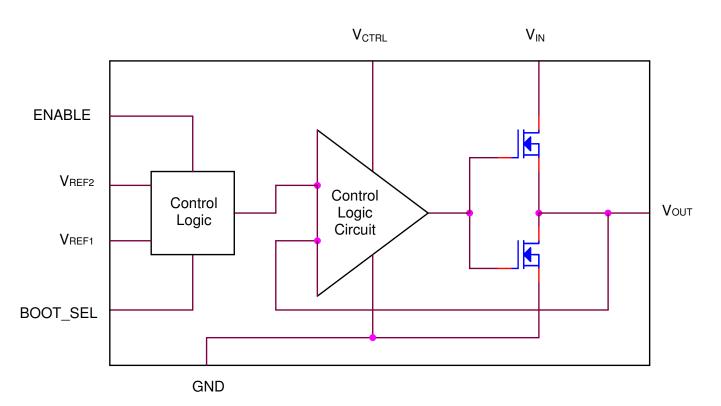
#### - Dual Layout of W83310DS/DG and W83310S-R2 for DDR $V_{TT}$ Application



W83310S-R2, W83310DS/DG

DUAL LAYOUT

# 6. Internal Block Diagram



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# 7. Electrical Characteristics AC CHARACTERISTICS

Cout=1000uF, T <sub>A</sub> = 0°C to +70°C							
Parameter	Symbol	Min	Тур	Max	Units	Test Conditions	
Output Offset Voltage	Vos	-5	0	+5	mV	lout=0A	
Load Pagulation			0.8		%	Loading: 0A→2.0A	
Load Regulation			0.8		70	Loading: 0A→-2.0A	
Innut Voltage Denge	VIN	1.62		3.63	V		
Input Voltage Range	VCNTL		3.3	3.63	V		
Operating Current of VCNTL	ICNTL		0.5	1	mA	No Load(Iout=0A)	
Short Current Limit	ILMT		4.0		Α		

Note: Load regulation is tested by using a 1ms current pulse and V<sub>OUT</sub> measuring.

Cout=1000uF, $T_A = 0$ °C to +70°C							
Parameter	Symbol	Min	Тур	Max	Units	Test Conditions	
Output Offset Voltage	Vos	-5	0	+5	mV	lout=0A	
Load Regulation			0.8		%	Loading: 0A→2.0A	
Load negulation			0.8		70	Loading: 0A→-2.0A	
Innut Voltage Bange	VIN	1.62		3.63	V		
Input Voltage Range	VCNTL		3.3	3.63	V		
Operating Current of VCNTL	ICNTL		0.5	1	mA	No Load(Iout=0A)	
VREF1 Threshold trigger		0.8			V	Output=High	
VNEFT Tilleshold (rigger				0.2	V	Output=Low	
POOT SEL Throphold Trigger		1			٧	BOOT_SEL=High	
BOOT_SEL Threshold Trigger				0.2	V	BOOT_SEL=Low	
Short Current Limit	ILMT		4.0		Α		

Note: Load regulation is tested by using a 1ms current pulse and V<sub>OUT</sub> measuring.

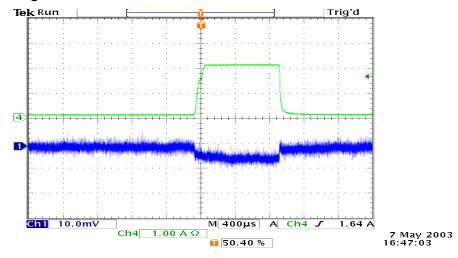
Cout=1000uF, $T_A = 0$ °C to +70°C							
Parameter	Symbol	Min	Тур	Max	Units	Test Conditions	
Output Offset Voltage	Vos	-5	0	+5	mV	lout=0A	
Load Regulation			0.8		%	Loading: 0A→2.0A	
Load negulation			0.8		70	Loading: 0A→-2.0A	
Input Voltage Range	VIN	1.62		3.63	V		
iliput voltage halige	VCNTL		3.3	3.63	V		
Operating Current of VCNTL	ICNTL		0.5	1	mA	No Load(Iout=0A)	
VREF2 Threshold trigger		0.8			V	Output=High	
VNEFZ Tillesilola (liggel				0.2	V	Output=Low	
POOT SEL Throshold Trigger		1			V	BOOT_SEL=High	
BOOT_SEL Threshold Trigger				0.2	V	BOOT_SEL=Low	
Short Current Limit	ILMT		4.0		Α		

Note: Load regulation is tested by using a 1ms current pulse and V<sub>OUT</sub> measuring.

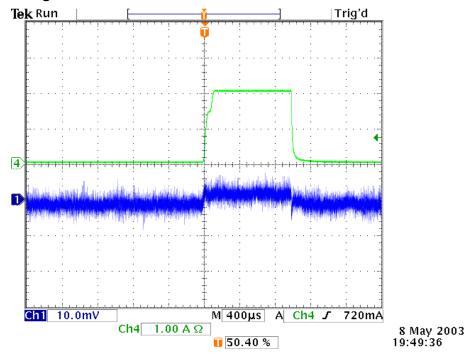


# 8. Typical Operating Waveform

Load regulation with test condition -  $V_{CTRL}$ =3.3V;  $V_{IN}$ =2.5V;  $V_{OUT}$ =1.225V; 2.0Amp pulse driving current.



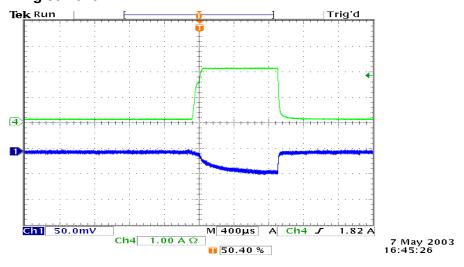
Load regulation with test condition -  $V_{CTRL}$ =3.3V;  $V_{IN}$ =2.5V;  $V_{OUT}$ =1.225V; 2.0Amp pulse sinking current.



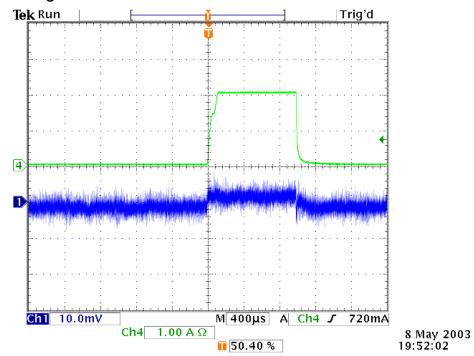
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Load regulation with test condition -  $V_{CTRL}$ =3.3V;  $V_{IN}$ =2.5V;  $V_{OUT}$ =1.45V; 2.0Amp pulse driving current.



Load regulation with test condition -  $V_{CTRL}$ =3.3V;  $V_{IN}$ =2.5V;  $V_{OUT}$ =1.45V; 2.0Amp pulse sinking current.

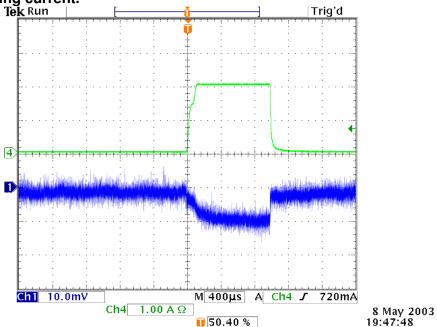


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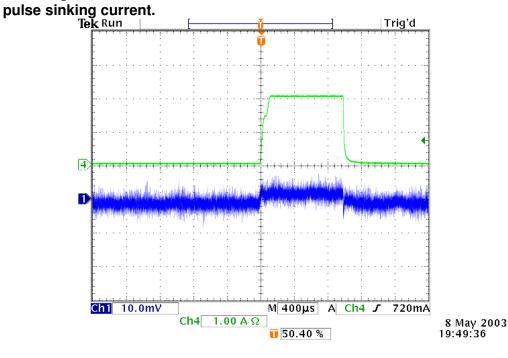


Load regulation with test condition - V<sub>CTRL</sub>=3.3V; V<sub>IN</sub>=2.5V; V<sub>OUT</sub>=1.25V; 2.0Amp pulse driving current.

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Load regulation with test condition - V<sub>CTRL</sub>=3.3V; V<sub>IN</sub>=2.5V; V<sub>OUT</sub>=1.25V; 2.0Amp

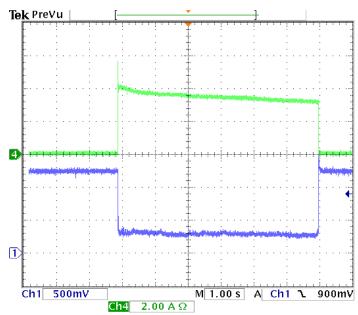


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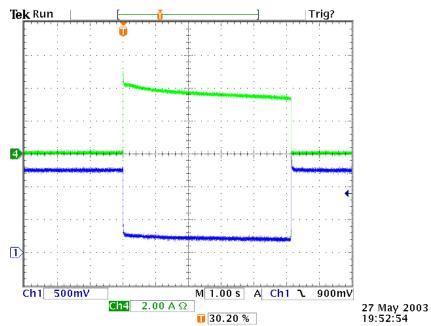
#### **Short Current Limit**

#### $-V_{CTRL} = 3.3V$



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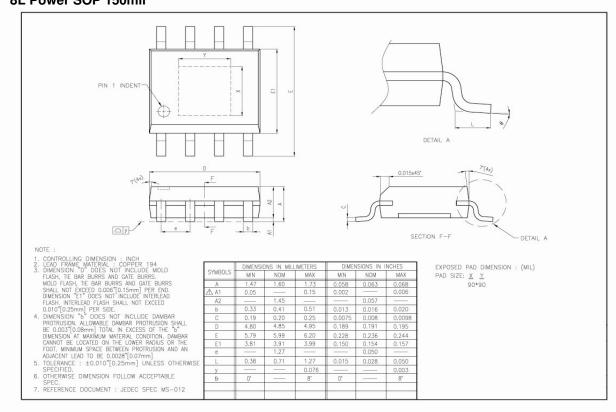
#### - $V_{CTRL} = 3.6V$



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#### 9. Package Dimension 8L Power SOP 150mil



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#### 10. Thermal Performance

Test on Four-Layer (2S2P) JEDEC Test Board									
Package	Package Power (W) Component Temp. (°C)								
1 dokage	i ower (w)	Package	Die	Downset	Lead	Ambient	(°C /W)		
PSOP-8	3.05	100	145	79	78	25	14.7		

An area of 190mil\*150mil on the top layer is use as a thermal pad for W83310DS and this is connected to the bottom layer by vias. The  $\Theta$ ja of the W83310DS mounted on this demo board is about 39 °C /W.Assuming the Ta=25 °C and TJ=160 °C,the maximum power dissipation is calculated as: PD(max)=(160-25)/39=3.46W

#### 11. Ordering Information

Part Number	Package Type	Production Flow		
W83310DS	Power SOP-8			

#### 12. How to Read the Top Marking





Left line: Winbond logo

1<sup>st</sup> & 2<sup>nd</sup> line: W83310DS/DG – the part number

3rd line: Tracking code 318 G A

318: packages assembled in Year 03', week 18

**G**: assembly house ID; O means OSE, G means GR, etc.

A: the IC version





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