

LNB Supply and Control-Voltage Regulators

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: November 1, 2010

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact your local Allegro Sales Representative.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

LNB SUPPLY AND CONTROL-VOLTAGE REGULATORS

Intended for analog and digital satellite receivers, these low-noise block converter regulators (LNBRs) are monolithic linear and switching voltage regulators specifically designed to provide the power and interface signals to the LNB down converter via the coaxial cable. If the device is in standby mode (EN terminal low), the regulator output is disabled, allowing the antenna down converters to be supplied or controlled by other satellite receivers sharing the same coaxial cable. In this mode, the device will limit the output reverse current.

The A8281SLB output is set to 13 or 18 V by the VSEL terminal. It is supplied in a 16-lead SOIC package with internally-fused leads for enhanced thermal dissipation. The fused leads are at ground potential and need no electrical isolation.

The A8282SLB output is set to 12, 13, 18, or 20 V by the VSEL terminals. Additionally, it is possible to increase the selected voltage by 1 V to compensate for the voltage drop in the coaxial cable (LLC terminal high). It is supplied in a 24-lead SOIC package with internally-fused leads for enhanced thermal dissipation. The fused leads are at ground potential and need no electrical isolation The A8282SLB is an improved version of the A8283SLB, without a bypass switch. The lead (Pb) free version has 100 % matter tin leadframe plating.

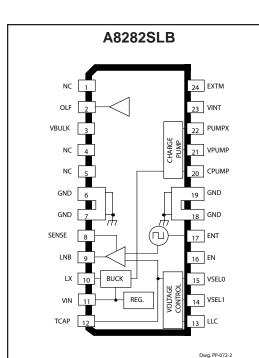
FEATURES

- LNB selection and standby function
- Built-in tone oscillator factory trimmed to 22 kHz, facilitates DiSEqCTM (a trademark of EUTELSAT) encoding
- Tracking switch-mode power converter for lowest dissipation
- Externally adjustable short-circuit protection
- LNB short-circuit protection and diagnostics
- Auxiliary modulation input
- Internal over-temperature protection
- Reverse-current protection
- Cable length compensation (A8282SLB only)

These devices incorporate features that have patents pending. Always order by the following complete part number.

Part Numbe	r Pb-Free	Package	Packing*
A8281SLB	TR –	16-pin SOICW	1000 pieces/13-in. reel
A8282SLB	TR –	24-pin SOICW	1000 pieces/13-in. reel
A8282SLB	TR-T Yes	24-pin SOICW	1000 pieces/13-in. reel

*Contact Allegro for additional packing options.



ABSOLUTE MAXIMUM RATINGS at $T_A = +25$ °C

Supply Voltage, V _{IN} 47 V
Output Current, I_{LNB} Internally Limited
Output Voltage Range, V_{LNB} 1 V to +22 V
Logic Input Voltage Range,

 T_A -20°C to +85°C Junction Temperature, T_J +150°C Storage Temperature Range,

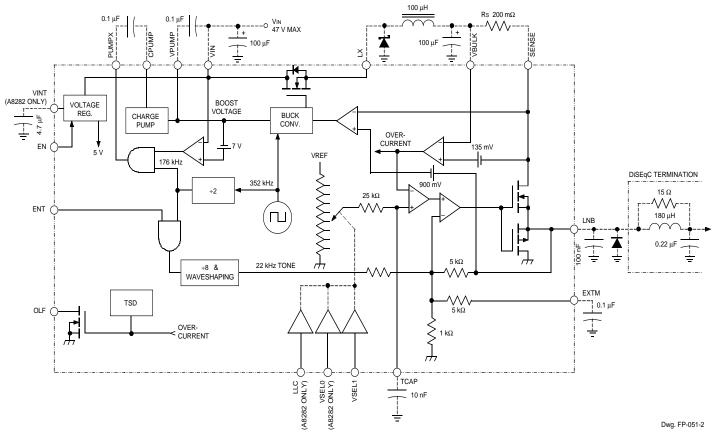
 T_S -55°C to +150°C



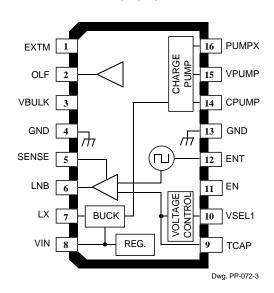


FUNCTIONAL BLOCK DIAGRAM

and typical application



A8281SLB



A8281SLB Output Voltage Select Table

VSEL1	V_{LNB}	
L	13 V	
Н	18 V	

A8282SLB Output Voltage Select Table

VSEL0	VSEL1	LLC	V_{LNB}
L	L	L	13 V
L	L	Н	14 V
L	Н	L	18 V
L	Н	Н	19 V
Н	L	L	12 V
Н	L	Н	13 V
Н	Н	L	20 V
н	Н	н	21 V

ELECTRICAL CHARACTERISTICS: unless otherwise noted at T $_J$ \leq 125°C, C $_{LNB}$ = 0.1 $\mu F,$ 4.5 V + V $_{LNB}$ \leq V $_{IN}$ \leq 47 V

			Limits			
Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Supply Voltage Range	V _{IN}	Operating	4.5+V _{LNB}	_	47	V
Output Voltage Error	E _{VLNB}	6 mA ≤ I _{LNB} ≤ 750 mA, ENT = L	_	0	±4.5	%
(reference Output Voltage Select table)		12 mA ≤ I _{LNB} ≤ 750 mA, ENT = H, average V _{LNB}		0	±4.5	%
Output Reverse Current	I _{RLNB}	EN = L, V_{LNB} = 22 V, V_{IN} = 22 V or floating	_	1	5	mA
Buck Switch On Resist.	r _{DS(on)}	$T_J = 25^{\circ}C$, $I_{LNB} = 750 \text{ mA}$	_	0.57	0.67	Ω
		$T_J = 125$ °C, $I_{LNB} = 750 \text{ mA}$	_	0.84	0.94	Ω
Buck Switch Current Limit	I _{BSM}		1	_	2.5	Α
Switching Frequency	f _O	16 x f _{tone}	320	352	384	kHz
Linear Reg. Volt. Drop	ΔV_{BUCK}	$V_{SENSE} - V_{LNB}$, ENT = L, I_{LNB} = 750 mA	700	900	1100	mV
Logic Input Voltage	V_{IL}		_	_	0.8	V
	V _{IH}		2	_	_	V
Logic Input Current	I _{IH}	V _{IH} = 5 V	_	<1.0	10	μΑ
Supply Current	I _{IN}	Outputs disabled (EN = L)	_	0.25	1	mA
		EN = H, I _{LNB} = 0	_	6	10	mA
Tone Characteristics						
Tone Frequency	f _{tone}	ENT = H	20	22	24	kHz
Tone Amplitude	V _{tone(PP)(ENT)}	ENT = H, 12 mA ≤ I _{LNB} ≤ 750 mA	400	650	900	mV
Tone Duty Cycle	dc _{tone}	ENT = H, 12 mA ≤ I _{LNB} ≤ 750 mA	40	_	60	%
Tone Rise or Fall Time	t _r , t _f	ENT = H, 12 mA ≤ I _{LNB} ≤ 750mA	5	10	15	μs
External Modulation Tone Amplitude	$V_{tone(PP)(EXTM)}$	f = 22 kHz square wave, I_{LOAD} = 12 mA to 450 mA, V_{IN} = 100mV to 125 mV; V_{PP} ac coupled	400	550	800	mV
External Modulation Input Voltage Range	V _{EXTM(PP)}	AC coupled	100	_	125	mV
External Modulation Input Impedance	Z _{EXTM}	f = 22 kHz	4		10	kΩ

continued next page

NOTES: 1. Typical data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

ELECTRICAL CHARACTERISTICS: unless otherwise noted at T $_J \leq$ 125°C, C $_{_{LNB}}$ = 0.1 $\mu\text{F},$ 4.5 V + V $_{_{LNB}} \leq$ V $_{_{IN}} \leq$ 47 V.

				Lin	nits	
Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Protection Circuitry	Protection Circuitry					
Current-Limiting Threshold	V _{ILNB(th)}	V _{BULK} - V _{SENSE}	115	135	155	mV
Overload Flag Output Low	V _{OLF}	I _{OLF} = 8 mA	_	0.28	0.5	V
Overload Flag Leakage Current	I _{OLF}	V _{OLF} = 5.5 V	_	<1.0	10	μΑ
Thermal Shutdown Temp.	T _J			165	_	°C
Thermal Shutdown Hysteresis	ΔT_J		_	20	_	°C

NOTES: 1. Typical data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Buck regulator. A current-mode buck converter provides the linear regulator a supply voltage that tracks the selected LNB output voltage. The buck converter operates at 16 times the internal tone frequency, nominally 352 kHz.

The tracking regulator provides minimum power dissipation across the range of output voltages by adjusting the SENSE terminal voltage, nominally 900 mV above the LNB output voltage. The tracking regulator also provides adequate headroom for tone injection.

Linear regulator. The output linear regulator will sink or source current. This allows tone modulation into a capacitive load of $0.1~\mu F$ over the output current range of 12~mA to 750~mA.

Slew rate control. The programmed output voltage rise and fall times can be set by an external capacitor (with an internal 25 k Ω resistor) located on the TCAP terminal. The range of acceptable capacitor values is 4.7 nF to 47 nF. This feature only affects the turn-on and programmed voltage rise and fall times. Modulation is unaffected by the capacitor. If LNB output voltage rise and fall time limiting is not required, the TCAP terminal should use a 100 nF ceramic as a default value to minimize output noise. If a small value capacitor is used, the rise time will be limited by the time required to charge the VBULK capacitor.

Short-circuit limit regulator. The LNB output is current limited. The short-circuit protection threshold is set by the value of an external resistor, R_S , in conjunction with an internal 135 mV reference voltage $(V_{ILNB(th)})$.

$$R_S = 0.135/I_{LNBM}$$

where I_{LNBM} is the desired current-limit value. The sense resistor should be chosen based on the maxi-

mum dc plus ac (tone) load current required, internal $V_{\rm ILNB(th)}$ tolerance, and sense resistor accuracy. For 750 mA applications, a precision 140 m Ω resistor is recommended. For 500 mA applications, the resistor value can be raised to 200 m Ω .

In operation, the short-circuit protection produces current limiting at the input due to the tracking converter. If the output is shorted, the linear regulator will limit the output current to I_{LNBM} .

Fault output. Short-circuit or thermal shutdown will cause the OLF terminal, an open-drain diagnostic output flag, to go LOW.

Internal tone modulation. The ENT (tone enable) terminal activates the internal tone signal, modulating the dc output with a 650 mV peak-to-peak trapezoidal waveform. The internal oscillator is factory trimmed to provide a tone of 22 kHz. No further adjustment is required. Burst coding of the tone can be accomplished, due to the fast response of the ENT input and rapid tone response. This allows implementation of the DiSEqCTM protocols.

External tone modulation. To improve design flexibility and to allow implementation of proposed LNB remote control standards, an analog modulation input terminal is available (EXTM). An appropriate dc-blocking capacitor must be used to couple the modulating signal source to the EXTM terminal. The peak-to-peak input amplitude should stay within 100~mV to 125~mV to ensure the DiSEqC amplitude specification over the output current range. If external modulation is not used, the EXTM terminal should be decoupled to ground with a $0.1~\mu\text{F}$ ceramic capacitor.

APPLICATIONS INFORMATION

Component selection:

Input capacitor, C_{IN}. An electrolytic capacitor should be located as close to the device VIN terminal as possible. The input current is a square wave with fast rise and fall times so the capacitor must be able to handle the rms current without excessive temperature rise. The value of this capacitor is not as important as the ESR. The worst-case current is with maximum load current, minimum V_{IN} , and maximum V_{LNB} (highest switch duty cycle). Choose a capacitor with a ripple current rating greater than

$$I_{cin} = I_{LNB} \times 1.2 \times V_{LNB(max)} / V_{IN(min)}$$

Buck inductor, L1. A 100 μ H power inductor is appropriate for all operating conditions. The rated saturation current of the inductor must be greater than 1.3 A. To maximize efficiency, the dc resistance should be less than 350 m Ω .

Clamp diode, D1. A Schottky diode is required at the switching node LX. This diode should be rated at 1.5 times the maximum load current.

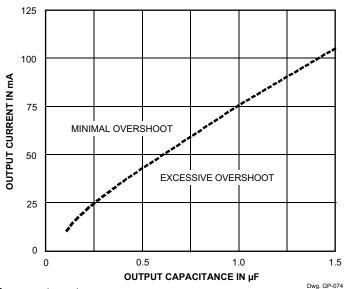
Output capacitor, C_{BULK} . A low-ESR (<200 m Ω) electrolytic capacitor is recommended to minimize the ripple voltage. Less than 50 mV peak-to-peak is a reasonable goal.

$$V_{ripple(PP)} = ESR \ x \ I_{ripple(max)}$$

where $I_{ripple(max)} = V_{BULK(min)} x (1 - [V_{BULK(min)}/V_{IN(max)}]) / (L1 x 352 kHz).$

Output capacitor, C_{LNB}. Increasing the output capacitance, C_{LNB} , will attenuate noise. However, this is limited by the requirement for low cable capacitance for 22 kHz tone transmission.

Also, because the linear regulator sink current is limited, high values of output capacitance combined with low levels of output current can cause overshoot of the 22 kHz tone. Operating points above the line in the following graph will not have excessive overshoot.



Layout notes:

- 1. The printed wiring board should use a heavy ground plane. A two-sided board with ground planes on both sides of the board is most desirable. Several copper vias under the device can be used to connect the ground planes and enhance thermal performance.
- 2. For optimum electrical and thermal performance, the device should be soldered directly onto the board.
- 3. Keep the sense resistor traces as short and as wide as possible to lower trace resistance.
- 4. Connect the bypass capacitors as close to the device as possible. The lower value ceramic capacitors should be closer to the device than the electrolytics. The supply voltage, $V_{\rm IN}$, should be decoupled with an electrolytic capacitor placed as close to the device as possible.
- 5. Place the TCAP capacitor as close to the device as possible.



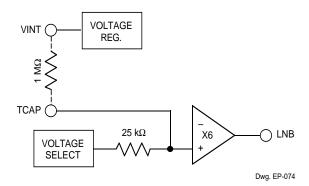
APPLICATIONS INFORMATION (cont'd)

Grounding. Use a star ground approach at the device ground terminals. This allows the analog and power grounds to be kept separate on the PWB up to the device.

Noise immunity. LNB systems can have a 50 mV peak specification for noise on the coaxial cable. This is easily achievable with proper layout and following a few guidelines:

- 1. Use a low-ESR capacitor for V_{BULK} . A maximum of 200 m Ω is recommended.
- 2. The LNB output is sensitive to the TCAP reference terminal. Keep the PWB traces short and location of C_{TCAP} close to the device. This terminal is a high-impedance node and noise can be induced from proximity to an unshielded inductor. If the inductor can not be placed far enough away to avoid noise pickup, it is important to ensure that the induced voltage is out of phase with the switching node LX. Rotating the inductor can change the phase of the induced voltage.
- 3. Be sure to place a 1 μ F to 10 μ F capacitor on internal reference V_{INT} (A8282 only).
- 4. Bypass EXTM with a $0.1~\mu F$ ceramic capacitor to ground.
- 5. Increasing the output capacitance will attenuate noise. However, this must be traded off with the requiremnent for low cable capacitance for 22 kHz-tone transmission.

DirecTV®. With the A8282, it is possible to raise the LNB output voltage 440 mV from the nominal 13 V setting to comply with DirecTV requirements. This is accomplished by connecting a 1 M Ω resistor between the VINT and TCAP terminals, sourcing approximately 2.76 μ A into the TCAP node. The LNB output voltage is approximately six times the setting of the voltage-select DAC as shown in the figure.



DISEQC™. The 22 kHz tone is specified to be compatible with EUTELSAT coaxial cable bus standards.

The LNB output will be able to drive the DiSEqC termination network. The inductor must pass the dc current with minimal loss while the parallel resistor provides the recommended source impedance at 22 kHz. Unidirectional communication systems such as DiSEqC 1.0 do not need this termination and the LNB can be directly connected to the coaxial cable.

13 V to 18 V transition. The LNB output can be rapidly switched between a high and a low setting as a method of receiver-to-LNB communication. The TCAP capacitor will control the slew rate based on the RC charging.

$$t_r$$
 or t_f = 25 x 10 3 x $C_{TCAP} \; ln(V_{LNB(H)}\!/V_{LNB(L)})$

APPLICATIONS INFORMATION (cont'd)

Small values of TCAP are used when the desired transition time is less than a millisecond. In this case, the minimum rise time is limited by the charge time of the switching regulator output capacitor. This is dependent on the LNB load current, peak current limit in the buck switch, and the output amplitude change.

$$t_r = C_{BULK} (V_{LNB(H)} - V_{LNB(L)})/I_{(AV)}$$

where $I_{(AV)}$ is the average current available to charge the output capacitor and can be estimated by $I_{(AV)} = 1.4 - I_{LNB}$. Note that this is only a limitation due to the ability to charge the output capacitor on a low-to-high change of the LNB voltage. For high-to-low transitions, the output voltage will be slew limited by TCAP.

The minimum value for C_{TCAP} is 4.7 nF.

Power dissipation. The power dissipated, and operating junction temperature of the device, can be estimated to ensure that the device is operating within the desired thermal budget.

The total device power dissipation (P_D) is comprised of three components:

$$P_D = P_{D(bias)} + P_{D(lin)} + P_{D(buck)}$$

where
$$P_{D(bias)} = V_{IN} (I_{IN} - 0.004)$$
,

$$P_{D(lin)} = \Delta V_{BUCK} \times I_{LNB},$$

$$P_{D(buck)} = I_{LNB}^2 \times r_{DS(on)} \times V_{BULK}/V_{IN}$$

where
$$V_{BULK} = \Delta V_{BUCK} + (I_{LNB} \times R_S) + V_{LNB}$$
.

The device junction temperature can then be estimated as

$$T_{J} = (P_{D} \times R_{\theta JA}) + T_{A}$$

or

$$T_{J} = (P_{D} \times R_{\theta JT}) + T_{T}$$

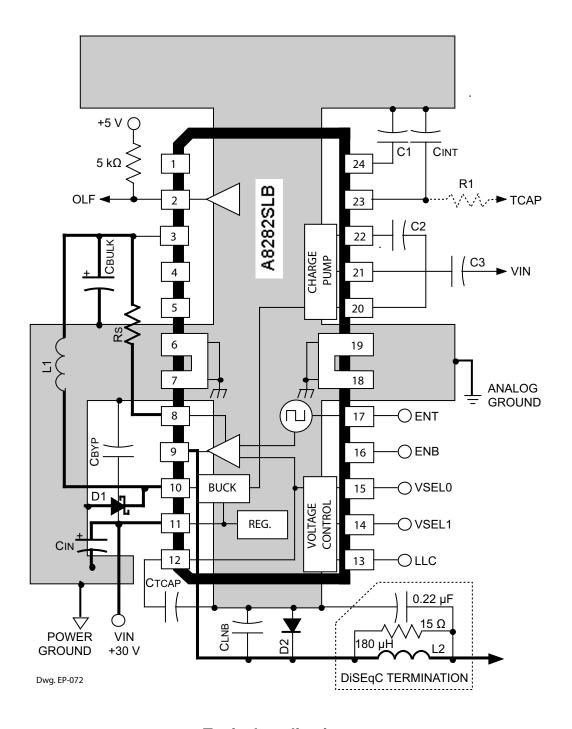
where T_T is the power tab temperature (leads 4 or 13 for the A8281SLB or leads 6, 7, 18, or 19 for the A8282SLB) and $R_{\theta IT}$ is 6°C/W.

Package thermal resistances, $R_{\theta JA}$, measured on JEDEC standard "high-K" four layer board:

A8281SLB	38°C/W
A8282SLB	35°C/W

measured on two-sided PWB with 3 square inches (1935 mm²) copper ground area on each side:

APPLICATIONS INFORMATION (cont'd)



Typical application

APPLICATIONS INFORMATION (cont'd)

Parts list for typical application

	Description	Representative Component
C1, C2, C3, C _{BYP} , C _{LNB}	0.1 μF/50 V ceramic X7R/X5R	
C _{IN}	100 μF/50 V low-ESR electrolytic	Nichicon UHD1H101MPT
C _{BULK}	100 μF/35 V low-ESR electrolytic	Nichicon UHC1V101
C _{INT}	4.7 μF/16 V tantalum electrolytic	
D1	1 A/40 V Schottky diode	Sanken EK04
D2	1.2 A/100 V fast-recovery diode	Sanken EU 2YX
L1	100 μH (750 mA max. load)	TDK TSL1112-101K1R4, or Coilcraft D03316P-104LW
	100 μH (500 mA max. load)	TDK TSL0808-101KR80
L2	180 μH (750 mA max. load)	TDK TSL1112S-181K1R0-PF
RS	140 mΩ to 200 mΩ/0.25 W	Meritek CR04RxxxF
C _{TCAP}	10 nF ceramic X7R/X5R	
R1	1 M Ω , ±5% (optional, see page 7)	

DiSEqC (Digital Satelite Equipment Control) is a trademark of EUTELSAT (European Telecommunications Satellite Corporation), Paris, France.

DirecTV is a trademark of DirecTV, Inc., a unit of Hughes Electronics Corp., El Segundo, CA

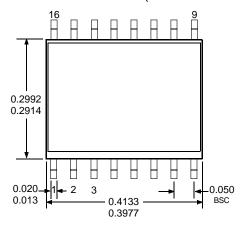


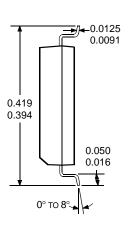
Terminal List

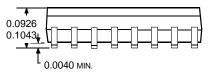
	A8281SLB	A8282SLB	
Terminal	Terminal	Terminal	
Name	Number	Number	Terminal Description
NC	-	1	No (internal) connection
OLF	2	2	Overload flag output: low (fault) when $I_{LNB} > I_{LNBM}$ or $T_J > 165$ °C, high when $I_{LNB} < I_{LNBM}$ and $T_J < 130$ °C
VBULK	3	3	Tracking supply voltage to linear regulator
NC	-	4, 5	No (internal) connection
GND	4	6, 7	Ground and substrate
SENSE	5	8	Current limit setup resistor
LNB	6	9	Output voltage to LNB
LX	7	10	Inductor drive point
VIN	8	11	Supply input voltage (minimum, V _{LNB} + 2.5 V)
TCAP	9	12	Capacitor for setting the rise and fall time of the outputs for line-length compensation
LLC	-	13	Logic input: output voltage select
VSEL1	10	14	Logic input: output voltage select
VSEL0	-	15	Logic input: output voltage select
EN	11	16	Logic input: when high, enables device
ENT	12	17	Logic input: when high, enables internal 22 kHz modulation
GND	13	18, 19	Ground and substrate
CPUMP	14	20	High side of charge-pump capacitor
VPUMP	15	21	Gate-supply voltage for high-side drivers
PUMPX	16	22	Charge-pump drive
VINT	-	23	Bypass capacitor for internal voltage reference
EXTM	1	24	External modulation input

A8281SLB

Dimensions in Inches (for reference only)

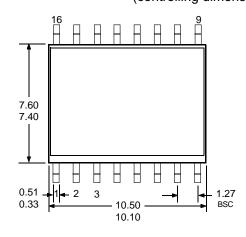


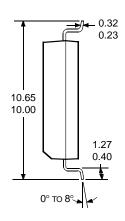


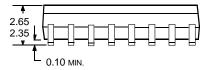


Dwg. MA-008-16A in

Dimensions in Millimeters (controlling dimensions)

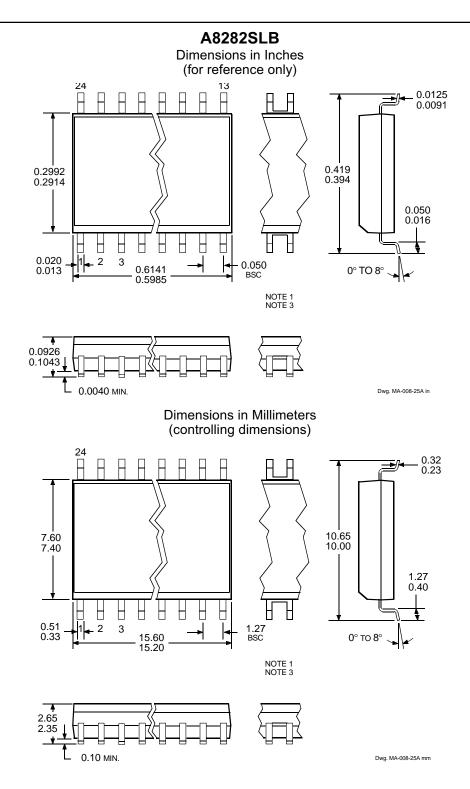






Dwg. MA-008-16A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 - 2. Lead spacing tolerance is non-cumulative.
 - 3. Leads 4 and 13 are internally one piece.
 - 4. Supplied in standard sticks/tubes of 47 devices or add "TR" to part number for tape and reel.



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

- 2. Lead spacing tolerance is non-cumulative.
- 3. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
- 4. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

