

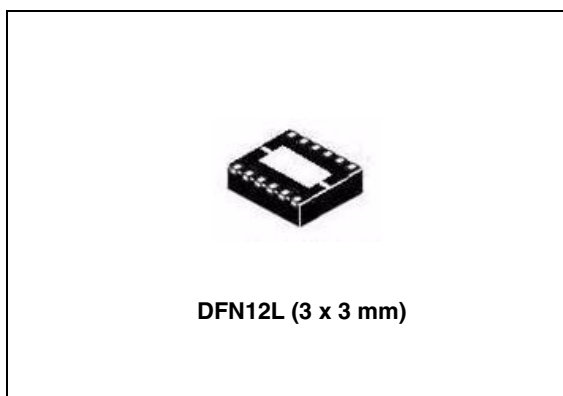
Dual DC-DC converter for powering AMOLED display

Features

- Step-up and inverter converters
- Operating input voltage range from 2.5 V to 4.5 V
- Synchronous rectification for both DC-DC converters
- 150 mA maximum output current
- 4.6 V fixed positive output voltage
- Programmable negative voltage by S-wire from -2.3 V to -5.9 V
- Typical efficiency: 85 %
- Pulse skipping mode in light load condition ($I_O < 10$ mA)
- 1.6 MHz PWM mode control switching frequency ($I_O > 10$ mA)
- Enable pin for shutdown mode
- Low quiescent current: < 1 μ A in shutdown mode
- Soft-start with inrush current protection
- Over temperature protection
- Temperature range: -40 °C to 85 °C
- True shutdown mode
- Fast outputs discharge circuit after shutdown
- Package: DFN 12 leads - (3 x 3 mm)

Applications

- Active matrix organic LED power supply (AMOLED)
- Mobile phones



- PDAs
- Camcorders and digital still cameras

Description

The STOD02 is a dual DC-DC converter meant to power AMOLED displays. It integrates a step up and an inverting DC-DC converter making it particularly suitable for battery operated products, where the major concern is the overall system efficiency. STOD02 works in pulse skipping mode during low load condition and in PWM-mode (at 1.6 MHz) for medium/high load condition. The high frequency allows reducing the value and number of external components just to 6 components needed. The enable pin allows turning off the device so reducing the current consumption to less than 1 μ A. The negative output voltage can be programmed by an MCU through a dedicated pin which implements single-wire protocol. Soft-start with controlled inrush current limit and thermal shutdown are integrated functions of the device.

Table 1. Device summary

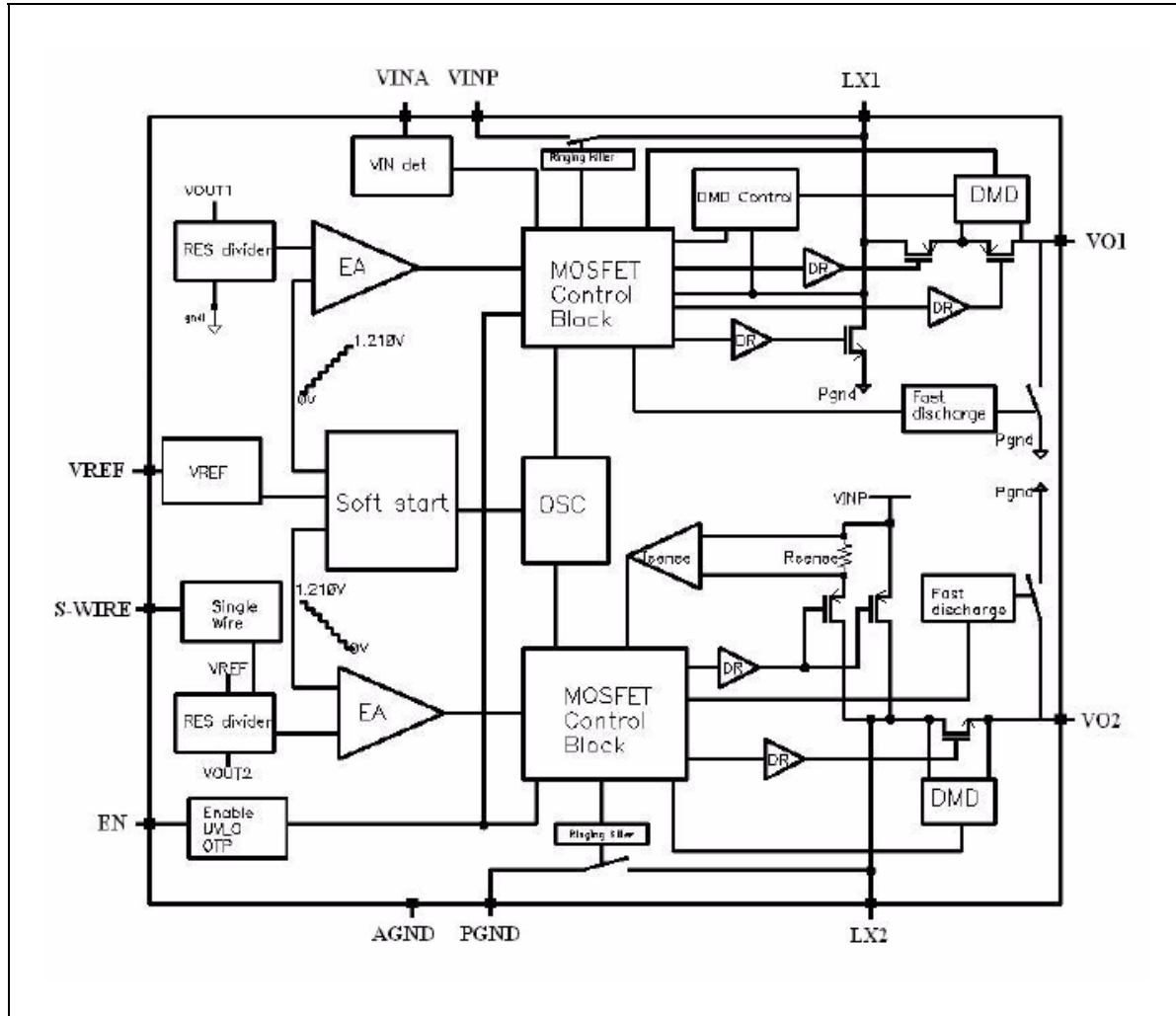
Order code	Package	Packaging
STOD02PUR	DFN12L (3 x 3 x 0.8 mm)	3000 parts per reel
STOD02TPUR	DFN12L (3 x 3 x 0.6 mm)	3000 parts per reel

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1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

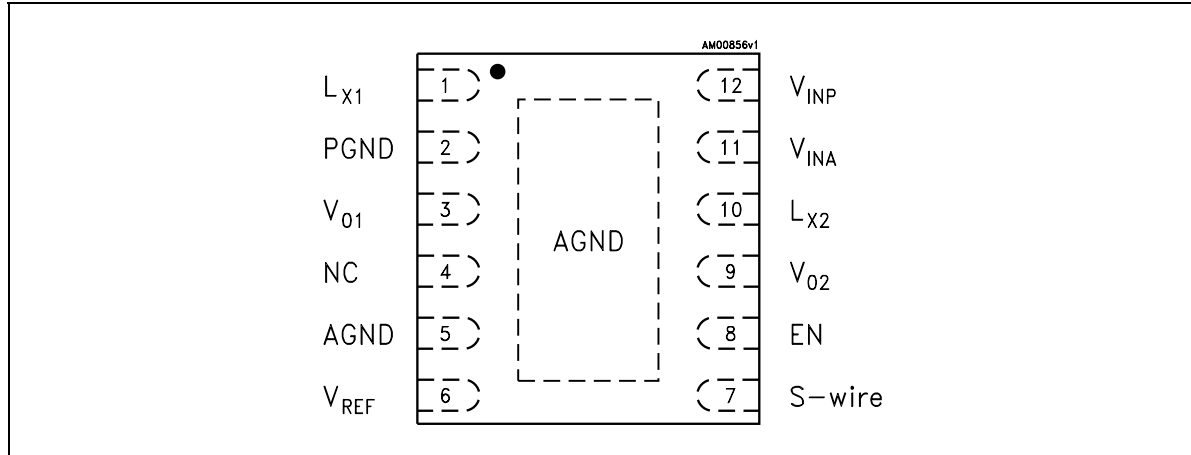


Table 2. Pin description

Pin n°	Symbol	Description
1	L_{X1}	Switching node of the step up converter
2	PGND	Power ground pin
3	V_{O1}	Step up converter output voltage
4	NC	Not connected
5	AGND	Signal ground pin. This pin must be connected to power ground pin
6	V_{REF}	External voltage reference
7	S-wire	Negative voltage setting pin, uses S-wire protocol
8	EN	Enable control pin. ON = V_I . When pulled low, the device goes in shutdown mode
9	V_{O2}	Inverting converter output voltage
10	L_{X2}	Switching node of the inverting converter
11	V_{INA}	Analog input supply voltage
12	V_{INP}	Power input supply voltage
	exposed pad	Internally connected to AGND. Exposed pad must be connected to AGND and PGND in the PCB layout in order to guarantee proper operation of the device.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INA}, V_{INP}	DC supply voltage	-0.3 to 6	V
EN,S-wire	Enable pin, S-wire pin	-0.3 to 6	V
I_{LX2}	Inverting converter's switching current	Internally limited	A
L_{X2}	Inverting converter switching node	-10 to $V_{INP}+0.3$	V
V_{O2}	Inverting converter output voltage	-10 to GND+0.3	V
V_{O1}	Step-up converter output voltage	-0.3 to 6	V
L_{X1}	Step-up converter switching node	-0.3 to $V_{O1}+0.3$	V
I_{LX1}	Step up converter's switching current	Internally limited	A
V_{REF}	Reference voltage	-0.3 to 3	V
P_D	Power dissipation	Internally limited	mW
T_{st}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	°C
ESD	ESD protection HBM	2	kV

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient referred to FR-4 PCB	49.1	°C/W
R_{thJC}	Thermal resistance junction-case	4.216	°C/W

4 Application

Figure 3. Typical application circuit

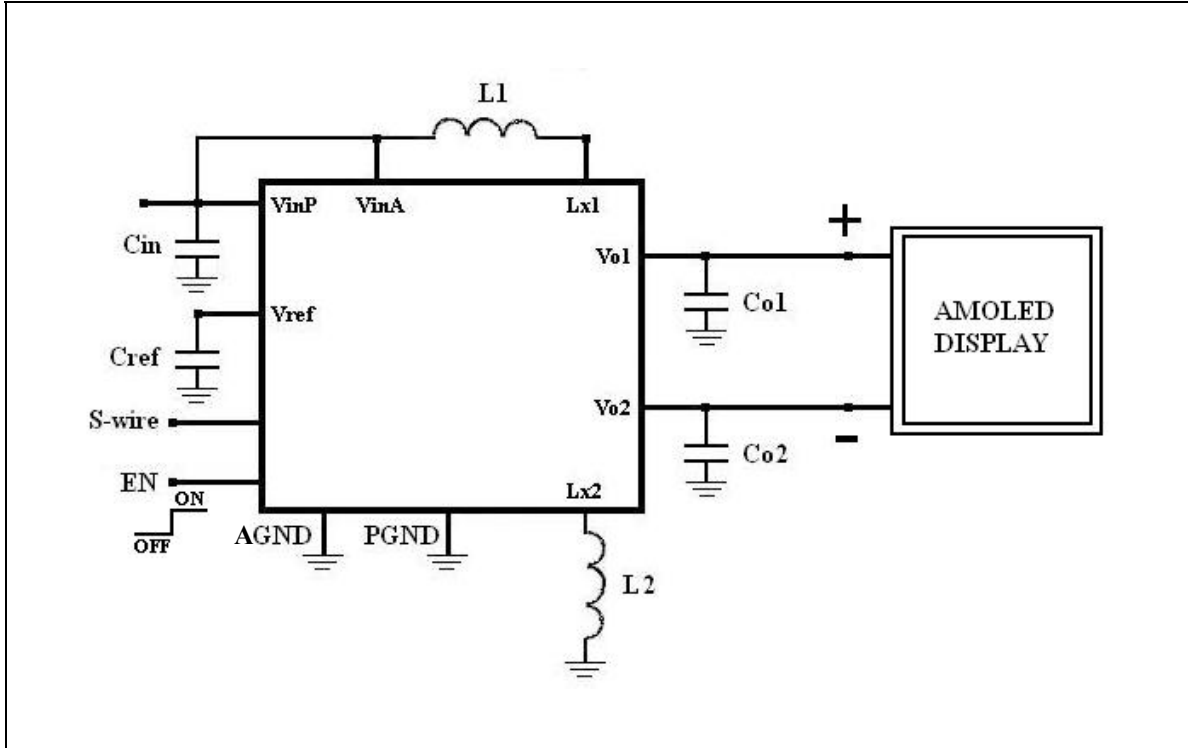


Table 5. Typical external components

Symbol	Parameter	Min.	Typ.	Max.	Unit
L_1	Inductor		4.7		μH
L_2	Inductor		4.7		μH
C_{IN}	Ceramic capacitor SMD		4.7		μF
C_{O1}, C_{O2}	Ceramic capacitor SMD		4.7		μF
C_{ref}	Ceramic capacitor SMD		1		μF

5 Electrical characteristics

$T_J = 25\text{ }^\circ\text{C}$, $V_{INA} = V_{INP} = 3.7\text{ V}$, $I_{O1,2} = 30\text{ mA}$, $C_1 = 4.7\text{ }\mu\text{F}$, $C_{O1,2} = 4.7\text{ }\mu\text{F}$, $C_{REF} = 1\text{ }\mu\text{F}$, $L_1 = 4.7\text{ }\mu\text{H}$, $L_2 = 4.7\text{ }\mu\text{H}$, $V_{EN} = V_{INA} = V_{INP}$, $V_{O1} = 4.6\text{ V}$, $V_{O2} = -4.9\text{ V}$ unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Operating input voltage range	$V_{O1}=4.6\text{V}$, $T_J = -40\text{ to }85^\circ\text{C}$	2.5		4.5	V
UVLO_H	Under voltage lockout HIGH	V_{INA} rising, $T_J = -40\text{ to }85^\circ\text{C}$		2.40	2.50	V
UVLO_L	Under voltage lockout LOW	V_{INA} falling, $T_J = -40\text{ to }85^\circ\text{C}$	2.30	2.35		V
I_{V_I}	Input current	No Load condition ($I_{V_I} = I_{INA} + I_{INP}$)		1	1.5	mA
I_S	Shutdown current	$V_{EN} = \text{GND}$, ($I_S = I_{INA} + I_{INP}$)			1	μA
$V_{EN\ H}$	Enable high threshold	$V_{INA} = 2.5\text{V to }4.5\text{V}$, $T_J = -40\text{ to }85^\circ\text{C}$	1.2			V
$V_{EN\ L}$	Enable low threshold	$V_{INA} = 2.5\text{V to }4.5\text{V}$, $T_J = -40\text{ to }85^\circ\text{C}$			0.4	
I_{EN}	Enable input current	$V_{EN} = V_I$			1	μA
F_{SW}	Frequency	PWM mode, $T_J = -40\text{ to }85^\circ\text{C}$	1.35	1.6	1.85	MHz
$D1_{MAX}$	Step-up maximum duty cycle			90		%
$D2_{MAX}$	Inverting maximum duty cycle			90		%
η	Total system efficiency	$I_{O1,2}=10\text{ to }30\text{mA}$, $V_{O1}=4.6\text{V}$, $V_{O2}=-4.9\text{V}$		80		%
		$I_{O1,2}=30\text{ to }150\text{mA}$, $V_{O1}=4.6\text{V}$, $V_{O2}=-4.9\text{V}$		85		
V_{REF}	Voltage reference	$I_{REF}=10\mu\text{A}$	1.196	1.209	1.222	V
I_{REF}	Voltage reference current capability	At $V_{REF} = V_{REF} - 1.5\%$	100			μA
Step-up converter section						
V_{O1}	Line/Load maximum output voltage variation	$V_{INA}=2.5\text{V to }4.5\text{V}$, $I_{O1}=5\text{mA to }100\text{mA}$	4.55	4.6	4.65	V
$\Delta V_{O1\ SL}$	Static line regulation ⁽¹⁾	$V_{INA}=2.5\text{V to }4.5\text{V}$, $I_{O1}=5\text{mA}$, I_{O2} no load; $T_J=-40^\circ\text{C to }85^\circ\text{C}$		0.5		%
		$V_{INA}=2.5\text{V to }4.5\text{V}$, $I_{O1}=100\text{mA}$, I_{O2} no load, $T_J=-40^\circ\text{C to }85^\circ\text{C}$		0.5		
$\Delta V_{O1\ LT}$	Line transient	$V_{INA}=3.5\text{V to }3.0\text{V}$, $I_{O1}=100\text{mA}$ $T_J=-40^\circ\text{C to }85^\circ\text{C}$, $T_R=T_F=50\mu\text{s}$ output voltage variation with respect to nominal V_{O1}		-12		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{O1}	Static load regulation ⁽²⁾	$I_{O1}=5$ to 100mA, I_{O2} no load, $V_{INA}=2.5V$; $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		%
		$I_{O1}=5$ to 100mA, I_{O2} no load, $V_{INA}=4.5V$; $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		
ΔV_{O1t}	Load transient regulation	$I_{O1}=3$ to 30mA and $I_{O1}=30$ to 3mA, $T_R=T_F=30\mu s$, output voltage variation with respect to nominal V_{O1}		± 30		mV
		$I_{O1}=10$ to 100mA and $I_{O1}=100$ to 10mA, $T_R=T_F=30\mu s$, output voltage variation with respect to nominal V_{O1}		± 35		
ΔV_{O1}	Ripple output voltage range (peak to peak)	$I_{O1}=5$ to 100mA; 0.5Vpp pulse signal applied to V_I at 200Hz; TDMA Noise			20	mV
I_{O1}	Maximum Step-up output current	$V_I=2.9V$ to 5.5V	150			mA
$I-L_{1MAX}$	I_{peak} current	V_{O1} below 10% of nominal value	0.9			A
R_{DSONP1}		$T_J = -40$ to $85^{\circ}C$		0.8	1.0	Ω
R_{DSONN1}		$T_J = -40$ to $85^{\circ}C$		0.5	1.0	Ω
Inverting converter section						
V_{O2}	Output negative voltage range	10 different values set by S-wire pin (see Table 9)	-2.3		-5.9	V
V_{O2} def.	V_{O2} default value	Default output voltage	-4.80	-4.9	-5.00	V
V_{O2} Toll.	V_{O2} tolerance	Output voltage variation with respect to nominal V_O selected		± 2		%
ΔV_{O2}	Static line regulation ⁽³⁾	$V_{INA}=2.5V$ to 4.5V, $I_{O2}=5mA$, I_{O1} no load; $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		%
		$V_{INA}=2.5V$ to 4.5V, $I_{O2}=100mA$, I_{O1} no load, $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		%
$\Delta V_{O1 LT}$	Line transient	$V_{INA}=3.5V$ to 3.0V, $I_{O2}=100mA$ $T_J=-40^{\circ}C$ to $85^{\circ}C$, $T_R=T_F=50\mu s$ output voltage variation with respect to nominal V_{O2}		+30		mV
ΔV_{O2}	Static load regulation ⁽⁴⁾	$I_{O2}=5$ to 100mA, I_{O1} no load, $V_{INA}=2.5V$; $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		%
		$I_{O2}=5$ to 100mA, I_{O1} no load, $V_{INA}=4.5V$; $T_J=-40^{\circ}C$ to $85^{\circ}C$		+ 1		
ΔV_{O2t}	Load transient regulation	$I_{O2}=3$ to 30mA and $I_{O2}=30$ to 3mA, $T_R=T_F=30\mu s$, output voltage variation with respect to nominal V_{O2}		± 40	± 80	mV
ΔV_{O2e}	Load transient regulation HC	$I_{O2}=10$ to 100mA and $I_{O2}=100$ to 10mA, $T_R=T_F=30\mu s$		± 30	± 50	mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{O2}	Ripple output voltage range	$I_{O2}=5$ to 100mA 0.5Vpp pulse signal applied to V_1 at 200Hz; TDMA Noise			25	mV
I_{O2s}	Maximum inverting output current	$V_{INA}=2.5V$ to 2.9V			-120	mA
I_{O2}	Maximum inverting output current	$V_{INA}=2.9V$ to 4.5V			-150	mA
$I-L2MAX$	I_{peak} current	V_{O2} below 10% of value set by S-wire		-1.2	-1.1	A
R_{DSONP2}		$T_J = -40$ to 85°C		0.4	2.0	Ω
R_{DSONN2}		$T_J = -40$ to 85°C		0.4	1.0	Ω
Thermal shutdown						
OTP	Over temperature protection			140		°C
OTPHYST	Over temperature protection hysteresis			15		°C
Discharge resistor						
R_{DIS}	Discharge resistor value			600		Ω
T_{DIS}	Discharge time			6		ms

1. $[(V_{O1MAX} - V_{O1MIN}) / (V_{O1}$ at 25°C and $V_{INA} = 2.5 V)] \times 100$
2. $[(V_{O1MAX} - V_{O1MIN}) / (V_{O1}$ at 25°C and $I_{O1} = 5 mA)] \times 100$
3. $[(V_{O2MAX} - V_{O2MIN}) / (V_{O2}$ at 25°C and $V_{INA} = 2.5 V)] \times 100$
4. $[(V_{O2MAX} - V_{O2MIN}) / (V_{O2}$ at 25°C and $I_{O2} = 5 mA)] \times 100$

6 S-wire protocol

Figure 4. S-wire protocol

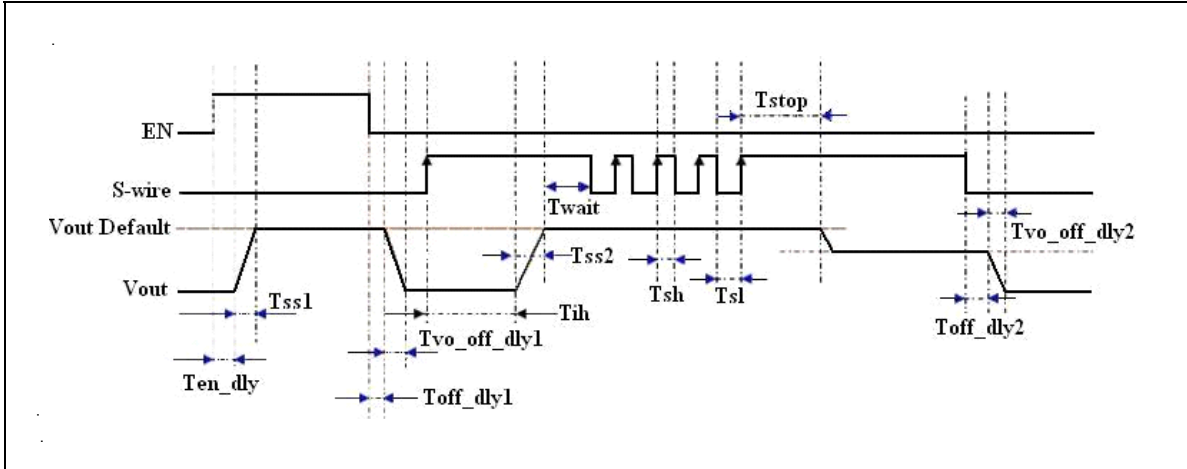


Table 7. Time

Rating	Symbol	Min.	Typ.	Max.	Unit
Enable high delay time	T_{en_dly}		300		μs
Soft-start delay	T_{ss1}		2		ms
Turn-off delay	T_{off_dly1}		50		μs
V_O turn-off delay	$T_{vo_off_dly1}$		12		ms
S-Wire initial time	T_{ih}		300	400	μs
Soft-start time by S-wire enable	T_{ss2}		2	3	ms
S-Wire High	T_{sh}	2	20	45	μs
S-Wire Low	T_{sl}	2	20	75	μs
S-Wire signal stop indicate time	T_{stop}	300		400	μs
V_O turn-off delay by S-Wire	$T_{vo_off_dly2}$		12	related to load	ms
Twait after data	T_{wait}		0	10	μs
S-Wire turn-off detection time	T_{off_dly2}	300		400	μs

Figure 5. Waveform

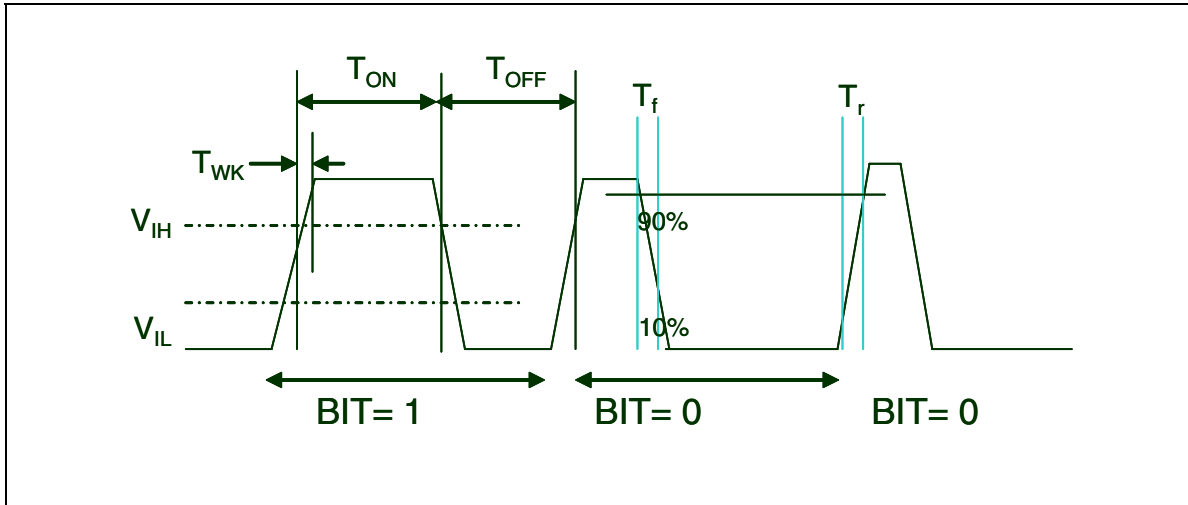


Table 8. Time

Rating	Symbol	Min.	Typ.	Max.	Unit
Rising input high threshold voltage level	V_{IH}	1.2		V_{INA}	V
Falling input high threshold voltage level	V_{IL}	0		0.6	V
Pull down resistor	R_{S-WIRE}		150		$k\Omega$
Wake up delay	T_{WK}			1	μs
S-Wire rising time	T_r			200	ns
S-Wire falling time	T_f			200	ns
Clocked s-wire high	T_{ON}	2		45	μs
S-wire low	T_{OFF}	2		75	μs
Input S-Wire frequency	F_{S-WIRE}			400	kHz

Table 9. Inverting output voltages

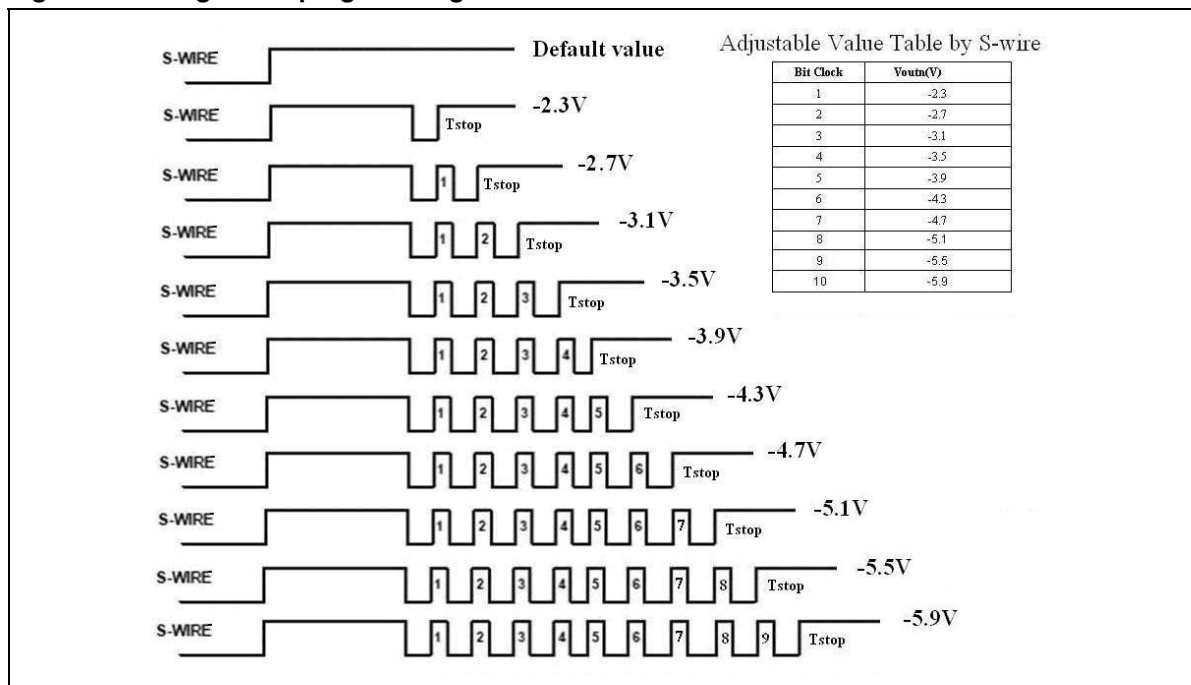
Bit clock	V_{O2} (V)
1	-2.3
2	-2.7
3	-3.1
4	-3.5
5	-3.9
6	-4.3
7	-4.7
8	-5.1
9	-5.5
10	-5.9

Table 10. Enable and s-wire pin settings

Enable	S-wire	Action
0	0	Device off
0	1	Output set by S-Wire
1	0	Default value output (- 4.9 V)
1	1	Default value output (- 4.9 V)

Note: Enable pin must be set to GND while using S-wire function.

Figure 6. Single wire programming



7 Typical performance characteristics

$C_1 = C_{O1,2} = 4.7 \mu\text{F}$, $C_{\text{REF}} = 1 \mu\text{F}$, $L_1 = L_2 = 4.7 \mu\text{H}$, $T_J = 25 \text{ }^\circ\text{C}$

Figure 7. Efficiency vs. input voltage

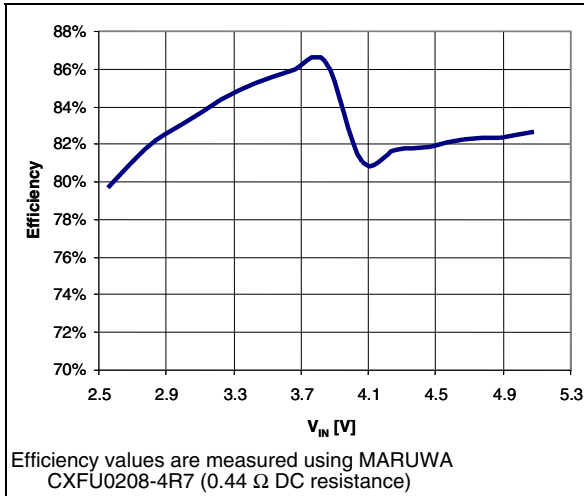


Figure 8. Efficiency vs. output current

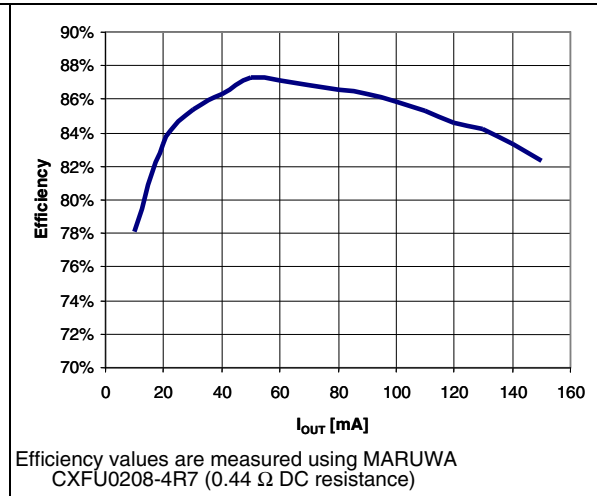


Figure 9. Step-up inductor peak current vs. input voltage

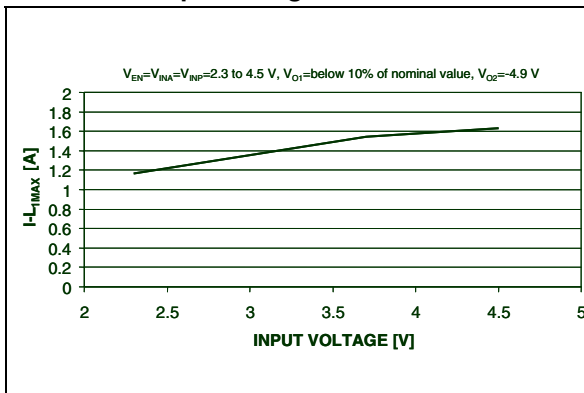


Figure 10. Inverting inductor peak current vs. input voltage

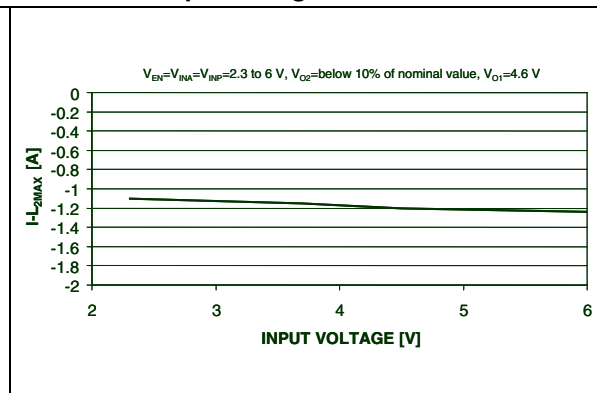


Figure 11. PWM step-up frequency vs. temperature

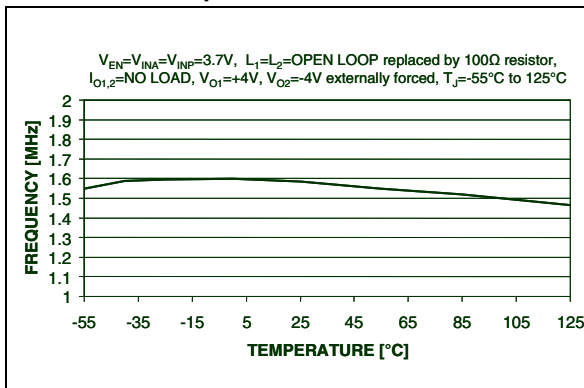


Figure 12. PWM inverting frequency vs. temperature

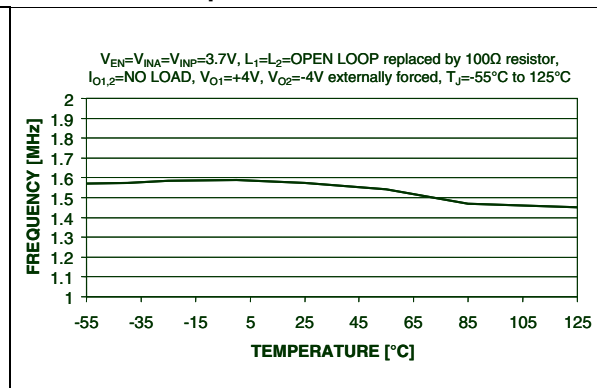


Figure 13. Quiescent current vs. temperature

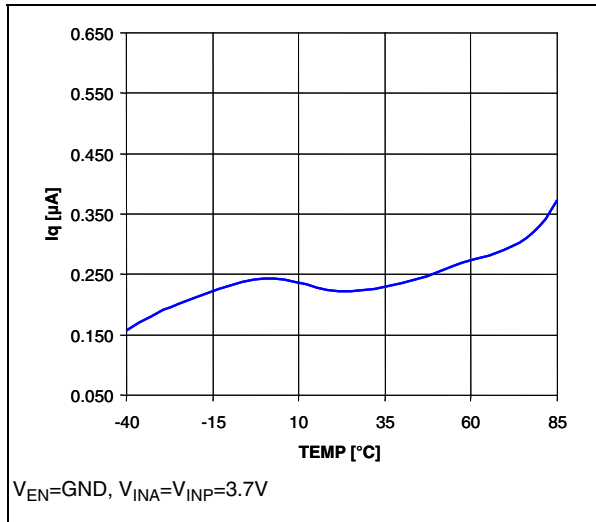


Figure 14. Input current vs. temperature

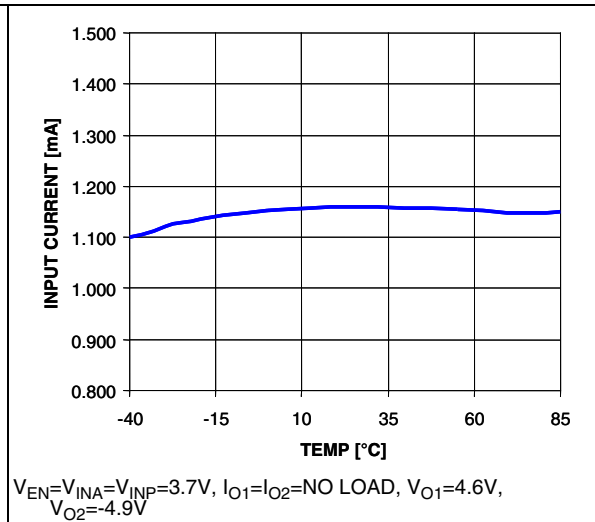


Figure 15. Step-up line transient regulation

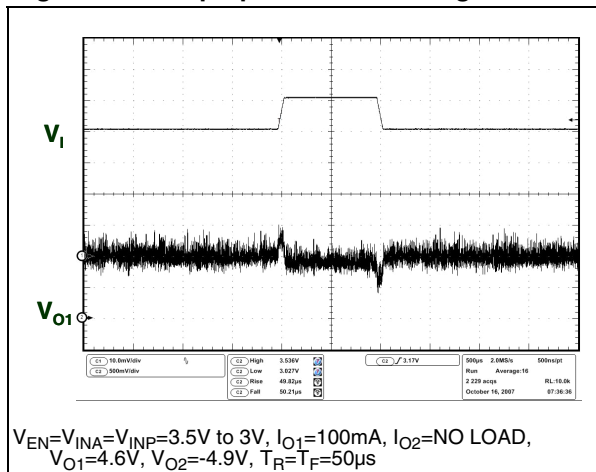


Figure 16. Inverting line transient regulation

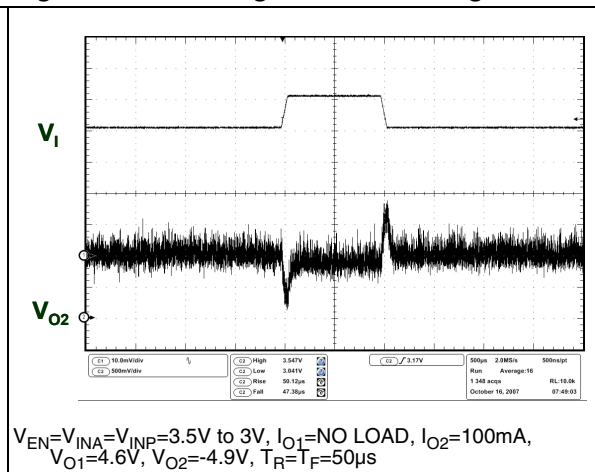


Figure 17. Step-up load transient regulation

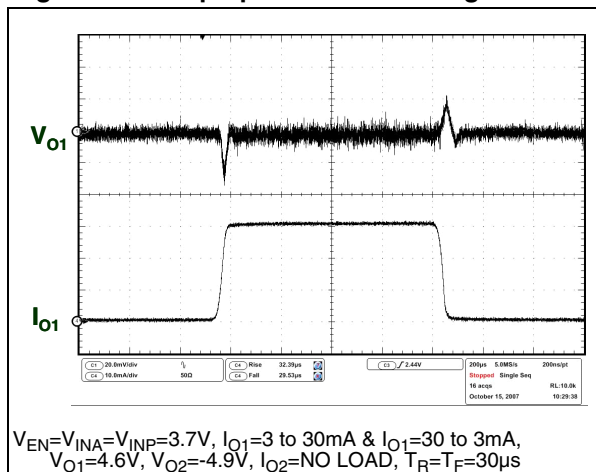
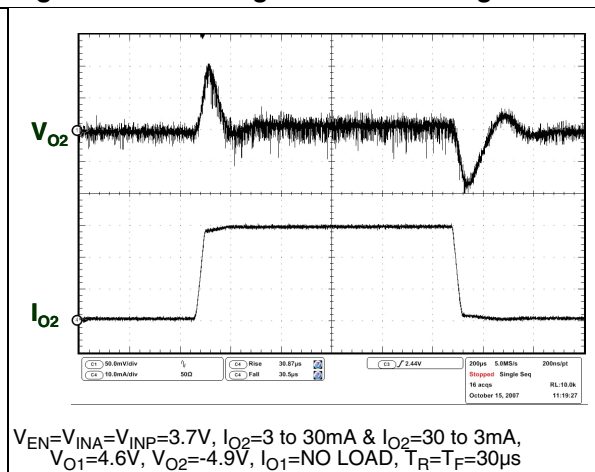


Figure 18. Inverting load transient regulation



8 Demonstration board

Figure 20. Suggested demonstration board schematic (top layer view)

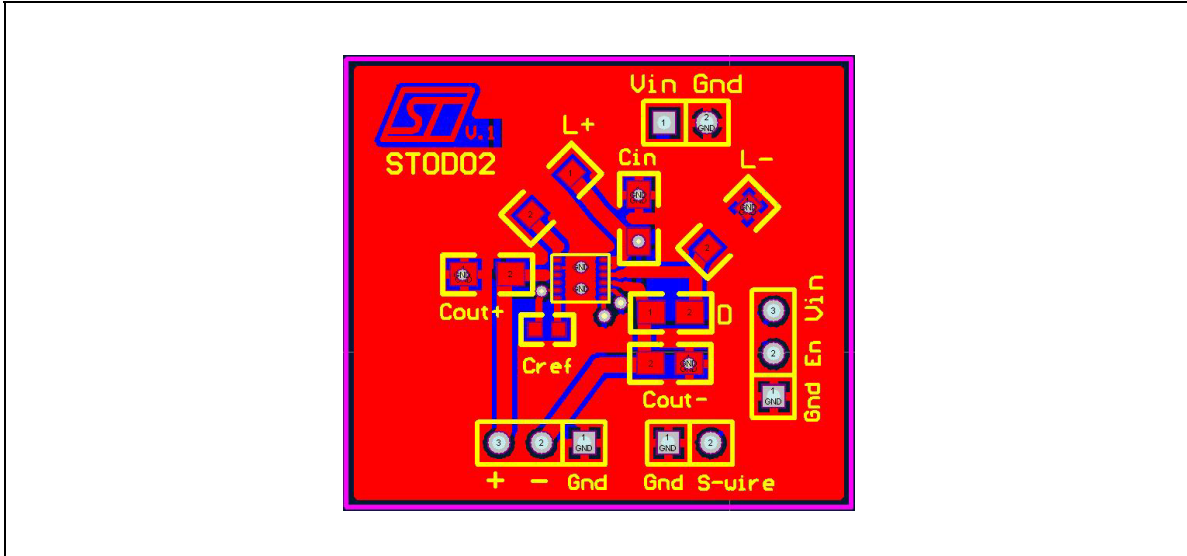
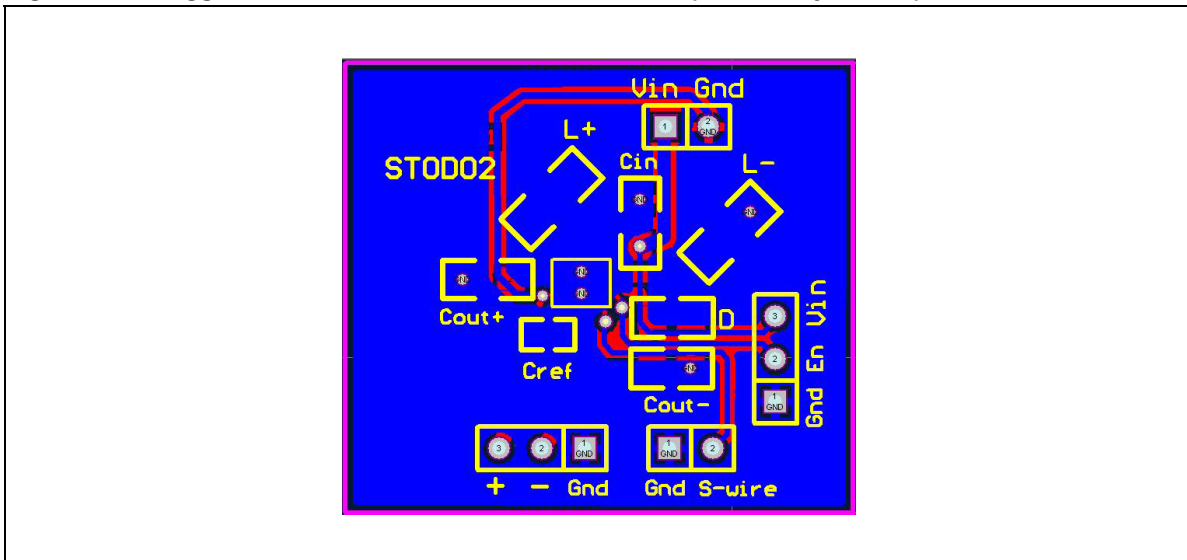


Figure 21. Suggested demonstration board schematic (bottom layer view)



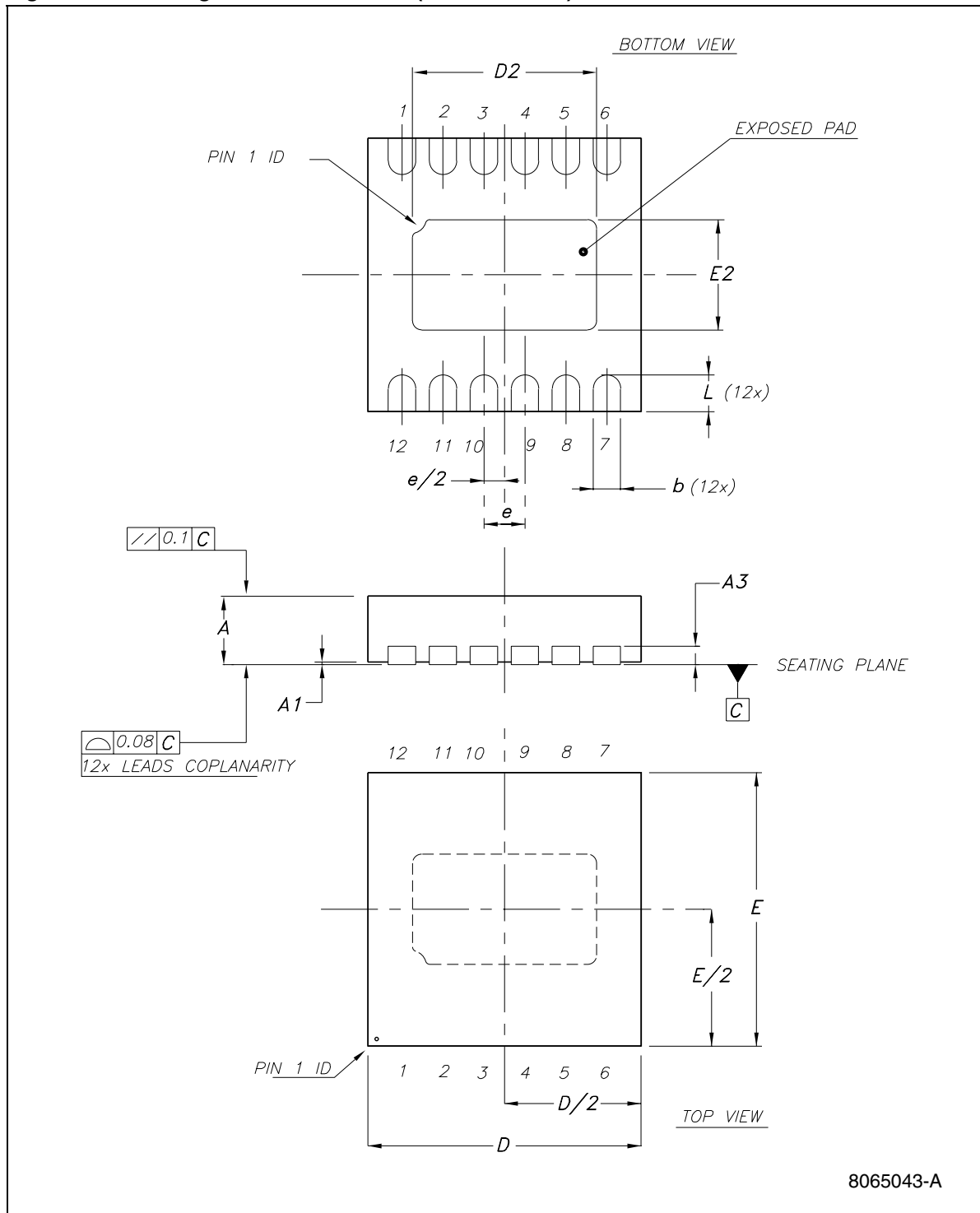
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 11. DFN12L (3 x 3 x 0.8 mm) mechanical data

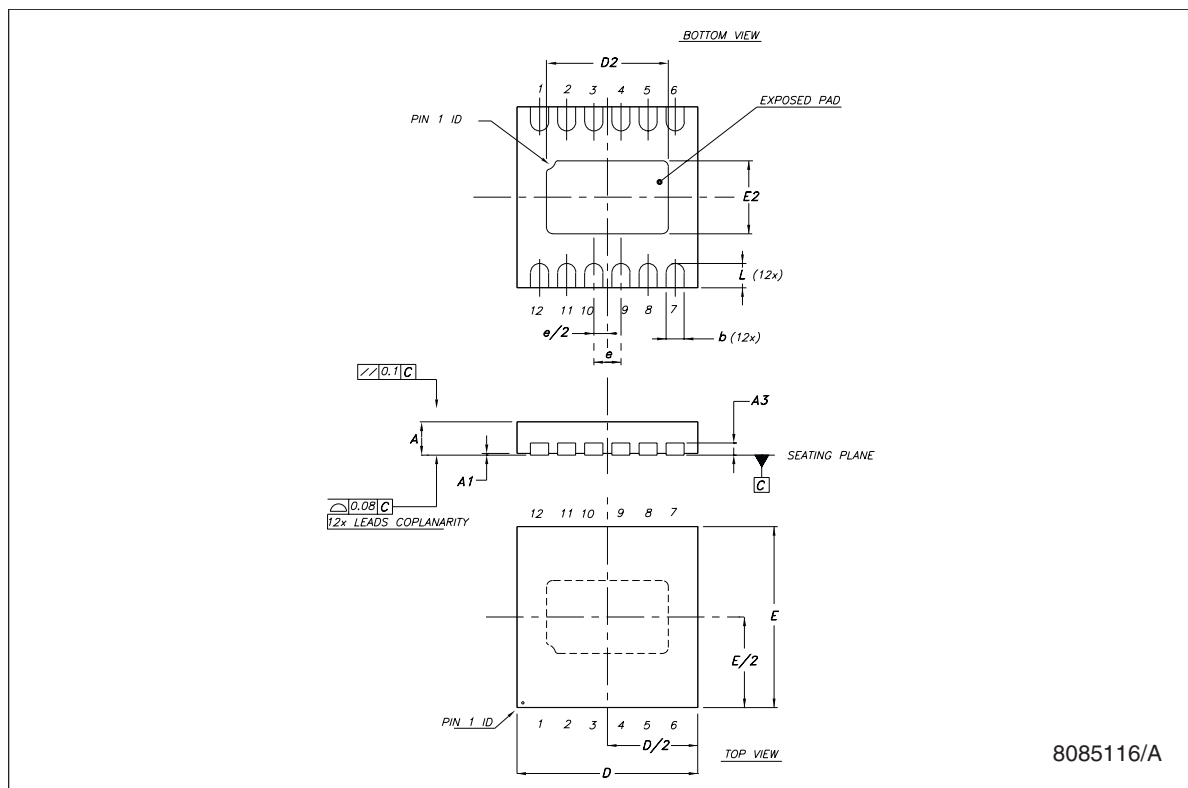
Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3	3.15
D2	1.87	2.02	2.12
E	2.85	3	3.15
E2	1.06	1.21	1.31
e		0.45	
L	0.30	0.40	0.50

Figure 22. Drawing dimension DFN12L (3 x 3 x 0.8 mm)



DFN12L (3 x 3 x 0.6 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.85	3	3.15	0.112	0.118	0.124
D2	1.87	2.02	2.12	0.074	0.080	0.083
E	2.85	3	3.15	0.112	0.118	0.124
E2	1.06	1.21	1.31	0.042	0.048	0.052
e		0.45			0.018	
L	0.30	0.40	0.50	0.012	0.016	0.020



Tape & reel QFNxx/DFNxx (3x3) mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

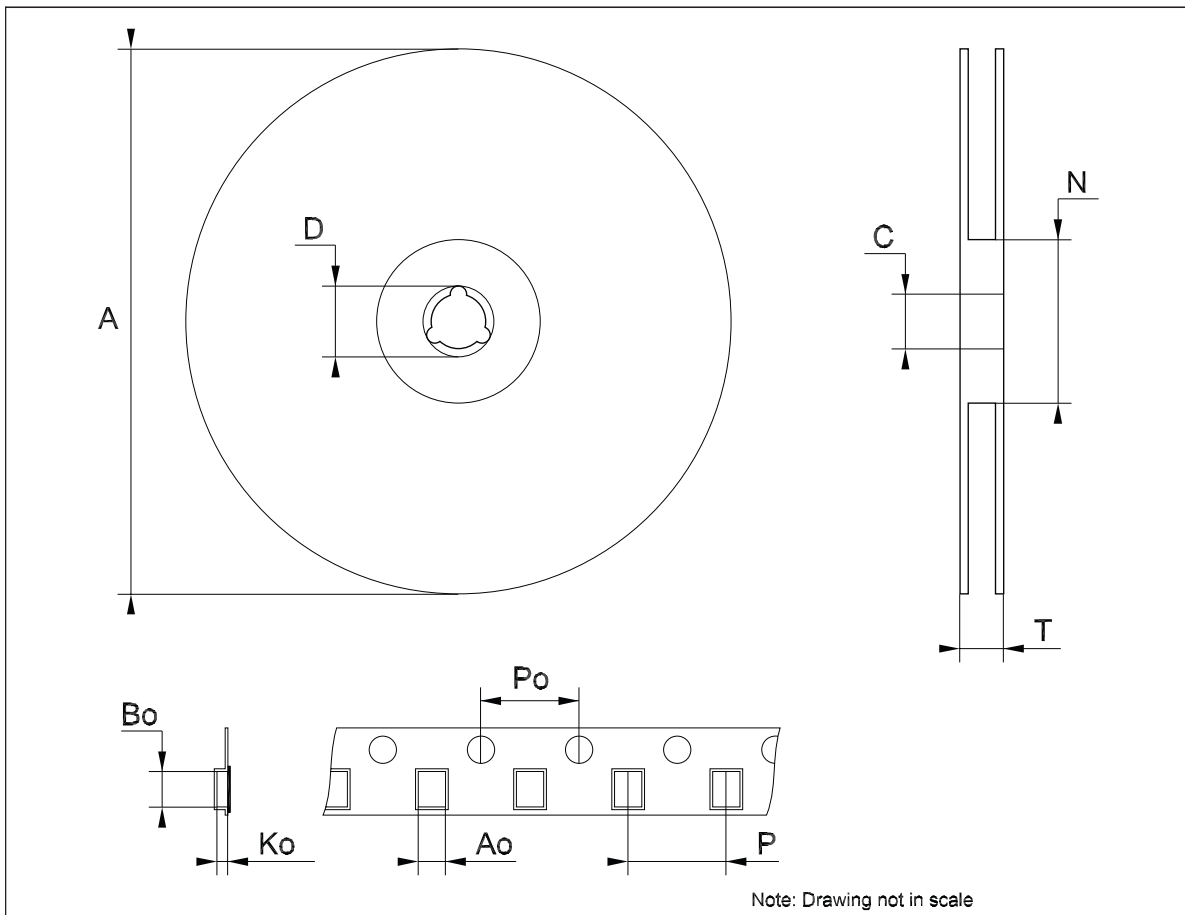
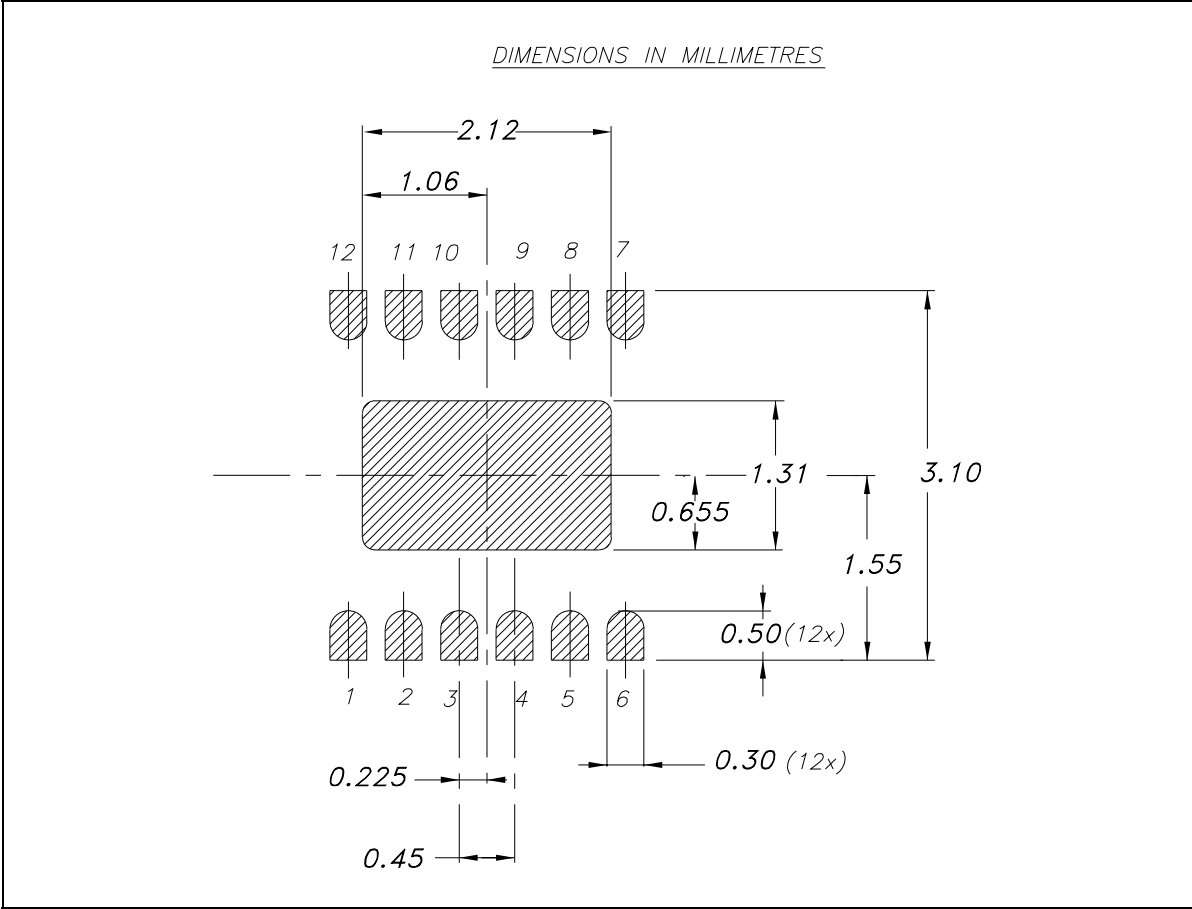


Figure 23. DFN12L (3 x 3 mm) footprint recommended data



10 Revision history

Table 12. Document revision history

Date	Revision	Changes
05-Dec-2008	1	Initial release.
15-Dec-2008	2	Added: pin description exposed pad Table 2 on page 4 .
30-Jun-2009	3	Modified: Table 2 on page 4 .

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