PM6685

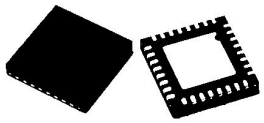
Dual step-down main supply controller with auxilary voltages for notebook system power

Features

- 6 V to 28 V input voltage range
- Fixed 5 V - 3.3 V output voltages
- 5 V and 3.3 V voltage always available to deliver 100 mA of peak current
- 1.230 V ±1% reference voltage available
- Lossless current sensing using low side
- MOSFETs' $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2 ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 4 mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation

Applications

- Notebook computers
- Tablet PC or slates
- Mobile system power supply
- 3 and -4 Cells Li+ battery-powered devices



VFQFPN-32 (5mm x 5mm)

Description

PM6685 is a dual step-down controller specifically designed to provide extremely high efficiency conversion with loss-less current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation.

An embedded integrator control loop compensates the DC voltage error due to the output ripple. The pulse skipping technique increases efficiency for very light loads. Moreover, a minimum switching frequency of 33kHz is selectable in order to avoid audio noise issues.

The PM6685 provides a selectable switching frequency, allowing either 200 kHz/300 kHz, 300 kHz/400 kHz, or 400 kHz/500 kHz operation of the 5 V/3.3 V switching sections.

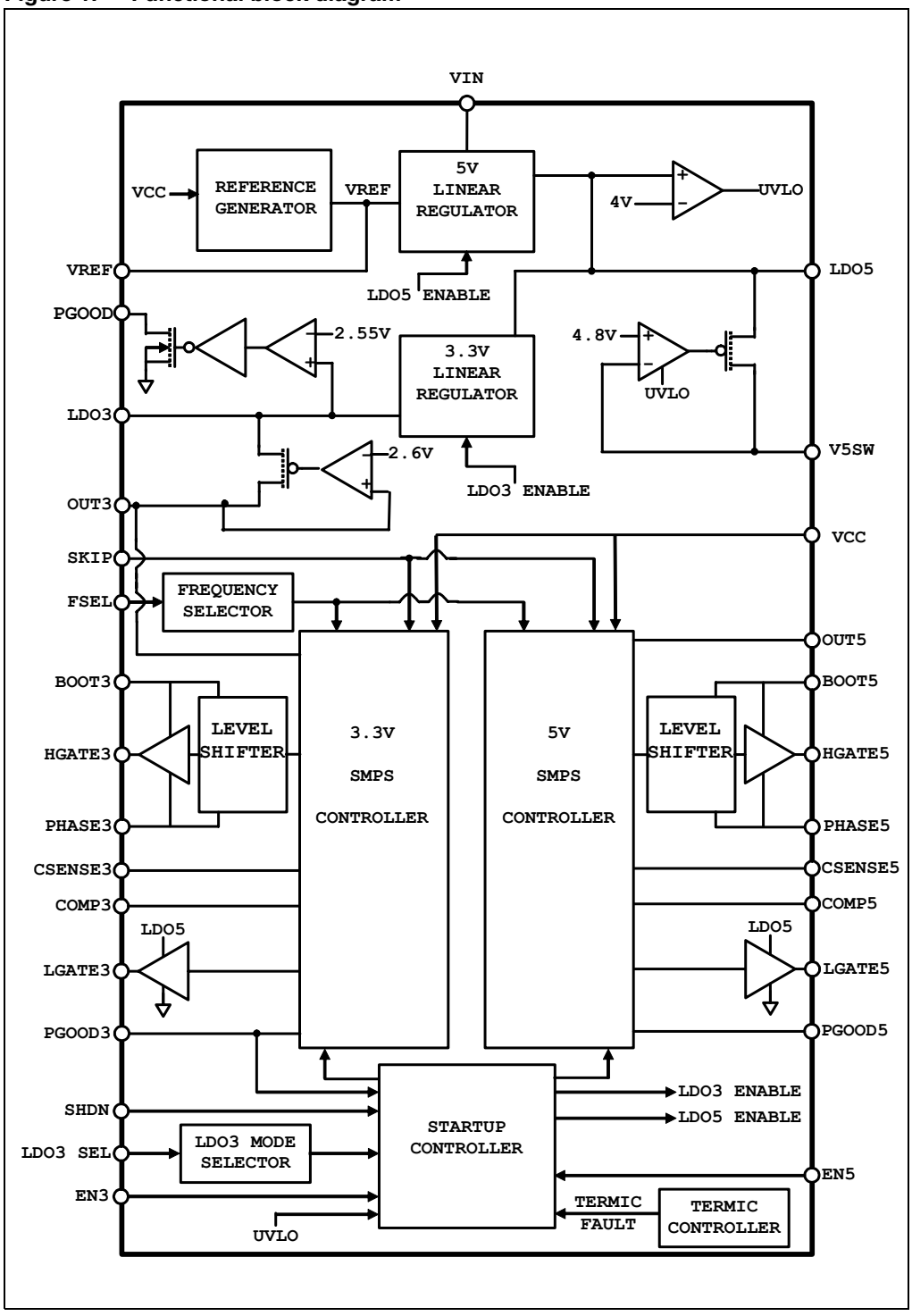
Table 1. Device summary

Order code	Package	Packaging
PM6685	VFQFPN-32 (5 mm x 5 mm)	Tube
PM6685TR		Tape and reel

Contents

1 Block diagram

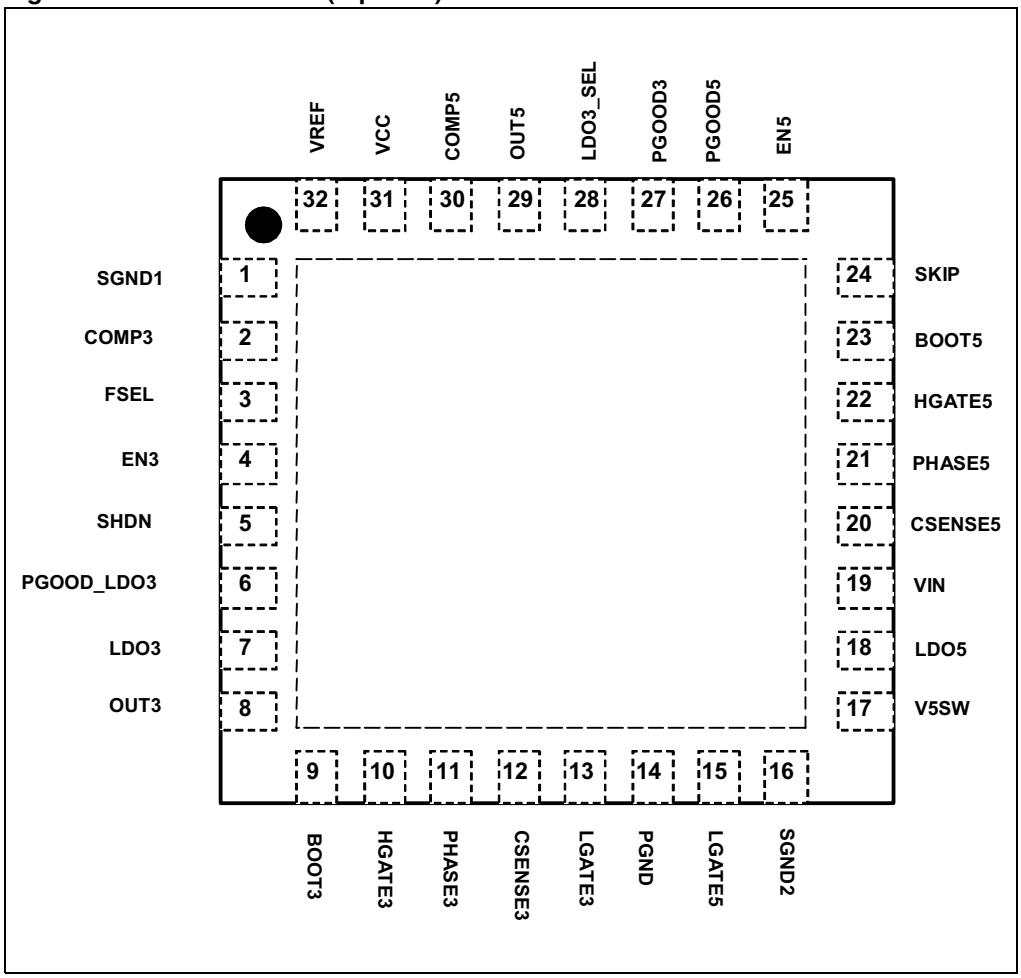
Figure 1. Functional block diagram



2 Pin settings

2.1 Connections

Figure 2. Pin connection (top view)



2.2 Functions

Table 2. Pin functions

Pin	Name	Description
1	SGND1	Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
2	COMP3	DC voltage error compensation pin for the 3.3V switching section.
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing, allowing three different values of switching frequencies for the 5V/3.3V switching sections.
4	EN3	3.3V SMPS enable input. – The 3.3V section is enabled applying a voltage greater than 2.4V to this pin. – The 3.3V section is disabled applying a voltage lower than 0.8V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN3 and EN5 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. – The device switch off if the SHDN voltage is lower than 0.8V (Shutdown mode) – The device switch on if the SHDN voltage is greater than 1.7V. The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	PGOOD LDO3	Power Good signal for the 3.3V linear regulator. This pin is an open drain output. It is shorted to GND if LDO3_SEL pin is at its low level or if the output voltage on LDO3 pin is lower than 2.6V.
7	LDO3	3.3V Linear regulator output. LDO3 can provide 100mA peak current.
8	OUT3	Output voltage sense for the 3.3V switching section.This pin must be directly connected to the output voltage of the switching section.
9	BOOT3	Bootstrap capacitor connection for the switching 3.3V section. It supplies the high-side gate driver.
10	HGATE3	High-side gate driver output for the 3.3V section.
11	PHASE3	Switch node connection and return path for the high side driver for the 3.3V section.
12	CSENSE3	Current sense input for the 3.3V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to set the current limit threshold.
13	LGATE3	Low-side gate driver output for the 3.3V section.
14	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
15	LGATE5	Low-side gate driver output for the 5V section.
16	SGND2	Signal ground for analog circuitry. It must be connected to the signal ground plan of the power supply.
17	V5SW	Internal 5V regulator bypass connection. – If V5SW is connected to OUT5 (or to an external 5V supply) and V5SW is greater than 4.9V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3W (max) switch. – If V5SW is connected to GND, the LDO5 linear regulator is always on.
18	LDO5	5V internal regulator output. It can provide up to 100mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load.

Table 2. Pin functions (continued)

Pin	Name	Description
19	VIN	Device input supply voltage. A bypass filter (4W and 4.7mF) between the battery and this pin is recommended.
20	CSENSE5	Current sense input for the 5V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to set the current limit threshold.
21	PHASE5	Switch node connection and return path for the high side driver for the 5V section.
22	HGATE5	High-side gate driver output for the 5V section.
23	BOOT5	Bootstrap capacitor connection for the 5V section. It supplies the high-side gate driver.
24	SKIP	Pulse skip mode control input. – If the pin is connected to LDO5 the PWM mode is enabled. – If the pin is connected to GND, the pulse skip mode is enabled. – If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33kHz (No-audible pulse skip mode).
25	EN5	5V SMPS enable input. – The 5V section is enabled applying a voltage greater than 2.4V to this pin. – The 5V section is disabled applying a voltage lower than 0.8V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high.
26	PGOOD5	Power Good signal for the 5V section. This pin is an open drain output. The pin is pulled low if the output is disabled or if it is out of approximately +/- 10% of its nominal value.
27	PGOOD3	Power Good signal for the 3.3V section. This pin is an open drain output. The pin is pulled low if the output is disabled or if it is out of approximately +/- 10% of its nominal value.
28	LDO3SEL	Control pin for the 3.3V internal linear regulator. This pin determines three operative modes for the LDO3. – If LDO3_SEL pin is connected to GND the LDO3 output is always disabled. – If LDO3_SEL pin is connected to LDO5 the LDO3 internal regulator is always enabled. – If LDO3_SEL pin is connected to VREF and OUT3 is greater than about 3V, the LDO3 regulator shuts down and the LDO3 pin is be directly connected to OUT3 through a 3W (max) switch.
29	OUT5	Output voltage sense for the 5V switching section.This pin must be directly connected to the output voltage of the switching section.
30	COMP5	DC voltage error compensation pin for the 5V switching section.
31	VCC	Device Supply Voltage pin. It supplies the all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5.
32	VREF	High accuracy output voltage reference (1.230V). It can deliver 50uA. Bypass to SGND with a 100nF capacitor.
33	EXP PAD	Exposed pad.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings

Parameter		Value	Unit
COMPx,FSEL,LDO3_SEL,VREF,SKIP to SGND1,SGND2		-0.3 to VCC + 0.3	V
ENx,SHDN,PGOOD_LDO3,OUTx,PGOODx,VCC to SGND1,SGND2		-0.3 to 6	V
LDO3 to SGND1,SGND2		-0.3 to LDO5 + 0.3	V
LGATEx to PGND		-0.3 (1) to LDO5 + 0.3	V
HGATEx and BOOTx, to PHASEx		-0.3 to 6	V
PHASEx to PGND		-0.6 (2) to 36	V
CSENSEx, to PGND		-0.6 to 42	V
CSENSEx to BOOTx_		-6 to 0.3	V
V5SW, LDO5 _to PGND		-0.3 to 6	V
VIN to PGND		-0.3 to 36	V
PGND to SGND1,SGND2_		-0.3 to 0.3	V
Power Dissipation at Tamb = 25ºC		2	W
Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	VIN pin	±1000	V
	Other pins	±2000	

1. LGATEx to PGND up to -1V for t < 40ns
2. PHASE to PGND up to -2.5V for t < 10ns

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-10 to 125	°C

4 Electrical characteristics

V_{IN} = 12V, T_A = 0°C to 85°C, unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
VIN	Input voltage range	Vout=Vref, LDO5 in regulation FSEL to GND	5.5		28	V
Vcc	IC supply voltage		4.5		5.5	V
V_{V5SW}	Turn-on voltage threshold			4.8	4.9	V
	Turn-off voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
V_{V5SW}	Maximum operating range				5.5	V
Rdson	LDO5 internal bootstrap switch resistance	V5SW > 4.9V		1.8	3	Ω
Rdson	LDO3 internal bootstrap switch resistance	VOUT3 = 3.3V		1.8	3	Ω
	OUT3, OUT5 discharge mode on-resistance			16	25	Ω
	OUT3, OUT5_ discharge mode synchronous rectifier turn-on level		0.2	0.35	0.5	V
Pin	Operating power consumption	V_{OUT5}>5.1V,V_{OUT3}>3.34V V5SW to 5V LDO5, LDO3 no load			4	mW
Ish	V_{IN} shutdown current	SHDN connected to GND,		14	18	µA
Isb	V_{IN} standby current	ENx to GND, V5SW to GND, LDO3_SEL to 5V		270	380	µA
Shutdown section						
V_{SHDN}	Device on threshold		1.2	1.5	1.7	V
	Device off threshold		0.8	0.85	0.9	V
Soft start section						
	Soft start ramp time		2		3.5	ms
Current limit and zero crossing comparator						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
I_{CSENSE}	Input bias current limit			90	100	110	µA
	Comparator offset	V_{CSENSE}-V_{PGND}		-6		6	mV
	Zero crossing comparator offset	V_{PGND}-V_{PHASE}		-1		11	mV
	Fixed negative current limit threshold	V_{PGND}-V_{PHASE}			-120		mV
On time pulse width							
Ton	ON-time duration	FSEL to GND	OUT5=5V	1685	1985	2285	ns
			OUT3=3.3V	780	920	1060	
		FSEL to VREF	OUT5=5V	1115	1315	1515	
			OUT3=3.3V	585	690	795	
		FSEL to LDO5	OUT5=5V	830	980	1130	
			OUT3=3.3V	470	555	640	
OFF time							
T_{OFFMIN}	Minimum off time				400	500	ns
Voltage reference							
V_{REF}	Voltage accuracy	4.2V<V_{LDO5}< 5.5V		1.217	1.230	1.243	V
	Load regulation	-100µA< I_{REF} < 100µA		-4		4	mV
	Undervoltage lockout fault threshold	Falling edge of REF				0.95	V
Integrator							
COMP	Over voltage clamp	Normal mode			250		mV
		Pulse skip mode			60		
	Under voltage clamp				-150		
Line regulation							
		Both SMPS, 6V<Vin<28V(1)			0.004		%/V
LDO5 linear regulator							
V_{LDO5}	LDO5 linear output voltage	6V<VIN<28V, 0<I_{LDO5}<50mA		4.9	5.0	5.1	V
	LDO5 line regulation	6V< VIN < 28V, I_{LDO5} =50mA , LDO3_SEL tied to GND				0.004	%/V
I_{LDO5}	LDO5 current limit	V_{LDO5} > UVLO, I_{LDO3}=0A V_{OUT5}>5.1V, V_{OUT3}>3.34V		270	350	400	mA
UVLO	Under voltage lockout of LDO5			3.94	4	4.13	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
LDO3 linear regulator						
V_{LDO3}	LDO3 linear output voltage	0.5mA<I_{LDO3}<50mA	3.23	3.3	3.37	V
I_{LDO3}	LDO3 current limit	V_{LDO5} > UVLO	130	165	200	mA
High and low gate drivers						
	HGATE Driver On-resistance	HGATEx high state (pull-up)		2.0	3	Ω
		HGATEx low state (pull-down)		1.6	2.7	Ω
	LGATE Driver On-resistance	LGATEx high state (pull-up)		1.4	2.1	Ω
		LGATEx low state (pull-down)		0.8	1.2	Ω
PGOOD pins UVP/OVP protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF.	113	116	120	%
UVP	Under voltage threshold		66	70	72	%
PGOOD3,5	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		90	92	94	%
$I_{PGOOD3,5}$	PGOOD leakage current	$V_{PGOOD3,5}$ forced to 5.5V			1	uA
$V_{PGOOD3,5}$	Output low voltage	ISink = 4mA		150	250	mV
PGOOD LDO3	Rising voltage threshold			77.7	81.1	%
	Falling voltage threshold		72.1	76.6		%
	Hysteresis		20	30		mV
I_{PGOOD_LDO3}	PGOOD leakage current	$V_{PGOOD\ LDO3}$ forced to 5.5V			1	uA
V_{PGOOD_LDO3}	Output low voltage	ISink = 4mA		150	250	mV
Thermal shutdown						
T_{SDN}	Shutdown temperature			150		°C
Power management pins						
EN3,5	SMPS disabled threshold	(2)	0.8			V
	SMPS enabled threshold	(2)			2.4	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
FSEL	Frequency selection range	Low level(2)			0.5	V
		Middle level(2)	1.0		V_{LDO5}-1.5	
		High level(2)	V_{LDO5}-0.8			
LDO3 SEL	3.3V linear regulator selection pin	Always-off level(2)			0.5	
		Bootstrap level(2)	1.0		V_{LDO5}-1.5	
		Always-on level(2)	V_{LDO5}-0.8			
SKIP	Pulse skip mode	(2)			0.5	V
	PWM mode	(2)	1.0		V_{LDO5}-1.5	
	Frequency clamp mode	(2)	V_{LDO5}-0.8			
	Input leakage current	$V_{EN3,4}$= 0 to 5V			1	µA
		V_{SKIP}= 0 to 5V			1	
		V_{SHDN}= 0 to 5V			0.1	
		V_{FSEL}= 0 to 5V			1	
		V_{LDO3_SEL}= 0 to 5V			1	

1. by demonstration board test
2. by design

5 Typical operating characteristics

FSEL = GND (200/300 kHz), SKIP = GND (skip mode), LDO3_SEL = VREF, V5SW = OUT5, input voltage VIN = 12 V, SHDN, EN3 and EN5 high, no load unless specified.

Figure 3. 5 V output efficiency vs load current

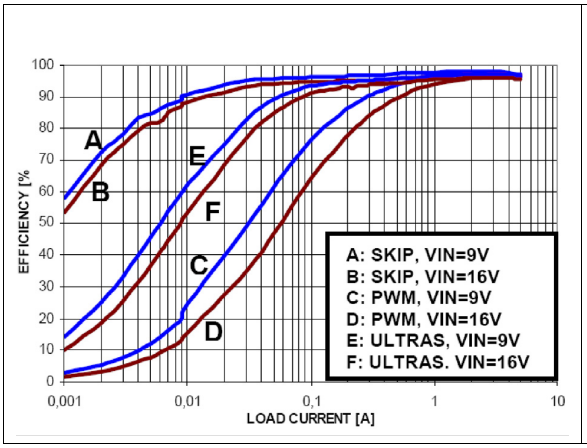


Figure 4. 3.3 V output efficiency vs load current

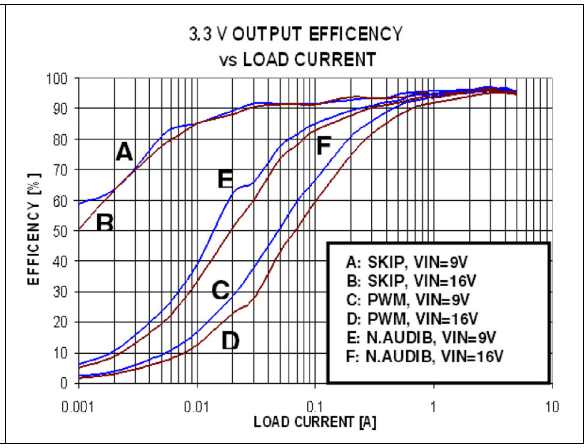


Figure 5. PWM no load input battery vs input voltage

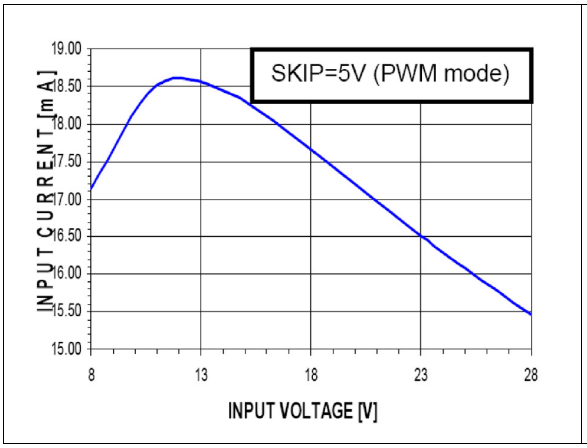


Figure 6. Skip no load battery current vs input voltage

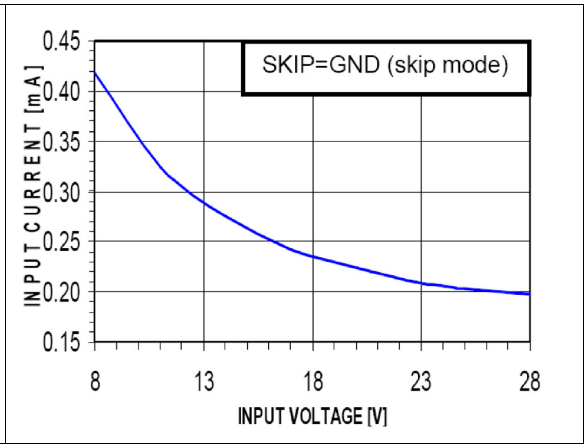


Figure 7. Standby mode input battery current vs input voltage

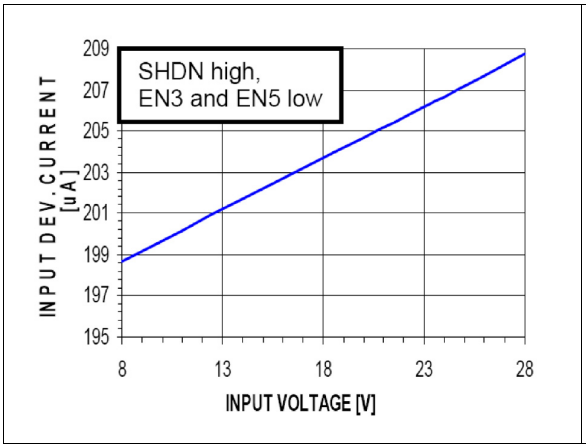


Figure 8. Shutdown mode input device current vs input voltage

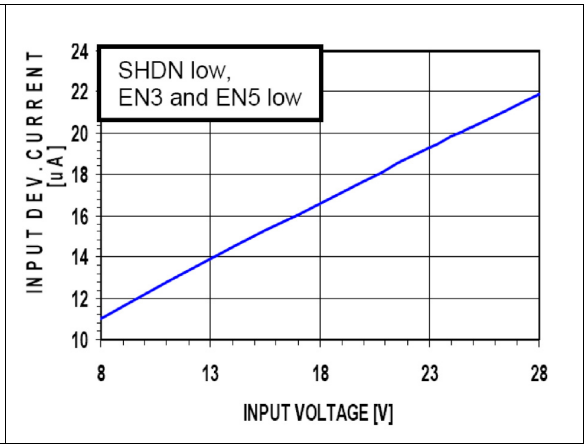


Figure 9. 5V switching frequency vs load current

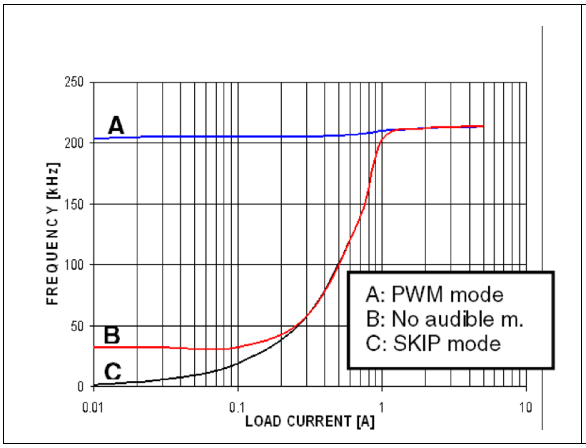


Figure 10. 3.3V switching frequency vs load current

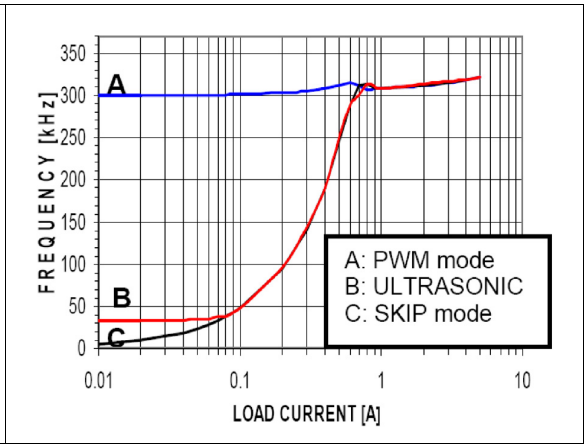


Figure 11. LDO5 vs output voltage

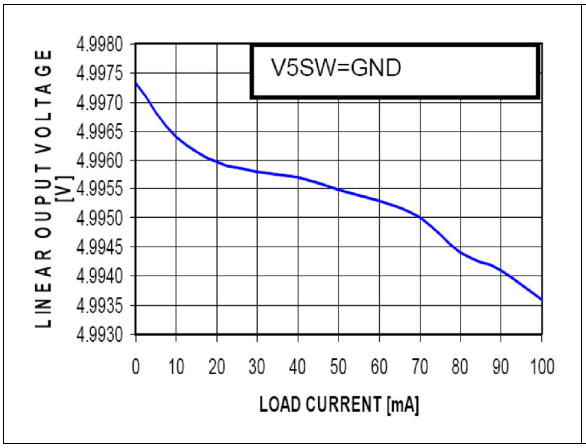


Figure 12. LDO3 vs output voltage

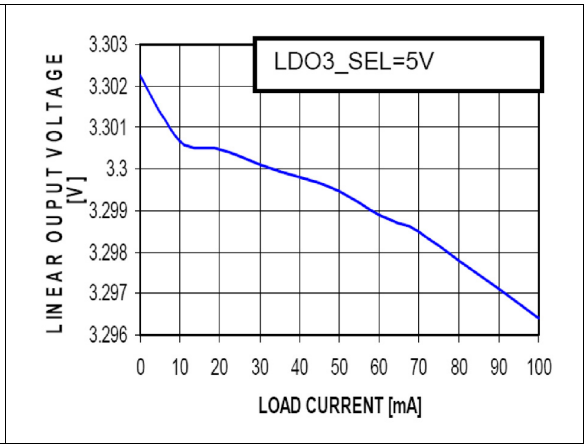


Figure 13. 5V voltage regulation vs load current

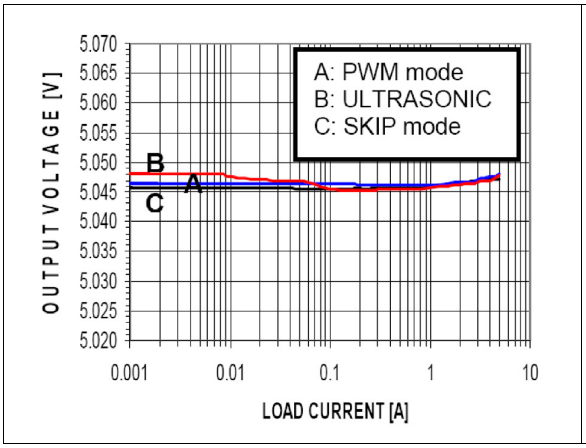


Figure 14. 3.3 V voltage regulation vs load current

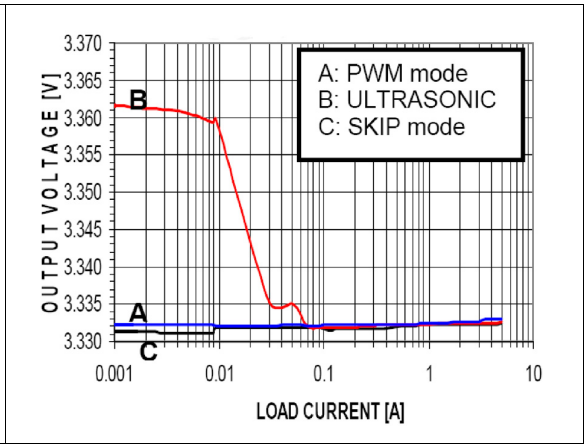


Figure 15. Voltage reference vs load current

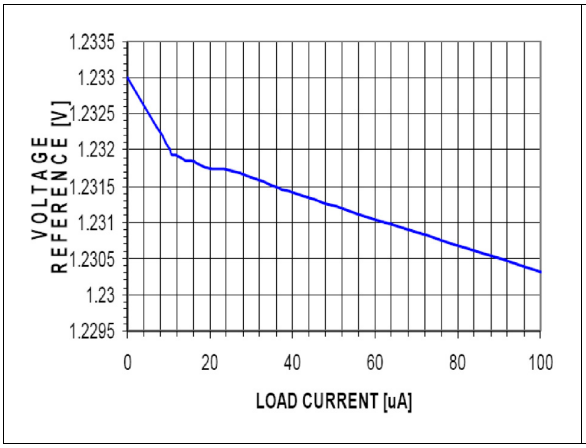


Figure 16. OUT5, LDO3 and LDO5 Power-Up

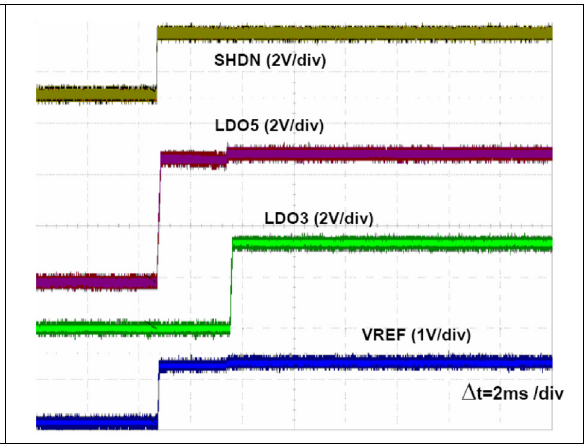


Figure 17. 5 V PWM load transient

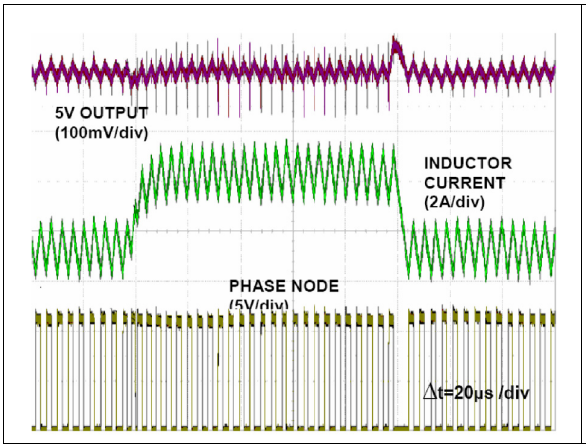


Figure 18. 3.3 V PWM load transient

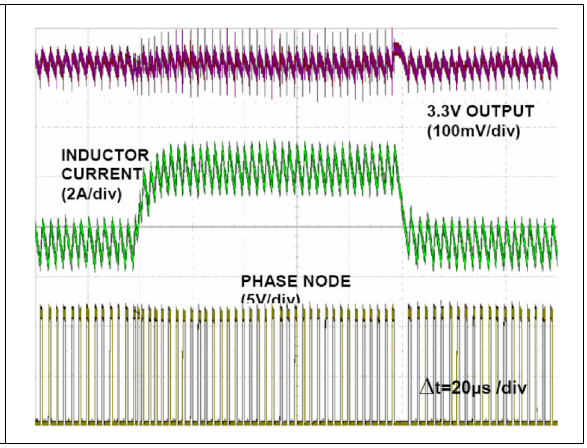


Figure 19. 5 V soft start (0.75 Ω load)

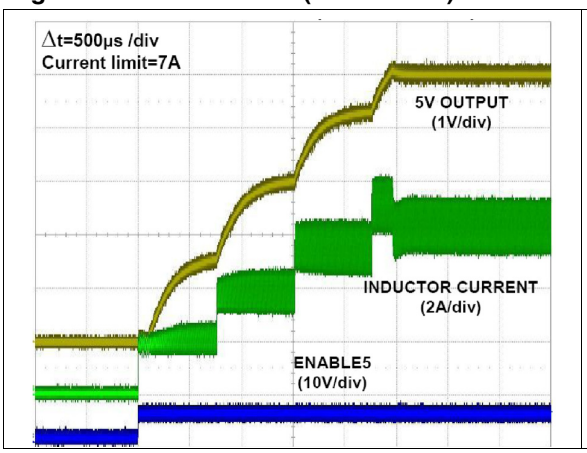


Figure 20. 3.3 V soft start (0.55 Ω load)

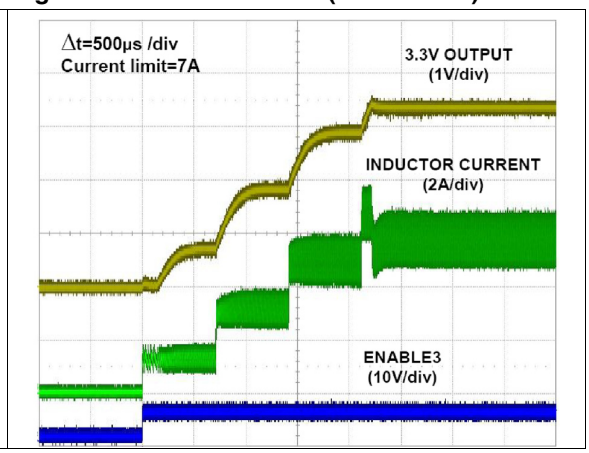


Figure 21. 5 V soft end (no load)

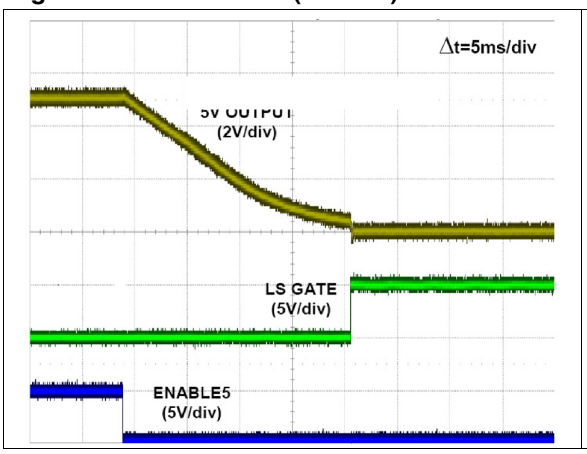


Figure 22. 3.3 V soft end (no load)

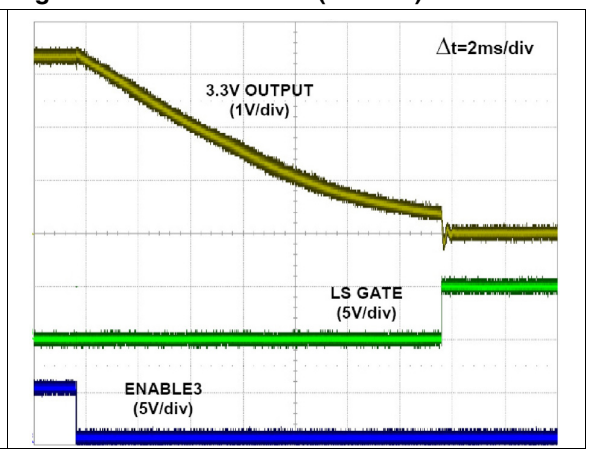


Figure 23. 5 V soft end (1 Ω load)

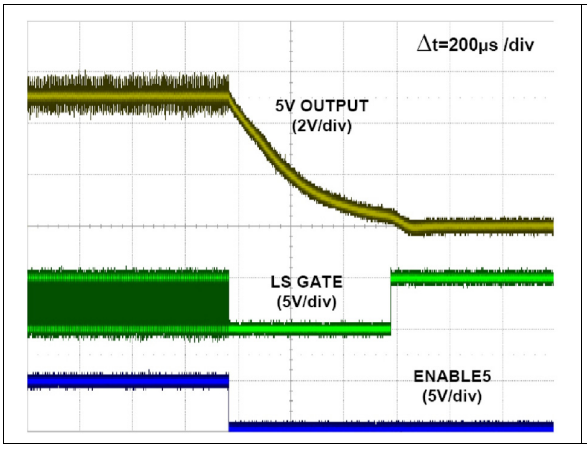


Figure 24. 3.3 V soft end (1 Ω load)

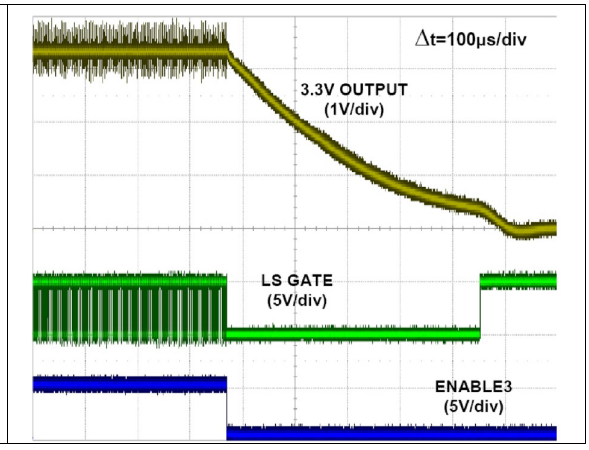


Figure 25. 5 V no audible skip mode

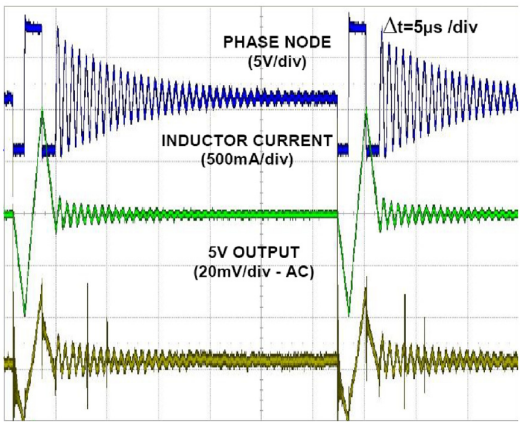
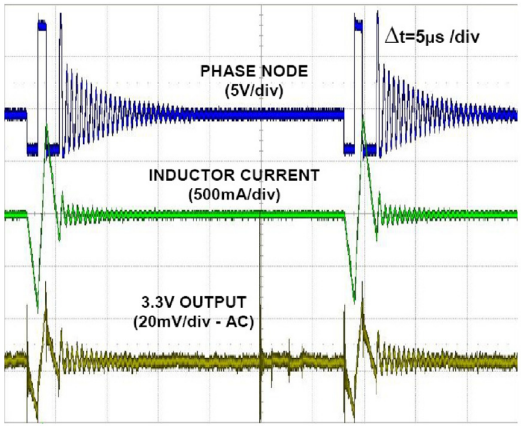
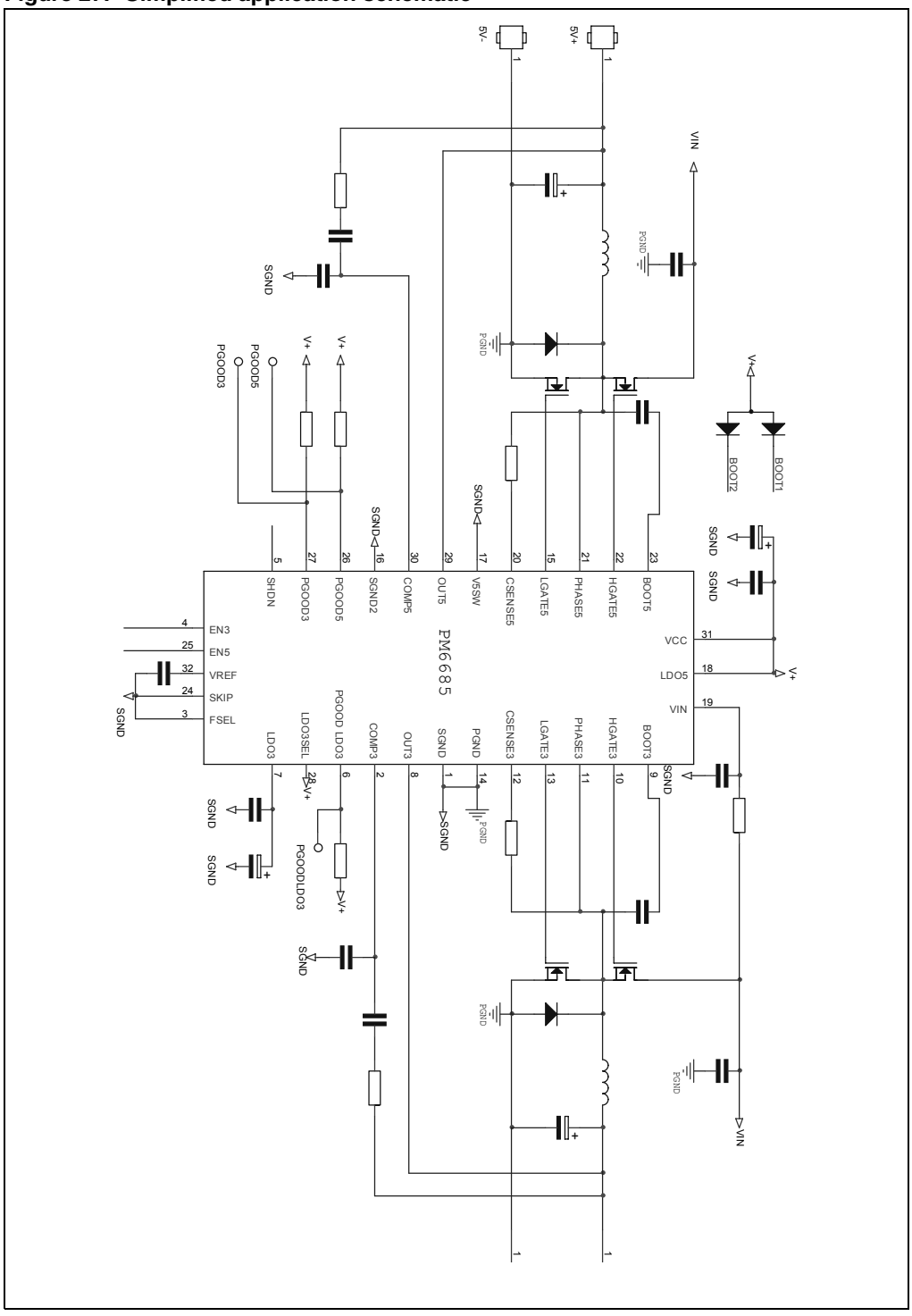


Figure 26. 3.3 V no audible skip mode



6 Application schematic

Figure 27. Simplified application schematic



7 Device description

The PM6685 is a dual step-down controller dedicated to provide logic voltages for notebook computers.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 27 on page 18*. The PM6685 regulates two fixed output voltages: 5 V and 3.3 V. The switching frequency of the two sections can be adjusted to approximately 200/300 kHz, 300/400 kHz or 400/500 kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected. The PM6685 includes also two linear regulators (LDO5 and LDO3) that allow the shutdown of the respective switching sections in low consumption status. On the other hand, to maximize the efficiency in higher consumption status, the linear regulators can be turned off and their outputs can be supplied directly from the switching outputs. The PM6685 provides protection versus overvoltage, undervoltage and overtemperature as well as power good signals for monitoring purposes. An external 1.230 V reference is available.

7.1 Constant on time PWM control

If the SKIP pin is tied to 5 V, the device works in PWM mode. Each power section has an independent on time control.The PM6685 implements a pseudo-fixed switching frequency, constant on time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage VOUT, sensed at the OUT5/OUT3 pins, and inversely proportional to the input voltage VIN, sensed at the VIN pin, as follows:

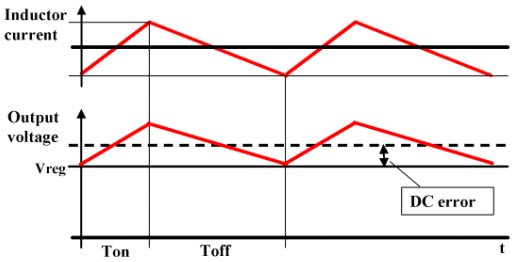
Equation 1

$$T_{ON} = K \times \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages.

When the output voltage goes lower than the regulated voltage Vreg, the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. *Figure 28 on page 20* shows the inductor current and the output voltage waveforms in PWM mode.

Figure 28. Constant on time PWM control



The duty cycle D of the buck converter in steady state is:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency f_{SW}:

Equation 3

$$f_{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{ON} \times \frac{V_{OUT}}{V_{IN}}} = 1/K_{ON}$$

As mentioned the steady state switching frequency is theoretically independent from battery voltage and from output voltage. Actually the frequency depends on parasitic voltage drops that are present during the charging path (high side switch resistance, inductor resistance (DCR)) and discharging path (low side switch resistance, DCR). As a result the switching frequency increases as a function of the load current. Standard switching frequency values can be selected for both sections by pin FSEL as shown in the following table:

Table 6. FSEL pin selection

FSEL	SMPS 5V		SMPS 3.3V	
	Frequency	K_{ON}	Frequency	K_{ON}
SGND	212kHz	4,7µs	297,6kHz	3.36µs
VREF	323kHz	3µs	400kHz	2.5µs
LDO5	432kHz	2.31µs	500kHz	2.0µs

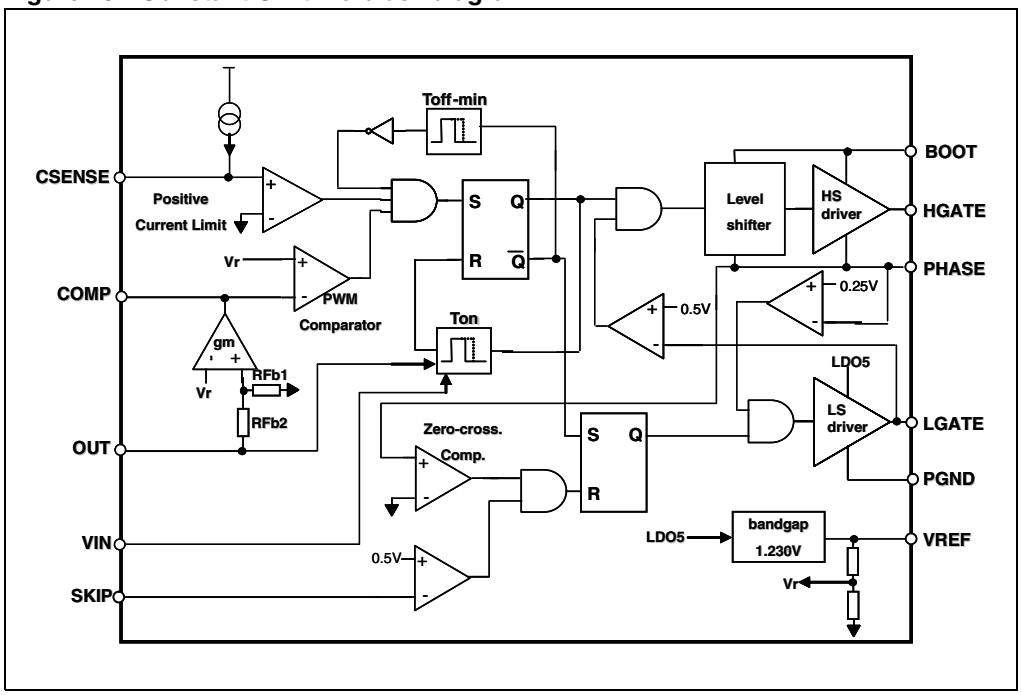
The values in the table are measured with V_{in} =12 V, operation mode = PWM and I_{load} = 2 A. The other output are unloaded.

7.2 Constant on time architecture

Figure 29 on page 21 shows the simplified block diagram of a constant on time controller. A minimum off-time constrain (380 ns typ) is introduced to allow inductor valley current sensing on the synchronous switch. A minimum on-time(150 ns typ) is also introduced to assure the start-up switching sequence.

PM6685 has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out. Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management. When the negative input voltage at the PWM comparator, which is a scaled-down replica of the output voltage ripple (see the R_{fb1}/R_{fb2} divider in *Figure 29*), reaches the valley limit (determined by internal reference V_r=0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 29. Constant ON-time block diagram

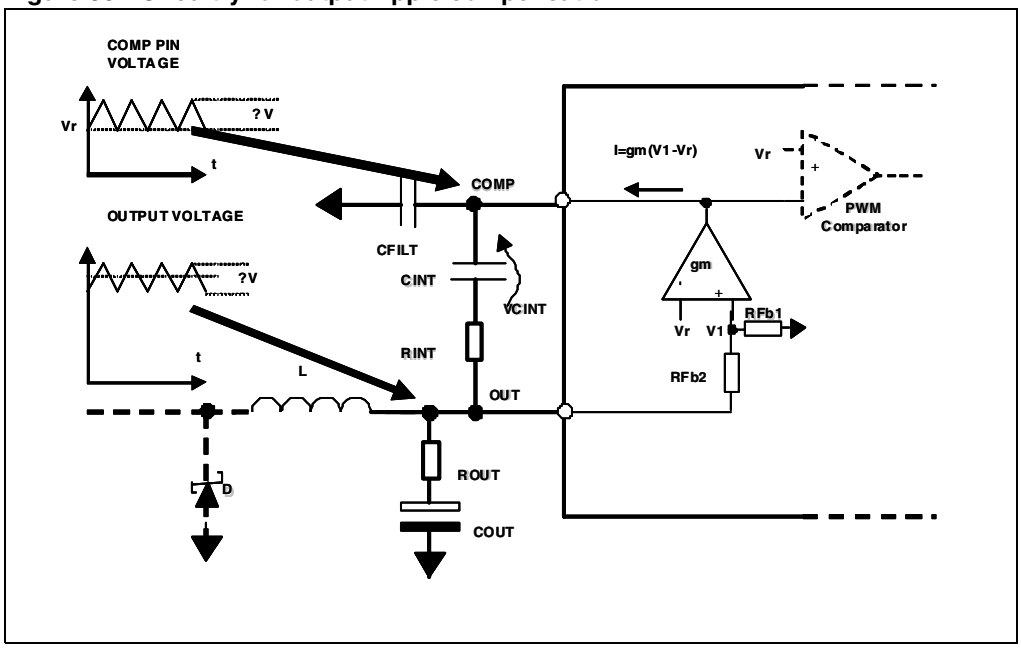


7.3 Output ripple compensation

In a classic constant on time control, the system regulates the valley value of the output voltage and not the average value, as shown in *Figure 28 on page 20*. In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP5/COMP3(for the 5 V and 3.3 V sections respectively) pin through a capacitor C_{INT} as in *Figure 30 on page 22*.

Figure 30. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors, which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, C_{INT} provides an AC path for the output ripple. In steady state, the voltage on COMP5/COMP3 pin is the sum of the reference voltage V_r and the output ripple (see *Figure 30*). In fact when the voltage on the COMP pin reaches V_r, a fixed Ton begins and the output increases.

For example, we consider V_{OUT}=5 V with an output ripple of ΔV=50m V. Considering C_{INT}>>C_{FILT}, the C_{INT} DC voltage drop V_{CINT} is about 5 V-Vr+25 mV=4.125 V. C_{INT} ensures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of Vr+25 mV =925 mV.

For more details about the output ripple compensation network, see the paragraph "*Closing the integrator loop*" in the *Design guidelines*.

7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

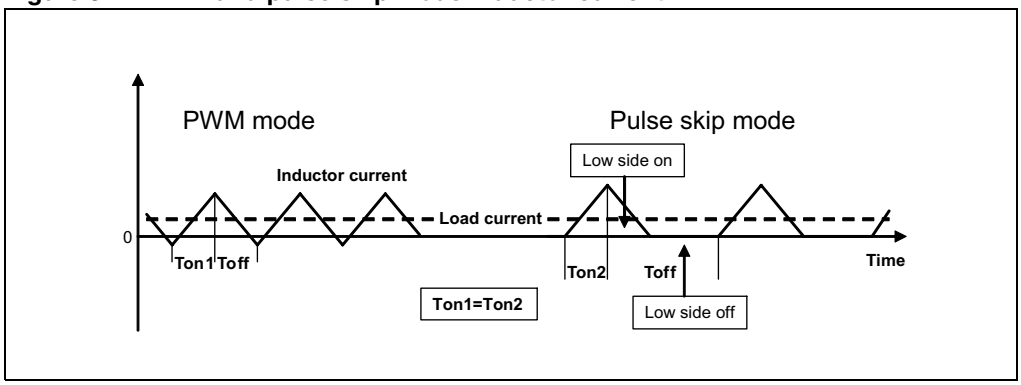
At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 4

$$ILOAD(SKIP) = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

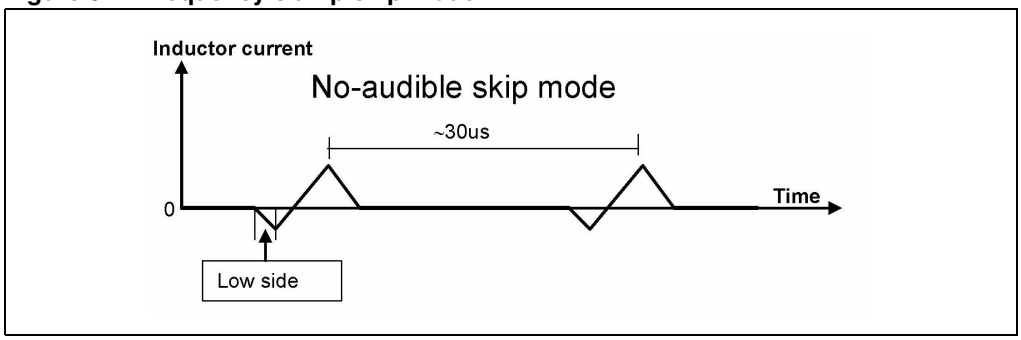
Figure 31. PWM and pulse skip mode inductor current



7.5 No-audible skip mode

If SKIP pin is tied to V_{REF}, a no-audible skip mode with a minimum switching frequency of 33 kHz is enabled. At light load condition, If there is not a new switching cycle within a 30 µs (typ.) period, a no-audible skip mode cycle begins.

Figure 32. Frequency clamp skip mode



The low side switch is turned on until the output voltage crosses about Vreg+1%. Then the high side MOSFET is turned on for a fixed on time period. Afterwards the low side switch is enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33 kHz. As a consequence of the control, the regulated voltage can be slightly higher than Vreg (up to 1%).

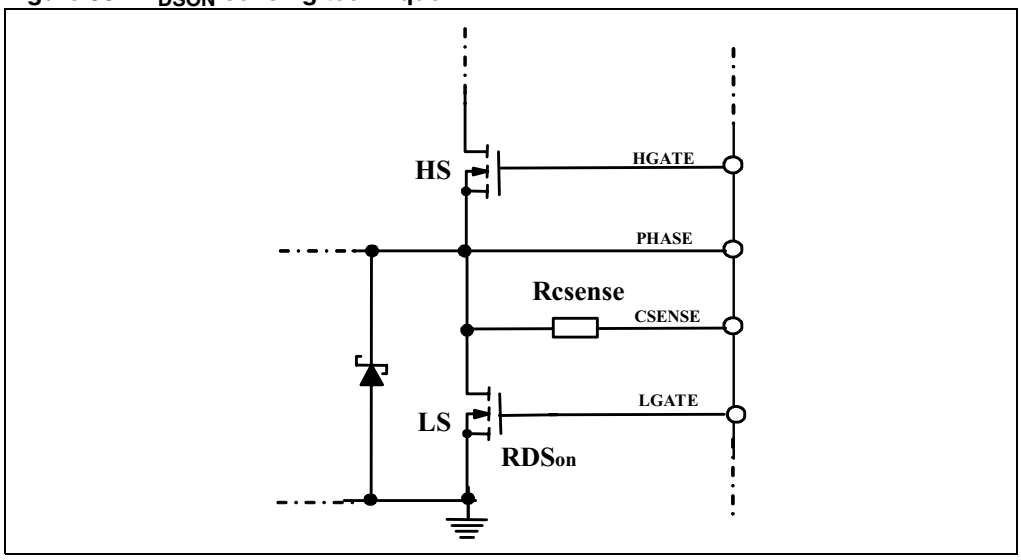
If, due to the load, the frequency is higher than 33 kHz, the device works like in skip mode.

No-audible skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

7.6 Current limit

The current-limit circuit employs a “valley” current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element is the low side MOSFET on-resistance(*Figure 33*)

Figure 33. R_{DSON} sensing technique



An internal 100 µA ΔI_L current source (I_{CSENSE}) is connected to C_{SENSE} pin and determines a voltage drop on R_{CSENSE}. If the voltage across the sensing element is greater than this voltage drop, the controller doesn't initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

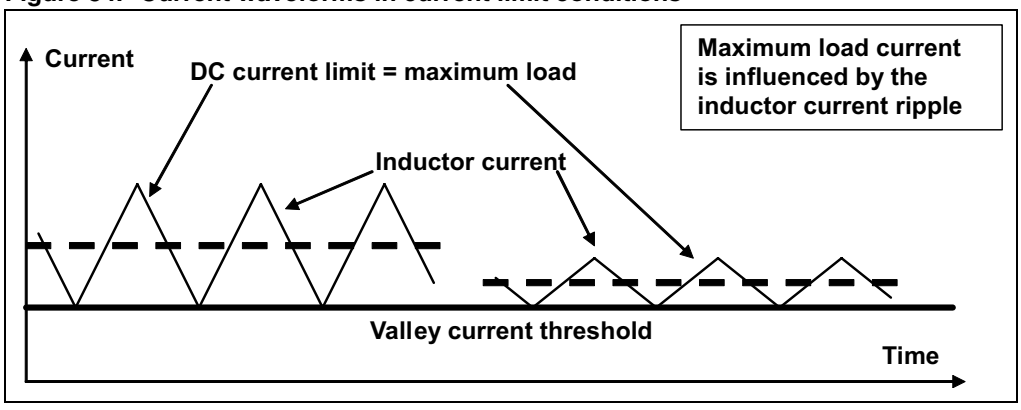
Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current. Moreover the maximum output current is equal to the valley current limit plus half of the inductor ripple current:

Equation 5

$$I_{LOAD}(max) = I_{Lvalley} + \frac{\Delta I_L}{2}$$

The output current limit depends on the current ripple, as shown in *Figure 34 on page 24*:

Figure 34. Current waveforms in current limit conditions



Being fixed the valley threshold, the greater the current ripple is, greater the DC output current is

The valley current limit can be set with resistor R_{CSENSE}:

Equation 6

$$R_{CSENSE} = \frac{R_{DSon} \times I_{Lvalley}}{I_{CSENSE}}$$

Where I_{CSENSE} = 100 µA, R_{DSon} is the drain-source on resistance of the low side switch. Consider the temperature effect and the worst case value in R_{DSon} calculation.

The accuracy of the valley current threshold detection depends on the offset of the internal comparator (ΔV_{OFF}) and on the accuracy of the current generator(ΔI_{CSENSE}):

Equation 7

$$\frac{\Delta I_{Lvalley}}{I_{Lvalley}} = \frac{\Delta I_{CSENSE}}{I_{CSENSE}} + \left[\frac{\Delta V_{OFF}}{R_{CSENSE} \times I_{CSENSE}} \times 100\right] + \frac{\Delta R_{CSENSE}}{R_{CSENSE}} + \frac{\Delta R_{SNS}}{R_{SNS}}$$

Where RSNS is the sensing element (R_{DSon}).

PM6685 provides also a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between PHASE and SGND pins, comparing the magnitude drop on the PHASE node during the conduction time of the low side MOSFET with an internal fixed voltage of 120 mV.

If the current is sensed on the low side MOSFET, the negative valley-current limit INEG (if the device works in PWM mode) is given by:

Equation 8

$$I_{NEG} = \frac{120mV}{R_{DSon}}$$

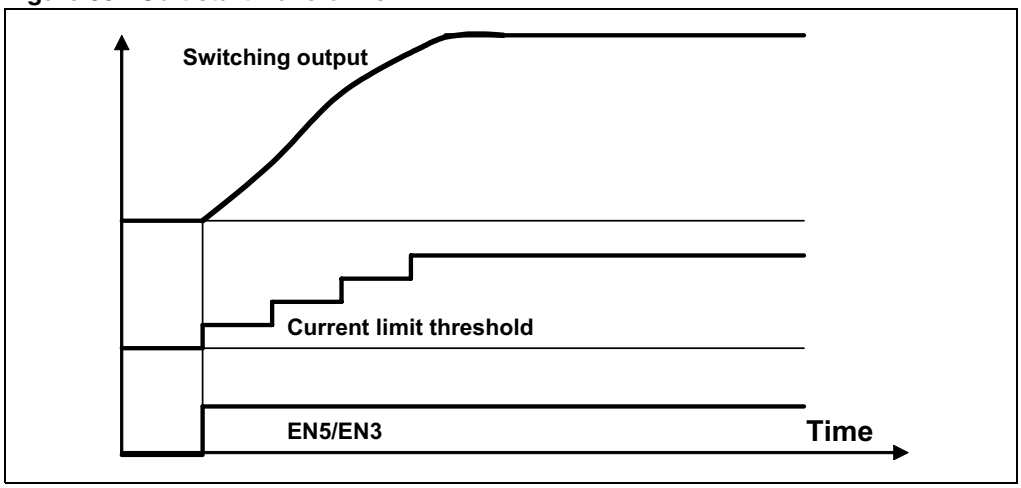
7.7 Soft start and soft end

Each switching section is enabled separately by asserting high EN5/EN3 pins respectively. In order to realize the soft start, at the startup the overcurrent threshold is set 25% of the nominal value and the undervoltage protection (see related sections) is disabled. The controller starts charging the output capacitor working in current limit. The overcurrent threshold is increased from 25% to 100% of the nominal value with steps of 25% every 700 µs (typ.). After 2.8 ms (typ.) the undervoltage protection is enabled. The soft start time is not programmable. A minimum capacitor C_{INT} is required to ensure a soft start without any overshoot on the output:

Equation 9

$$C_{INT} \geq \frac{6uA}{\frac{I_{Lvalley}}{4} + \frac{\Delta I_L}{2}} \times C_{out}$$

Figure 35. Soft start waveforms



When a switching section is turned off(EN5/EN3 pins low), the controller enters in soft end mode. The output capacitor is discharged through an internal 16 Ω P-MOSFET switch; when the output voltage reaches 0.3 V, the low-side MOSFET turns on, keeping the output to ground. The soft end time also depends on load condition.

7.8 Gate drivers

The integrated high-current drivers allow to use different power MOSFETs. The high side driver MOSFET uses a bootstrap circuit which is indirectly supplied by LDO5 output. The BOOT and PHASE pins work respectively as supply and return rails for the HS driver.

The low side driver uses the internal LDO5 output for the supply rail and PGND pin as return rail.

An important feature of the gate drivers is the adaptive anti-cross conduction protection, which prevents high side and low side MOSFETs from being on at the same time. When the high side MOSFET is turned off the voltage at the phase node begins to fall. The low side MOSFET is turned on when the voltage at the phase node reaches an internal threshold. When the low side MOSFET is turned off, the high side remains off until the LGATE pin voltage goes approximately under 1 V.

The power dissipation of the drivers is a function of the total gate charge Qg of the external power MOSFETs and of the switching frequency, as shown in the following equation:

$$P_{driver} = V_{driver} \times Q_g \times f_{sw}$$

Where V_{driver} is the 5 V driver supply.

7.9 Reference voltage and bandgap

The 1.230 V (typ.) internal bandgap voltage is accurate to ±1% over the temperature range. It is externally available (VREF pin) and can supply up to ±100µA and can be used as a voltage threshold for the multifunction pins FSEL, SKIP and LDO3_SEL to select the appropriate working mode. Bypass VREF to ground with a 100nF minimum capacitor.

If VREF goes below 0.87 V (typ.), the system detects a fault condition and all the circuitry is turned off. A toggle on the input voltage (power on reset) or a toggle on SHDN pin is necessary to restart the device.

An internal divider of the bandgap provides a voltage reference Vr of 0.9 V. This voltage is used as reference for the linear and the switching regulators outputs. The overvoltage protection, the undervoltage protection and the power good signals are referred to Vr.

7.10 Internal linear regulators

The PM6685 has two linear regulators providing respectively 5 V(LDO5) and 3.3 V(LDO3) at ±2% accuracy. High side drivers, low side drivers and most of internal circuitry are supplied by LDO5 output through VCC pin (an external RC filter may be applied between LDO5 and VCC). Both linear regulators can provide an average output current of 50 mA and a peak output current of 100 mA. Bypass both LDO5 and LDO3 outputs with a minimum 1 µF ceramic capacitor and a 4,7 µF tantalum capacitor (ESR < 2 Ω). If the 5 V output goes below 4V, the system detects a fault condition and all the circuitry is turned off. A power on reset or a toggle on SHDN pin is necessary to restart the device.

V5SW pin allows to keep the 5 V linear regulator always active or to enable the internal bootstrap-switch over function: if the 5 V switching output is connected to V5SW, when the voltage on V5SW pin is above 4.8 V, an internal 3.0 Ω max p-channel MOSFET switch connects V5SW pin to LDO5 pin and simultaneously LDO5 shuts down. This configuration allows to achieve higher efficiency. V5SW can be connected also to an external 5 V supply. LDO5 regulator turns off and LDO5 is supplied externally. If V5SW is connected to ground, the internal 5 V regulator is always on and supplies LDO5 output.

Table 7. V5SW multifunction pin

V5SW	Description
GND	The 5V linear regulator is always turned on and supplies LDO5 output.
Switching 5V output	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the switching 5V output.
External 5V supply	The 5V linear regulator is turned off when the voltage on V5SW is above 4.8V and LDO5 output is supplied by the external 5V.

The 3.3 V linear regulator is supplied by LDO5 output.

LDO3_SEL pin allows to keep 3.3 V linear regulator always enabled, always disabled or to enable the internal bootstrap-switch over function. According to *Table 7*:

- If LDO3_SEL is connected to VREF pin, when the power good signal of the 3.3 V switching output voltage PGOOD3(see related sections) is high, the internal linear

regulator is turned off and LDO3 output is connected directly to OUT3 pin through an internal 3 Ω max p-channel MOSFET switch.

- If LDO3_SEL is connected to 5V, the internal 3.3 V regulator is always on and supplies LDO3 output.
- If LDO3_SEL is connected to ground, the internal 3.3 V regulator is always off and LDO3 output is clamped to ground.

Table 8. LDO3_SEL multifunction pin

LDO3_SEL	Description
GND	The 3.3V linear regulator is always turned off.
VREF	The 3.3V linear regulator is turned off when PGOOD3 is high. LDO3 output is supplied by the switching 3.3V output.
LDO5	The 3.3V linear regulator is always turned on and supplies LDO3 output.

7.11 Power up sequencing and operative modes

Let's consider SHDN, EN5 and EN3 low at the beginning. The battery voltage is applied as input voltage. The device is in shutdown mode.

When the SHDN pin voltage is above the shutdown device on threshold(1.5V typ.), the controller begins the power-up sequence. All the latched faults are cleared. LDO5 undervoltage control is blanked for 4 ms and the internal regulator LDO5 turns on. If the LDO5 output is above the UVLO threshold after this time, the device enters in standby mode. The switching outputs are kept to ground by turning on the low side MOSFETs.

When EN5 and EN3 pins are forced high the switching sections begin their soft start sequence.

LDO3 management is independent from the general power up sequence and depends only on LDO3_SEL.

Table 9. Operatives modes

Mode	Conditions	Description
Run	SHDN is high *EN3/EN5* pins are high	Switching regulators are enabled; internal linear regulators outputs are enabled.
Stand	by Both *EN5/EN3* pins are low and *SHDN* pin is high	Internal Linear regulators active (LDO5 is always on while LDO3 depends on *LDO3_SEL* pin). In Standby mode *LGATE5/LGATE3* pins are forced high while *HGATE5/HGATE3* pins are forced low.
Shutdown	*SHDN* is low	All circuits off.

8 Monitoring and protections

8.1 Power good signals

The PM6685 provides three independent power good signals: one for each switching section(PGOOD5/PGOOD3) and the other for the internal linear regulator LDO3(PGOOD_LDO3).

PGOOD5/PGOOD3 signals are low if the output voltage is out of ±10% of the designed set point or during the soft-start, the soft end and when the device works in standby and shutdown mode.

PGOOD_LDO3 signal is low when the output voltage of LDO3 output is lower than its falling voltage threshold(2.6 V typ.). Each power good pin is an open-drain output and can sink current up to 4 mA.

8.2 Thermal protection

The PM6685 has a thermal protection to preserve the device from overheating. The thermal shutdown occurs when the die temperature goes above +150°C. In this case all internal circuitry is turned off and the power sections are turned off after the discharge mode.

A power on reset or a toggle on the SHDN pin is necessary to restart the device.

8.3 Overvoltage protection

When the switching output voltage is about 115% of its nominal value, a latched overvoltage protection occurs. In this case, the synchronous rectifier immediately turns on while the high-side MOSFET turns off. The output capacitor is rapidly discharged and the load is preserved from being damaged. The overvoltage protection is also active during the soft start. Once an overvoltage protection has been detected, a toggle on SHDN, EN3/EN5 pins or a power on reset is necessary to exit from the latched state.

8.4 Undervoltage protection

When the switching output voltage is below 70% of its nominal value, a latched undervoltage protection occurs. In this case the switching section is immediately disabled and both switches are open. The controller enters in soft end mode and the output is eventually kept to ground, turning low side MOSFET on. The undervoltage circuit protection is enabled only at the end of the soft-start. Once an overvoltage protection has been detected, a toggle on SHDN, EN5/EN3 pin or a power on reset is necessary to clear the undervoltage fault and starts with a new soft-start phase.

Table 10. Protections and operatives modes

Mode	Conditions	Description
Overvoltage protection	OUT5/OUT3 > 115% of the nominal value	*LGATE5*/LGATE3 pin is forced high, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN5/EN3*
Undervoltage protection	OUT5/OUT3 < 70% of the nominal value	*LGATE5/LGATE3* is forced high after the soft end mode, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN5/EN3*
Thermal shutdown	T_J > +150°C	All circuitry off. Exit by a POR on *VIN* or toggling *SHDN*.

8.5 Design guidelines

The design of a switching section starts from two parameters:

- Input voltage range: in notebook applications it varies from the minimum battery voltage, VINmin to the AC adapter voltage, VINmax.
- Maximum load current: it is the maximum required output current, ILOAD(max).

8.6 Switching frequency

It's possible to set 3 different working frequency ranges for the two sections: 200 kHz/300 kHz, 400 kHz/500 kHz, 600 kHz/700 kHz with FSEL pin.

Switching frequency mainly influences two parameters:

- Inductor size: for a given saturation current and RMS current, greater frequency allows to use lower inductor values, which means smaller size.
- Efficiency: switching losses are proportional to frequency. High frequency generally involves low efficiency.

8.7 Inductor selection

Once that switching frequency is defined, inductor selection depends on the desired inductor ripple current and load transient performance.

Low inductance means great ripple current and could generate great output noise. On the other hand, low inductor values involve fast load transient response.

A good compromise between the transient response time, the efficiency, the cost and the size is to choose the inductor value in order to maintain the inductor ripple current ΔIL between 20% and 50% of the maximum output current ILOAD(max). The maximum ΔIL occurs at the maximum input voltage. With this considerations, the inductor value can be calculated with the following relationship:

Equation 10

$$L = \frac{V_{IN} - V_{OUT}}{f_{sw} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where fsw is the switching frequency, VIN is the input voltage, VOUT is the output voltage and ΔIL is the selected inductor ripple current.

In order to prevent overtemperature working conditions, inductor must be able to provide an RMS current greater than the maximum RMS inductor current ILRMS:

Equation 11

$$I_{LRMS} = \sqrt{(I_{LOAD}(max))^2 + \frac{(\Delta I_L(max))^2}{12}}$$

Where ΔIL(max) is the maximum ripple current:

Equation 12

$$\Delta I_L(max) = \frac{V_{INmax} - V_{OUT}}{f_{sw} \times L} \times \frac{V_{OUT}}{V_{INmax}}$$

If hard saturation inductors are used, the inductor saturation current should be much greater than the maximum inductor peak current Ipeak:

Equation 13

$$Ipeak = I_{LOAD}(max) + \frac{\Delta I_L(max)}{2}$$

Using soft saturation inductors it's possible to choose inductors with saturation current limit nearly to Ipeak.

Below there is a list of some inductor manufacturers.

Table 11. Inductor manufacturer

Manufacturer	Series	Inductor value (µH)	RMS current (A)	Saturation current (A)
COILCRAFT	SER1360	4 to 8	6 to 8.6	7 to 12
COILCRAFT	MLC	2.2 to 4.5	13.6 to 8.8	11.5 to 17
TDK	RLF12560	2.7 to 10	7.5 to 11.5	7.5 to 14.4

8.8 Output capacitor

The selection of the output capacitor is based on the ESR value Rout and the voltage rating rather than on the capacitor value Cout.

The output capacitor has to satisfy the output voltage ripple requirements. Lower inductor value can reduce the size of the choke but increases the inductor current ripple ΔIL.

Since the voltage ripple VRIPPLEout is given by:

Equation 14

$$V_{RIPPLEout} = R_{out} \times \Delta I_L$$

A low ESR capacitor is required to reduce the output voltage ripple. Switching sections can work correctly even with 20 mV output ripple.

However, to reduce jitter noise between the two switching sections it's preferable to work with an output voltage ripple greater than 30 mV. If lower output ripple is required, a further compensation network is needed (see *Closing the integrator loop* paragraph).

Finally the output capacitor choice deeply impacts on the load transient response (see *Load transient response* paragraph). Below there is a list of some capacitor manufacturers.

Table 12. Output capacitor manufacturer

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)	ESR max (mΩ)
SANYO	POSCAP TPB,TPD	150 to 330	4 to 6.3	35 to 65
PANASONIC	SPCAP UD, UE	150 to 220	4 to 6.3	9 to 18

8.9 Input capacitors selection

In a buck topology converter the current that flows into the input capacitor is a pulsed current with zero average value. The input RMS current of the two switching sections can be roughly estimated as follows:

Equation 15

$$I_{CinRMS} = \sqrt{D_1 \times I_1^2 \times (1 - D_1) + D_2 \times I_2^2 \times (1 - D_2)}$$

Where D1, D2 are the duty cycles and I1, I2 are the maximum load currents of the two sections.

Input capacitor should be chosen with an RMS rated current higher than the maximum RMS current given by both sections.

Tantalum capacitors are good in term of low ESR and small size, but they occasionally can burn out if subjected to very high current during the charge. Ceramic capacitors have usually a higher RMS current rating with smaller size and they remain the best choice.

Below there is a list of some ceramic capacitor manufacturers.

Table 13. Input capacitor manufacturer

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TAYIO YUDEN	UMK325BJ106KM-T10	10	50
TAYIO YUDEN	GMK325BJ106MN	10	35
TDK	C3225X5R1E106M	10	25

8.10 Power MOSFETs

Logic-level MOSFETs are recommended, since low side and high side gate drivers are powered by LDO5. Their breakdown voltage VBR_{DSS} must be higher than VINmax.

In notebook applications, power management efficiency is a high level requirement. The power dissipation on the power switches becomes an important factor in switching selections. Losses of high-side and low-side MOSFETs depend on their working conditions.

The power dissipation of the high-side MOSFET is given by:

Equation 16

$$P_{DHighSide} = P_{conduction} + P_{switching}$$

Maximum conduction losses are approximately:

Equation 17

$$P_{conduction} = R_{DSon} \times \frac{V_{OUT}}{V_{INmin}} \times I_{LOAD}(max)^2$$

where RDSon is the drain-source on resistance of the high side MOSFET.

Switching losses are approximately:

Equation 18

$$P_{switching} = \frac{V_{IN} \times (I_{LOAD}(max) - \frac{\Delta I_L}{2}) \times t_{on} \times f_{sw}}{2} + \frac{V_{IN} \times (I_{LOAD}(max) + \frac{\Delta I_L}{2}) \times t_{off} \times f_{sw}}{2}$$

where ton and toff are the switching times of the turn off and turn off phases of the MOSFET.

As general rule, high side MOSFETs with low gate charge are recommended, in order to minimize driver losses.

Below there is a list of possible choices for the high side MOSFET.

Table 14. High side MOSFET manufacturer

Manufacturer	Type	Gate charge (nC)	Rated reverse voltage (V)
ST	STS12NH3LL	10	30
ST	STS17NH3LL	18	30

The power dissipation of the low side MOSFET is given by:

Equation 19

$$P_{DLowSide} = P_{conduction}$$

Maximum conduction losses occur at the maximum input voltage:

Equation 20

$$P_{conduction} = R_{DSon} \times \left(1 - \frac{V_{OUT}}{V_{INmax}}\right) \times I_{LOAD}(max)^2$$

Choose a synchronous rectifier with low R_{DSon}. When high side MOSFET turns on, the fast variation of the phase node voltage can bring up even the low side gate through its gate-drain capacitance CRSS, causing cross-conduction problems. Choose a low side MOSFET that minimizes the ratio CRSS/CGS (CGS = CISS - CRSS).

Below there is a list of some possible low side MOSFETs.

Table 15. Low side MOSFET manufacturer

Manufacturer	Type	RDSon (mΩ)		Rated reverse voltage (V)
ST	STS17NF3LL	5.5	0.047	30
ST	STS25NH3LL	3.5	0.011	30

Dual n-channel MOSFETs can be used in applications with a maximum output current of about 3 A. Below there is a list of some MOSFET manufacturers.

Table 16. Dual MOSFET manufacturer

Manufacturer	Type	RDSon (mΩ)	Gate charge (nC)	Rated reverse voltage (V)
ST	STS8DNH3LL	25	10	30
ST	STS4DNF60L	65	32	60

A rectifier across the low side MOSFET is recommended. The rectifier works as a voltage clamp across the synchronous rectifier and reduces the negative inductor swing during the dead time between turning the high-side MOSFET off and the synchronous rectifier on. It can increase the efficiency of the switching section, since it reduces the low side switch losses. A schottky diode is suitable for its low forward voltage drop (0.3 V). The diode reverse voltage must be greater than the maximum input voltage VINmax. A minimum recovery reverse charge is preferable. Below there is a list of some schottky diode manufacturers.

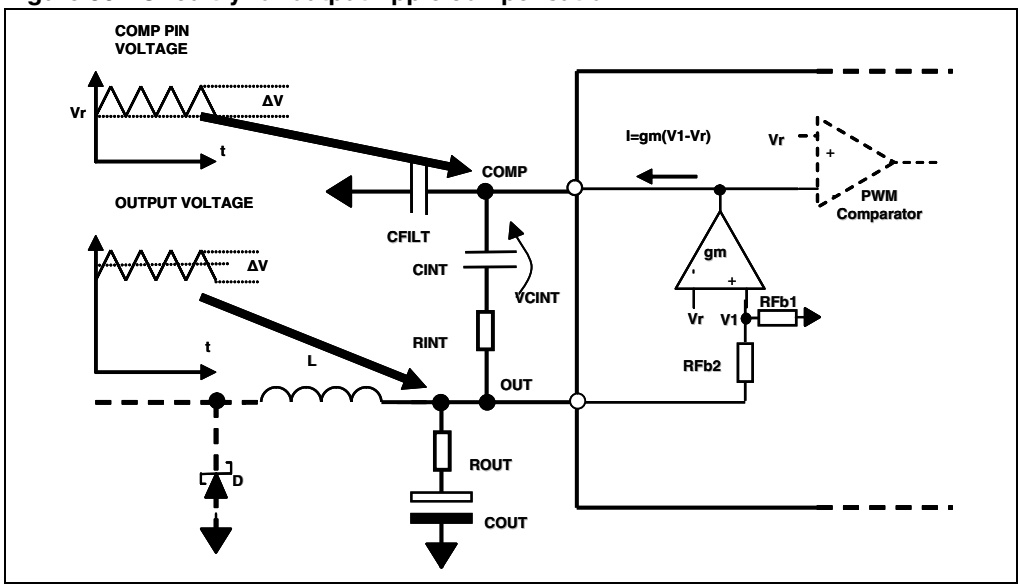
Table 17. Schottky diode manufacturer

Manufacturer	Series	Forward voltage (V)	Rated reverse voltage (V)	Reverse current (uA)
ST	STPS1L30M	0.34	30	0.00039
ST	STPS1L20M	0.37	20	0.000075

8.11 Closing the integrator loop

The design of external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 30 mV, the feedback network (*Figure 36*) is usually enough to keep the loop stable.

Figure 36. Circuitry for output ripple compensation



The stability of the system depends firstly on the output capacitor zero frequency. The following condition should be satisfied:

Equation 21

$$f_{sw} > k \times f_{Zout} = \frac{k}{2\pi \times C_{out} \times R_{out}}$$

where k is a design parameter greater than 3 and Rout is the ESR of the output capacitor. It determinates the minimum integrator capacitor value CINT:

Equation 22

$$C_{INT} > \frac{g_m}{2\pi \times \left(\frac{f_{sw}}{k} - f_{Zout}\right)} \times \frac{Vr}{V_{OUT}}$$

where gm=50us is the integrator transconductance.

In order to ensure stability it must be also verified that:

Equation 23

$$C_{INT} > \frac{g_m}{2\pi \times f_{Zout}} \times \frac{Vr}{V_{OUT}}$$

In order to reduce ground noise due to load transient on the other section, it is recommended to add a resistor RINT and a capacitor Cfilt that, together with CINT, realize a low pass filter (see *Figure 36*). The cutoff frequency fCUT must be much greater (10 or more times) than the switching frequency of the section:

Equation 24

$$R_{INT} = \frac{1}{2\pi \times f_{CUT} \times \frac{C_{INT} \times C_{filt}}{C_{INT} + C_{filt}}}$$

Due to the capacitive divider (CINT, Cfilt), the ripple voltage at the COMP pin is given by:

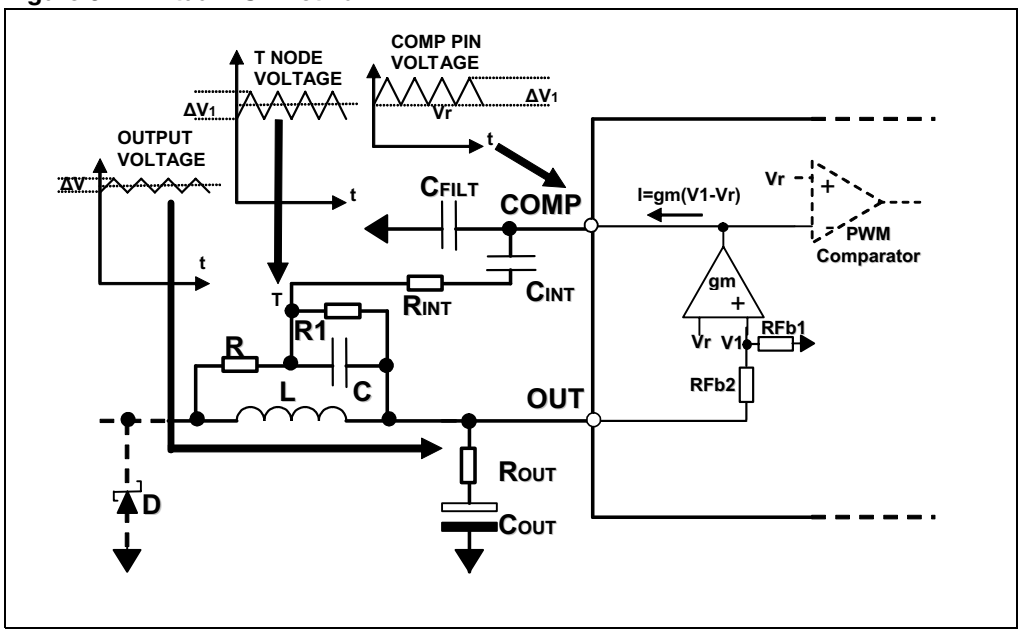
Equation 25

$$V_{RIPPLE_{INT}} = V_{RIPPLEout} \times \frac{C_{INT}}{C_{INT} + C_{filt}} = V_{RIPPLEout} \times q$$

Where VRIPPLEout is the output ripple and q is the attenuation factor of the output ripple.

If the ripple is very small (lower than approximately 30 mV), a further compensation network, named virtual ESR network, is needed. This additional part generates a triangular ripple that is added to the ESR output voltage ripple at the input of the integrator network. The complete control schematic is represented in *Figure 37*.

Figure 37. Virtual ESR network



The T node voltage is the sum of the output voltage and the triangular waveform generated by the virtual ESR network. In fact the virtual ESR network behaves like a further equivalent ESR RESR.

A good trade-off is to design the network in order to achieve an RESR given by:

Equation 26

$$R_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L} - R_{out}$$

where ΔIL is the inductor current ripple and VRIPPLE is the overall ripple of the T node voltage. It should be chosen higher than approximately 30mV.

The stability of the system depends firstly on the output capacitor value and on RTOT:

Equation 27

$$R_{TOT} = R_{ESR} + R_{out}$$

The following condition should be satisfied:

Equation 28

$$f_{sw} > k \times f_Z = \frac{k}{2\pi \times C_{out} \times R_{TOT}}$$

Where k is a free design parameter greater than 3 and determines the minimum integrator capacitor value CINT:

Equation 29

$$C_{INT} > \frac{g_m}{2\pi \times \left(\frac{f_{sw}}{k} - f_Z\right)} \times \frac{Vr}{V_{OUT}}$$

In order to ensure stability it must be also verified that:

Equation 30

$$C_{INT} > \frac{g_m}{2\pi \times f_{Zout}} \times \frac{Vr}{V_{OUT}}$$

C must be selected as shown:

Equation 31

$$C > 5 \times C_{INT}$$

R must be chosen in order to have enough ripple voltage on integrator input:

Equation 32

$$R = \frac{L}{R_{ESR} \times C}$$

R1 can be selected as follows:

Equation 33

$$R1 = \frac{R \times \left(\frac{1}{C \times \pi \times f_Z} \right)}{R - \frac{1}{C \times \pi \times f_Z}}$$

Example:

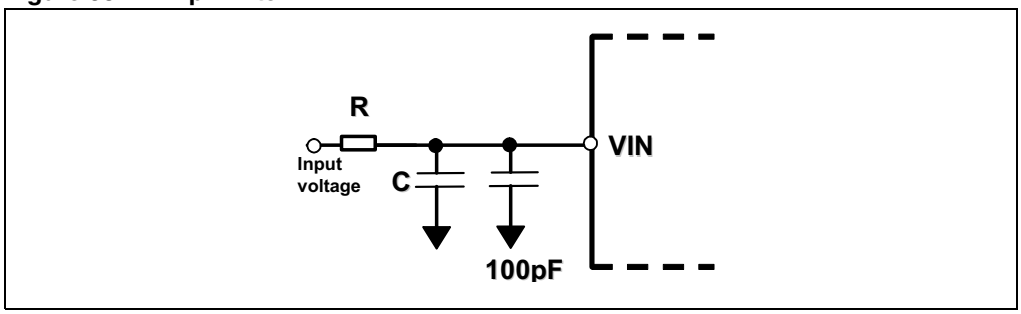
5 V section, f_{SW}=200 kHz, L=4.7 µH, Cout=100 µF ceramic (Rout~0 Ω). We design RESR = 30 mΩ. We choose CINT=1 nF by equations 31, 32 and Cfilt=47 pF, RINT=1.8 kΩ by eq.26,27. C=6.8 nF by Eq.33. Then R=22 kΩ (eq.34) and R1=1 kΩ (eq.35).

9 Other parts design

- VIN filter

  A VIN pin low pass filter is suggested to reduce switching noise. The low pass filter is shown in the next figure:

Figure 38. VIN pin filter

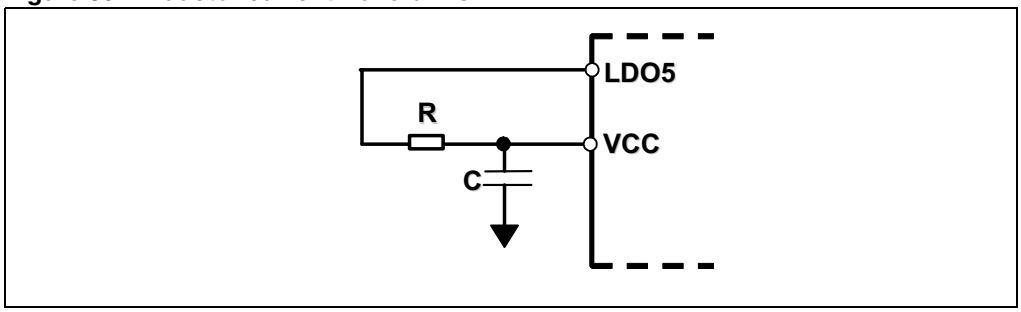


Typical components values are: R=3.9 Ω and C=4.7 µF.

- VCC filter

  A VCC low pass filter helps to reject switching commutations noise:

Figure 39. Inductor current waveforms



Typical components values are: R=47 Ω and C=1 µF.

- VREF capacitor

  A 10 nF to 100 nF ceramic capacitor on VREF pin must be added to ensure noise rejection.

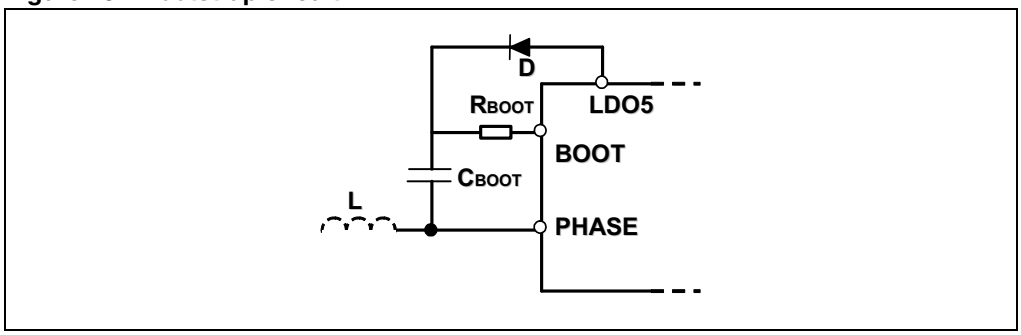
- LDO3 and LDO5 output capacitors

Bypass the output of each linear regulator with 1 µF ceramic capacitor closer to the LDO pin and a 4.7 µF tantalum capacitor (ESR=2 Ω). In most applicative conditions a 4.7 µF ceramic output capacitor can be enough to ensure stability.

- Bootstrap circuit

  The external bootstrap circuit is represented in the next figure:

Figure 40. Bootstrap circuit



The bootstrap circuit capacitor value CBOOT must provide the total gate charge to the high side MOSFET during turn on phase. A typical value is 100 nF.

The bootstrap diode D must charge the capacitor during the off time phases. The maximum rated voltage must be higher than VINmax.

A resistor RBOOT on the BOOT pin could be added in order to reduce noise when the phase node rises up, working like a gate resistor for the turn on phase of the high side MOSFET.

10 Design example

The following design example considers an input voltage from 7 V to 16 V. The two switching outputs must deliver a maximum current of 5A. The selected switching frequencies are 200 kHz for the 5 V section and 300 kHz for the 3.3 V section.

10.1 Inductor selection

OUT5: I_{LOAD}= 5 A, 60% ripple current.

Equation 34

$$L = \frac{5V \cdot (16V - 5V)}{200KHz \cdot 16V \cdot 0.6 \cdot 5} \approx 5.7\mu H$$

We choose standard value L = 6 µH

$\Delta I_{L(max)}$ = 2.86 A @V_{IN} =16 V

I_{LRMS} = 5.07 A

I_{peak} = 5 A + 0.95 A = 6.43 A

OUT3: ILOAD = 5 A, 50% ripple current.

Equation 35

$$L = \frac{3.33 \cdot (16 - 3.33)}{300KHz \cdot 16V \cdot 0.5 \cdot 5} \approx 3.52\mu H$$

We choose standard value L=4 µH.

$\Delta I_{L(max)}$ = 2.2 A @V_{IN} =16 V

I_{LRMS} = 5.04 A

I_{peak} = 5 A + 1.1 A = 6.1 A

10.2 Output capacitor selection

We would like to have an output ripple greater than 35mV.

OUT5: POSCAP 6TPB330M

OUT3: POSCAP 6TPB330M

10.3 Power MOSFETs

OUT5: High side: STS12NH3LL

Low side: STS12NH3LL

OUT3: High side: STS12NH3LL

Low side: STS12NH3LL

10.4 Current limit

OUT5:

Equation 36

$$I_{Lvalley}(min) = I_{LOAD}(max) - \frac{\Delta I_L(min)}{2} = 4.22$$

Equation 37

$$R_{CSENSE} \equiv \frac{4.22A}{100\mu A} \cdot 16.25m\Omega \approx 686\Omega$$

(Let's assume the maximum temperature Tmax = 75°C in R_{DSon} calculation)

OUT3:

Equation 38

$$I_{Lvalley}(min) = I_{LOAD}(max) - \frac{\Delta I_L(min)}{2} = 4.19A$$

Equation 39

$$R_{CSENSE} \equiv \frac{4.19A}{100\mu A} \cdot 16.25m\Omega \approx 681\Omega$$

(Let's assume Tmax = 75°C in R_{DSon} calculation)

10.5 Input capacitor

Maximum input capacitor RMS current is about 3.4 A. Then $I_{CinRMS} > 3.4$ A

We put three 10 µF ceramic capacitors with Irms = 1.5 A.

10.6 Synchronous rectifier

OUT5: Schottky diode STPS1L30M

OUT3: Schottky diode STPS1L30M

10.7 Integrator loop

(Refer to *Figure 30 on page 22*)

OUT5: The ripple is greater than 30 mV, then the virtual ESR network is not required.

C_{INT} =1 nF; C_{filt} = 47 pF; R_{INT} = 1 kΩ

OUT3: The ripple is greater than 30 mV, then the virtual ESR network is not required.

C_{INT} =1 nF; C_{filt} = 47 pF; R_{INT} = 1 kΩ

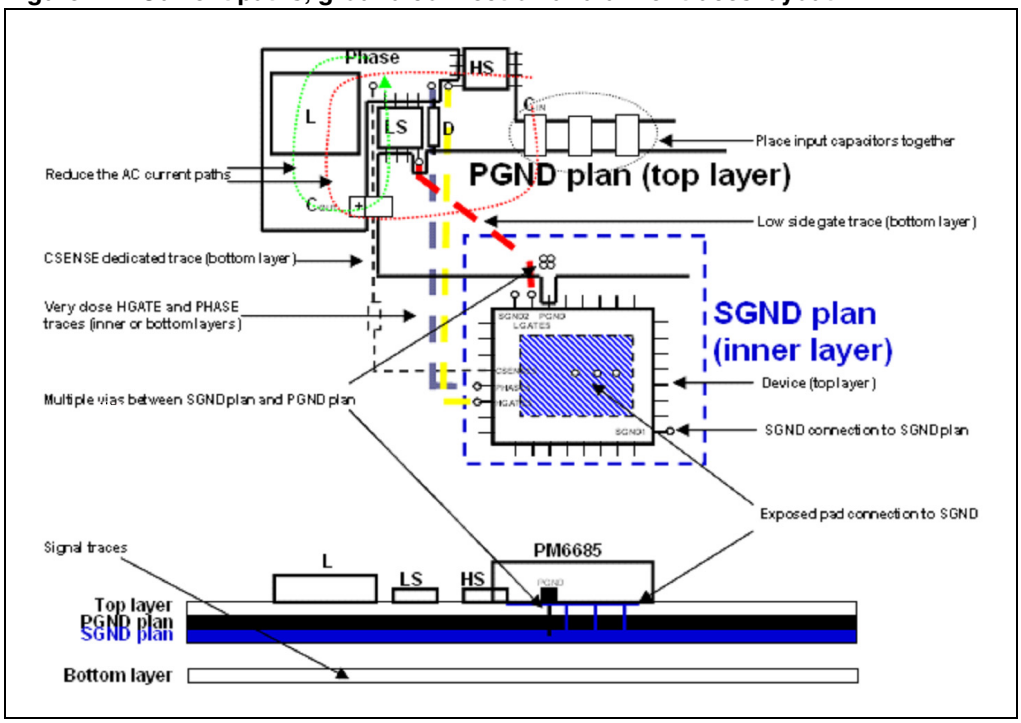
10.8 Layout guidelines

The layout is very important in terms of efficiency, stability and noise of the system. It is possible to refer to the PM6685 demonstration board for a complete layout example.

For good PC board layout follows these guidelines:

- Place on the top side all the power components (inductors, input and output capacitors, MOSFETs and diodes). Refer them to a power ground plan, PGND. If possible, reserve a layer to PGND plan. The PGND plan is the same for both the switching sections.
- AC current paths layout is very critical (see *Figure 41 on page 44*). The first priority is to minimize their length. Trace the LS MOSFET connection to PGND plan as short as possible. Place the synchronous diode D near the LS MOSFET. Connect the LS MOSFET drain to the switching node with a short trace.
- Place input capacitors near HS MOSFET drain. It is recommended to use the same input voltage plan for both the switching sections, in order to put together all input capacitors.
- Place all the sensitive analog signals (feedbacks, voltage reference, current sense paths) on the bottom side of the board or in an inner layer. Isolate them from the power top side with a signal ground layer, SGND. Connect the SGND and PGND plans only in one point (a multiple vias connection is preferable to a 0 ohm resistor connection) near the PGND device pin. Place the device on the top or on the bottom size and connect the exposed pad and the SGND pins to the SGND plan (see *Figure 41 on page 44*).

Figure 41. Current paths, ground connection and driver traces layout



- As general rule, make the high side and low side drivers traces wide and short.
  The high side driver is powered by the bootstrap circuit. It's very important to place capacitor CBOOT and diode DBOOT as near as possible to the HGATE pin (for example on the layer opposite to the device). Route HGATE and PHASE traces as near as possible in order to minimize the area between them.
  The Low side gate driver is powered by the 5V linear regulator output. Placing PGND and LGATE pins near the low side MOSFETs reduces the length of the traces and the crosstalk noise between the two sections.
- The linear regulator outputs are referred to SGND as long as the reference voltage Vref. Place their output filtering capacitors as near as possible to the device.
- Place input filtering capacitors near VCC and VIN pins.
- It would be better if the feedback networks connected to COMP and OUT pins are "referred" to SGND in the same point as reference voltage Vref. To avoid capacitive coupling place these traces as far as possible from the gate drivers and phase (switching) paths.
- Place the current sense traces on the bottom side. Use a dedicated connection between the switching node and the current limit resistor RCSENSE.

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 18. VFQFPN 5x5x1.0 32L pitch 0.50 package dimensions

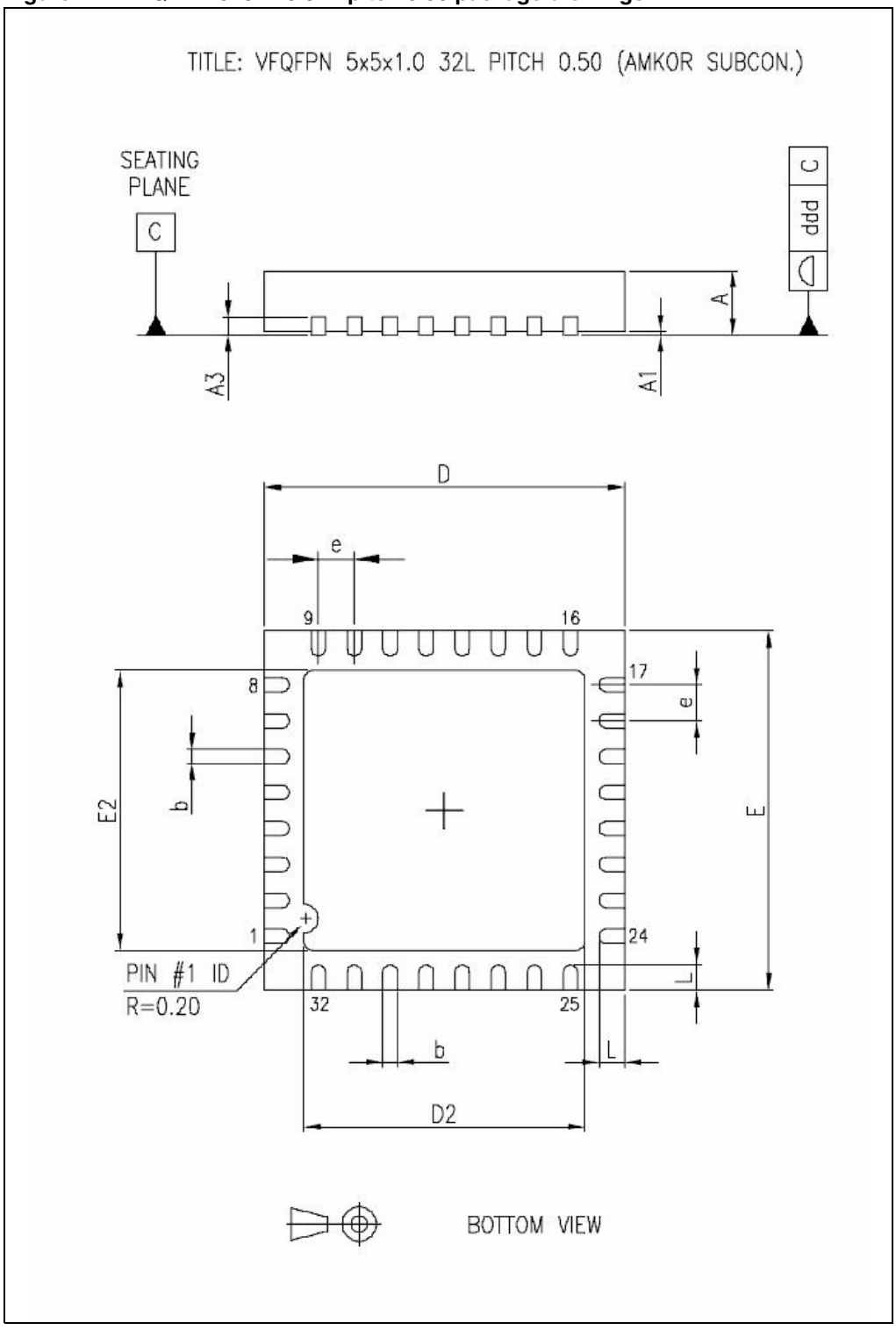
Dim.	Databook (mm)		
	Min	Typ	Max
A	0.8	0.9	1
A1	0	0.02	0.05
A3		0.2	
b	0.18	0.25	0.3
D	4.85	5	5.15
D2	See exposed pad variations (2)		
E	4.85	5	5.15
E2	See exposed pad variations (2)		
e		0.5	
L	0.3	0.4	0.5
ddd			0.05

Table 19. Exposed pad variations

D2			E2		
Min	Typ	Max	Min	Typ	Max
2.90	3.10	3.20	2.90	3.10	3.20

1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A = 1.00mm Max.
2. Dimensions D2 & E2 are not in accordance with JEDEC.

Figure 42. VFQFPN 5x5x1.0 32L pitch 0.50 package drawings



12 Revision history

Table 20. Document revision history

Date	Revision	Changes
17-Jan-2006	1	Initial release
21-Apr-2006	2	Few updates
03-May-2006	3	Graphical updates
29-Jun-2006	4	Mechanical data updated
11-Sep-2006	5	Changes electrical characteristics, added COMP value skip mode, pin out updated
24-Oct-2006	6	Order code table updated
18-Oct-2007	7	Updated: Current sensing option and absolute maximum ratings *Table 3 on page 8*.
30-Mar-2011	8	Updated: Coverpage, *Table 2*, *Table 5*, *Section 7*, *Figure 29*, *Section 7.9*

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