FAN5059

High Performance Programmable Synchronous DC-DC Controller for Multi-Voltage Platforms

Features

- Programmable output for Vcore from 1.3V to 3.5V using an integrated 5-bit DAC
- Controls adjustable linears for Vagp (selectable 1.5V/3.3V), Vclock (2.5V), and Vtt (1.5V) or Vnorthbridge (1.8V)
- Meets VRM specification with as few as 5 capacitors
- Meets 1.550V +40/-70mV over initial tolerance, temperature and transients
- Remote sense
- Programmable Active Droop™ (Voltage Positioning)
- Drives N-Channel MOSFETs
- Overcurrent protection using MOSFET sensing
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- 24 pin SOIC package

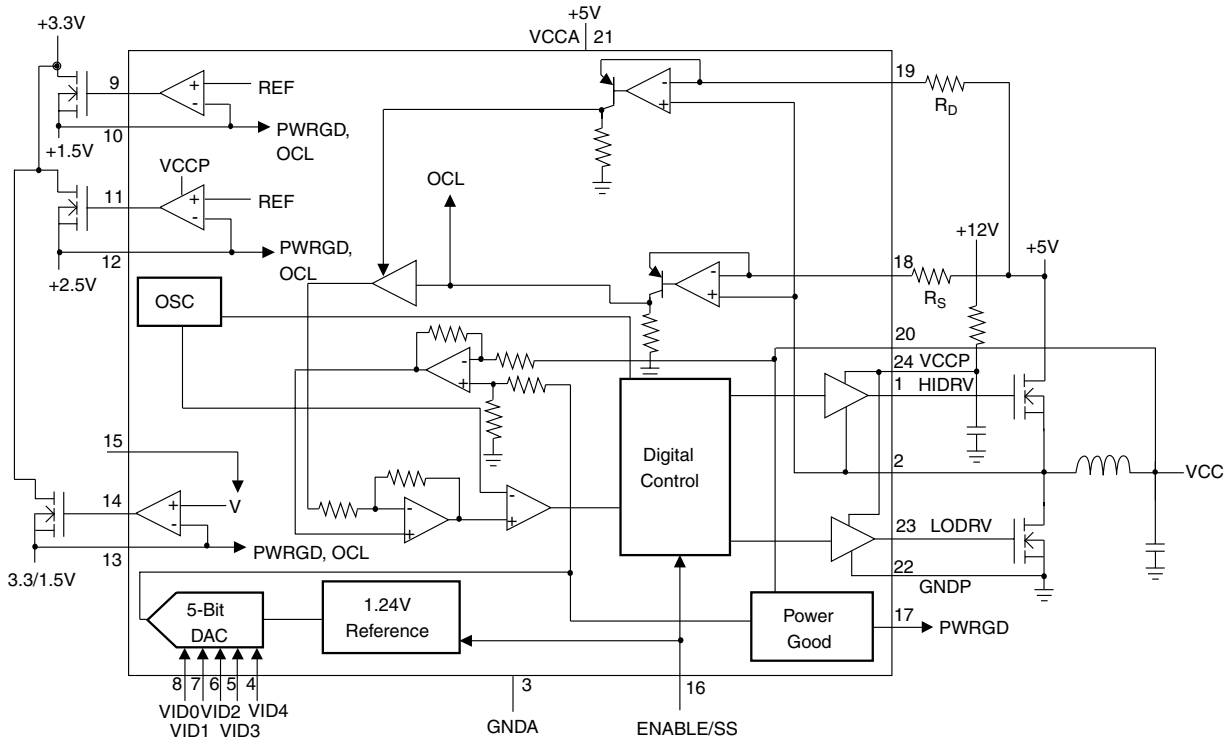
Applications

- Power supply for Pentium® III Camino Platform
- Power supply for Pentium III Whitney Platform
- VRM for Pentium III processor
- Programmable multi-output power supply

Description

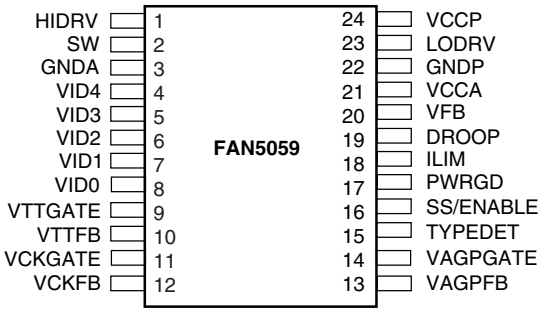
The FAN5059 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable set of output voltages for multi-voltage platforms such as the Intel Camino, and provides a complete solution for the Intel Whitney and other high-performance processors. The FAN5059 features remote voltage sensing, independently adjustable current limit, and a proprietary Programmable Active Droop™ for optimal converter transient response. The FAN5059 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The FAN5059 uses a high level of integration to deliver load

Block Diagram



currents in excess of 16A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components, while Programmable Active Droop™ permits exact tailoring of voltage for the most demanding load transients. The FAN5059 includes linear regulator controllers for Vtt termination (1.5V), Vclock (2.5V), and Vnorthbridge (1.8V) or Vagp (selectable 1.5V/3.3V), each adjustable with an external divider. The FAN5059 also offers integrated functions including Power Good, Output Enable/Soft Start and current limiting, and is available in a 24 pin SOIC package.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	HIDRV	**High Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
2	SW	**High side Driver Source and Low side Driver Drain Switching Node.** Together with DROOP and ILIM pins allows FET sensing for Vcc current.
3	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
4-8	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 2. Pull-up resistors are internal to the controller.
9	VTTGATE	**Gate Driver for VTT Transistor.** For 1.5V output.
10	VTTFB	**Voltage Feedback for VTT.**
11	VCKGATE	**Gate Driver for VCK Transistor.** For 2.5V output.
12	VCKFB	**Voltage Feedback for VCK.**
13	VAGPFB	**Voltage Feedback for VAGP.**
14	VAGPGATE	**Gate Driver for VAGP Transistor.** For 3.3/1.5V output.
15	TYPEDET	**Type Detect.** Sets 3.3V or 1.5V for AGP.
16	ENABLE/SS	**Output Enable.** A logic LOW on this pin will disable all outputs. An internal current source allows for open collector control. This pin also doubles as soft start for all outputs.
17	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if any output voltage is more than ±12% outside of the nominal output voltage setpoint.
18	ILIM	**Vcc Current Feedback.** Pin 18 is used in conjunction with pin 2 as the input for the Vcc current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
19	DROOP	**Droop set.** Use this pin to set magnitude of active droop.
20	VFB	**Vcc Voltage Feedback.** Pin 20 is used as the input for the Vcc voltage feedback control loop. See Application Information for details regarding correct layout.
21	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
22	GNDP	**Power Ground.** Return pin for high currents flowing in pin 24 (VCCP).
23	LODRV	**Vcc Low Side FET Driver.** Connect this pin through a resistor to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
24	VCCP	**Power VCC.** For all FET drivers. Connect to system 12V supply through a 33Ω, and decouple with a 1µF ceramic capacitor.

Absolute Maximum Ratings

Supply Voltage VCCA to GND	13.5V
Supply Voltage VCCP to GND	15V
Voltage Identification Code Inputs, VID0-VID4	VCCA
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-ambient, Θ_{JA}[1]	75°C/W

Note:

1. Component mounted on demo board in free air.

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCCA		4.5	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, VCCP		10.8	12	13.2	V

Electrical Specifications

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
VCC Regulator						
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				18		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.400V V_{OUT} = 2.000V V_{OUT} = 1.550V		2.397 2.000 1.550	2.424 2.020 1.565	2.454 2.040 1.580	V V V
Output Temperature Drift	T_A = 0 to 70°C, V_{OUT} = 2.000V V_{OUT} = 1.550V	• •		+8 +6		mV mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		-4		mV/V
Internal Droop Impedance	I_{LOAD} = 0.8A to 12.5A		13.0	14.4	15.8	KΩ
Maximum Droop				60		mV
Output Ripple	20MHz BW, I_{LOAD} = 18A			11		mVpk
Total Output Variation, Steady State[1]	V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.940 1.480		2.070 1.590	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to 18A, V_{OUT} = 2.000V V_{OUT} = 1.550V[3]	• •	1.900 1.480		2.100 1.590	V
Short Circuit Detect Current		•	45	50	60	µA
Efficiency	I_{LOAD} = 18A, V_{OUT} = 2.0V			85		%
Output Driver Rise & Fall Time	See Figure 3			50		nsec
Output Driver Deadtime	See Figure 3			50		nsec

Electrical Specifications (Continued)

(V_{CCA} = 5V, V_{CCP} = 12V, V_{OUT} = 2.0V, and T_A = +25°C using circuit in Figure 1 unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Duty Cycle			0		100	%
5V UVLO		•	3.74	4	4.26	V
12V UVLO		•	7.65	8.5	9.35	V
Soft Start Current		•	5	10	17	µA
VTT Linear Regulator						
Output Voltage[4]	$I_{LOAD} \leq 2A$	•	1.455	1.5	1.545	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VCLK Linear Regulator						
Output Voltage[4]	$I_{LOAD} \leq 2A$	•	2.425	2.5	2.575	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
VAGP Linear Regulator						
Output Voltage[4]	$I_{LOAD} \leq 2A$, TYPEDET=0V	•	1.455	1.5	1.545	V
Output Voltage	$I_{LOAD} \leq 2A$, TYPEDET=OPEN	•	3.135	3.3	3.465	V
Under Voltage Trip Level	Over Current			80		$\%V_O$
Common Functions						
Oscillator Frequency		•	255	310	345	kHz
PWRGD Threshold	Logic HIGH, All Outputs Logic LOW, Any Output	• •	88 84		112 116	$\%V_{OUT}$
Linear Regulator Under Voltage Delay Time	Over Current			30		µsec

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, the converter will be in compliance with Intel's VRM 8.4 specification of +50, –80mV. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specification of +40, –70mV at the capacitors will also be met.
4. Actual output voltage (V_{nom}) at 0A load is 1% higher than specified in the "Typical" column.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT}
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	2.0V
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

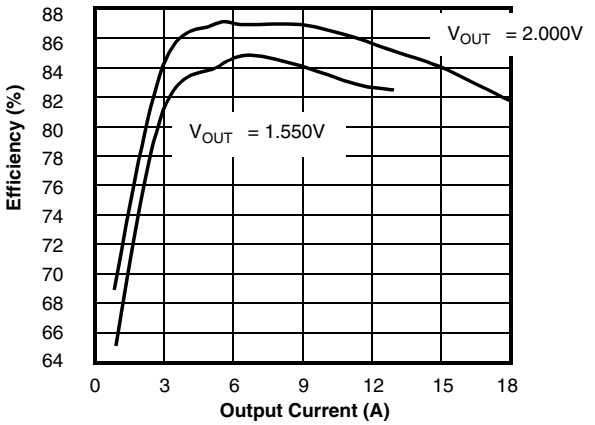
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

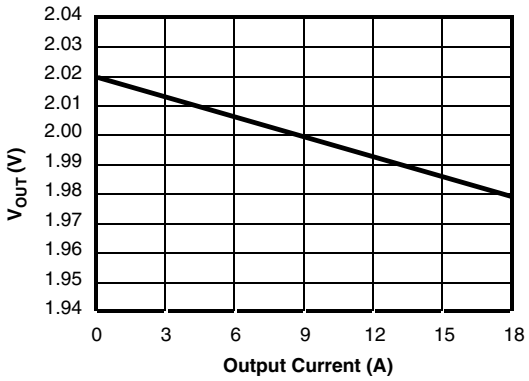
Typical Operating Characteristics

(V_{CCA} = 5V, V_{CCP} = 12V, and T_A = +25°C using circuits in Figure 1, unless otherwise noted.)

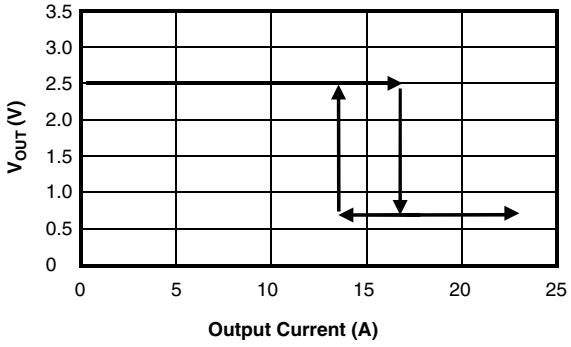
V_{CPU} Efficiency vs. Output Current



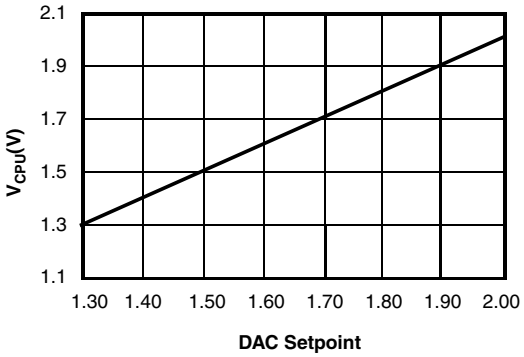
Droop, V_{CPU} = 2.0V, R_D = 8K Ω



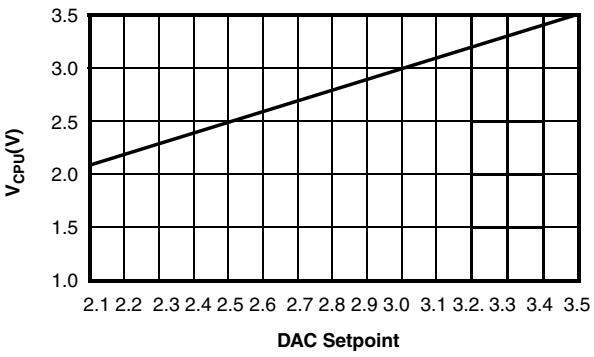
CPU Output Voltage vs. Output Current



Output Programming, VID4 = 0

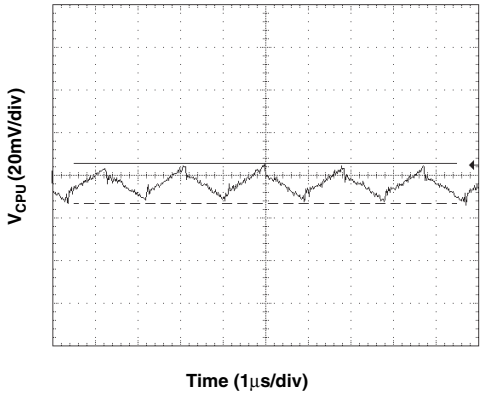


Output Programming, VID4 = 1

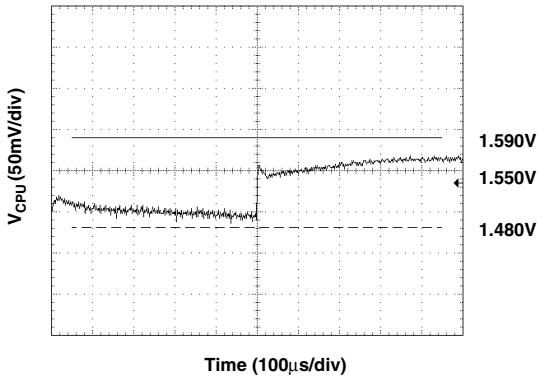


Typical Operating Characteristics (continued)

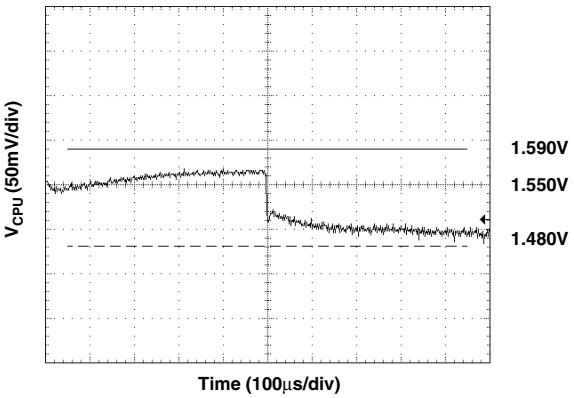
Output Ripple, 2.0V @ 18A



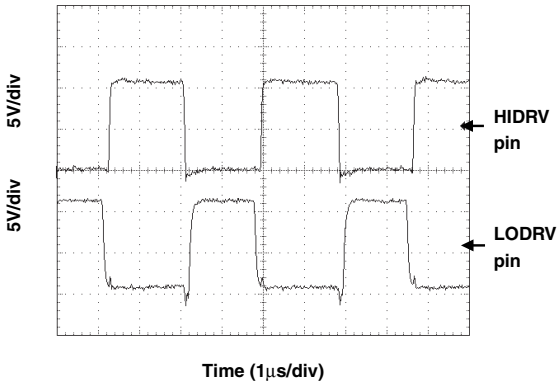
Transient Response, 12.5A to 0.5A



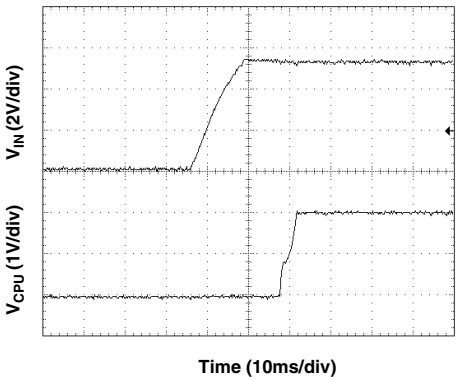
Transient Response, 0.5A to 12.5A



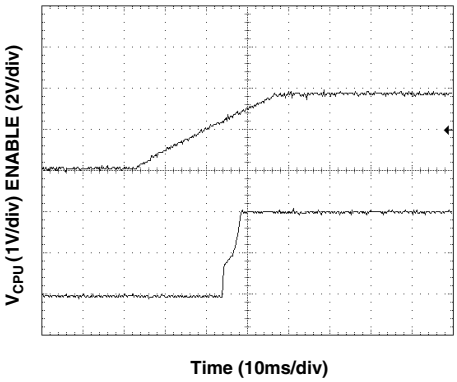
Switching Waveforms, 18A Load



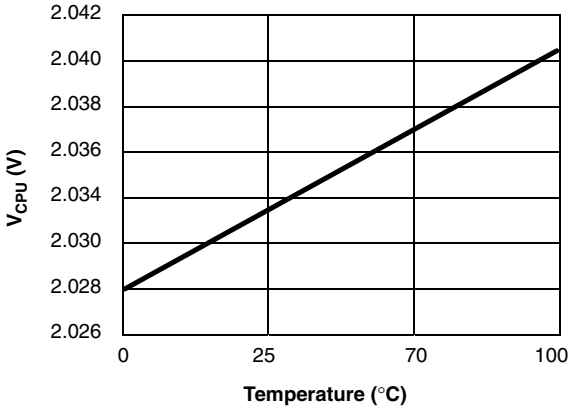
Output Startup, System Power-up

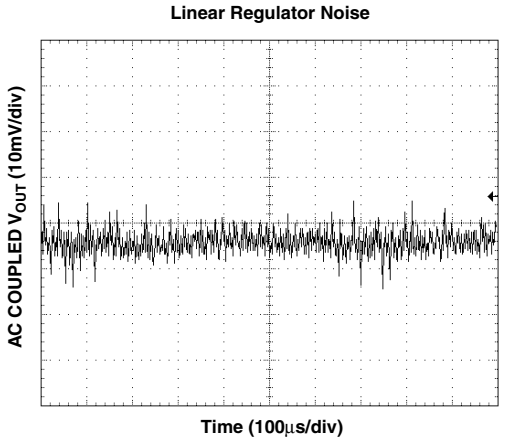


Output Startup from Enable



Typical Operating Characteristics (continued)





Application Circuit

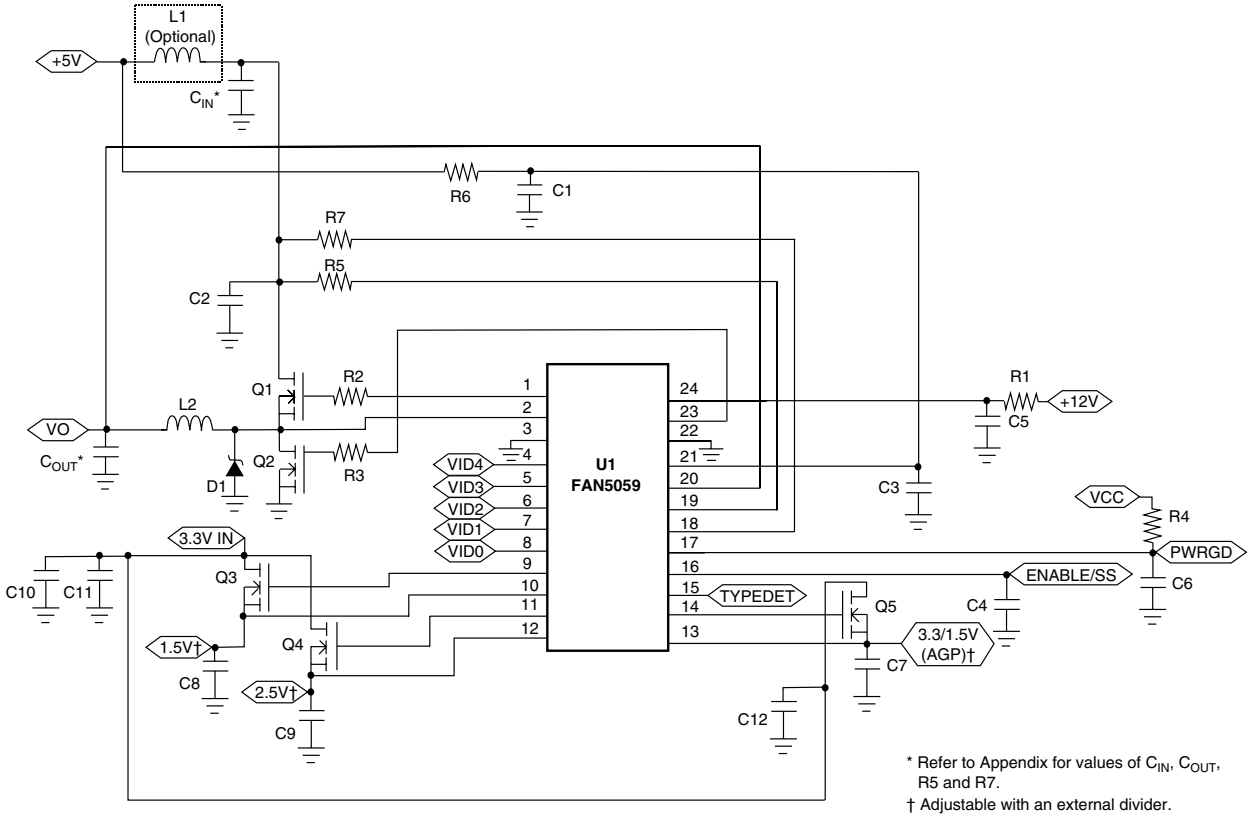


Figure 1. Typical Application Circuit
(Worst Case Analyzed! See Appendix for Details*)*

Table 2. FAN5059 Application Bill of Materials

(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C7-9	Sanyo 6MV1000FA	3	1000µF, 6.3V Electrolytic	
C10-12	Any	3	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 8A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 20A Inductor	DCR ~ 2mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-5	Fairchild FDB4030L	3	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5	Any	1	*	
R6	Any	1	10Ω	
R7	Any	1	*	
U1	Fairchild FAN5059M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 17.4A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

*Refer to Appendix for values.

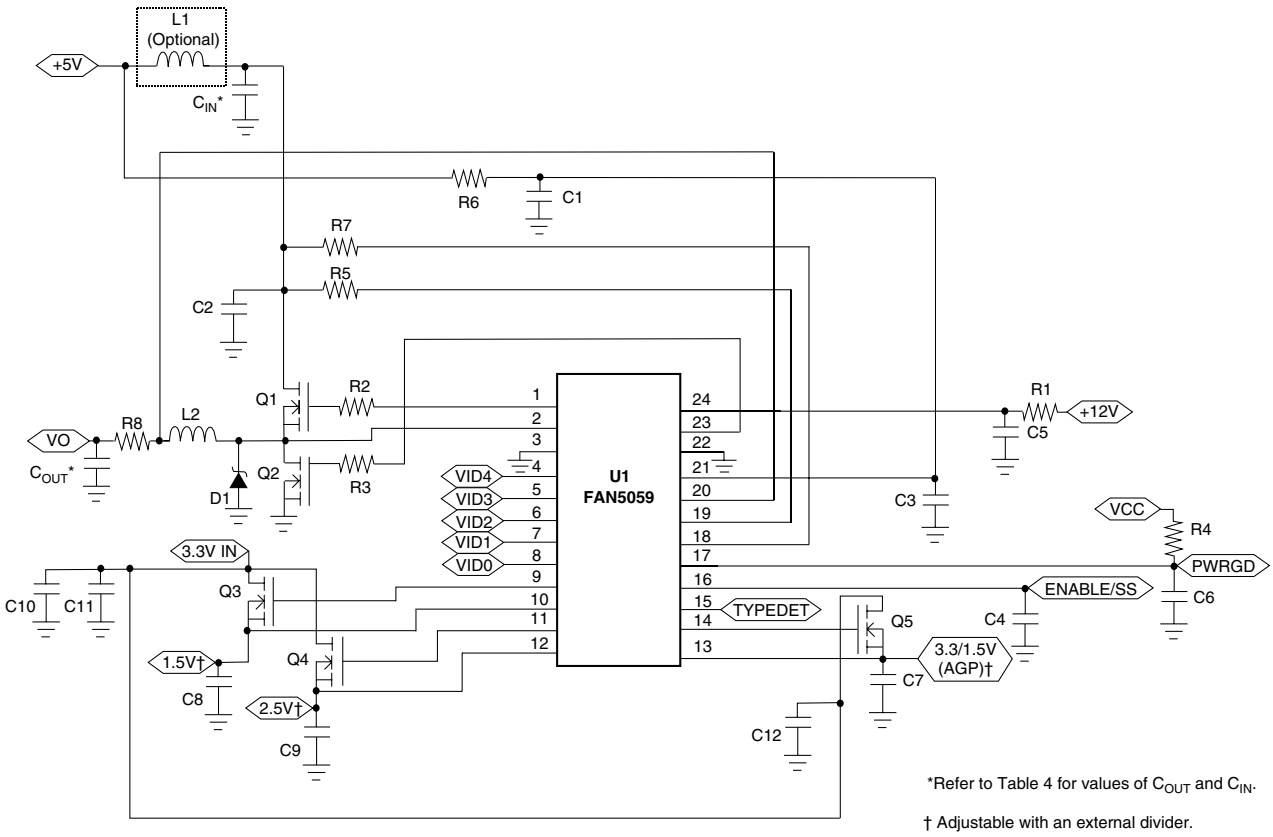


Figure 2. Application Circuit for Coppermine/Camino Motherboards
(Typical Design)

Table 3. FAN5059 Application Bill of Materials for Intel Coppermine/Camino Motherboards
(Typical Design)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7µF, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C3-4,C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C7-9	Sanyo 6MV1000FA	3	1000µF, 6.3V Electrolytic	
C10-12	Any	3	22µF, 6.3V Capacitor	Low ESR
C_{IN}	Sanyo 10MV1200GX	3	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	12	1500µF, 6.3V Electrolytic	ESR ≤ 44mΩ
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	2.5µH, 5A Inductor	DCR ~ 10mΩ See Note 1.
L2	Any	1	1.3µH, 15A Inductor	DCR ~ 3mΩ
Q1	Fairchild FDB6030L	1	N-Channel MOSFET	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2.
Q2	Fairchild FDB7030BL	1	N-Channel MOSFET	$R_{DS(ON)}$ = 10mΩ @ V_{GS} = 4.5V See Note 2.
Q3-5	Fairchild FDB4030L	3	N-Channel MOSFET	
R1	Any	1	33Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R5, R7	Any	2	6.24KΩ	
R6	Any	1	10Ω	
R8	N/A	1	3.0mΩ	PCB Trace Resistor
U1	Fairchild FAN5059M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 12.5A designs using the TO-220 MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

Test Parameters

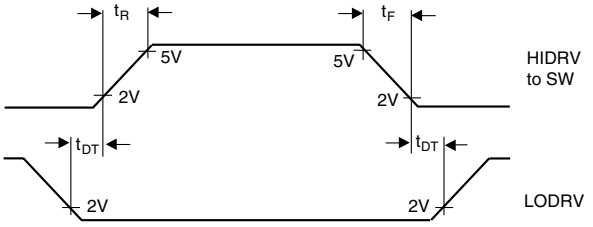


Figure 3. Ouput Drive Timing Diagram

Application Information

The FAN5059 Controller

The FAN5059 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the FAN5059 can be configured to deliver more than 16A of output current, as appropriate for the Katmai and Coppermine and other processors. The FAN5059 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the FAN5059 Block Diagram on page 1. The FAN5059 implements "summing mode control", which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the DROOP (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the DROOP and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the FAN5059 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The FAN5059 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers' power and ground are separated from the chip's power and ground for switching noise immunity. The power supply pin, VCCP, is supplied from an external 12V source through a series 33Ω resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the FAN5059 is a precision bandgap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V.

Power Good (PWRGD)

The FAN5059 Power Good function is designed in accordance with the Pentium II and III DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±16% of its nominal setpoint. Power Good outputs an open collector high when the output voltage is within ±12% of its nominal setpoint. The Power Good flag provides no other control function to the FAN5059.

Output Enable/Soft Start (ENABLE/SS)

The FAN5059 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to softstart the switching.

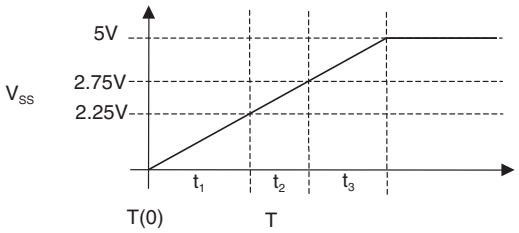
The softstart pin (ENABLE/SS) ramp can be divided into three time periods. The first part is represented by t_1, the second is represented by t_2 and the third is represented by t_3. The voltage on the pin is:

$$V_{SS} = \left(\frac{C_{SS}}{I_{SS}}\right) \times (T)$$

$$t_1 = 2.25 \times \left(\frac{C_{SS}}{I_{SS}}\right)$$

$$t_2 = 2.75 \times \left(\frac{C_{SS}}{I_{SS}}\right) - t_1$$

$$t_3 = 5 \times \left(\frac{C_{SS}}{I_{SS}}\right) - (t_1 + t_2)$$



The softstart ramp begins at T(0) where UVLO is released. During the period of t_1 the softstart pin ramps but the PWM switching is not enabled and thus the duty cycle is zero (D=0) and the output voltage is zero. During t_2 the duty cycle increased progressively from 0 to 1. This period is where the output voltage ramps, dependent on output capacitance and output load. If the duration of t_2 is long enough the output voltage will fully ramp to the point of regulation. During t_3 the softstart pin continues to ramp but without effect on the output voltage.

NOTE: If a very large output capacitor bank is used it may be required to use a larger C_{SS} to ensure a full output voltage ramp within t_2.

Over-Voltage Protection

The FAN5059 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds the selected program voltage, an over-voltage condition is assumed and the FAN5059 disables the output drive signal to the external high-side MOSFET. The DC-DC converter returns to normal operation after the output voltage returns to normal levels.

Oscillator

The FAN5059 oscillator section uses a fixed frequency of operation of 300KHz.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:
V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \frac{(V_{in} - V_{out})\, D_m\, V_{tb}}{I_{pp}^2}$$

where:
C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_O, which must be increased to increase L. Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The FAN5059 provides significant cost savings for the newer CPU systems that typically run at high supply current.

FAN5059 Short Circuit Current Characteristics

The FAN5059 protects against output short circuit on the core supply by turning off both the high-side and low-side MOSFETs and resetting softstart. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} * R_{DS,\,on}}{I_{Detect}}$$

Note: R_S cannot exceed 10.8K. If a higher current is required than 10.8K allows, a FET with lower R_{DSon} must be used.

with $I_{Detect} \approx 50\mu A$, I_{SC} is the desired current limit, and $R_{DS,on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS,on}$. Alternately, use of a sense resistor in series with the source of the MOSFET eliminates this source of inaccuracy in the current limit.

As an example, Figure 4 shows the typical characteristic of the DC-DC converter circuit with an FDB6030L high-side MOSFET (R_{DS} = 20mΩ maximum at 25°C * 1.25 at 75°C = 25mΩ) and a 8.2KΩ R_S.

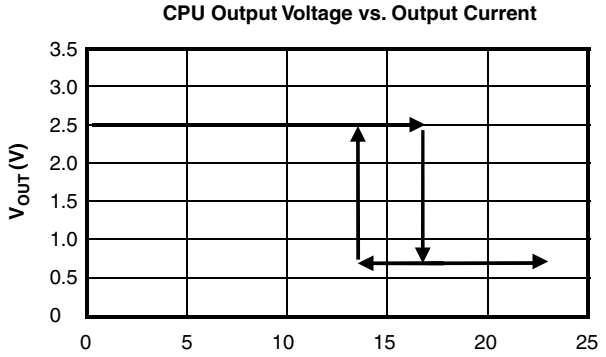


Figure 4. FAN5059 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of 50µA * 8.2KΩ = 410mV, which occurs at 410mV/25mΩ = 16.4A. (Note that this current limit level can be as high as 410mV/15mΩ = 27A, if the MOSFET has typical $R_{DS,on}$ rather than maximum, and is at 25°C).

At this point, the internal comparator trips and signals the controller to discharge the softstart capacitor. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 16.4A * 40mΩ = 650mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating ranges for the DC-DC converter.

If any of the linear regulator outputs are loaded heavily enough that their output voltage drops below 80% of nominal for >30µsec, all FAN5059 outputs, including the switcher, are shut off and remain off until power is recycled.

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 5. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 5 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Katmai and Coppermine, the capacitors should be rated to take 9A and 6A of ripple current respectively. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

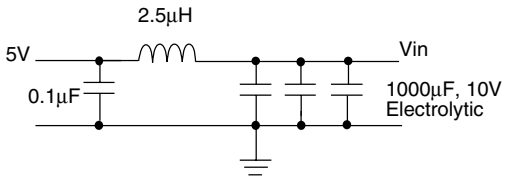


Figure 5. Input Filter

Programmable Active Droop™

The FAN5059 includes Programmable Active Droop™: as the output current increases, the output voltage drops, and the amount of this drop is user adjustable. This is done in order to allow maximum headroom for transient response of the converter. The current is typically sensed by measuring the voltage across the $R_{DS,on}$ of the high-side MOSFET during its on time, as shown in Figure 1.

To program the amount of droop, use the formula

$$R_D \simeq \frac{14.4K\Omega * I_{max} * R_{sense}}{V_{Droop} * 18}$$

where I_{max} is the current at which the droop occurs, and R_{sense} is the resistance of the current sensor, either the source resistor or the high-side MOSFET's on-resistance. For example, to get 30mV of droop with a maximum output current of 12.5A and a 10mΩ sense resistor, use R_D = 14.4KΩ * 12.5A * 10mΩ/(30mV * 18) = 3.33KΩ. Further details on use of the Programmable Active Droop™ may be found in Applications Bulletin AB-24.

Remote Sense

The FAN5059 offers remote sense of the output voltage to minimize the output capacitor requirements of the converter. It is highly recommended that the remote sense pin, Pin 20, be tied directly to the processor power pins, so that the effects of power plane impedance are eliminated. Further details on use of the remote sense feature of the FAN5059 may be found in Applications Bulletin AB-24.

Adjusting the Linear Regulators' Output Voltages

Any or all of the linear regulators' outputs may be adjusted high to compensate for voltage drop along traces, as shown in Figure 6.

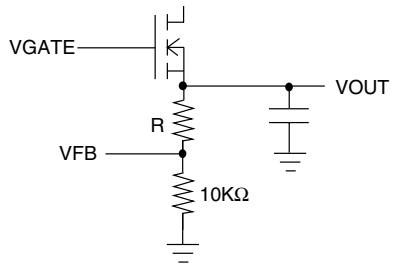


Figure 6. Adjusting the Output Voltage of the Linear Regulator

The resistor value should be chosen as

$$R = 10K\Omega * \left(\frac{V_{out}}{V_{nom}} - 1\right)$$

Note: See Note 4 in Electrical Specifications Table.

For example, to get the V_{TT} voltage to be 1.55V instead of 1.50V, use R = 10KΩ * [(1.55/1.50) – 1] = 333Ω.

Using the FAN5059 for Vnorthbridge = 1.8V

In some motherboards, Intel requires that the AGP power can not be greater than 2.2V while the chipset voltage (Vnorthbridge = 1.8V) is less than 1.0V. The FAN5059 can accomplish this by using the VTT regulator to generate Vnorthbridge. Use the circuit in Figure 6 with R = 2KΩ. Since the linear regulators on the FAN5059 all rise proportionally to one another, when Vnorthbridge = 1.0V, Vagp = 1.8V, meeting the Intel requirement.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the FAN5059 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the FAN5059 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the FAN5059. That is, traces that connect to pins 1, 2, 23, and 24 (HIDRV, SW, LODRV and VCCP) should be kept far away from the traces that connect to pins 3, 20 and 21.
- Place the 0.1µF decoupling capacitors as close to the FAN5059 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

Additional Information

For additional information contact Fairchild Semiconductor at http://www.fairchildsemi.com/cf/tsg.htm or contact an authorized representative in your area.

Appendix

Worst-Case Formulae for the Calculation of Cin, Cout , R5, R7 and Roffset (Circuits similar to Figure 1 only)

The following formulae design the FAN5059 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, internal droop impedance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{S+}, the value of the positive static voltage limit;

$|V_{S-}|$, the absolute value of the negative static voltage limit;

V_{T+}, the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O, the maximum output current;

V_{nom}, the nominal output voltage;

V_{in}, the input voltage (typically 5V);

I_{rms}, the ripple current rating of the input capacitors, per cap (2A for the Sanyo parts shown in this datasheet);

R_D, the resistance of the current sensor (usually the MOSFET);

ΔR_D, the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature); and

ESR, the ESR of the output capacitors, per cap (44mΩ for the Sanyo parts shown in this datasheet).

$$C_{in} = \frac{IO * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R_{offset} = \frac{V_{S+} - .024 * V_{nom}}{1.01 * V_{nom}} * 1K\Omega$$

$$R7 = \frac{I_O * R_D * (1 + \Delta R_D)}{45 * 10^{-6}}$$

$$R5 = \frac{14400 * I_O * R_D * (1 + \Delta R_D) * 1.1}{18 * (V_{S+} + |V_{S-}| - .024 * V_{nom})}$$

The value of R7 must be ≤ 8.3KΩ. If a greater value is calculated, R_D must be reduced.

Number of capacitors needed for C_{out} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}| + V_{S+} - .024 * V_{nom}}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - V_{S+} + \frac{14400 * I_O * R_D}{18 * R5 * 1.1}}$$

Example: Suppose that the static limits are +89mV/-79mV, transient limits are ±134mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing. We have $V_{S+} = 0.089$, $|V_{S-}| = 0.079$, $V_{T+} = |V_{T-}| = 0.134$, $I_O = 14.2$, $V_{nom} = 2.000$, and $\Delta R_D = 1.67$. We calculate:

Since Y > X, we choose Y, and round up to find we need 7 capacitors for C_{OUT}.

A detailed explanation of this calculation may be found in Applications Bulletin AB-24.

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R_{offset} = \frac{0.089 - .024 * 2.000}{1.01 * 2.000} * 1000 = 20.3\Omega$$

$$R7 = \frac{14.2 * 0.010 * (1 + 0.67)}{45 * 10^{-6}} = 5.25K\Omega$$

$$R5 = \frac{14400 * 14.2 * 0.020 * (1 + 0.67) * 1.1}{18 * (0.089 + 0.079 - .024 * 2.000)} = 3.48K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134 + 0.089 - .024 * 2.00} = 3.57$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.089 + \frac{14400 * 14.2 * 0.020}{18 * 3640 * 1.1}} = 6.14$$

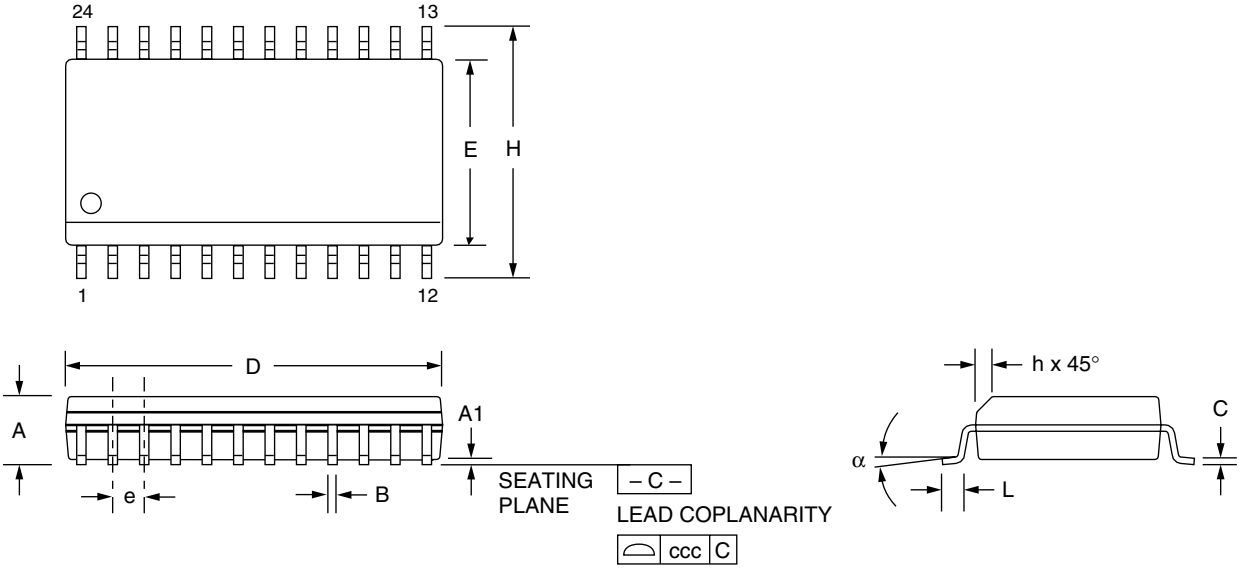
Mechanical Dimensions

24 Lead SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
FAN5059M	24 pin SOIC