NCP1500

Dual Mode PWM/Linear BUCK Converter

The NCP1500 is a dual mode converter that operates as either a pulse width modulated (PWM) buck converter or as a linear regulator. The converter automatically transitions between the two modes. The converter operates as a PWM when a synchronization signal is present at the sync input. The converter operates as a linear regulator in the absence of a synchronization signal. The PWM mode offers excellent performance at normal to heavy loads at the sacrifice of output ripple voltage. The linear mode offers excellent noise rejection at the sacrifice of system efficiency. The user is able to select which mode will give the best performance for a given operating condition. Internal protection features include thermal shutdown with hysteresis and cycle−by−cycle current limit in the PWM mode. Additionally, the converter transitions into PFM mode at very light loads if a synchronization signal is present and an output overvoltage condition is detected.

PWM Features

- Current Mode Control with Cycle−by−Cycle Current Limit
- Nominal Synchronization Frequency of 270 to 630 kHz
- Built−in Slope Compensation

Linear Regulator Features

- Low Output Noise

Overall Features

- Thermal Shutdown with Hysteresis
- Digitally Programmable Output Voltage Between 4 Voltages: 1.0, 1.3, 1.5, and 1.8
- Fast Transient Response
- Input Voltage Range From 2.7 V to 5.4 V
- Space Saving Micro8 Package
- Low Shutdown Current of 0.18 μA Typical
- Pb−Free Package is Available

Typical Applications

- Baseband Supplies for Portable Handsets
- PDAs
- Supplies for DSP Circuitry

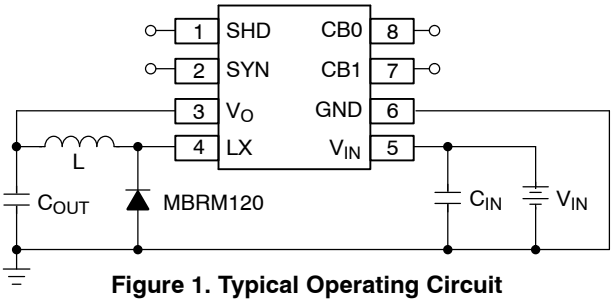

Figure 1. Typical Operating Circuit

L = 15 μH
C_{IN} = 10 μF
C_{OUT} = 10 μF

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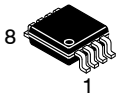
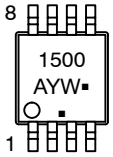
http://onsemi.com

MARKING DIAGRAM

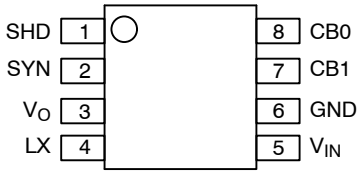


Micro8™ (MSOP−8) DM SUFFIX CASE 846A



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1500DMR2	Micro8	4000 Tape/Reel
NCP1500DMR2G	Micro8 (Pb−Free)	4000 Tape/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	SHD	Device is placed in shutdown when SHD is driven low. In shutdown mode, the internal MOSFET and output are turned off. Driven to high for normal operation. This pin is floating internally and needs to be tied to a fixed source externally.
2	SYN	External Synchronization Clock Signal Input. If a clock signal is present at this pin, the device will go into PWM mode. If SYN is driven low, the device operates in linear mode.
3	V_O	Connected to internal voltage divider for feedback.
4	LX	Pin for the connection between the drain of the internal P−MOSFET and the external inductor.
5	V_{IN}	Voltage Supply Input. Bypass with 10 μF capacitor.
6	GND	Ground.
7	CB1	Control Bit 1 Input for output voltage level selection. Internally pulled low.
8	CB0	Control Bit 0 Input for output voltage level selection. Internally pulled low.

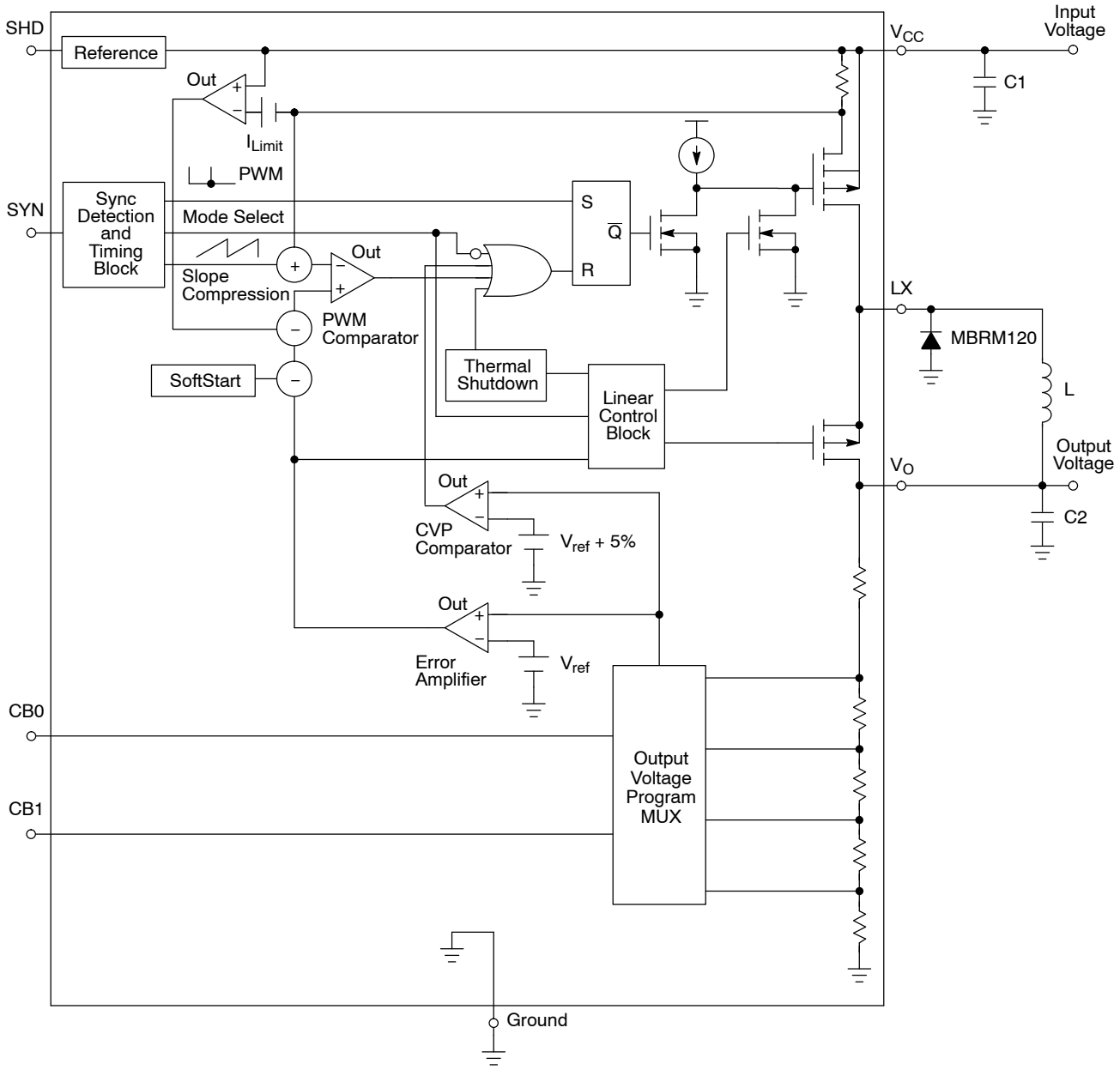
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 5)	V_{IN}	−0.3 to 6.0	V
Input/Output Pins Pin 1−4 & Pin 7−8	V_{IO}	−0.3 to 6.0	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance Junction to Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature Range	T_J	−40 to +140	°C
Operating Ambient Temperature Range	T_A	− 40 to +85	°C
Storage Temperature Range	T_{stg}	− 55 to +150	°C

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latch−up Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.6 V, V_O = 1.5 V, T_A = 25°C, Fsyn = 600 kHz 50% Duty Cycle sinewave with V_H = 2.0 V and V_L = 0 V for PWM mode; T_A = −40 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	2.7	–	5.4	V
Main FET Leakage Current (Pins 5 to 4) T_A = 25°C T_A = −40°C to 85°C	I_{LEAK}	– –	0.06 –	0.3 10	μA
Mode Selection Pin					
SYN “H” Input Voltage	V_{SYNH}	1.3	–	–	V
SYN “L” Input Voltage	V_{SYNL}	–	–	1.1	V
SYN “H” Input Current	I_{SYNH}	–	0	0.5	μA
SYN “L” Input Current	I_{SYNL}	−0.5	0	–	μA
External Synchronization Frequency	F_{SYNC}	270	–	630	kHz
Output Level Selection Pins					
CB “H” Input Voltage Threshold	V_{CBH}	0.90	–	–	V
CB “L” Input Voltage Threshold	V_{CBL}	–	–	0.63	V
CB “H” Input Current	I_{CBH}	–	0.1	–	μA
CB “L” Input Current	I_{CBL}	–	0	–	μA
Shutdown Pin					
SHD “H” Input Voltage Threshold	V_{SHDH}	0.59	–	–	V
SHD “L” Input Voltage Threshold	V_{SHDL}	–	–	0.26	V
SHD “H” Input Current	I_{SHDH}	–	0.1	–	μA
SHD “L” Input Current	I_{SHDL}	–	0	–	μA
PWM Mode					
Output Voltage (I_{OUT} = 35 mA, T_A = 25°C) CB0, CB1 = (H, H) CB0, CB1 = (H, L) CB0, CB1 = (L, L) CB0, CB1 = (L, H)	V_{OUT0}	 0.941 1.235 1.425 1.710	 0.99 1.30 1.50 1.80	 1.050 1.365 1.575 1.890	V
Line Regulation, I_{out} = 100 mA 3.0 to 3.6 V 3.0 to 4.2 V	ΔV_{out0}	 – –	 1.0 2.0	 – –	mV
Load Regulation 50 to 120 mA 20 to 200 mA	ΔV_{out0}	 – –	 1.0 13	 – –	mV
Minimum On−Time	TON_{MIN}	–	210	–	nsec
Internal PFET ON−Resistance (I_{LX} = 400 mA, V_{IN} = 2.0 V)	$R_{DS(ON)\_P}$	–	0.65	1.2	Ω
Main Output Switch Current Limit	I_{LIM}	–	800	–	mA
Linear Regulator Mode (Lx shorted to Vo)					
Output Voltage (I_{out} = 0 mA, T_A = 25°C) CB0, CB1 = (H, H) CB0, CB1 = (H, L) CB0, CB1 = (L, L) CB0, CB1 = (L, H)	V_{out0}	 0.941 1.235 1.425 1.710	 0.99 1.30 1.50 1.80	 1.050 1.365 1.575 1.890	V
Startup Current Load in Linear Mode	$ISTART_{LIN}$	80	–	–	mA
Overvoltage Protection					
Output Overvoltage Threshold in PWM Mode	VO_{PFM}	–	+5.0	+10	%
Total Device					
Power Supply Current Standby (SHD tied low, V_{IN} = 3.6 V, SYN tied low) T_A = 25°C T_A = −40°C to 85°C PWM Mode (SHD tied high, V_{IN} = 3.6 V, V_{out} = 1.6 V, V_{CB0} = V_{CB1} = 0 V, SYN @ 600 kHz/50% duty cycle, I_{out} = 0 mA) Linear Mode (SHD tied high, V_{IN} = 3.6 V, V_{out} = 1.5 V, SYN tied low, I_{out} = 0 mA)	I_{CC}	 – – – –	 0.18 – 96 30	 0.5 10 150 70	μA



Component	Value	Manufacturer
C1, C2	10 μF, 6.3 V	TDK, C3216X5R0J106M
L	15 μH	TDK, RLF5018T−150MR76 (I_{out} = 300 mA) Coilcraft, D01606T−153 (I_{out} = 300 mA) TDK, NLC252018T−150 (I_{out} = 100 mA)

Figure 2. Typical Circuit with the Internal Schematic

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1500 is a dual mode regulator intended for use in baseband supplies for portable equipment. Its unique features provide power to the baseband circuitry while, at the same time save valuable battery energy. When the handset is idle, the user can activate the linear regulator function. In this mode, the regulator provides a regulated low current, low noise output voltage keeping the baseband circuit biased. When the handset is in its normal operating mode, the regulator synchronizes to the baseband clock and turns into a switching regulator. This allows the regulator to provide efficient power to the baseband circuit.

Operating Description

Synchronization Protocol and Mode Selection

The NCP1500 has a SYNC input. The device operates at a fixed switch frequency determined by the frequency of the synchronization signal applied. The part automatically operates in PWM mode after synchronization pulses are present for several cycles. The NCP1500 will output 2 pulses when a sync signal is present. The first is a PWM pulse. This pulse 'sets' a latch that initiates output switch conduction. The width of this pulse controls the minimum on time in PWM mode. The second signal is a slope compensation ramp. A ramp signal is generated. This signal is summed with the current information before being fed into the PWM comparator. The purpose of this circuit is to provide stable operation at output switch duty cycles in excess of 50%. The device automatically switches to linear mode when the SYNC signal is removed for approximately 6.0 μsec**. It is recommended that the sync signal be externally pulled low to enable the linear mode**. Pulling the pin high or open may cause portions of the circuit to remain active, increasing the total current consumption of the IC. The threshold level of the SYNC signal is typically 1.3 V. The duty cycle of the sync signal must be within 20 to 80%.

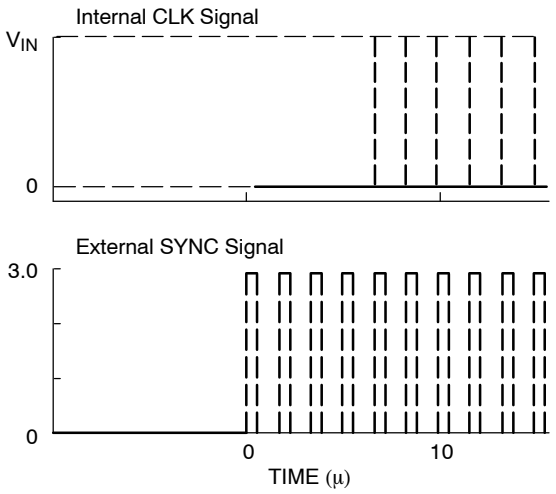


Figure 3. Timing Diagram of the SYNC Signal

Figure 3 shows the waveform when the SYNC signal is applied. After several cycles, the MODE select changes and PWM operation is activated with the internal clock signal.

Reference/Shutdown

The NCP1500 uses an internal reference, typically at 0.8 V. An external shutdown pin is provided. When this pin is pulled low, the reference and other circuitry are disabled, placing the part into a low quiescent current standby mode. In this mode, the pass device is off and the output voltage will be zero. The typical standby current is 0.18 μA.

Error Amplifier/Output Voltage Program

A fully compensated error amplifier is provided inside the NCP1500. No external circuitry is required to stabilize the operation of the NCP1500. The error amplifier provides an error signal to both the PWM circuit and the linear regulator circuit. The output of the error amplifier is directly connected to the linear regulator control circuit. However, the output of the error amplifier is connected first to a subtraction circuit before going to the input of the PWM comparator. The subtraction circuit is activated only during an over current condition. During this condition, a signal proportional to the amount of over current is subtracted from the error amplifier signal. This subtraction results in a lower signal applied to the PWM comparator, thus lowering the output duty cycle.

The output voltage is digitally programmable up to four voltages. Two program pins are provided to accomplish this task. The program pins control a mux, which switch a bank of resistors. The appropriate resistor bank is switched to the error amplifier input, depending on the program input. The following truth table can be used to program the output voltage:

CB0	CB1	Output Voltage
0	0	1.5
0	1	1.8
1	0	1.3
1	1	1.0

Both program pins are internally pulled low. Thus, if the input pins are left open, the output voltage will be 1.5 V.

PWM Section

The PWM section consists of a PWM comparator, set dominant latch, slope compensation circuit, current sense circuit, and current limit circuit.

The NCP1500 operates as a current mode regulator in PWM mode. In this mode, a PWM pulse from the synchronization section initiates the output switch conduction. Output switch conduction is terminated when the peak inductor current reaches a threshold level established by the error amplifier. The output switch conduction duty cycle is allowed to go to 100% to increase transient load response when going from light load to heavy load.

A reset dominant latch is provided in the NCP1500. A 3 input OR gate controls the reset pin. Any one of the 3 inputs will terminate output switch conduction. Once terminated, output switch conduction cannot begin again until the next PWM pulse. The only state the NCP1500 does not switch every cycle is if the 5% overvoltage comparator trips. When the comparator trips, the switching regulator will remain off until the voltage drops below the nominal voltage. This state is similar to a PFM mode of operation. Output switch conduction can begin at the next PWM cycle after the OVP input is reset.

Current mode controllers can exhibit an instability at duty cycles over 50%. A slope compensation circuit is provided inside the NCP1500 to overcome the potential instability. Slope compensation consists of a ramp signal generated by the synchronization block and adding this to the current signal. The summed signal is then applied to the PWM comparator.

A current limit feature is provided in the PWM mode only. The current limit is set to allow peak switch current in excess of 800 mA. It is implemented as a cycle−by−cycle current limit. Each on−cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction. An error signal is generated upon sensing an over−current condition. This signal is subtracted from the error amplifier output. This in turn reduces the PWM comparison threshold voltage, thus limiting the output duty cycle.

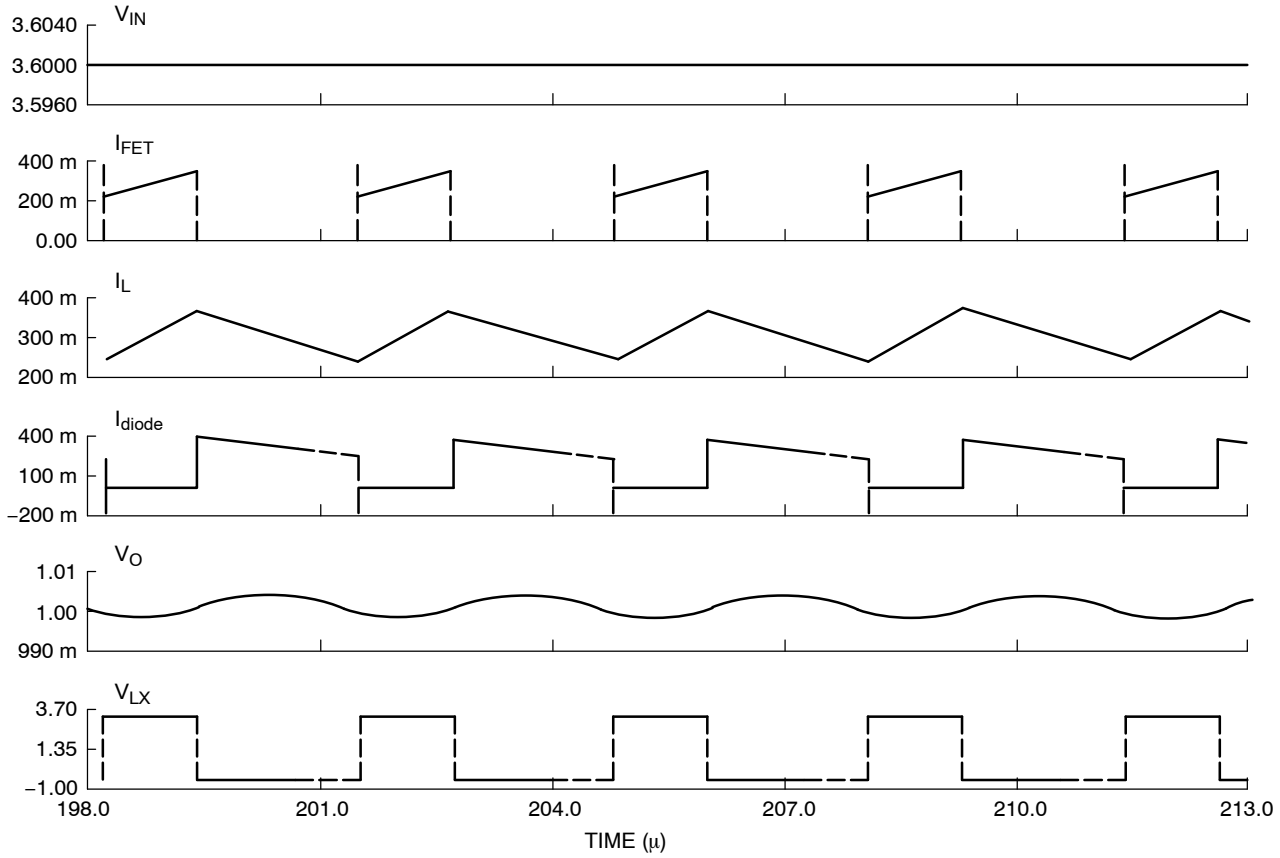


Figure 4. PWM Waveforms During Normal Operation

Linear Mode Operation

The NCP1500 operates as a linear regulator if the synchronization signal is absent. The part is designed to provide up to 50 mA nominally in this mode. Transients of up to 100 mA can be accommodated if the thermal impact is low. The main output is in series with an external inductor. This can cause a lag in the transient response of the device when going from light load to heavy load. A bypass transistor is incorporated to release the energy stored in the inductor in order to avoid oscillation within the operation range. (Patent Pending).

The following figure shows the transient step load response of the NCP1500 in this mode of operation.

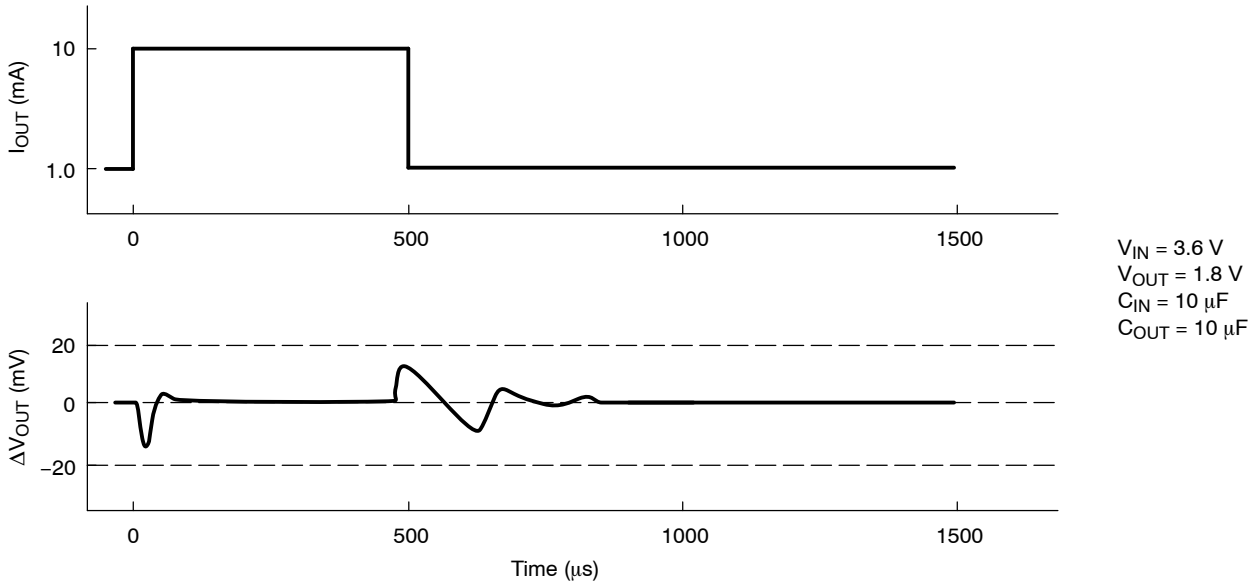


Figure 5. Load Transient Response in Linear Mode

Over Voltage Protection

NCP1500 has an overvoltage protection circuit that protects the output during the PWM mode. Normally, in PWM mode, the output switch will conduct at the onset of every synchronization pulse. The minimum output duty cycle is 3%. The output voltage will rise at minimum duty cycle and a light load or no load condition is present at the output. If the output rises more than 5% of the programmed voltage, an overvoltage comparator will trip. This signal will reset the PWM latch and hold it in a reset condition until the output voltage decays below its threshold. The output will then be allowed to switch at the next synchronization pulse. This type of operation is usually referred to as PFM or skip mode operation.

The following figure is a simulation of the regulator during this condition:

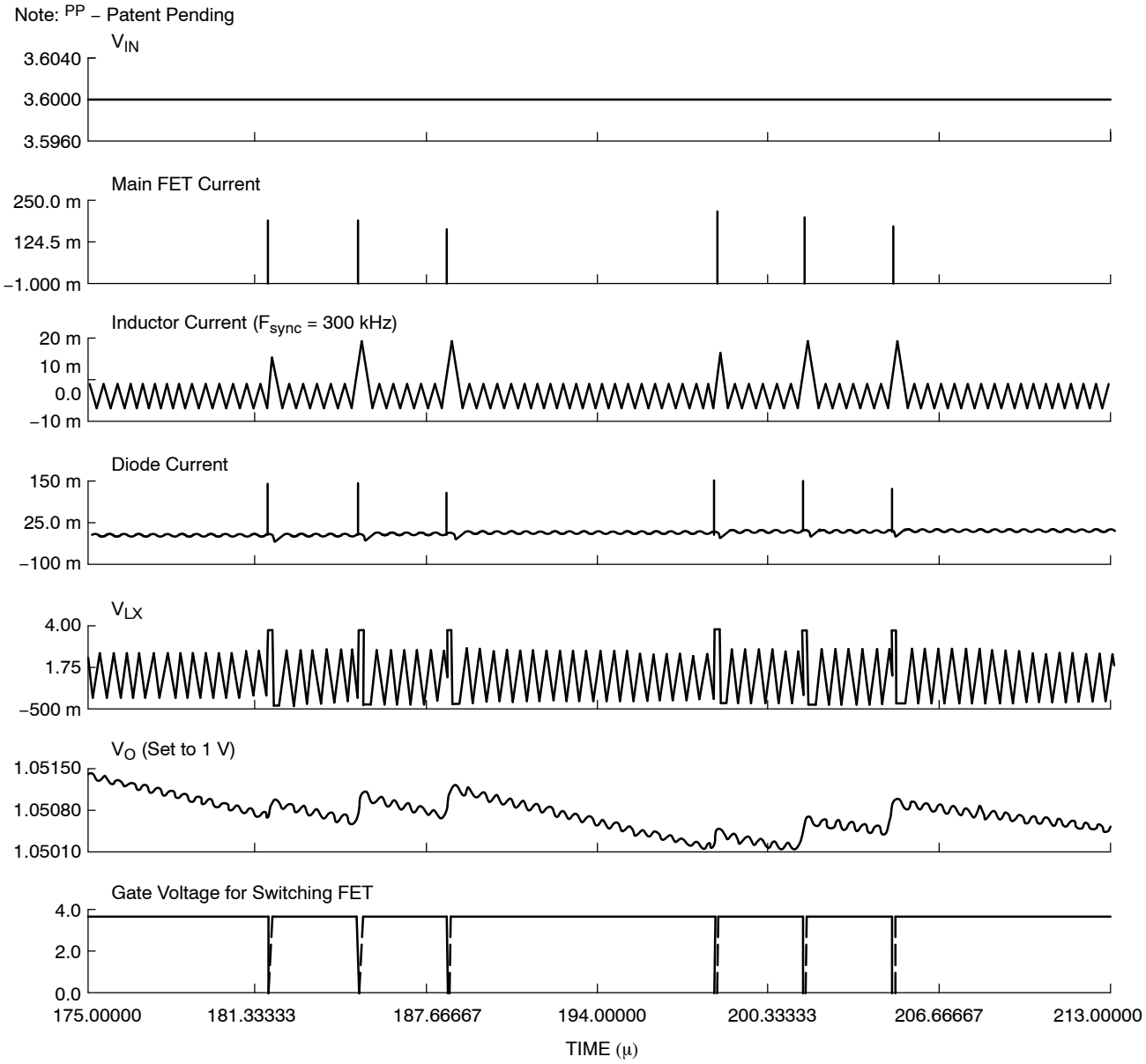


Figure 6. Waveforms of PFM Mode Operation During Over Voltage

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event at the maximum junction temperature is exceeded. When activated, typically at 150°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the PWM latch and the regulator control circuitry cannot be re−enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended as a substitute for proper heatsinking**. The NCP1500 is contained in the Micro8 package.

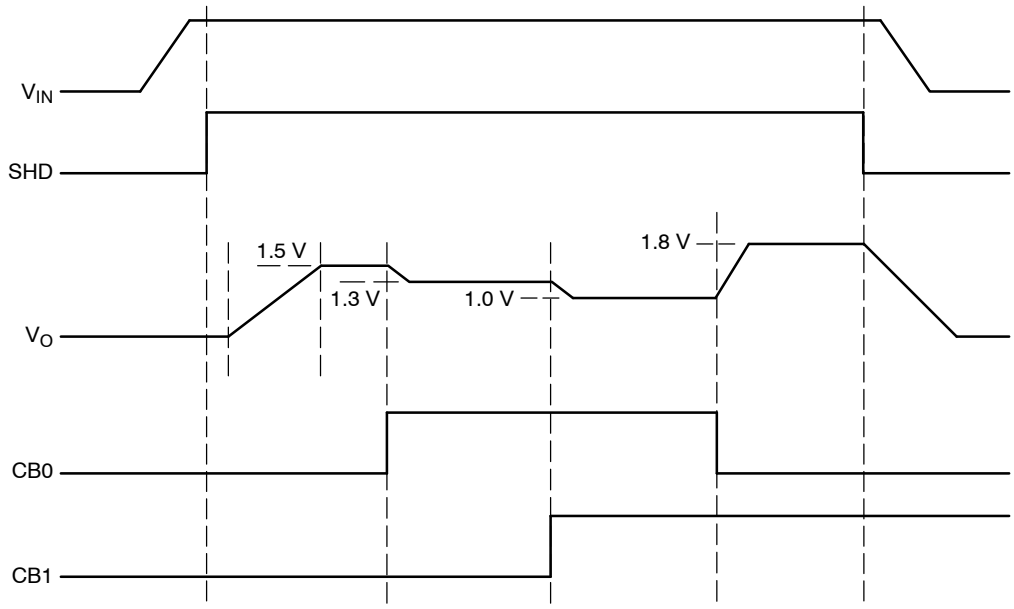


Figure 7. Power−Up and Power−Down Sequence

APPLICATIONS INFORMATION

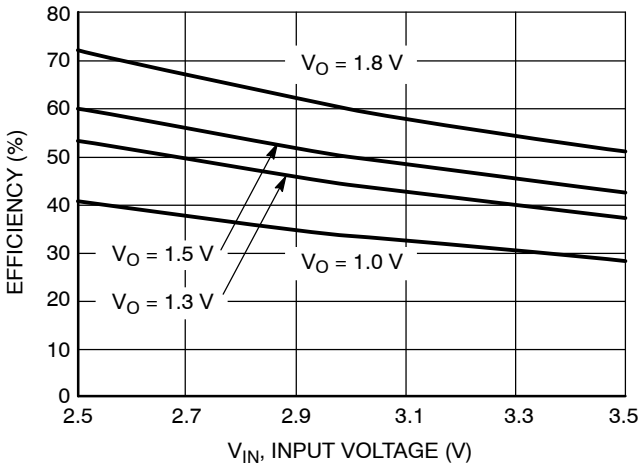


Figure 8. Efficiency in Linear Mode Operation vs. Input Voltage (I_{OUT} = 10 mA)

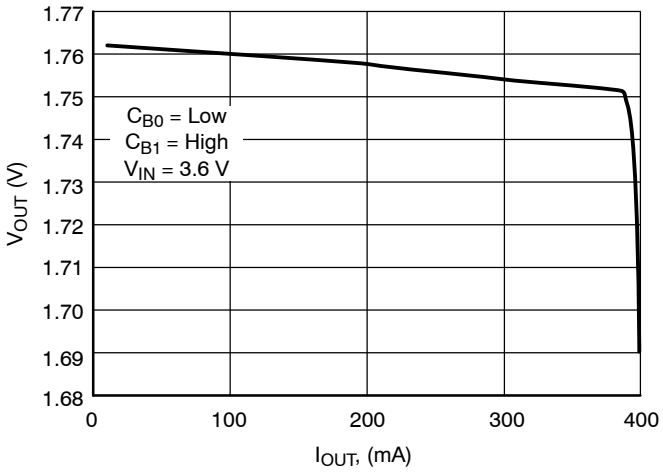


Figure 9. Output Voltage vs. Output Current in LDO Mode

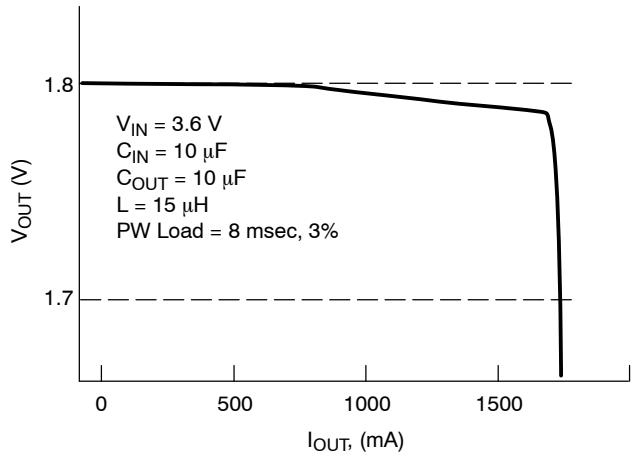


Figure 10. Output Voltage vs. Output Current in PWM Mode

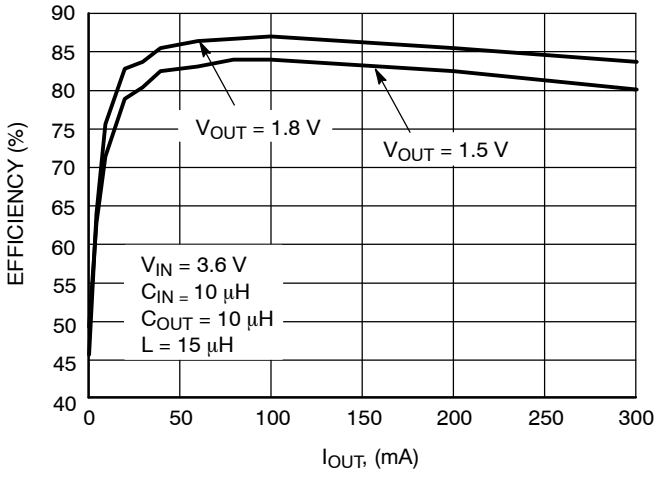


Figure 11. PWM Efficiency

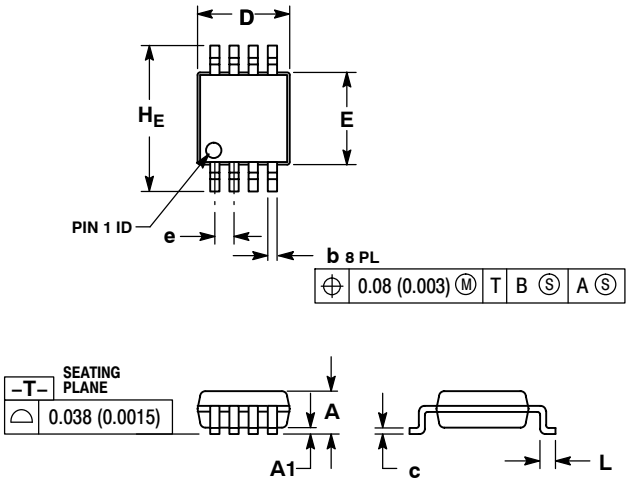
Table 1. Efficiency Measurement in PWM Mode

V_{OUT} (V)	V_{IN} (V)	I_{OUT} (mA)										
		1	5	10	20	30	40	60	80	100	200	300
1.5	2.5	44%	75%	82%	86%	87%	88%	88%	88%	90%	84%	80%
	3.0	44%	68%	76%	82%	84%	85%	86%	86%	86%	83%	80%
	3.6	49%	62%	71%	79%	80%	83%	83%	84%	84%	82%	80%
	4.2	51%	64%	66%	75%	77%	80%	81%	82%	82%	82%	79%
1.8	2.5	48%	79%	86%	90%	90%	91%	91%	91%	91%	87%	84%
	3.0	41%	73%	80%	85%	88%	88%	89%	89%	89%	86%	84%
	3.6	45%	64%	76%	83%	84%	86%	86%	87%	87%	85%	84%
	4.2	52%	63%	71%	78%	81%	83%	84%	85%	85%	85%	83%

NOTE: See figure 1 for circuit configuration.
C_{in} = C_{out} = C3216X5R106M
L = D01606T−153

PACKAGE DIMENSIONS

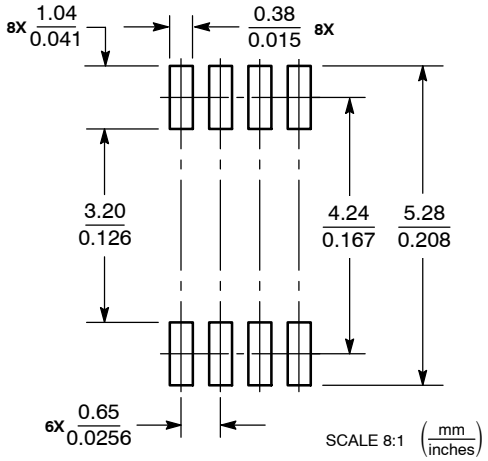
Micro8™
CASE 846A–02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	––	––	1.10	––	––	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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NCP1500/D