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April 1st, 2010 Renesas Electronics Corporation

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ess ope Note: Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp. Customer Support Dept. April 1, 2003



M66240P/FP

4-CH 16-BIT PWM GENERATOR

DESCRIPTION

The M66240 is a programmable channel PWM generator produced using the silicon gate CMOS process.

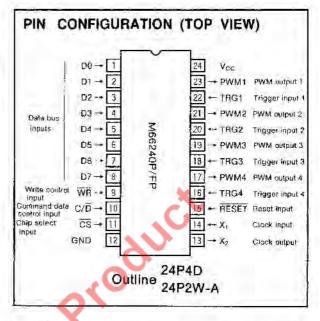
The M66240 can connect directly to the MPU data bus and consists of a 16-bit prescaler and a PWM counter. The pulse output includes three kinds of modes, allowing the independent control of each channel. Combining the A-D function and the timer function of the one-chip microcomputer provides a software servo system.

FEATURES

- 4-channel independent control possible
- Three pulse output modes incorporated.
- PWM repetitive frequency: 50kHz (max.)
 (Mode 0, 8-bit resolution, fxin/255 at prescaler setting=0)
- Output polarity selection possible
- · External triggering possible
- The output after reset is in the high impedance state.
- Change of mode setting becomes effective after the current cycle.
- The RESET incorporates a negative-going noise eliminator and the TRG1-4 incorporates a positive-going noise eliminator.
- High output current : Io = ±24mA

APPLICATION

Control of DC motors and stepping motors, heater phase controllers, software serves for office automation equipment, and industrial equipment.



FUNCTION

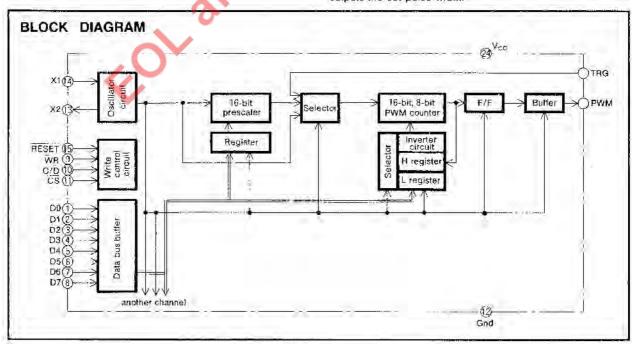
Four separate 16-bit prescalers and 16-bit PWM counters can be separately programmed by the control instruction from the MPU.

The output is made in one of three modes (Mode 0, Mode 1, and Mode 2).

In Mode 0, setting only the value of H width repeatedly outputs the set pulse width.

In Mode 1, setting only the value of H width outputs one shot of the pulse width set by trigger input.

In Mode 2, setting both H width and L width repeatedly outputs the set pulse width.



PIN DESCRIPTIONS

Plu name	Description	I/O	Function
RESET	Heset input	Input	C'ears the command register and the flip-flop at "L"
D0~D7	Data bus input	Input	Inputs the data from MPU over the 8-bit data bus.
WR	Write input	Input	Willes the data bus data to the control register or data register when the state changes from "L" to "H".
C/D	Command/data input	Input	Data at the data bus is regarded as a command at high level and as data at low level.
CS	Chip select input	Input	Communication with MPU is enabled at low-level. Any control from MPU is ignored at high lovel.
X1	Clock input	Input	I/O to the built-in clock generator circuit. Providing a crystal resonator between X ₁ and X ₂ sets the frequency.
X2	Glock output	Output	To make external clock input, connect the clock source to X ₁ pin and leave X ₂ pin open.
TRG1~ TRG4	Trigger input	lippul	This is used when external trigger is selected in mode setting. Set to low level when not in use.
PWM1~ PWM4	PWM output	Output	PWM output pins. Outputs become the high-impedance state after reset or after disable is specified by command 3. D0 of command 1 allows the selection of output polarity.

OPERATION Commands

The information on data bus inputs D0 through D7 is loaded as command when command data control input $C/\overline{D}=1$ and as data when $C/\overline{D}=0$.

There are three kinds of commands. (See Figure 1.)

Command 1 selects the output mode and external trigger input of each channel and sets the output polarity of H width. Command 2 specifies, on a byte basis, to which 16-bit register of the prescaler and PWM counter of each channel data is to be written.

The second and subsequent bytes of command 2 write prescaler value and PWM value. Depending on the location specified by command 2, the data of the second and subsequent bytes must be written in the order shown in Figure 2.

Command 3 is used to start or stop the prescaler and PWM counter operation.

Data input

At initialization, all 16 bits of the prescaler value must be written

In mode 0 or 1, the PWM value must be written to all 16 bits of H register (In mode 0 at 8-bit resolution, only the lower byte of the H register is used.); In mode 2, the value must be written to all 16 bits of H and L registers.

To change the values of all 16 bits in the prescaler or the PWM counter during operation, values should be written to the upper byte first and then to the lower byte. To change the values of the lower byte only, the values of only the lower byte should be written.

To change the values of the upper byte, the values of all 16 bits should be written. To change the values of H register in Mode 2, the H register value should be written followed by the L register value.

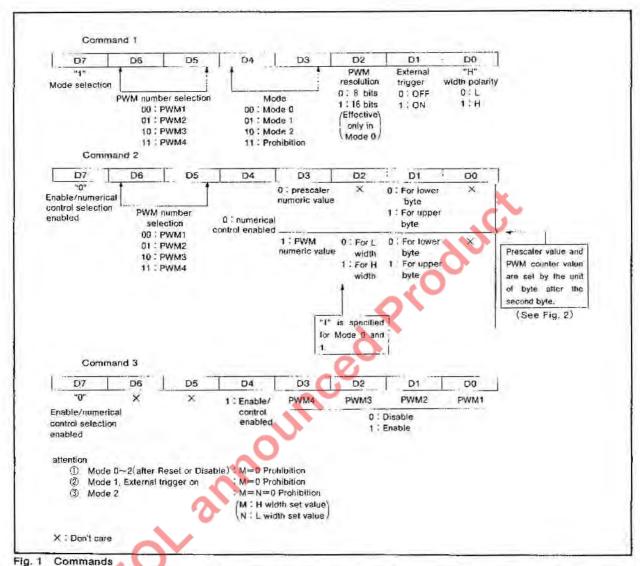
When values are written to the lower byte (lower byte of L register in Mode 2), the write cycle of data register is completed.

If the data register value is changed during a PWM signal output operation (exactly, after the end of the write operation), the PWM output is updated starting with the cycle next to the current output cycle.

To change the mode (i.e., to execute command 1), disable the output first (i.e., execute command 3).

Figure 3 shows the flow chart of the basic operation. (The order of the prescafer's and PWM counter's data setting is not fixed.)





First b	yte (comr	nand 2)	A . 6 (1) (1) (1)		1 1000000	400.00	
D3	D2	D1	Second byte	Third byte	Fourth byte	Fifth byte	Bemark
1	1	a	Upper byte for PWM H register	Lower byte for PWM H register	-		- When Mode0 or
1	. 1	0	Lower byte for PWM H register	-		3-	when woden or
1	1	1	Upper byte for PWM H register	Lower byte for PWM H register	Upper byte for PWM L register	Lower byte for PWM L register	
1	1	0	Lower byte for PWM H register	Upper byte for FWM L register	Lower byle for PWM L register		
1	0)	Upper byte for PWM L register	Lower byte for PWM L register	-	-	When Mode 2
1	0	0	Lower byte for PWM L register		-	-	
0	×	1	Upper byte for prescaler register	Lower byte for prescalor register	-	-	
0	×	0	Lower byte for prescaler register		-	-	

Fig. 2 Data-setting sequence for registers



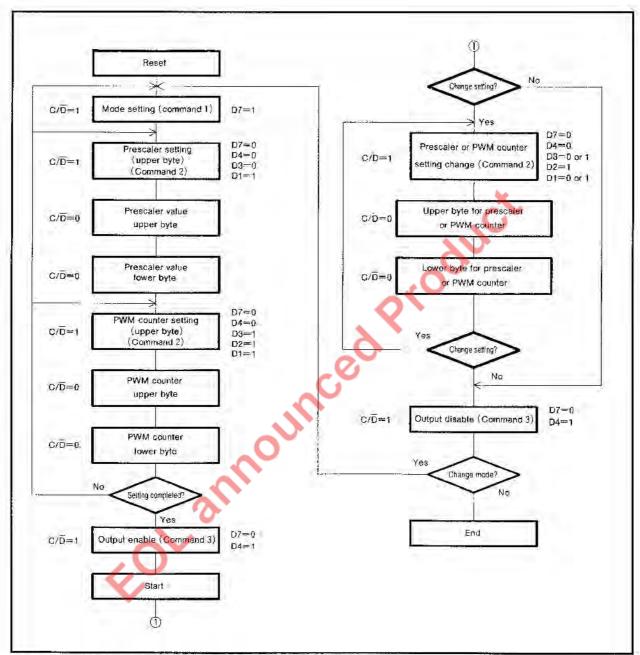


Fig. 3 Flow chart in Mode 0 or 1 (for one channel)

PWM waveform output

The M66240 has a built-in 16-bit prescaler and a PWM counter. The duty cycle of output pulse can be freely specified by changing the values of the prescaler and the PWM counter. The output is made in one of three modes (Mode 0, Mode 1, and Mode 2). The description of these modes is given below.

(1) Mode 0

This mode is selected by writing "0" to D4 and D3 in com-

Figure 9 shows the block diagram (for one channel) in this mode.

The 16-bit PWM counter can be used as an 8-bit PWM counter only in this mode (command 1: D2=0). The setting with PWM resolution=8 bits must be written to the lower 8 bytes of H register. In this mode, the H output pulse width is determined by the prescaler register value L and PWM register value M. The PWM output cycle time is determined by the prescaler register value L, irrespective of the PWM register value M. (See Fig. 4)

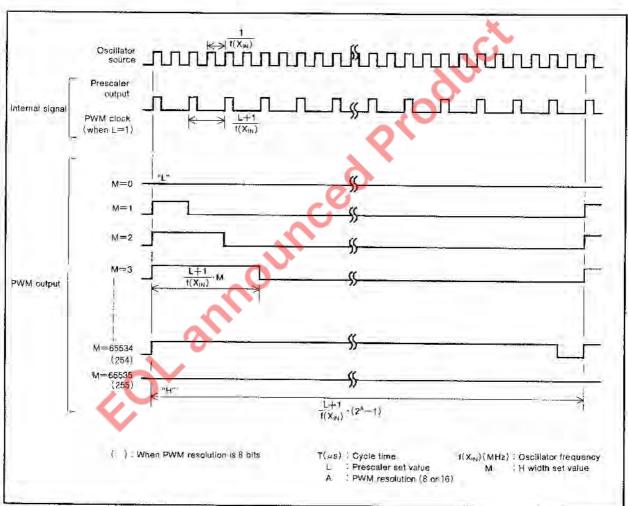


Fig. 4. (When H width polarity is "H")



[2] Mode 1

This mode is selected by setting D4=0 and D3=1 in command 1.

Figure 10 shows the block diagram in this mode (for one channel).

This mode outputs, on the trigger signal, one shot of the pulse determined by value M of PWM register. The type of this output operation is determined by whether the external trigger signal or the internal trigger signal is used. Operation varies according to the choice of external and internal trigger signals.

① External trigger selected (D1=1 in command 1): This mode outputs, when a trigger pulse is applied to trigger input TRG, one shot of output pulse. Therefore, cycle time T becomes cycle time f_{IN} of the trigger pulse to be applied to trigger input TRG.

The output pulse width is determined by the prescaler register value L and PWM register value M. (See Fig. 5)

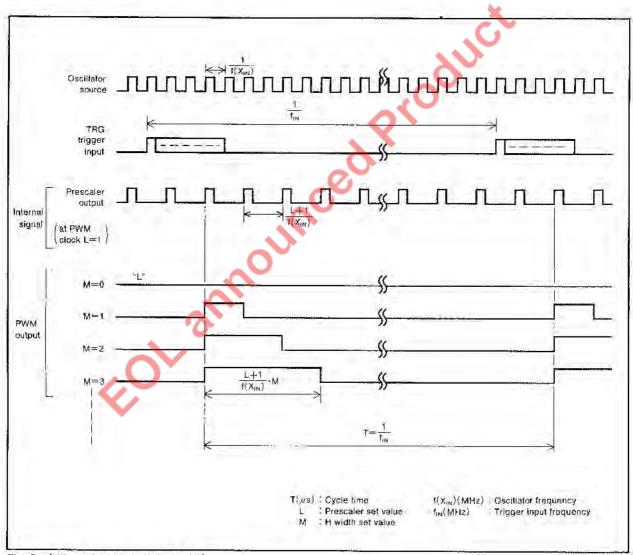


Fig. 5 (When H width polarity is "H")

② Internal trigger selected (D1=0 in command 1): In this mode, the trigger signal is generated by the prescaler. Therefore, the cycle time \top of output pulse is determined by the prescaler register value L. In this case, the

oscillator source becomes the PWM counter clock and the output pulse width is determined by the PWM register value M. (See Fig. 6)

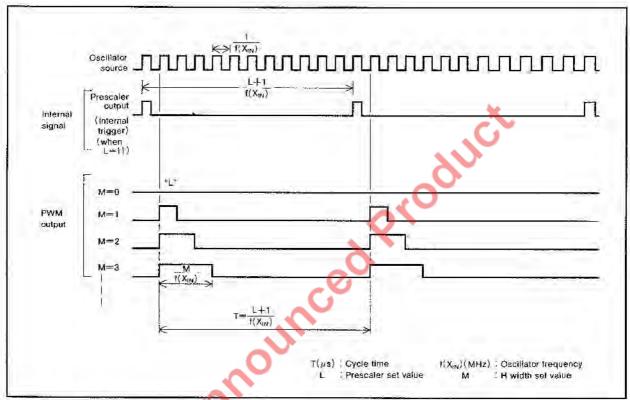


Fig. 6 (When H width polarity is "H")

In Mode 1, the retrigger state is caused when the cycle time of trigger pulse gets smaller than value M of PWM register.



(3) Mode 2

This mode is selected by writing D4=1 and D3=0 in command 1. Fig. 11 shows the block diagram of this mode (for one channel).

The high-level pulse value M is set to the H register of PWM in Modes 0 and 1, but, in this mode, the high-level

pulse value M is set to the H register of PWM and the lowtevel pulse value N is set to the L register of PWM. Therefore, the pulse width and cycle time T of PWM output are determined by value L of the prescaler register and values M and N of H and L registers of PWM (see Fig. 7).

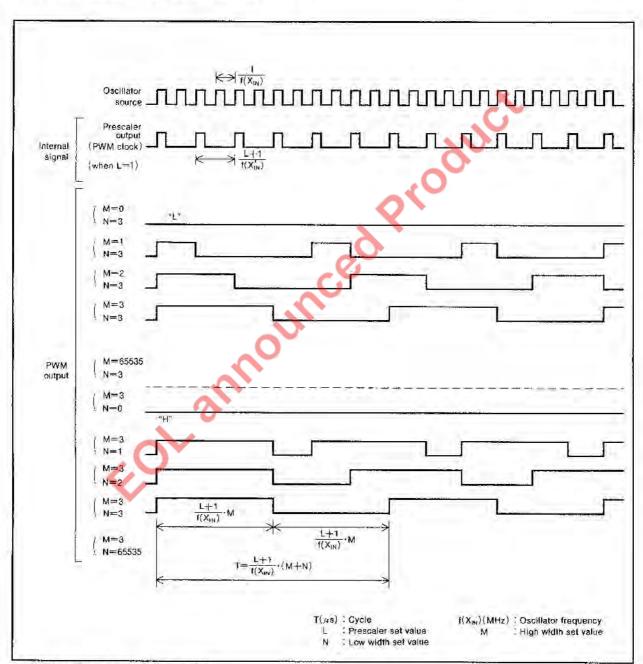


Fig. 7 (When H width polarity is "H")

Initial state

When external trigger ON is selected in D1 in the case of Command 1, starting the operation of the internal circuit by writing enable by Command 3 does not output a pulse to PWM output, which is held in the high impedance state.

The pulse can be output to PWM output by entering H level

in TRG input for Mode 0 or Mode 2 or H pulse in TRG input in Mode 1 (see Fig. 8).

Putting TRG input to L level during PWM output in Mode 0 or Mode 2 makes PWM output keep its state. Putting TRG input back to H level starts the operation from that point.

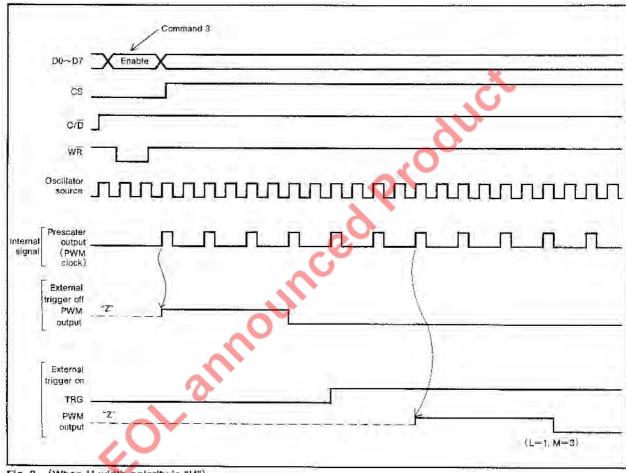


Fig. 8 (When H width polarity is "H")

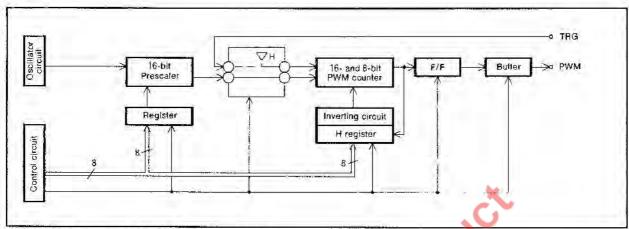


Fig. 9 Block dlagram in Mode 0 (for one channel)

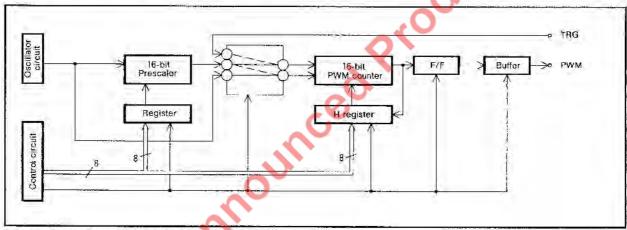


Fig. 10 Block diagram in Mode 1 (for one channel)

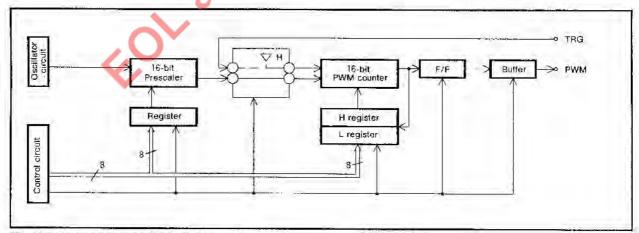


Fig. 11 Block diagram in Mode 2 (for one channel)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Hatings	Unit
Vac	Power voltage		-0.5~+7.D	V
V _i	Input voltage	100	-0.5~Vco+0.5	٧
Vo	Output voltage		-0.5~Vcc+0.5	V
lik	Input protect diode current	V ₁ <0V	20	1.55
sik.	inplic protect diode current	V ₁ >V _{CC}	+20	mA
Acres 1	Output parasitic diode current	V ₀ <0V	-20	75.4
Ток	Output parastile ologia current	V _O >V _{CC}	+20	mA
lo	Output current	1 - 0	±50	mA
lee	Power/GND current	Vcc GND	±200	mA
Pd	Power dissipation		500	mW
Tsig	Storage temperature		<u>−65~150</u>	°C

RECOMMENDED OPERATING CONDITIONS

Postal List	Parameter	1 - William 1	Limits		Unit
Symbol	Farameter	Min.	Тур.	Max.	Unit
Vac	Power voltage	4.5	5, 0	5.5	V
GND	Power vollage		0		٧
V ₁	input voltage	0	111200	Voc	٧
Vo	Output voltage	0		Vcc	V
Topr	Ambient operating temperature	40		85	°C

ELECTRICAL CHARACTERISTICS (Ta=-40~85°C Vcc=5V±10%)

Symbol	Description	Test conditions		Limits	Unit
Symbol	Parameter	l est conditions	Min,	Тур. Мах.	Unit
V _T +	Positive going threshold voltage	V ₀ =0.1, V ₀₀ -0.1V, I ₀ =20μA RESET, TRG1~4		2. 4	٧
V _T	Negative going threshold voltage	V ₀ =0.1, V ₀₀ =0.1V, I ₀ =20μΛ RESET, TRG1~4	0.6		v
V _H	Hysteresis width	V _O =0.1, V _{OC} =0.1V, I _O =20µA RESET, TRG1~4	0.2		V
V _{IH}	"H" Input voltage	V ₀ =0.1, V _{CC} =0.1V, I ₀ =20μA D ₀ ~D ₇ , CS, WR, C/D	2.0		V
Vil	"L" Input voltage	$V_0 = 0.1$, $V_{00} = 0.1$ V, $I_0 = 2G\mu A$ $D_0 \sim D_7$, CS, WR, C/D		0.8	V
V _{tH}	"H" input voltage	$V_0=0.1, V_{CC}=0.1V, I_0=20\mu A$	V _{GC} ×0.8		v
VIL	"L" input vollage	V _O =0.1, V _{GC} -0.1V, I _O =20μA X1		V _{cc} ×0.	2 V
VoH	"H" output voltage	V _I =V _{IN} , V _{IL} I _{OH} =24mA PWM1~PWM4	V _{cc} -0.8		V
VoL	"L" output voltage	V _I =V _{IH} , V _{IL} I _{OL} =24mA PWM1~PWM4		0.55	v
lie.	"H" input current	V _t =V _{CC}		1.0	μА
his	"L" input current	V _I =GND		-1.0	μA
lozh	Off-state "H" output corrent	Vo≔Vcc		5.0	μA
lozL	Off-state "L" output current	Vo=GND		-5.0	μ A
loc	Quiescent current consumption	V _i =V _{OC} , GND I _O =θμΑ		100	μА
Alco	Max. quiescent current consumption	V _i =2, 4V, 0, 4V (Note 1)		2.9	mA

Note 1: Set only one input to this value; fix other inputs to V_{CC} or GND.



SWITCHING CHARACTERISTICS (Ta=-40~85°C, Vcc=5 V±10%)

Symbol	Parameter	Test conditions		Limits		Unit
	***	, ast conditions	Min.	Тур.	Max.	Uni
t _{PZu} (₩-pww)	Output cnable time after write (Mode 0, 2, external trigger OFF)			L+2 1 +44	L+2 +110	ns
tezhiw-pwm:	Output enable time after write (Mode 0, 2, external trigger OFF)	-1		L+2 1+43	L+2 1+110	пз
Inzulw-pwm)	Output enable time after write (Modo 1, external trigger OFF)	I		L+3 1+34	L+3 1+110	ns
tezh(W pwM)	Output enable time after write (Mode 1, external trigger OFF)		I	L+3 1+33	L+3 1+110;	ns
tezuit-pwni	Output enable time after trigger (Mode 0, 2, external trigger ON)			2(1-1)	2(L+1) f +110	ns
t _{P2H1*··PWM})	Output enable time after trigger (Mode 0, 2, external trigger ON)		C.	2(L F1) 1 +38	2(1+1) 1 +110	ns
Inzlit-PWM)	Output enable time after trigger (Mode 1, external trigger ON)	100	1	2(L+1) 1 +4:	2(L+1) 1+10	ns
lezh(T-PYM)	Output enable time after trigger (Mode 1, external trigger ON)			2(L+1) 1 +39	2(L+1) 1+110	ns
FLH(XI-PWM)	Output propagation time after clock (all modes)	— : C _L =50pF		41	110	ns
bac(x)-awa)	Output propagation time after clock (all modes)			44	110	ns
bluil swan	Output propagation time after trigger (Mode 1, external trigger ON)	.0		2(L+1) 1 +40	2(£+1) +110	ns
(PHL(T PWM)	Output propagation time after trigger (Mode 1, external trigger ON)	700	365000	$\frac{2(L+1)}{l}+4c$	2(L+1) +(10	ns
PLZIB-PWM:	Output disable time after reset		1	58	150	ns
tenzin-pwm:	Output disable time after reset			: 60	150	ns
t _{P: 2} :w - нум)	Output disable lime after writio		-	32	150	ns
lenz:w-evm).	Output disable time after write		1	30	150	ris

f(MHz) : Clock input frequency L : Prescaler setting

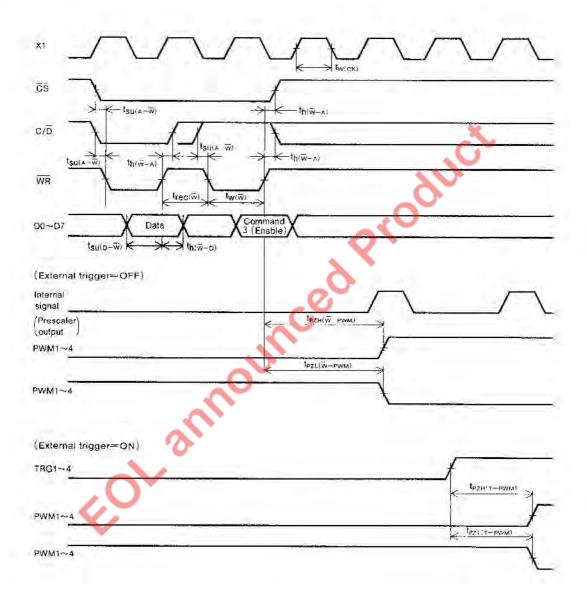
TIMING CONDITIONS (Ta=-40~85°C, Vgc=5 V±10%)

Symbol	Parameter	Test conditions		Limits		13-36
	Talallisto)	rest conditions	Min.	Тур.	Max.	Unit
tackii	Clock cycle		78.5			ns
twn(xt)	Clock "H" pulse width		35	9		ns
twi(x1)	Clock "L" pulse width		35	12	-	ns
tr(x1)	Clock rise time				20	ns
tf(x1)	Clock fall time	+	-		20	ns
tsu(AW)	Address setup time before write (CS, C/D)		0	11		ns
th(w-A)	Address hold time after write (OS, O/D)		0	-11	C ()	ns
tsu(n-w)	Dala setup time before write	7	100	55		ns
th(w-o)	Data hold time after write		0	28		ns
tw(W)	Write pulse width	1	100	12	() (de)	ns
trectwi	Write recovery time		1 100	12		ns
tw(r)	Trigger pulse width	4	100	23		ns
tw(H)	Reset pulse width		100	30		ns
trec(k-w)	Recovery time before write		100			ns



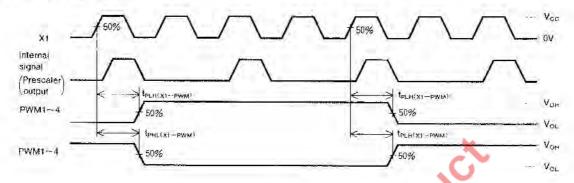
TIMING CHART

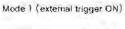
(1) MCU Interface

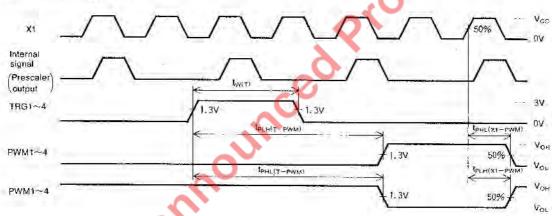


(2) In operation

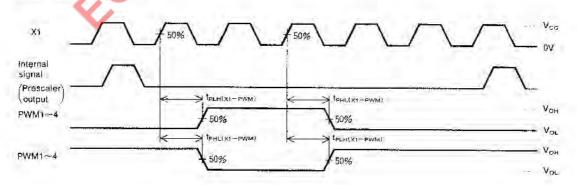
Mode 0, 2 (external trigger ON, OFF)



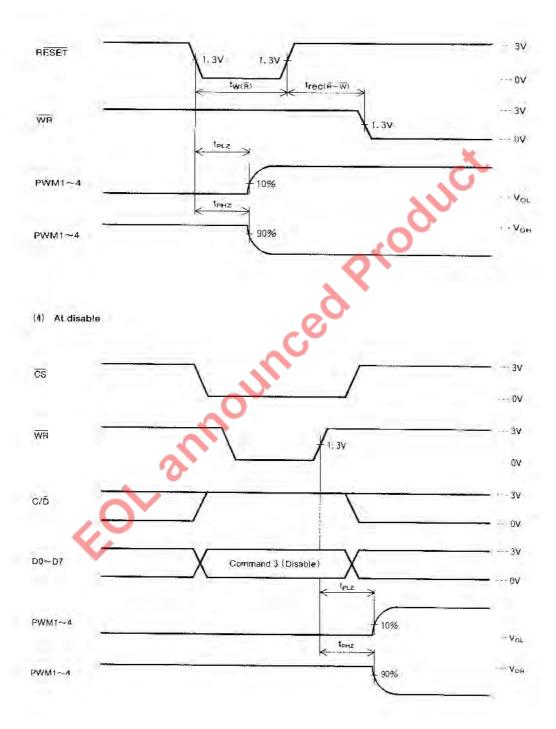




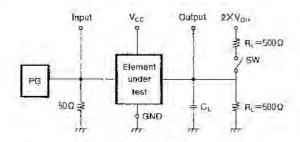
Mode 1 (external trigger OFF)



(3) At reset



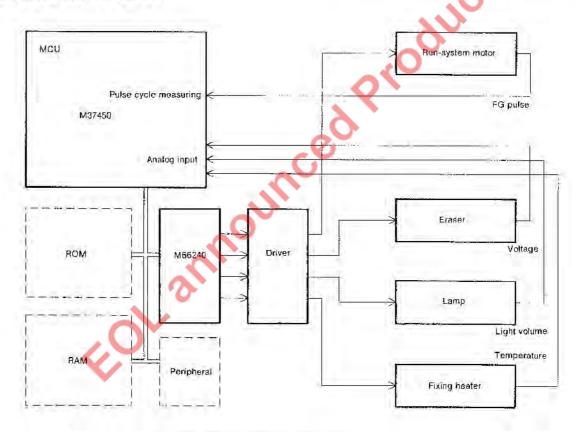
Measuring circuit



Parameter	sw
t _{TOH} , t _{THL} t _{PLH} , t _{PHL}	Open
tracz	Closed
tenz.	Open
t _{PZL}	Closed
l _{PZH}	Open

- Characteristics of pulse generator (PG)(10%~90%) t_r=3ns, t_f=3ns
- (2) C_L includes stray probe and wiring capacitance.

APPLICATION EXAMPLE



Note) M37450 : ROM 4KB~16KB RAM 128B~384B

Timer Multifunctional 16-bit type with pulse cycle measuring mode X3

A-D 8-bits, 8 channels PWM 20kHz cycle, 1 channel

UART Clock sync and async, 1 channel