Data Sheet March 20, 2007 FN6285.1

Multiphase PWM Controller with Linear 6-Bit DAC Capable of Precision $r_{DS(ON)}$ or DCR Differential Current Sensing

The ISL6564A is a Multiphase PWM controller which controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels. It features a high bandwidth control loop to provide optimal response to the load transients. With switching frequency up to 1.5MHz per phase, the ISL6564A based voltage regulator requires minimum components and PCB area in DC/DC converter application.

The ISL6564A senses current by utilizing patented techniques to measure the voltage across the on resistance, $r_{DS(ON)}$, of the lower MOSFETs or DCR of the output inductor during their conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, and overcurrent protection.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be completely eliminated using the remote-sense amplifier. Eliminating ground differences improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start up of the ISL6564A with any other voltage rail. Dynamic-VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting. The ISL6564A uses a 5V bias and has a built-in shunt regulator to allow 12V bias using only a small external limiting resistor.

Ordering Information

PART NUMBER	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6564ACRZ* (Note)	ISL6564 ACRZ	0 to +70	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL6564AIRZ* (Note)	ISL6564 AIRZ	-40 to +85	40 Ld 6x6 QFN (Pb-free)	L40.6x6

*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

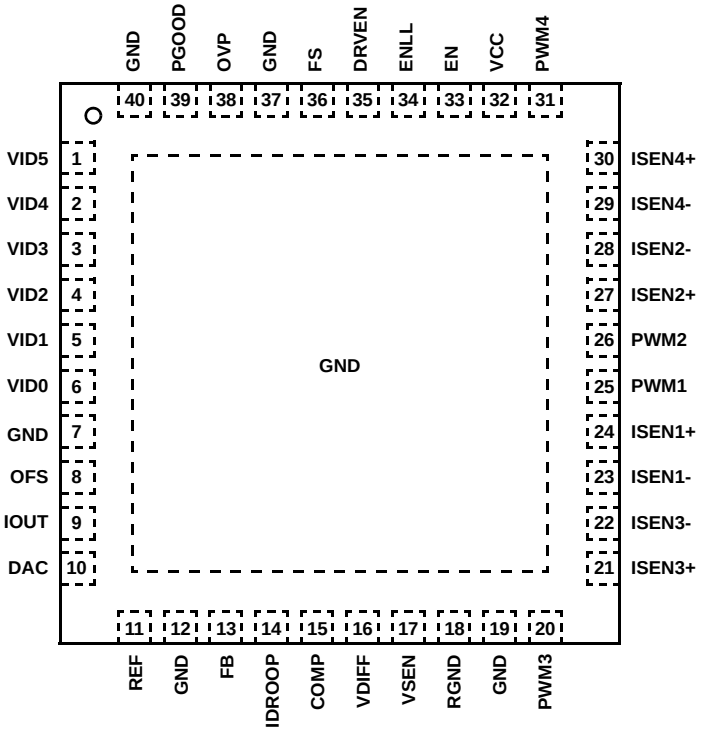
- Precision Multiphase Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy
  - Adjustable Reference-Voltage Offset
- Precision $r_{DS(ON)}$ or DCR Current Sensing
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Differential Current Sense
  - Low-Cost, Lossless Current Sensing
- Internal Shunt Regulator for 5V or 12V Biasing
- Microprocessor Voltage Identification Input
  - Self Clocked Dynamic VID™ Control Technology
  - 6-Bit VID Input
  - 0.525V to 1.300V in 12.5mV Steps
- Threshold-Sensitive Enable Function for Power Sequencing Control
- Overcurrent Protection
- Overvoltage Protection
  - No Additional External Components Needed
  - OVP Pin to Drive Crowbar Device
- 1, 2, 3, or 4 Phase Operation
- Up to 1.5MHz Per Phase Operation (>6MHz Ripple)
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2006-2007. All Rights Reserved. Dynamic VID™ is a trademark of Intersil Americas Inc.
All other trademarks mentioned are the property of their respective owners.

Downloaded from Elcodis.com electronic components distributor

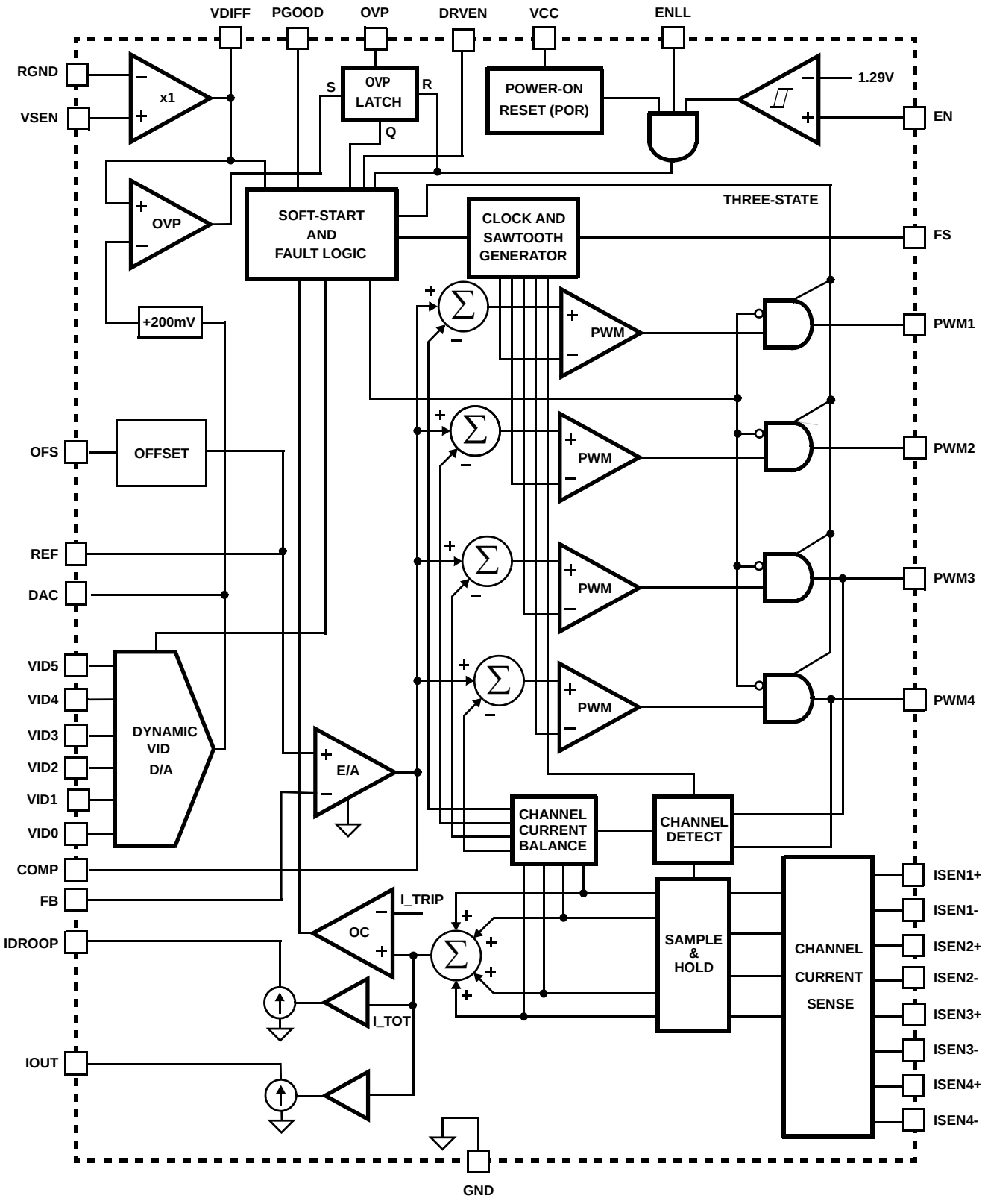
Pinout

ISL6564A
(40 LD QFN)
TOP VIEW



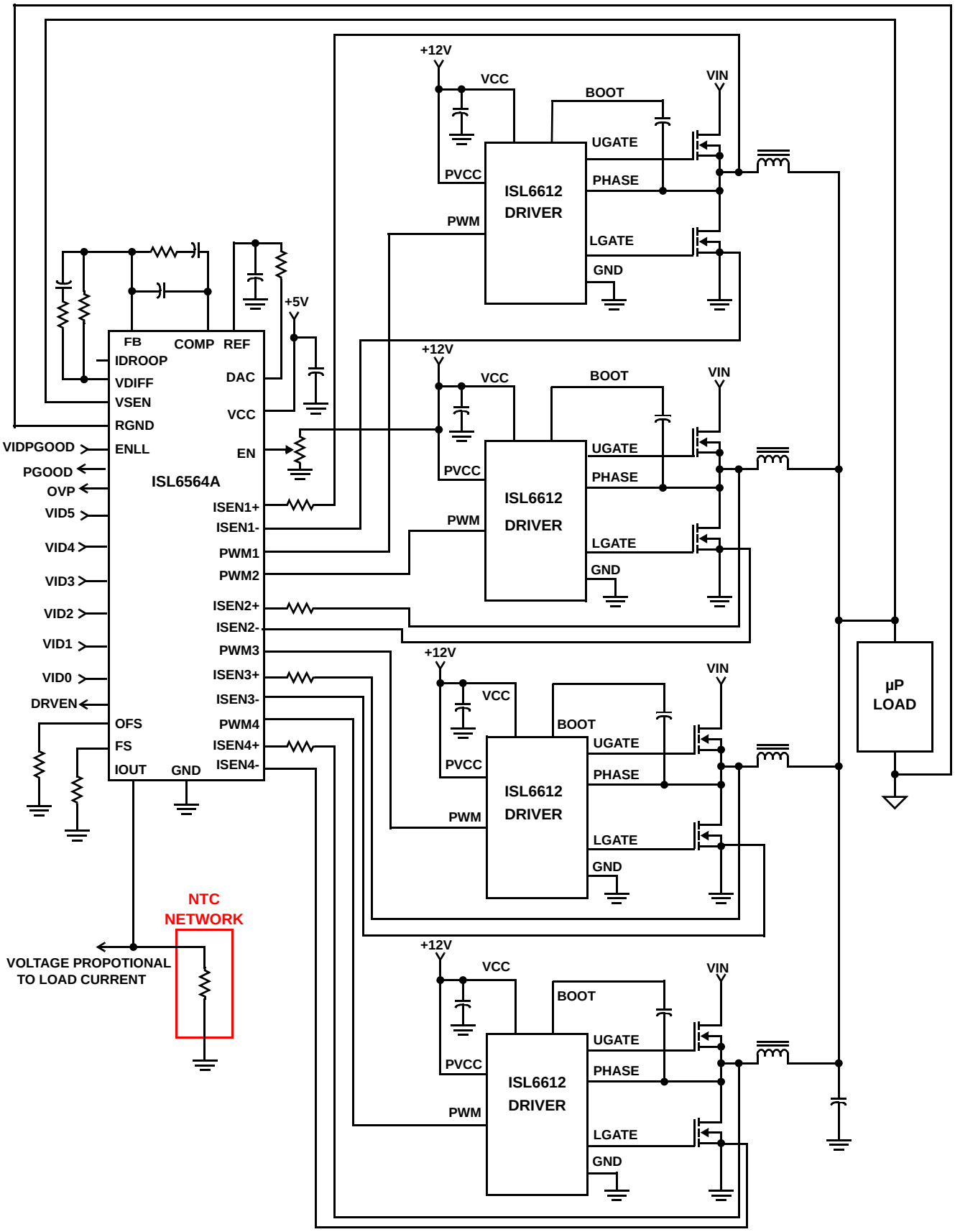
Downloaded from Elcodis.com electronic components distributor

ISL6564A Block Diagram



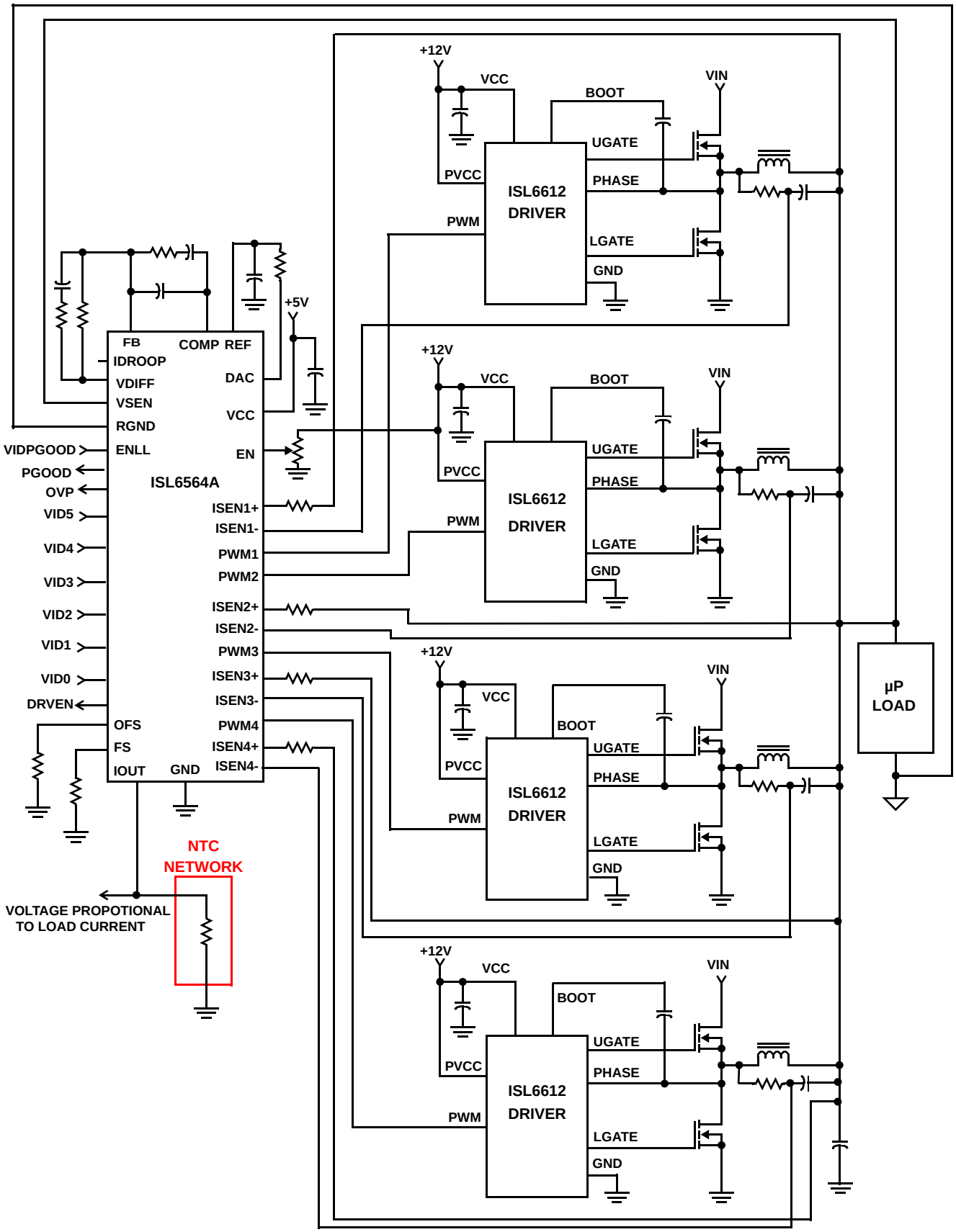
Downloaded from Elcodis.com electronic components distributor

Typical Application for Voltage Regulation without Droop Using $r_{DS(ON)}$ Sensing



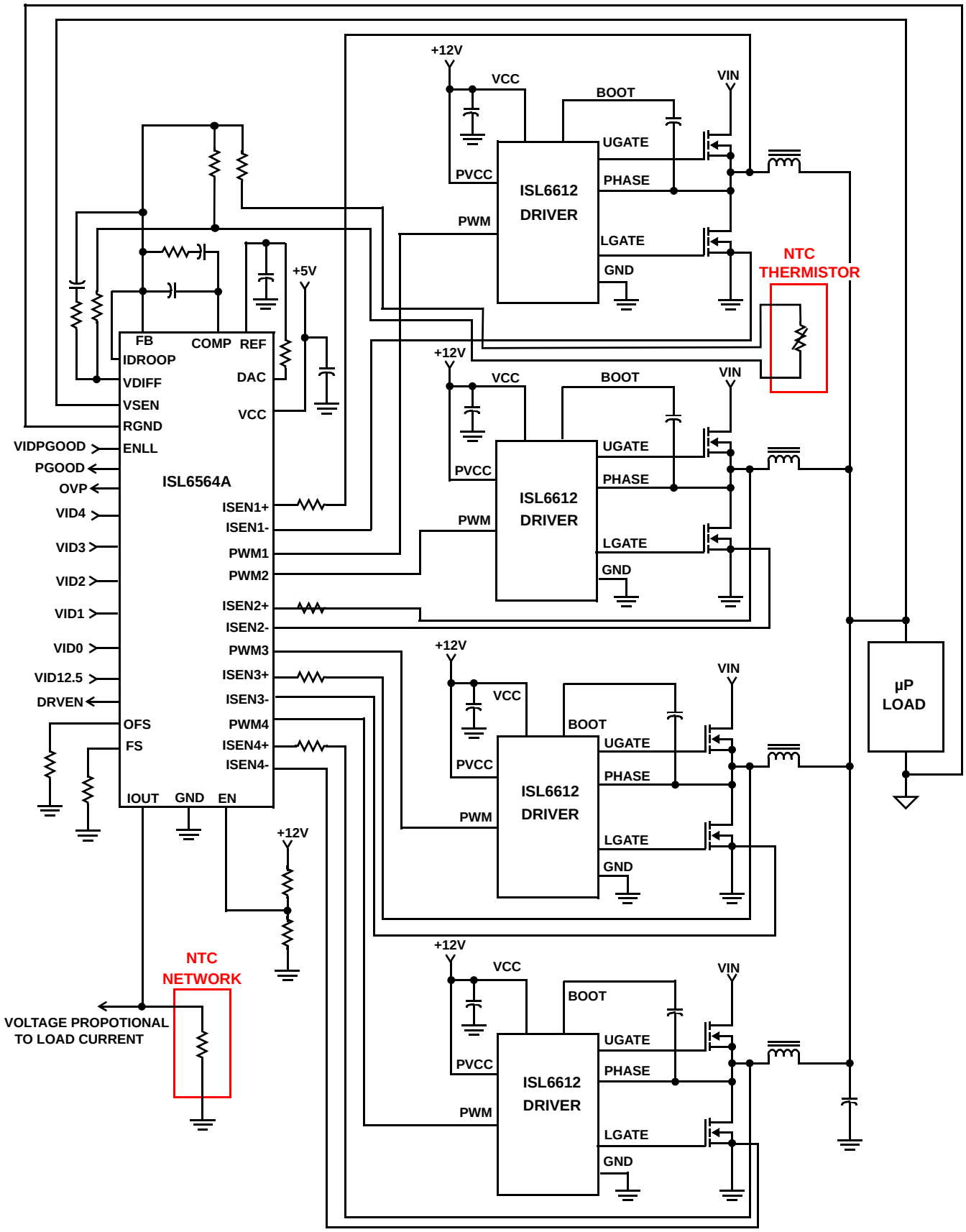
Downloaded from Elcodis.com electronic components distributor

Typical Application for Voltage Regulation without Droop Using DCR Sensing



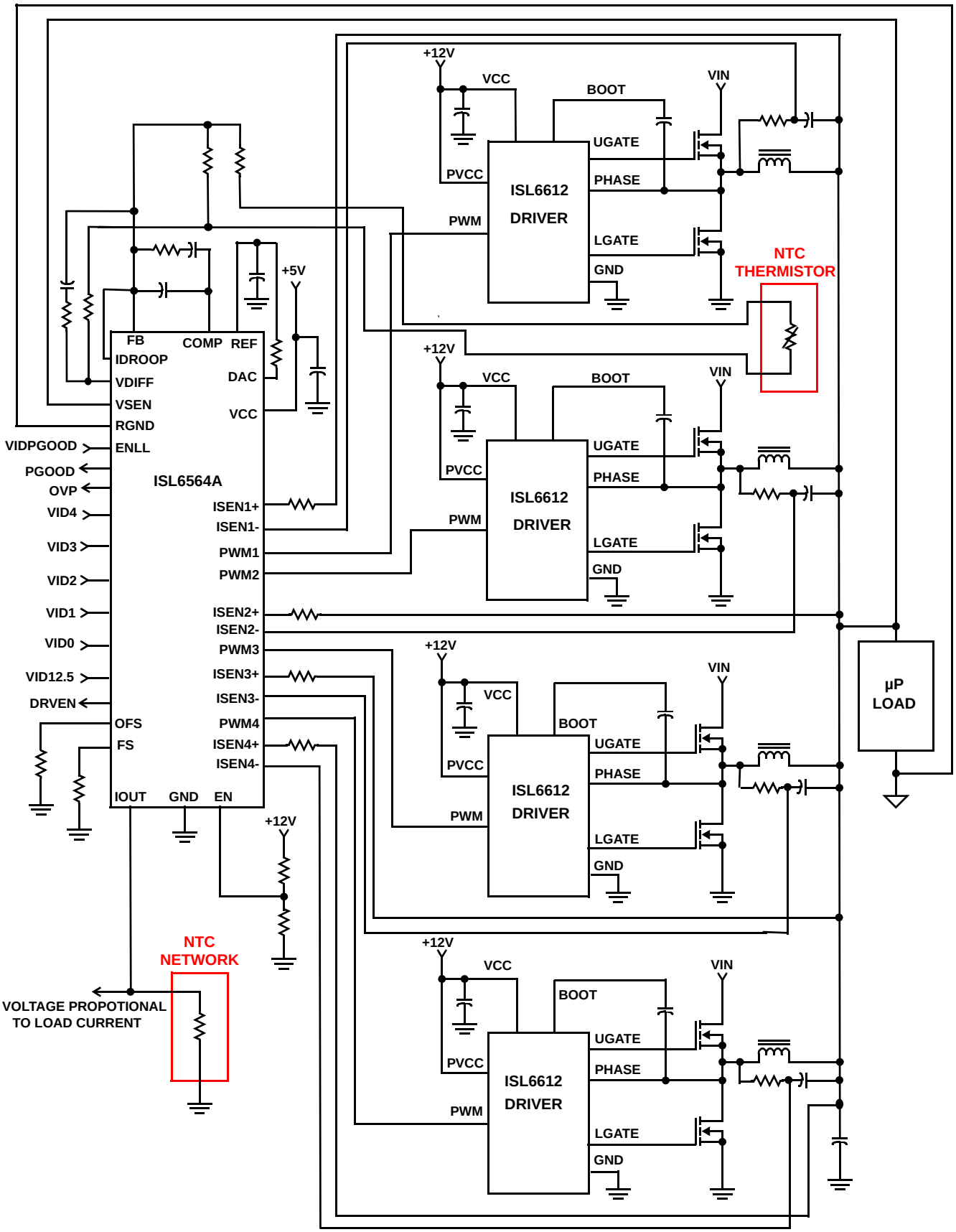
Downloaded from Elcodis.com electronic components distributor

Typical Application for Load Line Regulation Using $r_{DS(ON)}$ Sensing and External NTC



Downloaded from Elcodis.com electronic components distributor

Typical Application for Load Line Regulation Using DCR Sensing and External NTC



Downloaded from Elcodis.com electronic components distributor

Absolute Maximum Ratings

Supply Voltage, VCC . . . . . +5.5V
Input and Output Voltage (except OVP). . GND -0.3V to V_{CC} + 0.3V
OVP Voltage . . . . . +15V
ESD (Human body model) . . . . . >4kV
ESD (Machine model) . . . . . >300V
ESD (Charged device model) . . . . . >2kV

Operating Conditions

Supply Voltage, VCC (5V bias mode, Note 3) . . . . . +5V ±5%
Ambient Temperature (ISL6564ACRZ) . . . . . 0°C to +70°C
Ambient Temperature (ISL6564AIRZ) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	32	3.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . - 65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V or ICC < 25mA (Note 3). Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R_T = 100kΩ, ISEN1 = ISEN2 = ISEN3 = ISEN4 = -70µA	-	14	18	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R_T = 100kΩ	-	10	14	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC rising	4.20	4.31	4.50	V
	VCC falling	3.60	3.80	4.00	V
ENABLE Threshold	EN rising	1.26	1.29	1.32	V
	Hysteresis	110	125	135	mV
	Fault reset	1.12	1.16	1.20	V
ENLL Input Logic Low Level		-	-	0.4	V
ENLL input Logic High Level		0.8	-	-	V
ENLL Leakage Current	ENLL = 5V	-	-	1	µA
REFERENCE VOLTAGE AND DAC					
System Accuracy (VID = 1.V-1.3V)	(Note 4)	-0.5	-	0.5	%VID
System Accuracy (VID = 0.525V-0.9875V)	(Note 4)	-0.9	-	0.9	%VID
VID Pull-Up		-55	-45	-35	µA
VID Input Low Level		-	-	0.4	V
VID Input High Level		0.8	-	-	V
DAC Source/Sink Current	VID = 010100	-200	-	200	µA
VID Input Voltage when Floated		1.0	1.15	1.30	V
REF Source/Sink Current		-50	-	50	µA
PIN-ADJUSTABLE OFFSET					
Voltage at OFS Pin	Offset resistor connected to ground	388	400	412	mV
	VCC = 5.000V, offset resistor connected to VCC	2.91	3.0	3.09	V
Maximum OFS Source and Sink Current		-	-	50	µA

Downloaded from Elcodis.com electronic components distributor

Electrical Specifications Operating Conditions: VCC = 5V or ICC < 25mA (Note 3). Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Accuracy	R_T = 100kΩ	260	300	345	kHz
Adjustment Range		0.08	-	1.5	MHz
Sawtooth Amplitude		-	2	-	V
Max Duty Cycle		-	66.7	-	%
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	-	80	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground	-	18	-	MHz
Maximum Output Voltage		4.0	4.3	-	V
Output High Voltage @ 2mA		3.7	-	-	V
Output Low Voltage @ 2mA		-	-	1.35	V
REMOTE-SENSE AMPLIFIER					
Bandwidth		-	20	-	MHz
Output Voltage @ 1mA Load	VSEN - RGND = 2.5V	2.48	2.50	2.52	V
PWM OUTPUT					
PWM Output Voltage LOW	Iload = ±500µA	-	-	0.5	V
PWM Output Voltage HIGH	Iload = ±500µA	4.0	-	-	V
DRIVER ENABLE OUTPUT					
DRVEN Output Voltage LOW	Iload = ±1mA	-	-	0.3	V
DRVEN Output Voltage HIGH	Iload = ±1mA	4.0	-	-	V
SENSE CURRENT OUTPUT					
Sensed Current Accuracy	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80µA	75	85	93	µA
Overcurrent Trip Level		95	110	125	µA
Maximum Voltage at IDROOP and IOUT	VCC = 4.5V (Note 5)			2	V
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = 4mA	-	-	0.3	V
Undervoltage Offset From VID	VSEN falling	70	75	80	%VID
Overvoltage Threshold	Voltage above VID, after soft-start (Note 6)	180	200	230	mV
	Before enable	1.40	1.45	1.50	V
	VCC < POR threshold	1.7	1.8	1.87	V
Overvoltage Reset Voltage	VCC ≥ POR threshold, VSEN falling	-	0.6	-	V
	VCC < POR threshold	-	1.5	-	V
OVP Drive Voltage	I_{OVP} = -10mA, VCC = 5V	3.0	3.6	5.0	V

NOTES:

3. When using the internal shunt regulator, VCC is clamped to 6.2V (max). Current must be limited to 25mA or less.
4. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
5. Guaranteed by design.
6. During soft-start, VDAC rises from 0 to VID. The overvoltage trip level is the higher of 1.5V and VDAC + 0.2V.

Downloaded from Elcodis.com electronic components distributor

Functional Pin Description

VCC

Supplies all the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply or through a series 300Ω resistor to a +12V supply.

GND

Bias and reference ground for the IC.

EN

This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN is driven above 1.29V, the ISL6564A is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN below 1.16V will clear all fault states and prime the ISL6564A to soft-start when re-enabled.

ENLL

This pin is a logic-level enable input for the controller. When asserted to a logic high, the ISL6564A is active depending on status of EN, the internal POR, VID inputs and pending fault states. Deasserting ENLL will clear all fault states and prime the ISL6564A to soft-start when re-enabled.

When floating, ENLL pin will be pulled to high internally with a typical voltage as 1.15V.

FS

A resistor, RT, placed from FS to ground will set the switching frequency. There is an inverse relationship between the value of the resistor and the switching frequency. See Figure 20 and Equation 30.

VID5, VID4, VID3, VID2, VID1, and VID0

These are the inputs to the internal DAC that provides the reference voltage for output regulation. Connect these pins either to open-drain outputs with or without external pull-up resistors or to active-pull-up outputs. VID5-VID0 have 45µA internal pull-up current sources that diminish to zero as the voltage rises above the logic-high level. These inputs can be pulled up as high as VCC plus 0.3V.

VDIFF, VSEN, and RGND

VSEN and RGND form the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and RGND to the sense pins of the remote load.

FB and COMP

Inverting input and output of the error amplifier, respectively. FB is connected to VDIFF through a resistor. A negative current, proportional to output current is present on the FB pin. A properly sized resistor between VDIFF and FB sets the load line (droop). The droop scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$. COMP is tied back to FB through an external R-C network with no DC connection to compensate the regulator.

DAC and REF

The DAC output pin is the output of the precision internal DAC reference. The REF input pin is the positive input of the Error Amp. In typical applications, a 1kΩ, 1% resistor is used between DAC and REF to generate a precise offset voltage. This voltage is proportional to the offset current determined by the offset resistor from OFS to ground or VCC. A capacitor is used between REF and ground to smooth the voltage transition during Dynamic VID™ operations.

PWM1, PWM2, PWM3, PWM4

Pulse-width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC. The number of active channels is determined by the state of PWM3 and PWM4. Leave PWM4 unconnected and tie PWM3 to VCC to configure for 2-phase operation. Tie PWM4 to VCC to configure for 3-phase operation. Tie both PWM4 and PWM3 to high for 1-phase operation.

ISEN1+, ISEN1-; ISEN2+, ISEN2-; ISEN3+, ISEN3-; ISEN4+, ISEN4-

The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers. The sensed current is used as a reference for channel balancing, protection, and regulation. Inactive channels should have their respective sense inputs left open (for example, for 3-phase operation open ISEN4+).

For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. The sensed current is proportional to the output current, and scaled by the DCR of the inductor, divided by R_{ISEN}.

When configured for $r_{DS(ON)}$ current sensing, the ISEN1-, ISEN2-, ISEN3-, and ISEN4- pins are grounded at the lower MOSFET sources. The ISEN1+, ISEN2+, ISEN3+, and ISEN4+ pins are then held at a virtual ground, such that a resistor connected between them, and the drain terminal of the associated lower MOSFET, will carry a current proportional to the current flowing through that channel. The current is determined by the negative voltage developed across the lower MOSFET's $r_{DS(ON)}$, which is the channel current scaled by $r_{DS(ON)}$.

Downloaded from Elcodis.com electronic components distributor

PGOOD

PGOOD is used as an indication of the end of soft-start per the microprocessor specification. It is an open-drain logic output that is low impedance until the soft-start is completed. It will be pulled low again once the undervoltage point is reached.

OFS

The OFS pin provides a means to program a DC offset current for generating a DC offset voltage at the REF input. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated.

OVP

Overvoltage protection pin. This pin pulls to VCC and is latched when an overvoltage condition is detected. Connect this pin to the gate of an SCR or MOSFET tied from V_{IN} or V_{OUT} to ground to prevent damage to the load. This pin may be pulled above VCC as high as 15V to ground with an external resistor. However, it is only capable of pulling low when VCC is above 2V.

DRVEN

Driver enable pin. This pin can be used to enable the drivers which have enable pins such as ISL6605 or ISL6608. If ISL6564A is used with Intersil ISL6612 drivers, it's not necessary to use this pin.

IDROOP and IOUT

IDROOP and IOUT are the output pins of sensed average channel current which is proportional to load current. They are designed for flexible application purposes.

In the application which does not require loadline, leave IDROOP pin open. In the application which requires load line, connect IDROOP pin to FB so that the sensed average current will flow through the resistor between FB and VDIFF to create a voltage drop which is proportional to load current.

IOUT is typically used for load current indication.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multiphase. The ISL6564A controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagrams on pages 3, 4, 5, 6, and 7 provide top level views of multiphase power conversion using the ISL6564A controller.

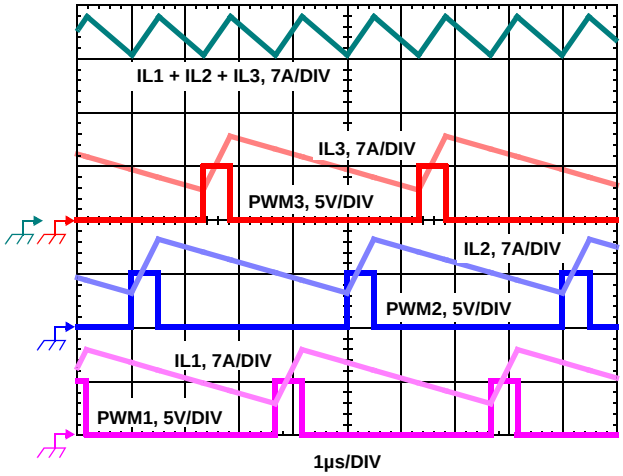


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \qquad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

Downloaded from Elcodis.com electronic components distributor

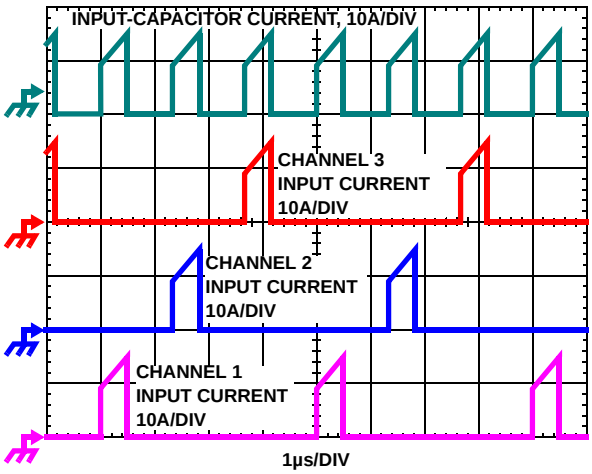


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N\,V_{OUT})\,V_{OUT}}{L f_S V_{IN}} \qquad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 21, 22 and 23 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 24 shows the single phase input-capacitor RMS current for comparison.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6564A is four. One switching cycle is defined as the time between PWM1 pulse termination signals. The pulse termination signal is an internally generated clock signal which triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands the channel 1 PWM output to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel 1 upper MOSFET and turn on the channel 1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/4 of a cycle after PWM1. The PWM3 output follows another 1/4 of a cycle after PWM2. PWM4 terminates another 1/4 of a cycle after PWM3.

If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle later. Connecting PWM4 to VCC selects three channel operation and the pulse-termination times are spaced in 1/3 cycle increments. Connecting both PWM3 and PWM4 to VCC selects single-channel operation.

Once a PWM signal transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 7. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sampling

During the forced off-time following a PWM transition low, the associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. No matter the current sense method, the sense current, I_{SEN}, is simply a scaled version of the inductor current. Coincident with the falling edge of the PWM signal, the sample and hold circuitry samples I_{SEN}, as illustrated in Figure 3. The sample window hold time, t_{HOLD}, is fixed and equal to 1/3 of the switching period, t_{SW}.

$$t_{HOLD} = \frac{t_{SW}}{3} = \frac{1}{3 \cdot f_{SW}} \qquad \text{(EQ. 3)}$$

Therefore, the sample current, I_n, is proportional to the output current and held for one switching cycle. The sample current is used for current balance, load-line regulation, and overcurrent protection.

Downloaded from Elcodis.com electronic components distributor

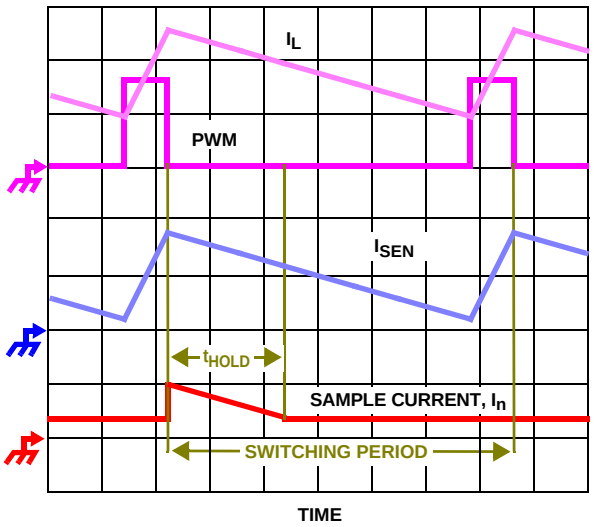


FIGURE 3. SAMPLE AND HOLD TIMING

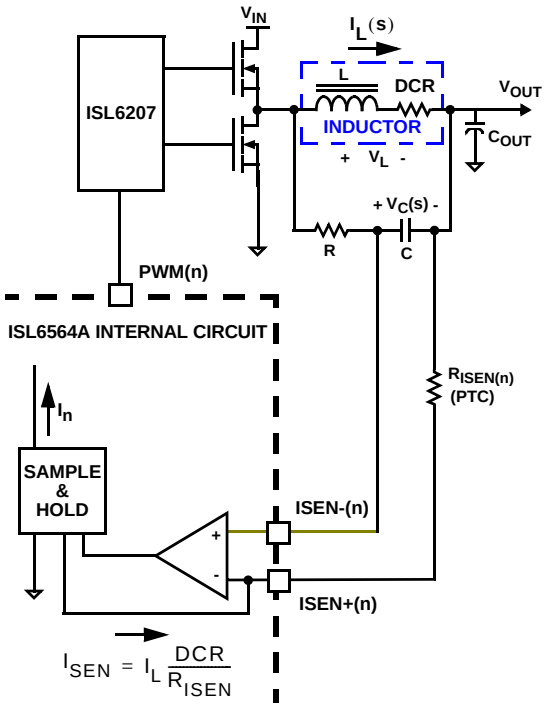


FIGURE 4. DCR SENSING CONFIGURATION

Current Sensing

The ISL6564A supports inductor DCR sensing, MOSFET $r_{DS(ON)}$ sensing, or resistive sensing techniques. The internal circuitry, shown in Figures 4, 5, and 6, represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM3 and PWM4 pins, as described in the *PWM Operation* section.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 4 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \qquad \text{(EQ. 4)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 4.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L, see Equation 5.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \qquad \text{(EQ. 5)}$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant, then V_C is equal to the voltage drop across the DCR.

The capacitor voltage V_C, is then replicated across the sense resistor R_{ISEN}. The current through the sense resistor is proportional to the inductor current. Equation 6 shows the proportion between the channel current and the sensed current I_{SEN}, is driven by the value of the sense resistor chosen and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \qquad \text{(EQ. 6)}$$

DCR varies with temperature, so a Positive Temperature Coefficient (PTC) resistor should be selected for the sense resistor R_{ISEN}.

RESISTIVE SENSING

If DCR sensing is not utilized, independent current-sense resistors in series with each output inductor can serve as the sense element (see Figure 5). This technique is more accurate, but reduces overall converter efficiency due to the addition of a lossy element directly in the output path.

Downloaded from Elcodis.com electronic components distributor

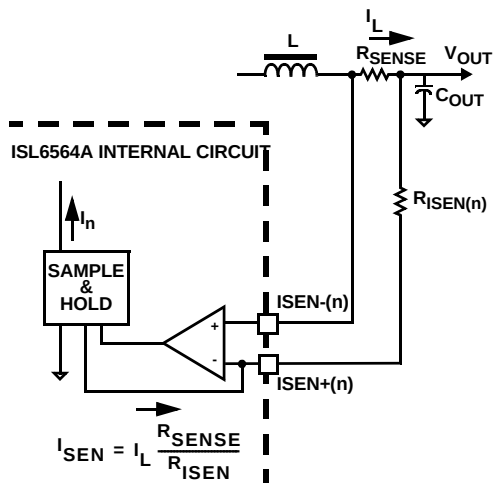


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

MOSFET $r_{DS(ON)}$ SENSING

The controller can also sense the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$ (see Figure 6). The amplifier is ground-reference by connecting the ISEN- input to the source of the lower MOSFET. ISEN+ connects to the PHASE node through a resistor R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN+ pin is proportional to the channel current I_L. The ISEN current is then sampled and held after sufficient settling time. The sampled current I_n, is used for channel-current balance, load-line regulation, and overcurrent protection. From Figure 6, Equation 7 for I_{SEN} is derived.

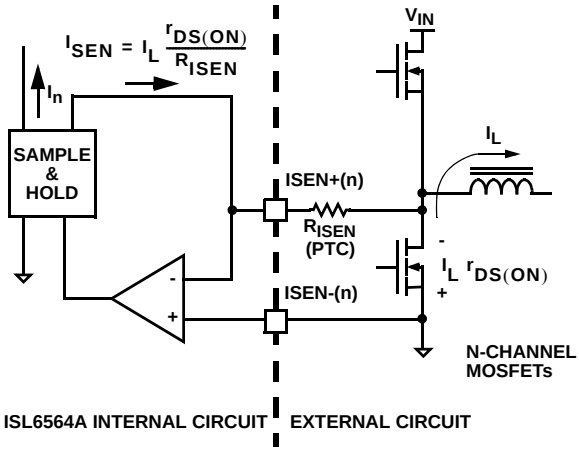


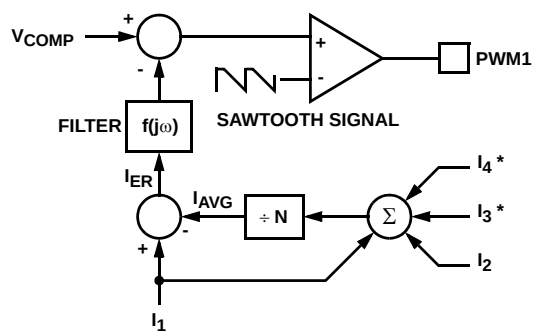
FIGURE 6. MOSFET $r_{DS(ON)}$ CURRENT-SENSING CIRCUIT

$$I_{SEN} = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \qquad \text{(EQ. 7)}$$

where I_L is the channel current. Since MOSFET $r_{DS(ON)}$ increases with temperature, a PTC resistor should be chosen for R_{ISEN} to compensate for this change.

Channel-Current Balance

The sampled currents I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current I_{AVG}, provides a measure of the total load current demand on the converter during each switching cycle. Channel current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making an appropriate adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 7, with error correction for channel 1 represented. In the figure, the cycle average current combines with the channel 1 sample, I_1, to create an error signal I_{ER}. The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: *Channels 3 and 4 are optional.

FIGURE 7. CHANNEL 1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Channel current balance is essential in realizing the thermal advantage of multiphase operation. The heat generated in down converting is dissipated over multiple devices and a greater area. The designer avoids the complexity of driving multiple parallel MOSFETs, and the expense of using heat sinks and nonstandard magnetic materials.

Voltage Regulation

The integrating compensation network shown in Figure 8 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6564A to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry which control voltage regulation is illustrated in Figure 8.

Downloaded from Elcodis.com electronic components distributor

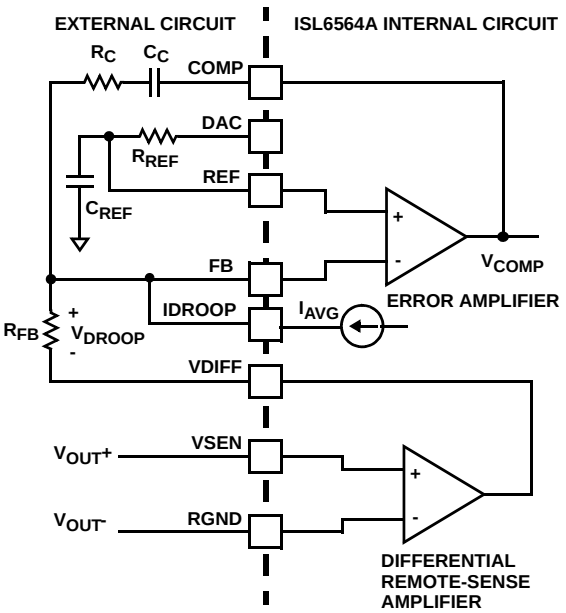


FIGURE 8. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

The ISL6564A incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF}, is connected to the inverting input of the error amplifier through an external resistor.

A digital to analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID4 through VID12.5. The DAC decodes the a 6-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 45µA pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources if case leakage into the driving device is greater than 45µA.

Load-Line Regulation

Some microprocessor manufacturers require a precisely-controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
400 mV	200 mV	100 mV	50 mv	25 mV	12.5 mV	
1	1	1	1	1	1	OFF
1	1	1	1	1	0	1.3000V
1	1	1	1	0	1	1.2875V
1	1	1	1	0	0	1.2750V
1	1	1	0	1	1	1.2625V
1	1	1	0	1	0	1.2500V
1	1	1	0	0	1	1.2375V
1	1	1	0	0	0	1.2250V
1	1	0	1	1	1	1.2125V
1	1	0	1	1	0	1.2000V
1	1	0	1	0	1	1.1875V
1	1	0	1	0	0	1.1750V
1	1	0	0	1	1	1.1625V
1	1	0	0	1	0	1.1500V
1	1	0	0	0	1	1.1375V
1	1	0	0	0	0	1.1250v
1	0	1	1	1	1	1.1125V
1	0	1	1	1	0	1.1000V
1	0	1	1	0	1	1.0875V
1	0	1	1	0	0	1.0750V
1	0	1	0	1	1	1.0625V
1	0	1	0	1	0	1.0500V
1	0	1	0	0	1	1.0375V
1	0	1	0	0	0	1.0250V
1	0	0	1	1	1	1.0125V
1	0	0	1	1	0	1.0000V
1	0	0	1	0	1	0.9875V
1	0	0	1	0	0	0.9750V
1	0	0	0	1	1	0.9625V
1	0	0	0	1	0	0.9500V
1	0	0	0	0	1	0.9375V
1	0	0	0	0	0	0.9250V
0	1	1	1	1	1	0.9125V
0	1	1	1	1	0	0.9000V
0	1	1	1	0	1	0.8875V
0	1	1	1	0	0	0.8750V

Downloaded from Elcodis.com electronic components distributor

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
400 mV	200 mV	100 mV	50 mv	25 mV	12.5 mV	
0	1	1	0	1	1	0.8625V
0	1	1	0	1	0	0.8500V
0	1	1	0	0	1	0.8375V
0	1	1	0	0	0	0.8250V
0	1	0	1	1	1	0.8125V
0	1	0	1	1	0	0.8000V
0	1	0	1	0	1	0.7875V
0	1	0	1	0	0	0.7750V
0	1	0	0	1	1	0.7625V
0	1	0	0	1	0	0.7500V
0	1	0	0	0	1	0.7375V
0	1	0	0	0	0	0.7250V
0	0	1	1	1	1	0.7125V
0	0	1	1	1	0	0.7000V
0	0	1	1	0	1	0.6875V
0	0	1	1	0	0	0.6750V
0	0	1	0	1	1	0.6625V
0	0	1	0	1	0	0.6500V
0	0	1	0	0	1	0.6375V
0	0	1	0	0	0	0.6250V
0	0	0	1	1	1	0.6125V
0	0	0	1	1	0	0.6000V
0	0	0	1	0	1	0.5875V
0	0	0	1	0	0	0.5750V
0	0	0	0	1	1	0.5625V
0	0	0	0	1	0	0.5500V
0	0	0	0	0	1	0.5375V
0	0	0	0	0	0	0.525V

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 8, a current proportional to the average current in all active channels, I_{AVG}, flows from FB through a load-line regulation resistor, R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as

$$V_{DROOP} = I_{AVG} R_{FB} \quad \text{(EQ. 8)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 8 with the appropriate sample current expression defined by the current sense method employed.

$$V_{OUT} = V_{REF} - V_{OFFSET} - \left(\frac{I_{OUT}}{4} \frac{R_X}{R_{ISEN}} R_{FB}\right) \quad \text{(EQ. 9)}$$

Where V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the sense resistor in the ISEN line, and R_{FB} is the feedback resistor. R_X has a value of DCR, $r_{DS(ON)}$, or R_{SENSE} depending on the sensing method.

Output-Voltage Offset Programming

The ISL6564A allows the designer to accurately adjust the offset voltage. When a resistor, R_{OFS}, is connected between OFS to VCC, the voltage across it is regulated to 2.0V. This causes a proportional current (I_{OFS}) to flow into OFS. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows out of OFS. A resistor between DAC and REF, R_{REF}, is selected so that the product (I_{OFS} x R_{OFS}) is equal to the desired offset voltage. These functions are shown in Figure 9.

As it may be noticed in Figure 9, the OFSOUT pin must be connected to the REF pin for this current injection to function in ISL6564A. The current flow through R_{REF} creates an offset at the REF pin, which is ultimately duplicated at the output of the regulator.

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{2 \times R_{REF}}{V_{OFFSET}} \quad \text{(EQ. 10)}$$

For Negative Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \times R_{REF}}{V_{OFFSET}} \quad \text{(EQ. 11)}$$

Downloaded from Elcodis.com electronic components distributor

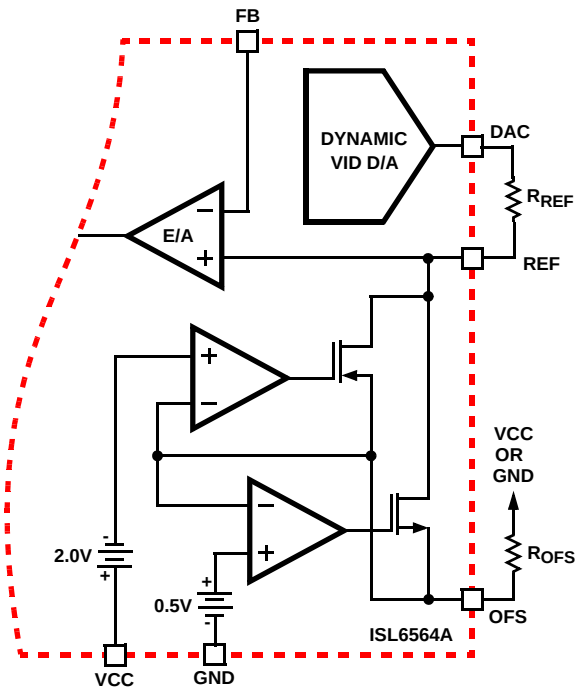


FIGURE 9. OUTPUT VOLTAGE OFFSET PROGRAMMING WITH ISL6564A

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs during regulator operation. The power management solution is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

The ISL6564A checks the VID inputs at the three edges of 16MHz clock. If the VID code is found to have changed, the controller waits half of a complete cycle before executing a 12.5mV change. If during the half-cycle wait period, the difference between DAC level and the new VID code changes sign, no change is made. If the VID code is more than 1 bit higher or lower than the DAC (not recommended), the controller will execute step-up and step down VID change at a speed of 12.5mV every 4µs until VID and DAC are equal.

In order to ensure the smooth transition of output voltage during VID change, a VID step change smoothing network composed of R_{REF} and C_{REF} is required for an ISL6564A based voltage regulator. The selection of R_{REF} is based on the desired offset as detailed above in *Output-Voltage Offset Programming*. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID}, the relationship between the time constant of R_{REF} and C_{REF} network and T_{VID} is given by Equation 12.

$$C_{REF} R_{REF} = k T_{VID} \quad \text{(EQ. 12)}$$

Where, T_{VID} = 4µs, k is the number of the internal VID change cycle. If Typically R_{REF} is selected to be 1kΩ, the allowable delay time for VR to respond to new VID code is 5 VID change cycles (totally 20µs), the value of C_{REF} should be 22nF based on Equation 12.

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, PGOOD asserts logic 1.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the ISL6564A is released from shutdown mode.

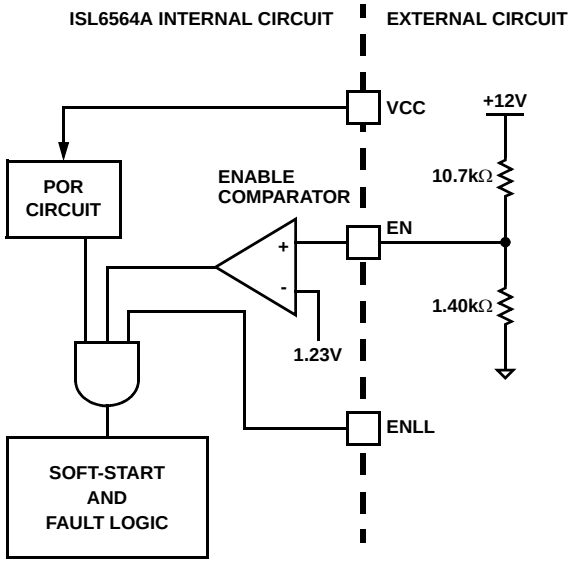


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6564A is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6564A will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

Downloaded from Elcodis.com electronic components distributor

2. The ISL6564A features an enable input (EN) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6564A in shutdown until the voltage at EN rises above 1.29V. The enable comparator has about 125mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the ISL6564A becomes enabled. The schematic in Figure 10 demonstrates sequencing the ISL6564A with the ISL66Xx family of Intersil MOSFET drivers, which require 12V bias.
3. The voltage on ENLL must be logic high to enable the controller. This pin is typically connected to the VID_PGOOD.
4. The VID code must not be 111111. This code signals the controller that no load is present. The controller will enter shut-down mode after receiving this code and will execute soft-start upon receiving any other code. This code can be used to enable or disable the controller but it is not recommended. After receiving this code, the controller executes a 2-cycle delay before changing the overvoltage trip level to the shut-down level and disabling PWM. Overvoltage shutdown can not be reset using this code.

To enable the controller, VCC must be greater than the POR threshold; the voltage on EN must be greater than 1.29V; For ISL6564A, ENLL must be logic high; and VID cannot be equal to 111111. When each of these conditions is true, the controller immediately begins the soft-start sequence.

Soft-Start

During soft-start, the DAC voltage ramps linearly from zero to the programmed VID level as shown in Figure 11. The PWM signals remain in the high-impedance state until the controller detects that the ramping DAC level has reached the pre-bias output-voltage level. This protects the system against the large, negative inductor currents that would otherwise occur when starting with a pre-existing charge on the output as the controller attempted to regulate to zero volts at the beginning of the soft-start cycle. The soft-start time, t_{SS}, begins with a delay period equal to 64 switching cycles followed by a linear ramp with a fixed rate at a speed of 12.5mV/32µs.

$$t_{SS} = (2560)VID \qquad \text{(EQ. 13)}$$

Equation 13 can be used to calculate the soft-start time. For example, when VID is set to 1.2V, the soft-start time will be 3.072ms.

A 100mV offset exists on the remote-sense amplifier at the beginning of soft-start and ramps to zero during the first 640 cycles of soft-start (704 cycles following enable). This prevents the large inrush current that would otherwise occur should the output voltage start out with a slight negative bias.

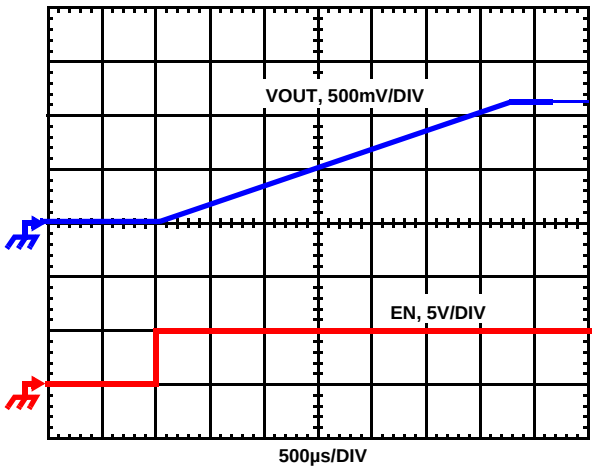


FIGURE 11. SOFT-START WAVEFORMS WITH AN UN-BIASED OUTPUT

Fault Monitoring and Protection

The ISL6564A actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 12 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output indication that the converter is operating after soft-start. PGOOD pulls low during shutdown and releases high after a successful soft-start. PGOOD will only transition low when an undervoltage condition is detected or the controller is disabled by a reset from EN, ENLL, POR, or one of the no-CPU VID codes. After an undervoltage event, PGOOD will return high unless the controller has been disabled. PGOOD does not automatically transition low upon detection of an overvoltage condition.

Downloaded from Elcodis.com electronic components distributor

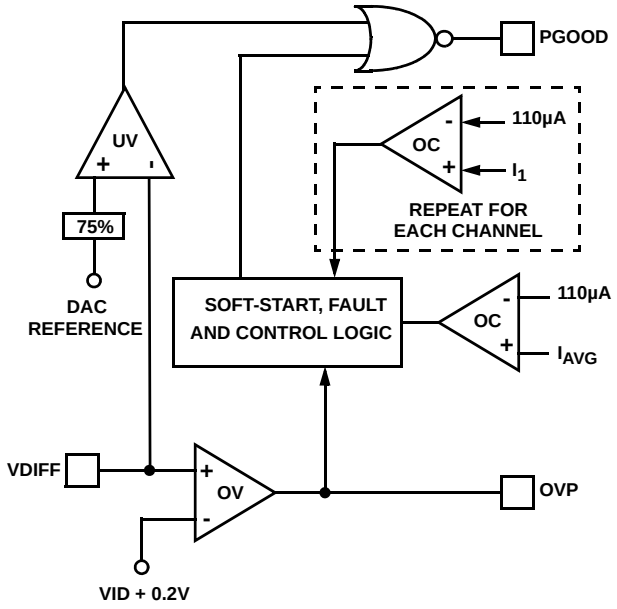


FIGURE 12. POWER GOOD AND PROTECTION CIRCUITRY

Undervoltage Detection

The undervoltage threshold is set at 75% of the VID code. When the output voltage at VSEN is below the undervoltage threshold, PGOOD gets pulled low.

Overvoltage Protection

When VCC is above 1.4V, but otherwise not valid as defined under **Power-on Reset** in *Electrical Specifications*, the overvoltage trip circuit is active using auxiliary circuitry. In this state, an overvoltage trip occurs if the voltage at VSEN exceeds 1.8V.

With valid VCC, the overvoltage circuit is sensitive to the voltage at VDIFF. In this state, the trip level is 1.7V prior to valid enable conditions being met as described in *Enable and Disable*. The only exception to this is when the IC has been disabled by an overvoltage trip. In that case the overvoltage trip point is VID plus 200mV. During soft-start, the overvoltage trip level is the higher of 1.5V or VID plus 200mV. Upon successful soft-start, the overvoltage trip level is 200mV above VID. Two actions are taken by the ISL6564A to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly (less than 20ns) until the voltage at VSEN falls below 0.6V with valid VCC or 1.5V otherwise. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The PWM outputs remain low until VDIFF falls to the programmed DAC level when they enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, the ISL6564A will again command the lower MOSFETs to turn on. The ISL6564A will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Simultaneous to the protective action of the PWM outputs, the OVP pin pulls to VCC delivering up to 100mA to the gate of a crowbar MOSFET or SCR placed either on the input rail or the output rail. Turning on the MOSFET or SCR collapses the power rail and causes a fuse placed further up stream to blow. The fuse must be sized such that the MOSFET or SCR will not overheat before the fuse blows. The OVP pin is tolerant to 12V (see *Absolute Maximum Ratings*), so an external resistor pull-up can be used to augment the driving capability. If using a pull-up resistor in conjunction with the internal overvoltage protection function, care must be taken to avoid nuisance trips that could occur when VCC is below 2V. In that case, the controller is incapable of holding OVP low.

Once an overvoltage condition is detected, normal PWM operation ceases until the ISL6564A is reset. Cycling the voltage on EN or ENLL or VCC below the POR-falling threshold will reset the controller. Cycling the VID codes will not reset the controller.

Overcurrent Protection

ISL6564A has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition on a delayed basis, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, the ISL6564A takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an overcurrent condition. See the *Channel-Current Balance* section for more detail on how the average current is measured. The average current is continually compared with a constant 110µA reference current as shown in Figure 12. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown.

In individual overcurrent protection mode, the ISL6564A continuously compares the current of each channel with the same 110µA reference current. If any channel current exceeds the reference current continuously for eight consecutive cycles, the comparator triggers the converter to shutdown.

Downloaded from Elcodis.com electronic components distributor

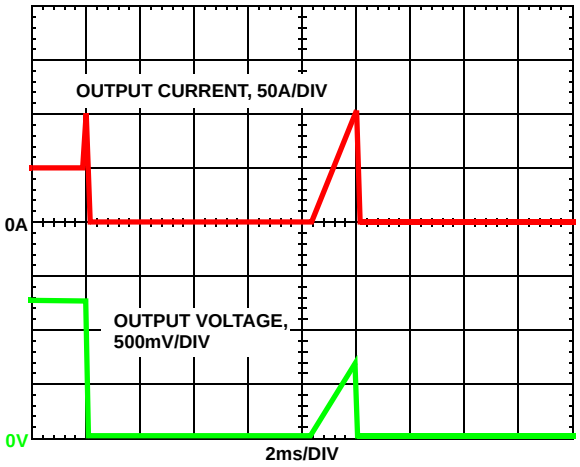


FIGURE 13. OVERCURRENT BEHAVIOR IN HICCUP MODE, F_{SW} = 500kHz

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state within 20ns commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (as shown in Figure 13) until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there, there is no thermal hazard during this kind of operation.

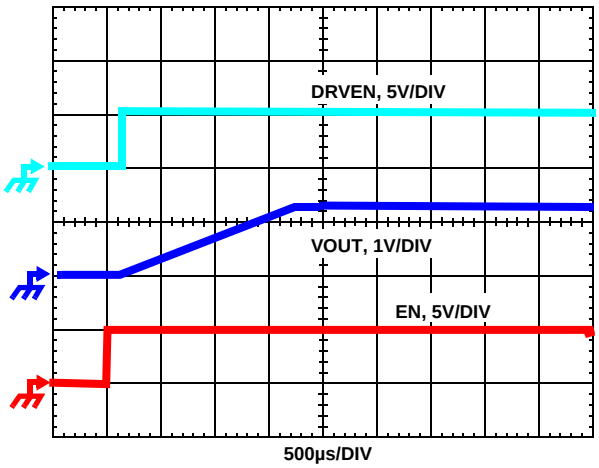


FIGURE 14. DRVEN WAVEFORM AT START-UP

Driver Enable Output

The ISL6564A has a driver enable output pin DRVEN. The DRVEN is designed for the application where ISL6564A needs to work with drivers that can not recognize three-state PWM input.

In normal operation, DRVEN remains low until ISL6564A begins soft-start ramp and then changes to high (Figure 14). When an overcurrent event occurs, DRVEN is pulled to low instantly (less than 20ns) to disable the driver so that both upper and lower FETs be turned off (Figure 15). During an overvoltage condition, DRVEN remains high to allow the driver turn on the lower FETs based on the PWM input to discharge the energy stored in the output inductor. Once the Output voltage is reduced to 0.6V, DRVEN is pulled to low as shown in Figure 16.

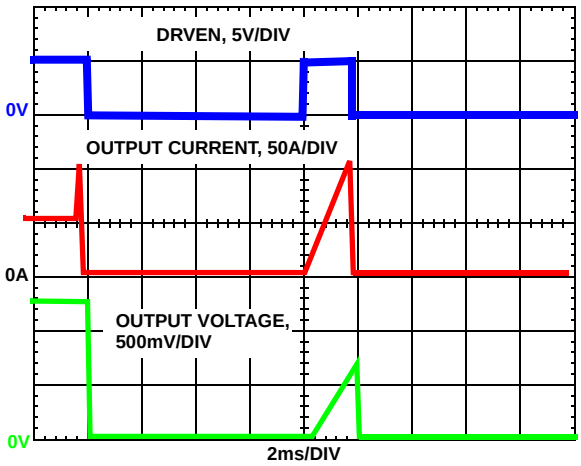


FIGURE 15. DRVEN DURING OVERCURRENT OPERATION

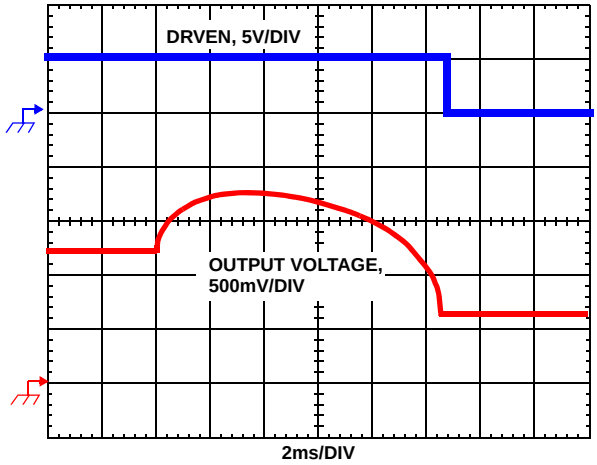


FIGURE 16. DRVEN DURING OVERCURRENT OPERATION

There's no need to use DRVEN when ISL6564A is used to work with Intersil's drivers such as ISL6612 and ISL6605.

Current Sense Output

The ISL6564A has 2 current sense output pins IDROOP and IOUT. They are identical. In typical application, IDROOP pin is connected to FB pin for the application where load line is required. IOUT pin was designed for load current measurement. As shown in typical application schematics

Downloaded from Elcodis.com electronic components distributor

on pages 4 to 7, load current information can be obtained by measuring the voltage between IOUT to ground when a NTC network from IOUT pin to the ground is placed. The output current at IOUT pin is proportional to load current as shown in Figure 17.

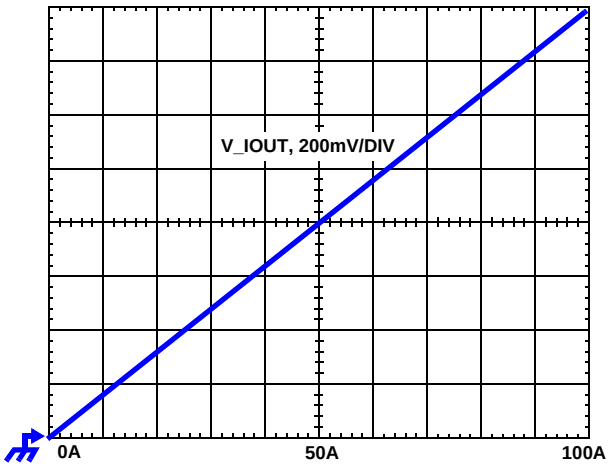


FIGURE 17. VOLTAGE AT IOUT PIN WITH A NTC NETWORK PLACED BETWEEN IOUT TO GROUND WHEN LOAD CURRENT CHANGES

When selecting the equivalent resistor network components values, it is important to ensure the voltage at IOUT pin not exceed 2V.

When ISL6564A is operated at single phase mode (both PWM3 and PWM4 connected to VCC and PWM2 unconnected). The output current at IOUT and IDROOP is half of the sensed phase current.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power-supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15 and 20A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 14, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2(1-d) + \frac{I_{L,PP}^2(1-d)}{12}\right] \quad \text{(EQ. 14)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_S; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_S\left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)t_{d2}\right] \quad \text{(EQ. 15)}$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET

Downloaded from Elcodis.com electronic components distributor

ramps up to assume the full inductor current. In Equation 16, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right) f_S \quad \text{(EQ. 16)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 17, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right) f_S \quad \text{(EQ. 17)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$ and is approximately

$$P_{UP,3} = V_{IN} Q_{rr} f_S \quad \text{(EQ. 18)}$$

Finally, the resistive part of the upper MOSFET's is given in Equation 19 as $P_{UP,4}$.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 16, 17, 18 and 19. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 19)}$$

Current Sensing Resistor

The resistors connected between these pins and the respective phase nodes determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs, DCR of inductor or additional resistor; the full-load operating current, I_{FL}; and the number of phases, N using Equation 20.

$$R_{ISEN} = \frac{R_X}{70 \times 10^{-6}} \frac{I_{FL}}{N} \quad \text{(EQ. 20)}$$

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistor. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of RISEN for the affected phases (see the section entitled *Channel-Current Balance*). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 21)}$$

In Equation 21, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 21 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 8. Its value depends on the desired full-load droop voltage (V_{DROOP} in Figure 8). If Equation 20 is used to select each ISEN resistor, the load-line regulation resistor is as shown in Equation 22.

$$R_{FB} = \frac{V_{DROOP}}{70 \times 10^{-6}} \quad \text{(EQ. 22)}$$

If one or more of the ISEN resistors is adjusted for thermal balance, as in Equation 21, the load-line regulation resistor should be selected according to Equation 23 where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the nth ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL}\, r_{DS(ON)}} \sum_n R_{ISEN(n)} \quad \text{(EQ. 23)}$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in *Load-Line Regulation*, there are two distinct methods for achieving these goals.

COMPENSATING LOAD-LINE REGULATED CONVERTER

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator by compensating the L-C poles and the ESR zero of the voltage-mode approximation yields a solution that is always stable with very close to ideal transient performance.

Downloaded from Elcodis.com electronic components distributor

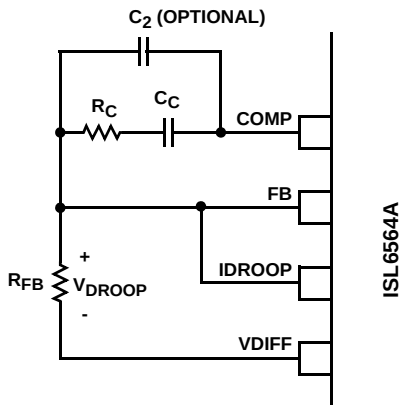


FIGURE 18. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6564A CIRCUIT

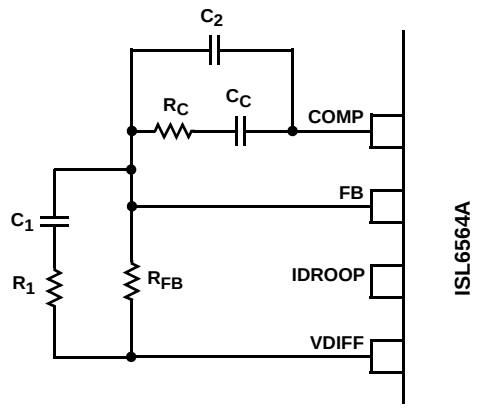


FIGURE 19. COMPENSATION CIRCUIT FOR ISL6564A BASED CONVERTER WITHOUT LOAD-LINE REGULATION

The feedback resistor, R_{FB}, has already been chosen as outlined in *Load-Line Regulation Resistor*. Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the three cases which follow, there is a separate set of equations for the compensation components.

Case 1:

$$\frac{1}{2\pi\sqrt{LC}} > f_0$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}\sqrt{LC}}{0.75V_{IN}}$$

$$C_C = \frac{0.75V_{IN}}{2\pi V_{PP}R_{FB}f_0}$$

Case 2:

$$\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.75\,V_{IN}} \qquad \text{(EQ. 24)}$$

$$C_C = \frac{0.75V_{IN}}{(2\pi)^2 f_0^2 V_{PP}R_{FB}\sqrt{LC}}$$

Case 3:

$$f_0 > \frac{1}{2\pi C(ESR)}$$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}L}{0.75\,V_{IN}(ESR)}$$

$$C_C = \frac{0.75V_{IN}(ESR)\sqrt{C}}{2\pi V_{PP}R_{FB}f_0\sqrt{L}}$$

In Equation 24, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 7 and *Electrical Specifications*.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 18). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading-edge jitter problem is noted.

Once selected, the compensation values in Equation 24 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 24 unless some performance issue is noted.

COMPENSATION WITHOUT LOAD-LINE REGULATION

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 19, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 24, R_{FB} is selected arbitrarily. The remaining

Downloaded from Elcodis.com electronic components distributor

compensation components are then selected according to Equation 25.

$$R_1 = R_{FB}\frac{C(ESR)}{\sqrt{LC} - C(ESR)}$$

$$C_1 = \frac{\sqrt{LC} - C(ESR)}{R_{FB}}$$

$$C_2 = \frac{0.75V_{IN}}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}}$$

$$R_C = \frac{V_{PP}\left(2\pi\right)^2 f_0 f_{HF} LCR_{FB}}{0.75\,V_{IN}\left[\left(2\pi f_{HF}\sqrt{LC}-1\right)\right]}$$

$$C_C = \frac{0.75V_{IN}\left(2\pi f_{HF}\sqrt{LC}-1\right)}{(2\pi)^2 f_0 f_{HF}\sqrt{LC}R_{FB}V_{PP}} \quad \text{(EQ. 25)}$$

In Equations 25, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 7 and *Electrical Specifications*.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 26)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}$(ESR). Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR)\frac{\left(V_{IN} - N V_{OUT}\right)V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \quad \text{(EQ. 27)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 28 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 29 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2NCV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \quad \text{(EQ. 28)}$$

$$L \leq \frac{(1.25)NC}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right]\left(V_{IN} - V_O\right) \quad \text{(EQ. 29)}$$

Downloaded from Elcodis.com electronic components distributor

Input Supply Voltage Selection

The VCC input of the ISL6564A can be connected either directly to a +5V supply or through a current limiting resistor to a +12V supply. An integrated 5.8V shunt regulator maintains the voltage on the VCC pin when a +12V supply is used. A 300Ω resistor is suggested for limiting the current into the VCC pin to a worst-case maximum of approximately 25mA.

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T (see the figures labeled *Typical Application* on pages 4, 5, 6 and 7). Figure 20 and Equation 30 are provided to assist in selecting the correct value for R_T.

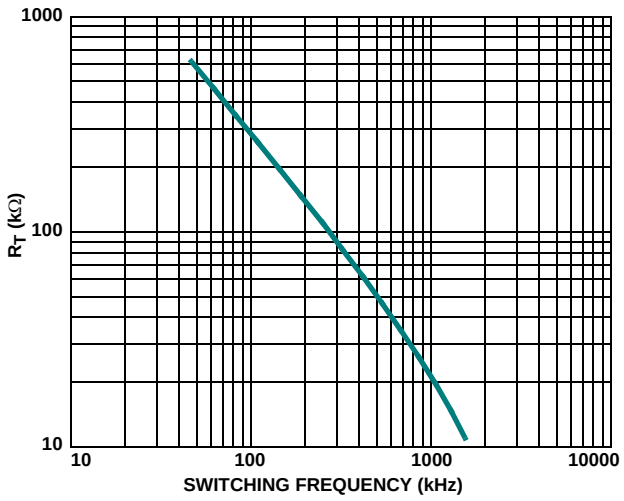


FIGURE 20. R_T vs SWITCHING FREQUENCY

$$R_T = 10^{[10.886 - 1.0792\log(f_S)]} \quad \text{(EQ. 30)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

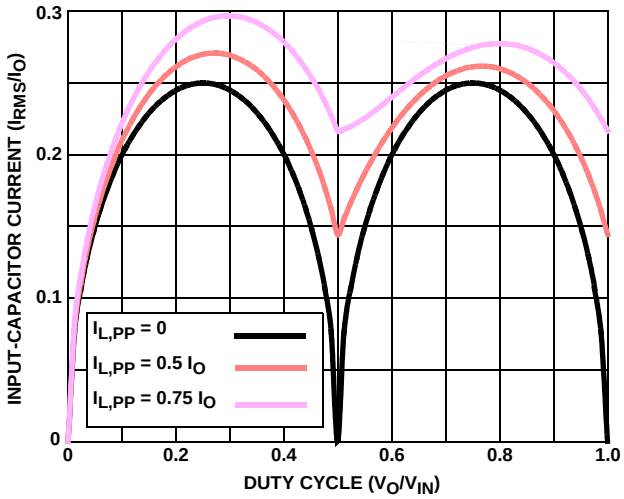


FIGURE 21. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

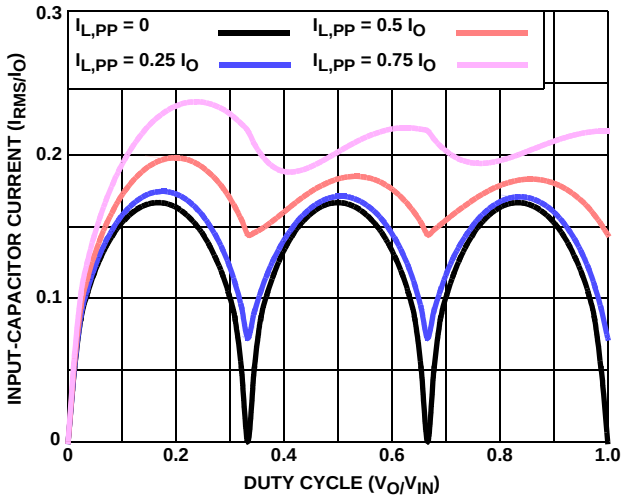


FIGURE 22. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

For a two phase design, use Figure 21 to determine the input-capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

Figures 22 and 23 provide the same input RMS current information for three and four phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as described above.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on

Downloaded from Elcodis.com electronic components distributor

and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize suppression.

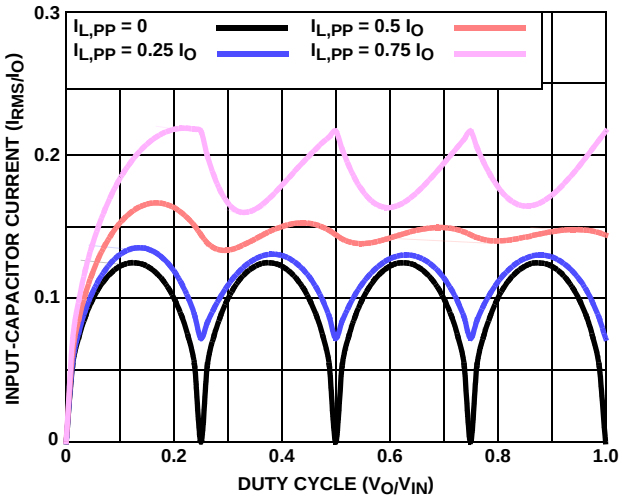


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

MULTIPHASE RMS IMPROVEMENT

Figure 24 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a two-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L,PP}$ to I_O of 0.5. The single phase converter would require 17.3 Arms current capacity while the two-phase converter would only require 10.9 Arms. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

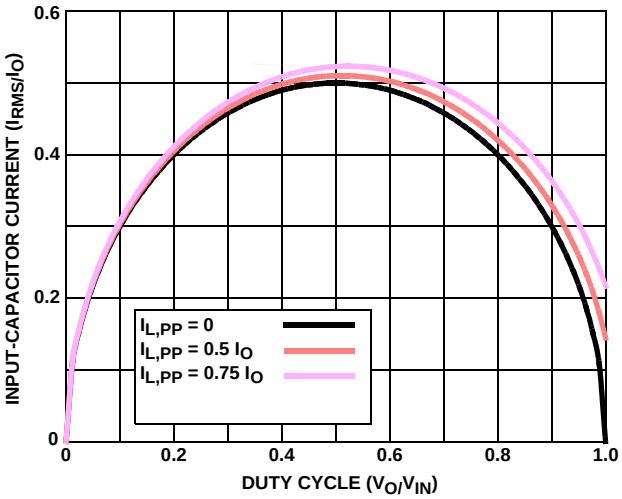


FIGURE 24. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

Layout Considerations

The following layout strategies are intended to minimize the impact of board parasitic impedances on converter performance and to optimize the heat-dissipating capabilities of the printed-circuit board. These sections highlight some important practices which should not be overlooked during the layout process.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

The ISL6564A can be placed off to one side or centered relative to the individual phase switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the ISEN resistors, R_T resistor, feedback resistor, and compensation components.

Bypass capacitors for the ISL6564A and ISL66XX driver bias supplies must be placed next to their respective pins. Trace parasitic impedances will reduce their effectiveness.

Plane Allocation and Routing

Dedicate one solid layer, usually a middle layer, for a ground plane. Make all critical component ground connections with vias to this plane. Dedicate one additional layer for power planes; breaking the plane up into smaller islands of common voltage. Use the remaining layers for signal wiring.

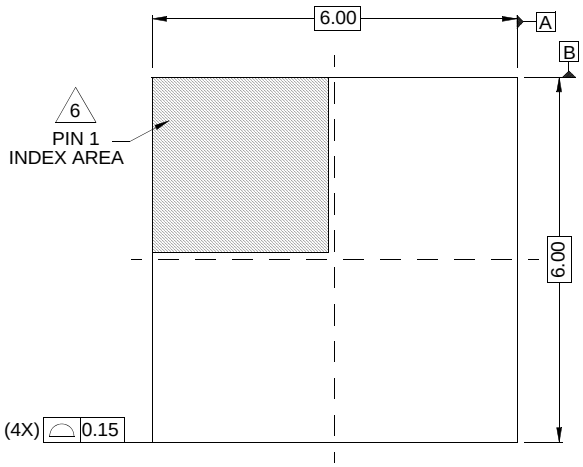
Route phase planes of copper filled polygons on the top and bottom once the switching component placement is set. Size the trace width between the driver gate pins and the MOSFET gates to carry 4A of current. When routing components in the switching path, use short wide traces to reduce the associated parasitic impedances.

Downloaded from Elcodis.com electronic components distributor

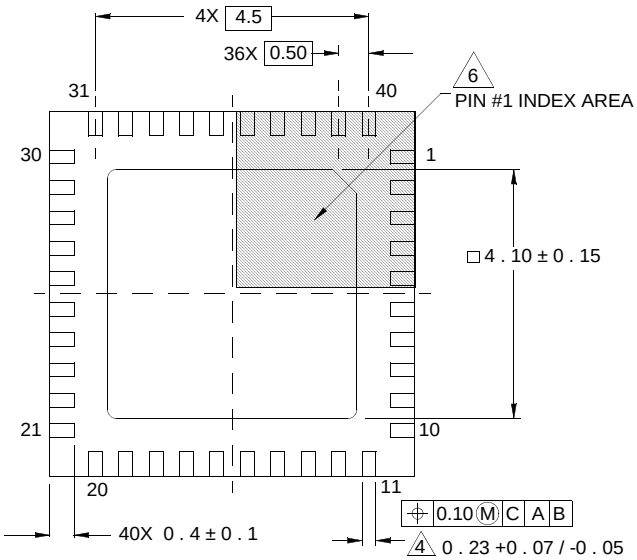
Package Outline Drawing

L40.6x6

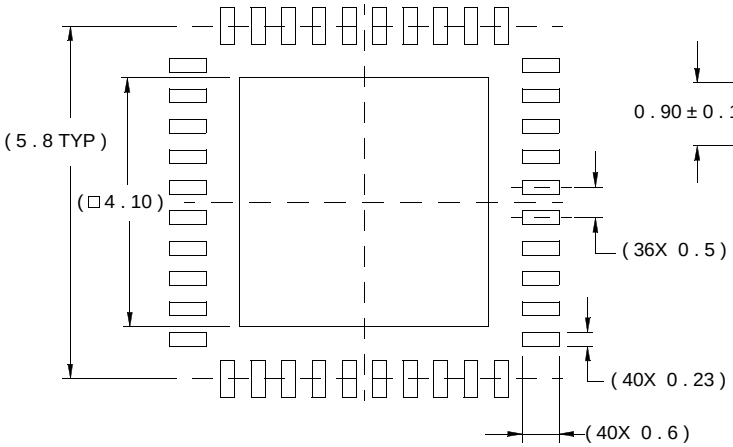
40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 10/06



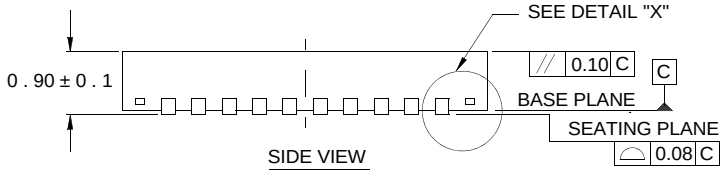
TOP VIEW



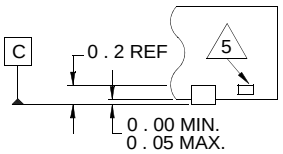
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Downloaded from Elcodis.com electronic components distributor

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Downloaded from Elcodis.com electronic components distributor