Data Sheet | October 29, 2008 | FN6605.0

Single-Phase Pulse-Width Modulation (PWM) Controller with Integrated High-Side Gate Drivers

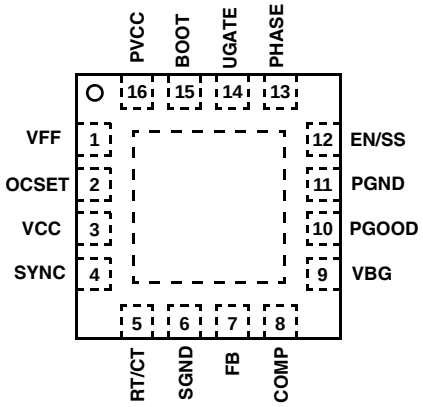
The ISL8107 is a single phase, non-synchronous buck controller with an integrated high-side MOSFET driver. The controller operates from 9V to 75V input voltage range. The internal 1.192V reference voltage has a tolerance of ±1% over the industrial temperature range.

The ISL8107 employs voltage-mode control with feedforward compensation to provide optimal transient response and a constant loop gain over a wide input voltage range. The switching frequency can be programmed from 100kHz to 600kHz by external resistor and capacitor. The switching frequency can be synchronized to an external clock signal through the SYNC pin.

The ISL8107 features programmable soft-start, hiccup mode for short circuit protection, and over-temperature protection. The overcurrent protection is implemented using MOSFET's $r_{DS(ON)}$ sensing. This approach simplifies the implementation without deteriorating the converter efficiency.

Pinout

ISL8107
(16 LD 5X5 QFN)
TOP VIEW



Features

- Operates from +9V to +75V Bias Supply Voltage
- +1.192V Internal Voltage Reference
  - ±1% tolerance Over the Industrial Temperature Range
- Programmable Switching Frequency 100kHz to 600kHz
- Simple Single-Loop Voltage Mode Control
- Voltage Feedforward Compensation
- Switching Frequency Synchronization
- Lossless, Programmable Overcurrent Protection
  - Uses MOSFET's $r_{DS(ON)}$
  - Hiccup Mode
- Integrated N-Channel MOSFET Gate Drivers
- Programmable Soft-Start
- Over-Temperature Protection
- QFN (5x5) Package
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-Free (RoHS Compliant)

Applications

- Test and Measurement Instruments
- Routers and Switchers
- Point of Load Modules
- Distributed DC/DC Power Architecture
- Industrial Applications
- Telecom/Datacom Applications

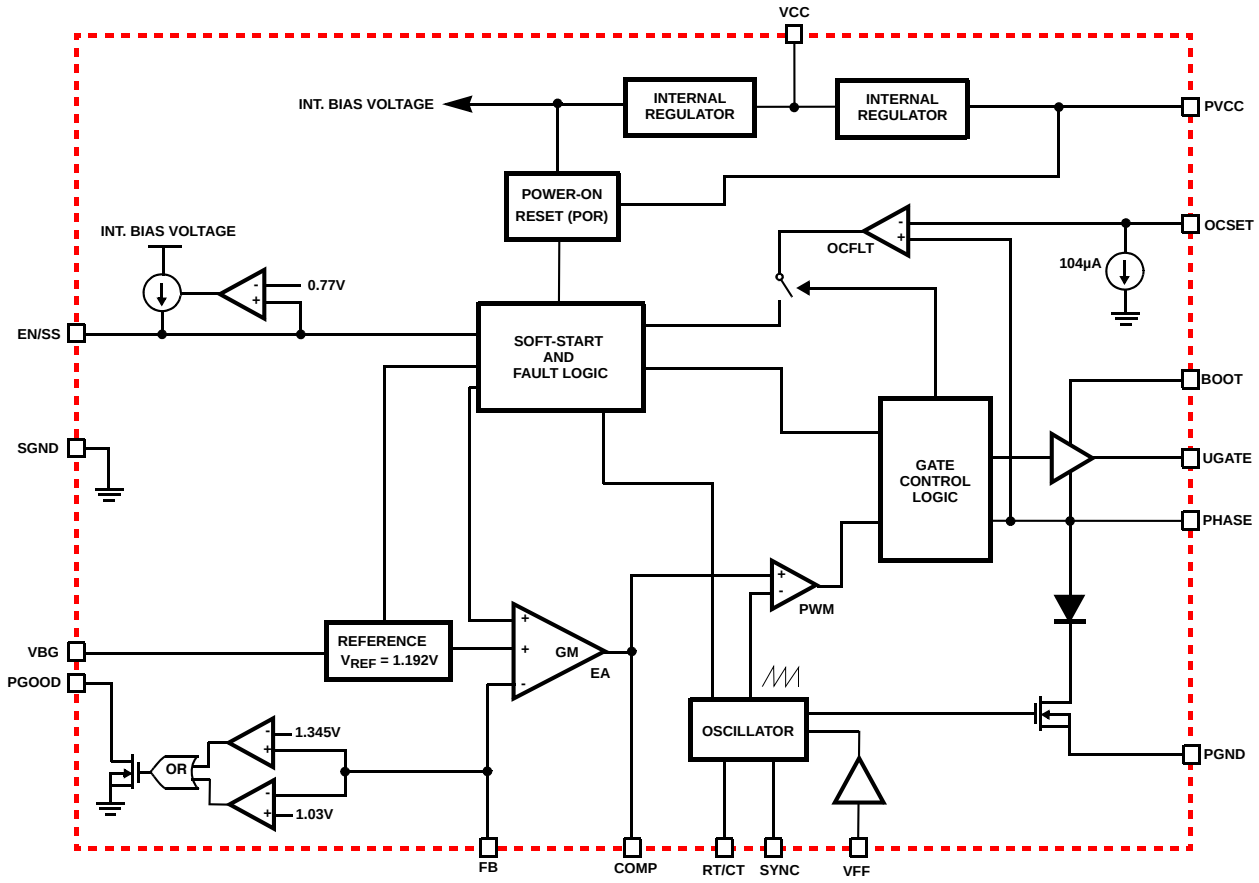
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8107IRZ	ISL8107 IRZ	-40 to +85	16 Ld 5x5 QFN	L16.5x5B
ISL8107IRZ-T*	ISL8107 IRZ	-40 to +85	16 Ld 5x5 QFN Tape and Reel	L16.5x5B

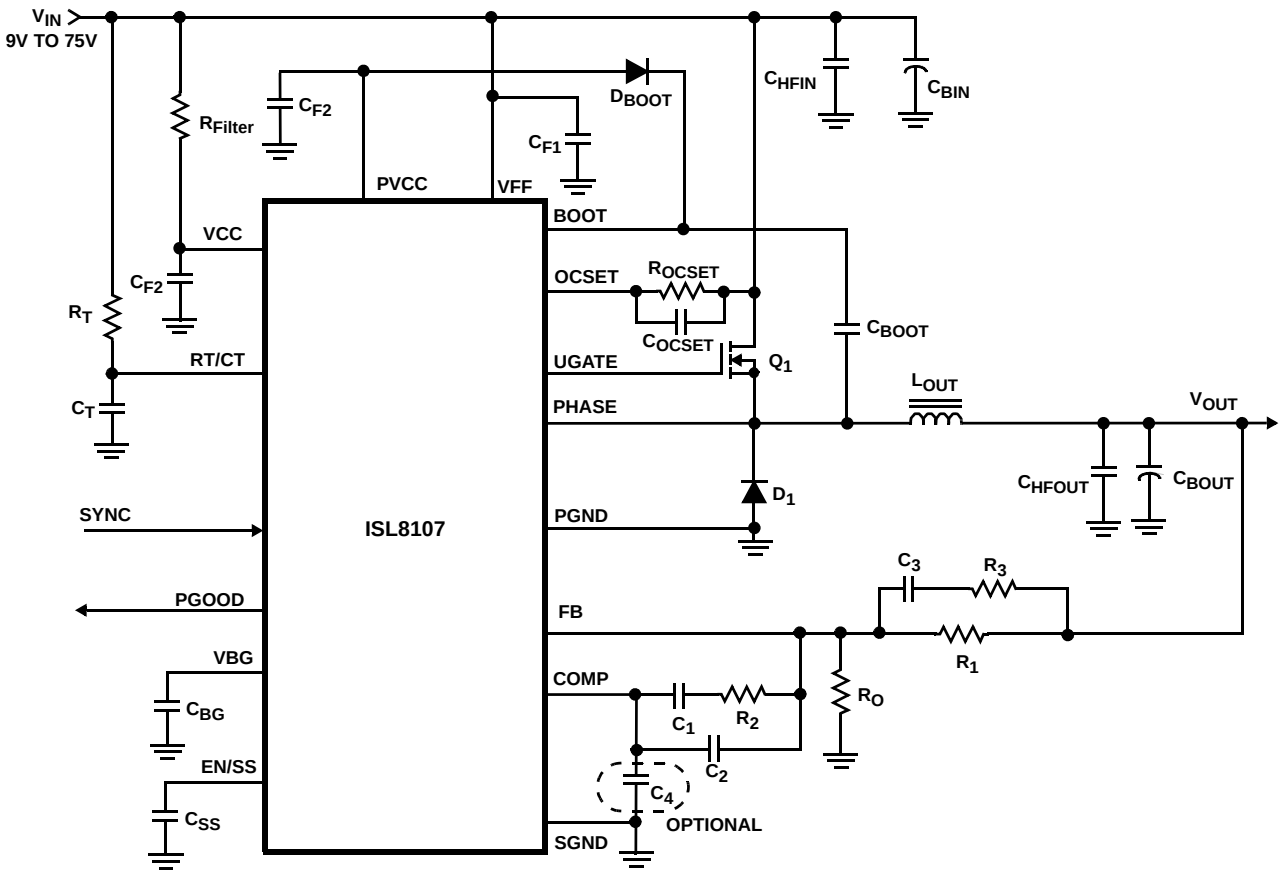
*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

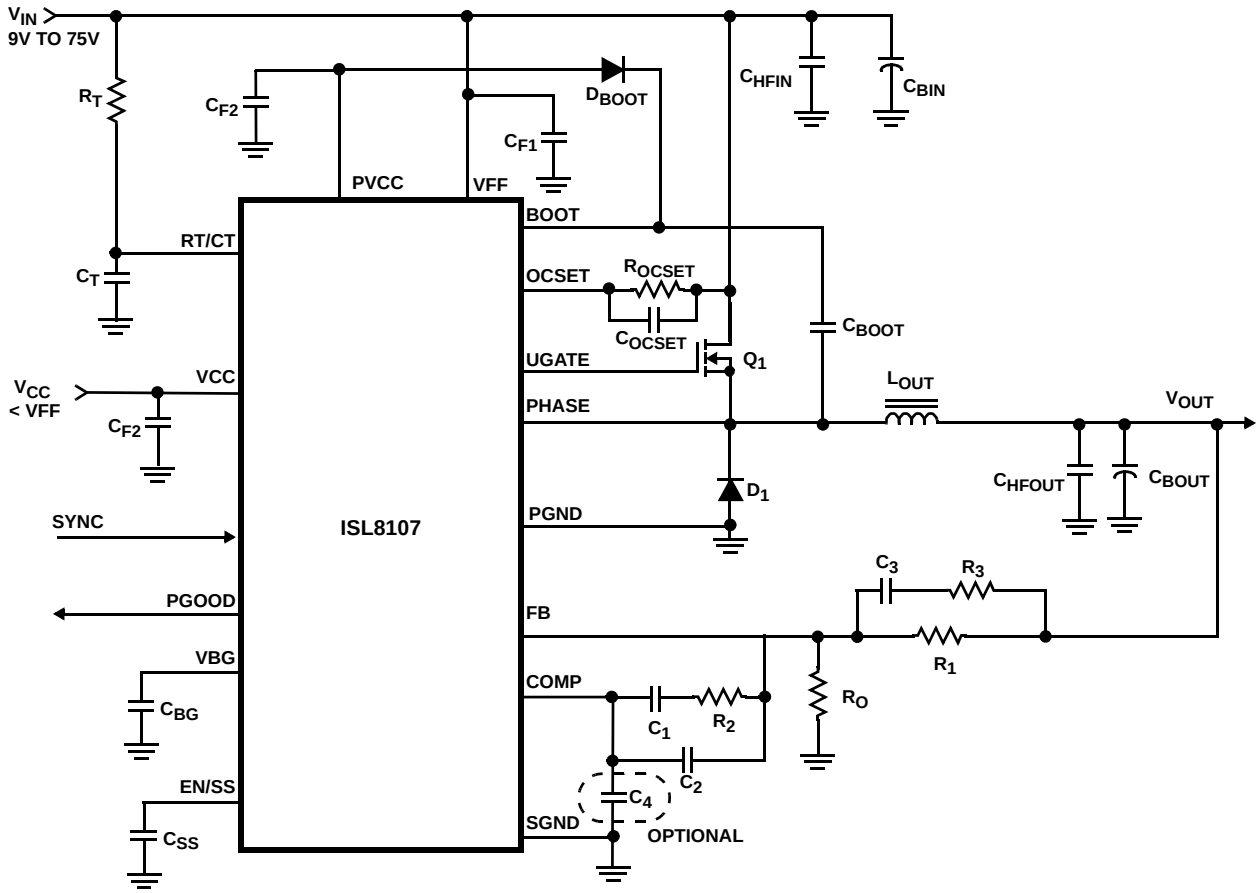
Block Diagram



Typical Application



Typical Application



Absolute Maximum Ratings

Input Voltage (VCC,VFF) to GND 100V
BOOT to GND 105V
ENSS pin 6V
FB, COMP, SYNC pins 8V

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range . . . . . 9.0V to 75V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	33	3

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Limits should be considered typical and are not production tested.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Bias Voltage Range			9.0	-	75	V
Bias Supply Current	I_{VCC}	UGATE open	-	2	3	mA
VCC Shutdown Current	I_{VCC_SD}	VCC = 48V, ENSS = 0V	-	40	60	µA
INTERNAL LINEAR REGULATOR (PVCC)						
Output Voltage	PVCC	VCC = 15V to 75V, Load = 3mA to 20mA	-	10	-	V
Maximum Output Current			20	-	-	mA
Short Current Protection			-	60	-	mA
POWER-ON RESET						
POR Threshold		VCC = VFF	6.8	7.8	8.5	V
POR Threshold Hysteresis		VCC = VFF	-	220	-	mV
OSCILLATOR						
Total Variation on Set Frequency		R_T = 20kΩ, C_T = 1200pF		330		kHz
Frequency Range		Set by R_T and C_T. R_T range = 20k to 100k, C_T range = 470pF to 1200pF	100	-	600	kHz
SYNC Frequency Range		above R_TC_T natural frequency	100	-	600	kHz
Ramp Amplitude	ΔV_{OSC}	VCC varied from 9.0V to 75V	-	0.11*VFF	-	V_{P-P}
Min OFF Time			-	190	300	ns
REFERENCE VOLTAGE						
Feedback Voltage	V_{FB}		-	1.192	-	V
Accuracy			-1.0	-	+1.0	%
ENABLE/SS						
Soft-Start Current	I_{SS}	VENSS = 0V	-	2	-	µA
		VENSS = 1.3V	22	33	43	µA
Enable Threshold	V_{EN}	Voltage level where soft-start current changes from low to high	0.5	0.77	1.0	V

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Disable Voltage	V_{DISEN}		-	-	0.5	V
ERROR AMPLIFIER						
Transconductance			4.2	5.7	7.2	mS
Gain-Bandwidth Product (Note 3)	GBW		-	15	-	MHz
Slew Rate (Note 3)	SR		-	6	-	V/µs
COMP Pin Drive(Note 3)	I_{COMP}		-	±300	-	µA
POWER GOOD (OPEN DRAIN)						
Power-Good Lower Threshold	V_{PG-}	Percentage of Nominal VFB; ~ 3µs noise filter	84	-	88	%
Power-Good Higher Threshold	V_{PG+}	Percentage of Nominal VFB; ~ 3µs noise filter	112	-	116	%
PGOOD Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOOD Voltage Low		I_{PGOOD} = 4mA	-	-	0.5	V
GATE DRIVER						
Gate Drive Source Current (Note 3)	I_{G_SOURCE}	VBOOT - PHASE = 10V	-	1.5	-	A
Gate Drive Source Impedance	R_{G_SOURCE}		-	0.25	-	Ω
Gate Drive Sink Current (Note 3)	I_{G_SINK}	VBOOT - PHASE = 10V	-	1.5	-	A
Gate Drive Sink Impedance	R_{G_SINK}		-	0.24	-	Ω
OVERCURRENT PROTECTION						
Dynamic Current Limit OFF-time	t_{OCOFF}		-	4	-	SS cycle
OCP (OCSET) Current Source	I_{OCSET}		89	104	119	µA
SYNCHRONIZATION						
Input HIGH Level (Asserted)	V_{SYNC_HIGH}		3.0	-	-	V
Input LOW Level (Unasserted)	V_{SYNC_LOW}		-	-	0.8	V
Input Current HIGH	$I_{SYNCHIGH}$		-	-	1	µA
Input Current LOW	$I_{SYNCLOW}$		-	-	1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		Rising Threshold	-	150	-	°C
Thermal Shutdown Hysteresis			-	40	-	°C

Functional Pin Description

VFF (Pin 1)

The voltage at this pin is used for input voltage feed forward compensation and sets the internal oscillator ramp peak to peak amplitude at 0.11*VFF. The oscillator ramp amplitude varies from approximately 1V to 8.5V as VFF changes from 9V to 75V to maintain constant frequency and provide feed forward compensation.

An external RC filter may be required at this pin in noisy input environments.

OCSET (Pin 2)

The current limit is set by placing a resistor, R_{OCSET} and capacitor, C_{OCSET}, between this pin and the drain of the MOSFET. The maximum allowable R_{OCSET} resistor is 50kΩ. A 104µA current source develops a voltage across R_{OCSET} which is then compared with the voltage developed across the MOSFET when on. An initial ~200ns blanking period is used to eliminate the sampling error due to switching noise before the current is measured.

VCC (Pin 3)

VCC is power connection for the ISL8107. The pin should be connected to a 9V to 75V bias supply and must be well decoupled to signal ground (SGND) with a ceramic capacitor.

The voltage at this pin must always be equal to or less than the voltage at VFF pin.

SYNC (Pin 4)

The switching frequency can be synchronized to an external clock through this pin. When the sync function is not used, this pin must be tied to ground. If the sync function is used, the R_T/C_T natural frequency must be set to a frequency lower than the sync input frequency. The termination of the ramp is synchronized with the rising edge of the sync input signal.

RT/CT (Pin 5)

A resistor to VFF and a capacitor to GND determines the frequency of the sawtooth oscillator. The resistor should be in the range of 20k to 100k, the capacitor range should be in the range of 470pF to 1.2nF.

When the controller is disabled, the voltage at RT/CT pin rises up to VFF. Hence, the voltage rating of the CT capacitor must be sufficient to support the maximum VFF.

SGND (Pin 6)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

FB (Pin 7)

This is the feedback pin. The feedback ratio is set by an external resistor divider connected to the output.

COMP (Pin 8)

This pin is connected to the output of the transconductance error amplifier and is used to compensate the feedback loop.

VBG (Pin 9)

Band gap reference output. A 0.01µF capacitor to SGND is required for decoupling this signal. This pin should not be loaded.

PGOOD (Pin 10)

This pin provides a power good status. It is an open drain output that is asserted when the voltage at FB pin is within ±14% of the reference voltage.

PGND (Pin 11)

This pin provides the power ground to the IC. Tie this pin to the ground plane through the lowest impedance connection.

EN/SS (Pin 12)

This pin provides enable/disable function and soft-start timing function for the PWM output. The IC is disabled when this pin is held below 0.5V.

PHASE (Pin 13)

Connect this pin to the source of MOSFET. This pin provides the return path for the gate drive current. During normal switching, this pin is also used for current limiting measurements.

UGATE (Pin 14)

This pin provides the drive for the MOSFET and should be connected to its gate.

BOOT (Pin 15)

This pin provides the bootstrap bias for the gate driver. A 2.2Ω resistor may be placed in series with the bootstrap diode to prevent over charging of the BOOT capacitor during normal operation.

PVCC (Pin 16)

This pin is the output of the internal series linear regulator. A minimum 1µF capacitor is required for decoupling PVCC to PGND. For proper operation the PVCC capacitor must be within 150 mils of the PVCC and the PGND pins and must be connected to these pins with dedicated traces.

Exposed Thermal Pad

This pad is electrically isolated. Connect this pad to the signal ground plane using at least five vias for a robust thermal conduction path.

Typical Performance Curves

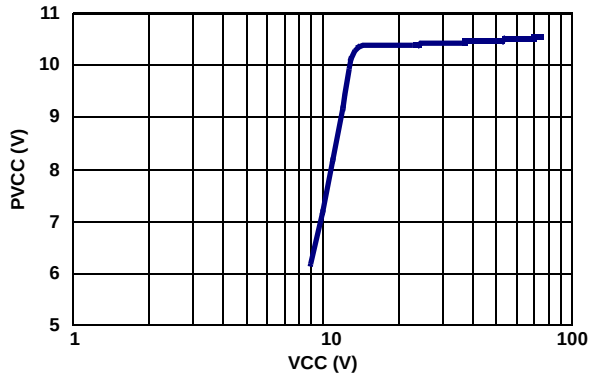


FIGURE 1. PVCC vs VCC (I_{PVCC} = 20mA)

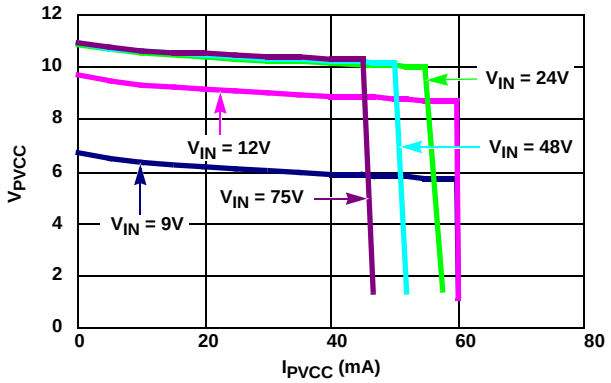


FIGURE 2. VI CHARACTERISTIC of PVCC

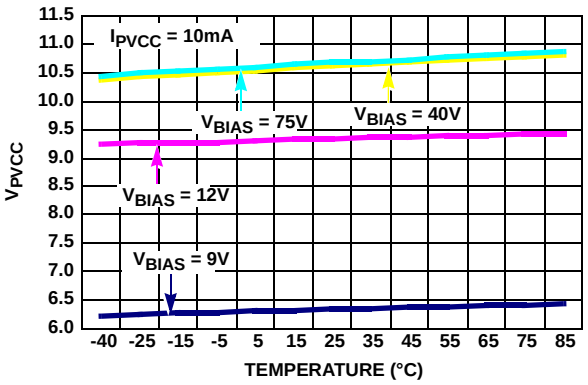


FIGURE 3. PVCC vs TEMPERATURE

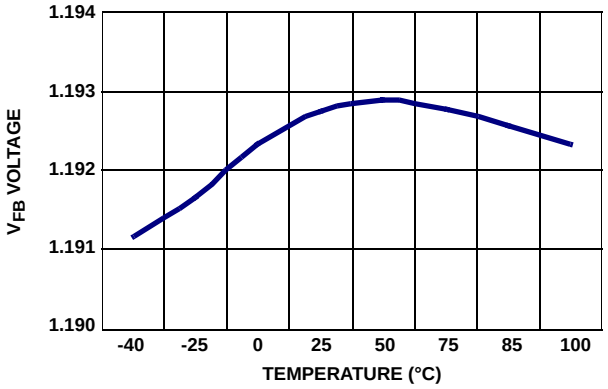


FIGURE 4. V_{FB} vs TEMPERATURE

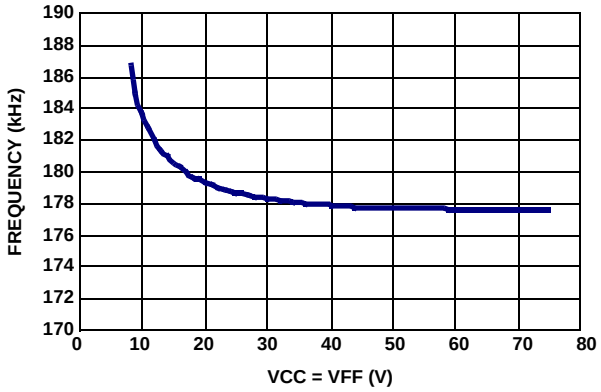


FIGURE 5. R_T/C_T FREQUENCY vs INPUT VOLTAGE (R_T = 40.2kΩ, C_T = 1000pF COG)

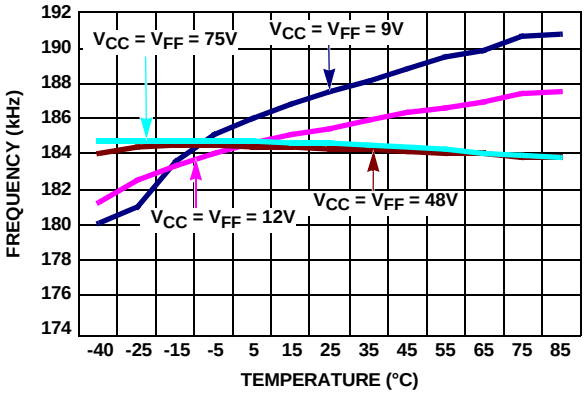


FIGURE 6. R_T/C_T FREQUENCY vs TEMPERATURE (R_T = 40.2kΩ, C_T = 1000pF COG)

Typical Performance Curves (Continued)

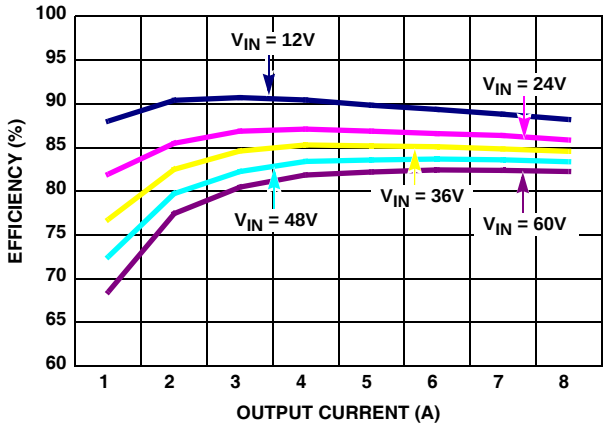


FIGURE 7. EFFICIENCY VS LOAD (OUTPUT VOLTAGE = 5V, F_{SW} = 200kHz (SEE APPLICATION NOTE FOR MORE DETAILS)

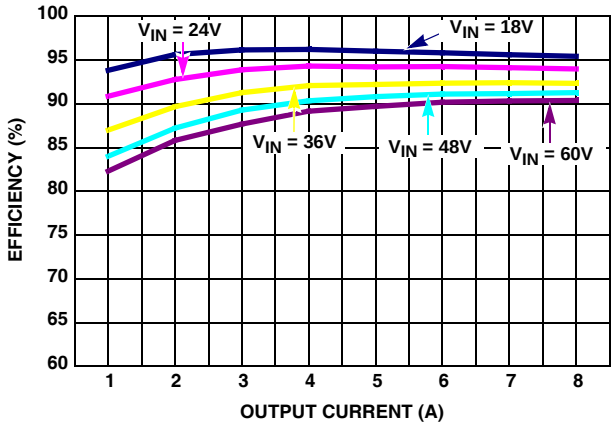


FIGURE 8. EFFICIENCY VS LOAD (OUTPUT VOLTAGE = 12V, F_{SW} = 200kHz (SEE APPLICATION NOTE FOR MORE DETAILS)

Functional Description

Enable/Soft-Start

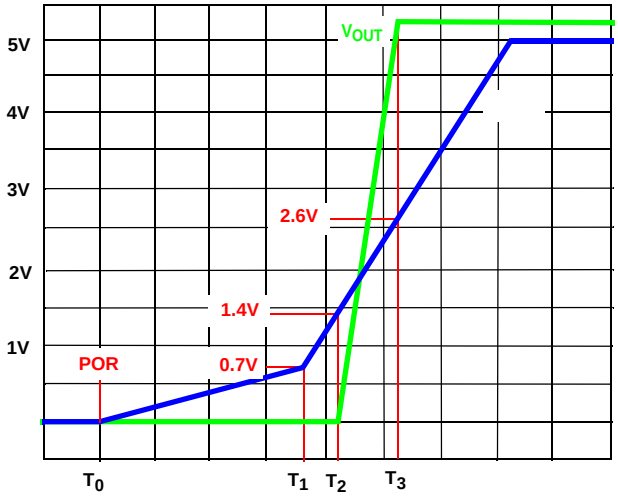


FIGURE 9. TYPICAL SOFT-START DIAGRAM

Figure 9 illustrates the start-up scheme of the ISL8107. The Power-On Reset (POR) function continually monitors the bias voltage at VCC and VFF. When the voltage at VCC and VFF exceed their rising POR thresholds (T_0), the ISL8107 provides initially 2µA to charge the soft-start capacitor, C_{SS}, connected to the ENSS pin. If the voltage at this pin is allowed to rise, it will ramp-up with at a slope determined by the 2µA current and the value of the soft-start capacitor. When the voltage at ENSS reaches 0.77V (Typ) at T_1, the oscillator circuit is active, causing the voltage at RT/CT pin to drop from V_{IN} and generate sawtooth waveform. At the same time, the soft-start current is increased to 33µA; the ENSS voltage then ramps up at a faster rate. The UGATE starts switching when the ENSS voltage reaches 1.4V (Typ).

The delay from POR (T_0) to the time the IC starts switching (T_2) can be approximated by using Equation 1:

$$T_{delay,switching} = 3.712 \times 10^{5} \cdot C_{SS} \quad \text{(EQ. 1)}$$

The output voltage soft-start time is determined by the rise time of ENSS voltage from 1.4V to 2.6V (T_3 -T_2). The output voltage ramp time can be calculated from:

$$T_{SS} = \frac{1.2}{33 \times 10^{-6}} \cdot C_{SS} \quad \text{(EQ. 2)}$$

The soft-start capacitor C_{SS} is continuously charged up linearly and clamped at 5V. Note that any leakage current on ENSS node will extend the start-up period.

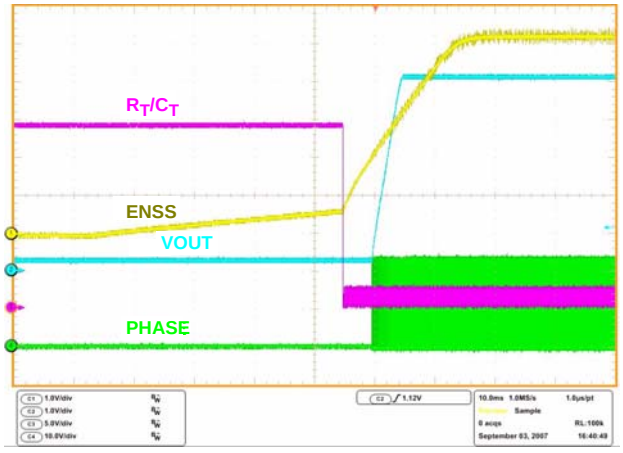


FIGURE 10. TYPICAL SOFT-START WAVEFORM

Oscillator and Synchronization

The ISL8107 provides adjustable frequency from 100kHz to 600kHz by changing external resistor R_T and capacitor C_T.

The time constant of R_T/C_T determines the oscillator frequency, which can be calculated through Equation 3:.

$$F_{OSC} = \frac{1}{0.1215 R_T C_T + 140 \times 10^{-9}} \quad \text{(EQ. 3)}$$

Note that when the controller is disabled, the voltage at RT/CT pin rises up to the input voltage. Hence, the voltage rating of the C_T capacitor must be sufficient to support the maximum input voltage.

The SYNC pin provides the ISL8107 to synchronize its switching frequency to the fundamental frequency of the input waveform. The rising edge of the input synchronization signal is used to terminate the R_T/C_T ramp signal; therefore, when frequency synchronization is used, the time constant of R_T/C_T must be set longer than the period of the sync signal. Tie the sync pin to ground when the sync feature is not used.

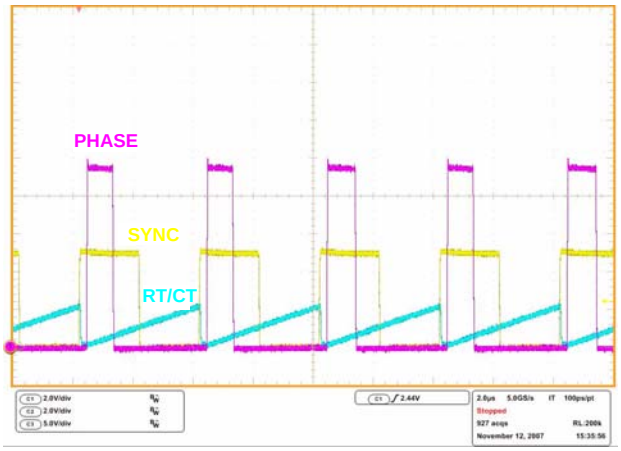


FIGURE 11. SYNCHRONIZATION OPERATION

MINIMUM ON-TIME

The ISL8107 requires the MOSFET to be turned on to a minimum of 200ns (Typ). This minimum gate pulse width is required to ensure proper samplings of the overcurrent protection circuit.

For low duty cycle applications, the switching frequency must be selected to satisfy the condition shown in Equation 4:

$$F_{OSC} < \frac{V_{OUT}}{\eta \cdot V_{IN}} \cdot \frac{1}{t_{on-min}} \quad \text{(EQ. 4)}$$

Where η is converter efficiency.

MINIMUM OFF-TIME

At the termination of the oscillator's ramp, there is a 190ns time interval before the next ramp starts. This time interval creates the minimum-off time of the PWM. This period ensures that the boot capacitor is refreshed. Equation 5 can be used to calculate the switching frequency to meet the condition:

$$F_{OSC} < \left(1 - \frac{V_{OUT}}{\eta \cdot V_{IN}}\right) \cdot \frac{1}{t_{off-max}} \quad \text{(EQ. 5)}$$

Overcurrent Protection

The overcurrent protection function protects the converter from overcurrent conditions by monitoring the current flowing through the MOSFET. OCP is implemented via a resistor (R_{OCSET}) and a capacitor (C_{OCSET}) connecting the OCSET pin and the drain of the MOSFET. An internal 104µA current source develops a voltage across R_{OCSET} which is then compared with the voltage developed across the MOSFET at turn on as measured at the PHASE pin. When the voltage drop across the MOSFET exceeds the voltage drop across the resistor, a OCP event occurs. C_{OCSET} is placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input bus.

A 200ns blanking period is used to reduce the current sampling error due to leading-edge switching noise.

The OCP trip point varies mainly due to MOSFET $r_{DS(ON)}$ variations and layout noise concerns. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from the following equations with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature;
2. The minimum I_{OCSET} from the specification table

Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

Simple OCP Equation

$$R_{OCSET} = \frac{I_{OC} \bullet r_{DS(ON)}}{100\mu A}$$

Detailed OCP Equation

$$R_{OCSET} = \frac{\left(I_{OC\_SOU} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)}}{I_{OCSET}} \quad \text{(EQ. 6)}$$

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L_{OUT}} \bullet \frac{V_{OUT}}{V_{IN}}$$

F_{SW} = Regulator Switching Frequency

If overcurrent is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (4 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely.

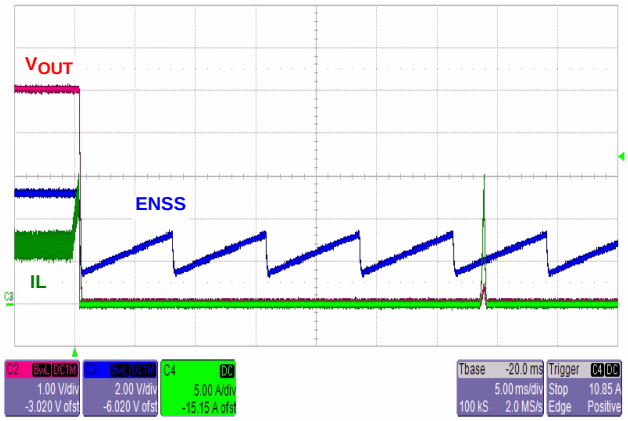


FIGURE 12. TYPICAL OVERCURRENT PROTECTION

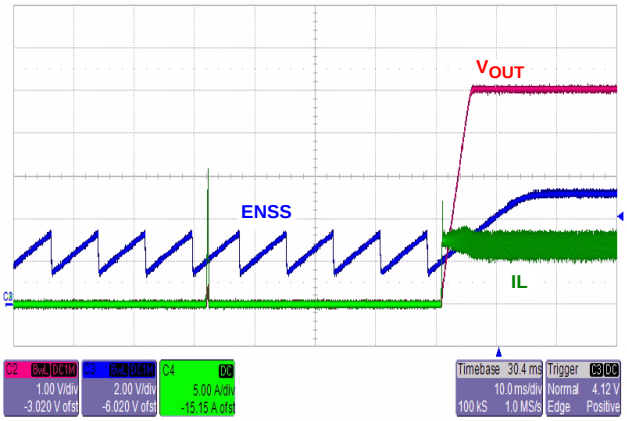


FIGURE 13. TYPICAL HICCUP RECOVER

Thermal Protection

If the ISL8107 IC junction temperature reaches a nominal temperature of +150°C, the controller will be disabled. The ISL8107 will not be re-enabled until the junction temperature drops below +110°C.

Power-Good

The PGOOD comparator monitors the voltage on the FB pin. PGOOD is asserted (open drain) when the FB pin voltage is within 14% of the reference voltage. The turn-on response of the PGOOD circuit has a typical 3µs delay. The PGOOD is deasserted under disable, overcurrent event, or over-temperature event.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

For applications that have transient load rates above 1A/ns, high frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 7:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor

current. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 8 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 8)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFET and the diode. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFET and the diode, and between the drain of the MOSFET and the anode of diode.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select a bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage, a voltage rating of 1.5x greater is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately as shown in Equation 9.

$$I_{IN,RMS} = \sqrt{I_O^2 (D - D^2) + \frac{\Delta I^2}{12} D} \qquad D = \frac{V_O}{VIN}$$

OR

$$I_{IN,RMS} = K_{ICM} \bullet I_O \qquad \text{(EQ. 9)}$$

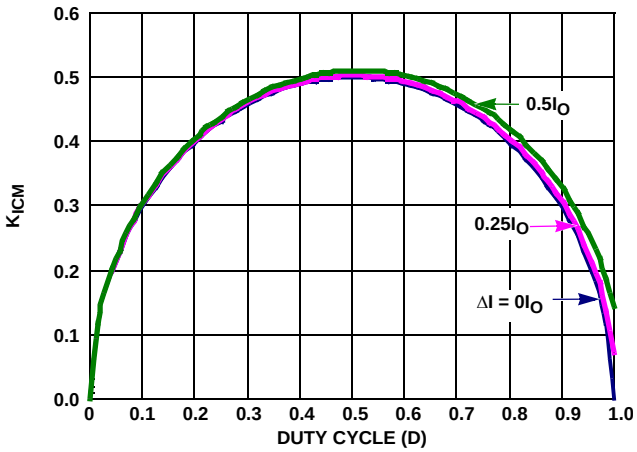


FIGURE 14. INPUT-CAPACITOR CURRENT MULTIPLIER FOR SINGLE-PHASE BUCK CONVERTER

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The ISL8107 requires a N-Channel power MOSFET. This should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

The power dissipation includes two loss components; conduction loss and switching loss.

$$P_{MOSFET} = I_O^2 \times r_{DS(ON)} \times D + \frac{1}{2} \times I_O \times V_{IN} \times T_{SW} \times F_S \qquad \text{(EQ. 10)}$$

where: D is the duty cycle = V_O / V_{IN},
T_{SW} is the switching interval, and
F_s is the switching frequency.

The gate-charge losses are dissipated by the ISL8107 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that the MOSFET is within its maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Note that at 9V input voltage, the PVCC voltage can be as low as 6V. Low gate-voltage threshold MOSFET must be used in this condition.

Rectifier Selection

Power Schottky diode is recommended for better converter efficiency. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor. The power dissipation is shown in Equation 11:

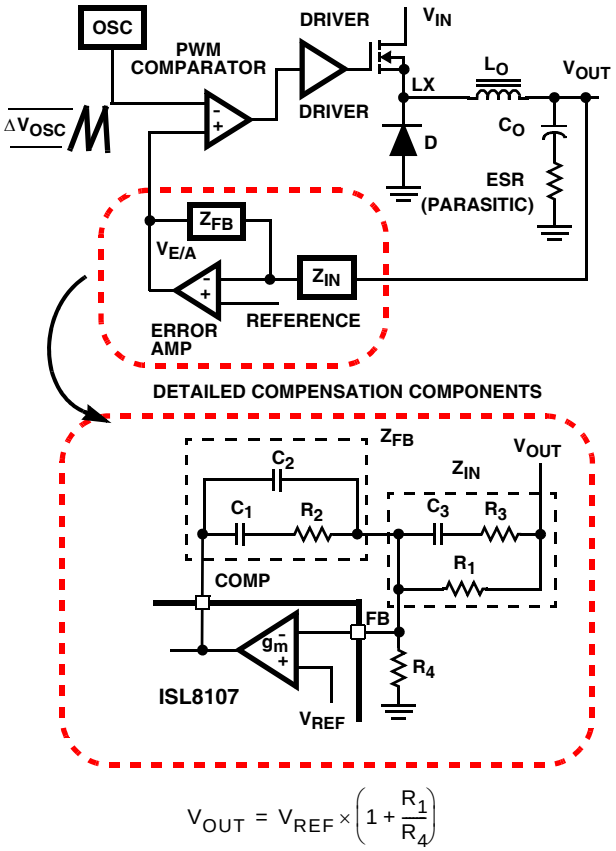
$$P_D[W] = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(EQ. 11)}$$

where V_D is the voltage of the Schottky diode = 0.5V to 0.7V

Application Guidelines

Feedback Compensation

Figure 15 highlights the voltage-mode control loop for a buck converter with type-III compensator. The output voltage is regulated to the reference voltage level. The error amplifier output is compared with the oscillator ramp wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter. The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_4}\right)$$

FIGURE 15. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. The DC gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}. The ISL8107 incorporates a feed forward loop that accounts for changes in the input voltage. This maintains a constant modulator gain.

For the purpose of this analysis, L and DCR represent the output inductance and its DCR, while C and ESR represents the total output capacitance and its equivalent series resistance in Equation 12.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR} \quad \text{(EQ. 12)}$$

The compensation network consists of the transconductance amplifier (internal to the ISL8107) and the external R_1 to R_4, C_1 to C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, R_4, C_1, C_2, and C_3) in Figures 4 and 5. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_2, (10k to 100k typically)
2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC}. The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \times F_{Z1} \times R_2} \quad \text{(EQ. 13)}$$

3. Calculate C_3 such that F_{BW} is placed at desired frequency (typically, 0.1x to 0.5x F_{SW}). F_{SW} represents the switching frequency of the regulator.

$$C_3 = \frac{2\pi \times F_{BW} \times L \times C_0 \times V_{OSC}}{V_{IN} \times R_2} \quad \text{(EQ. 14)}$$

ISL8107 has feed forward compensation that adjusts the amplitude of $0.11 * V_{IN}$. Therefore, the Equation 14 can be simplified as Equation 15:

$$C_3 = \frac{0.22\pi \times F_{BW} \times L \times C_0}{R_2} \quad \text{(EQ. 15)}$$

4. Calculate C_2 such that the placement of F_{P2} is at a fraction of the F_{SW}. The lowering of the frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$C_2 = \frac{1}{2\pi \times F_{P2} \times R_2} \quad \text{(EQ. 16)}$$

5. Calculate R_3 such that the placement of F_{P1} is at the F_{CE}.

$$R_3 = \frac{1}{2\pi \times C_3 \times F_{CE}} \quad \text{(EQ. 17)}$$

6. Calculate R_1 such that the placement of F_{Z2} is at the F_{LC}.

$$R_1 = \frac{1}{2\pi \times C_3 \times F_{LC}} - R_3 \quad \text{(EQ. 18)}$$

7. Calculate R_4 based on target output voltage.

$$R_4 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_1 \quad \text{(EQ. 19)}$$

It is recommended that a mathematical model be used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. Equations 20 and 21 describe the frequency response of the buck converter in continuous conduction mode (G_{vd}), feedback compensation (G_{comp}) and loop response (G_{LP}):

$$G_{vd}(f) = \frac{D_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{COMP}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}\right)} \quad \text{(EQ. 20)}$$

$$G_{LP}(f) = G_{vd}(f) \cdot G_{COMP}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \text{(EQ. 21)}$$

Figure 16 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the previous guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The loop gain, G_{LP}, is constructed on the log-log graph of Figure 16 by adding the modulator gain, G_{vd} (in dB), to the feedback compensation gain, G_{COMP} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select

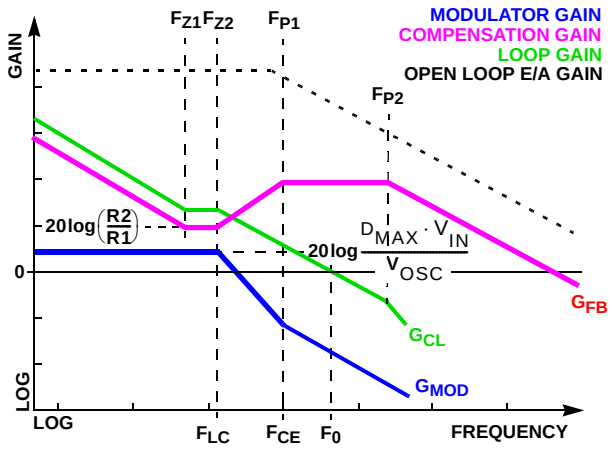


FIGURE 16. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

target crossover frequencies in the range of 10% to 30% of the switching frequency (F_{SW}).

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

A multi-layer printed circuit board is recommended. Figure 17 shows the critical components of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, (usually a middle layer of the PC board) for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE nodes. Use the remaining printed circuit layers for small signal wiring.

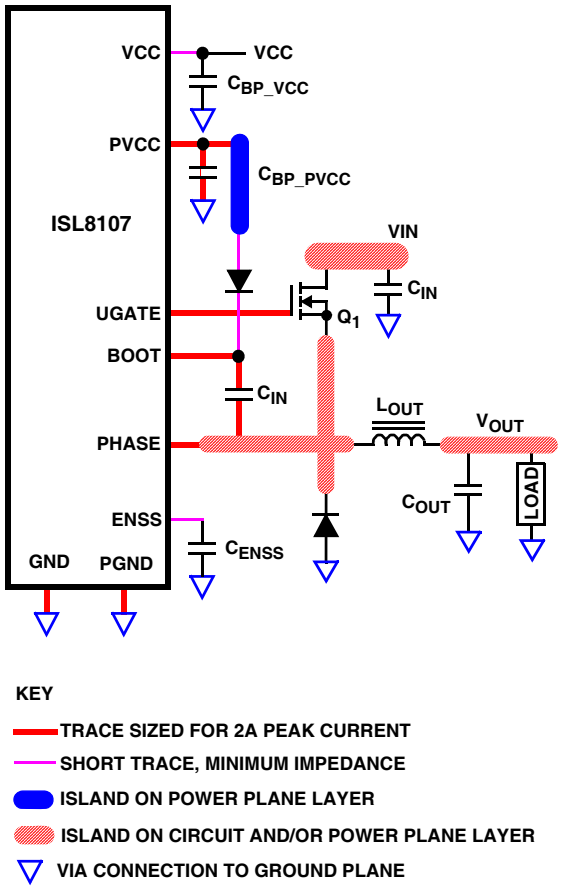


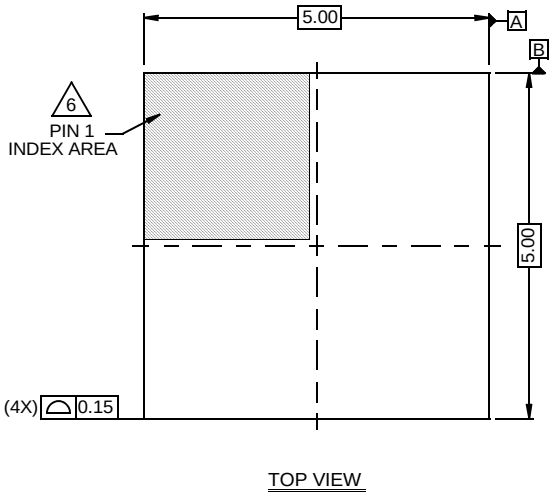
FIGURE 17. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Locate the ISL8107 within 2 to 3 inches of the MOSFET, Q1, (1 inch or less for 500kHz or higher operation). The circuit traces for the MOSFETs' gate and source connections from the ISL8107 must be sized to handle up to 2A peak current. Minimize any leakage current paths on the ENSS pin and locate the capacitor, C_{ENSS} close to the ENSS pin as the internal current source is only 33µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT pin and the phase node.

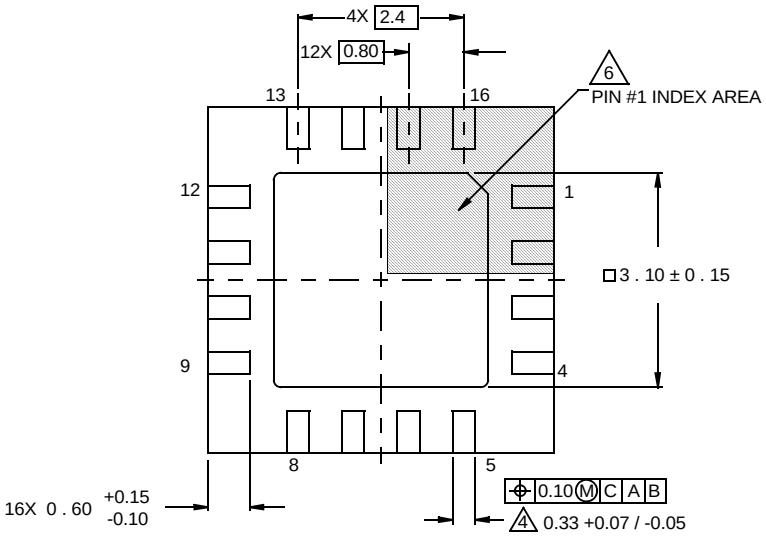
Package Outline Drawing

L16.5x5B

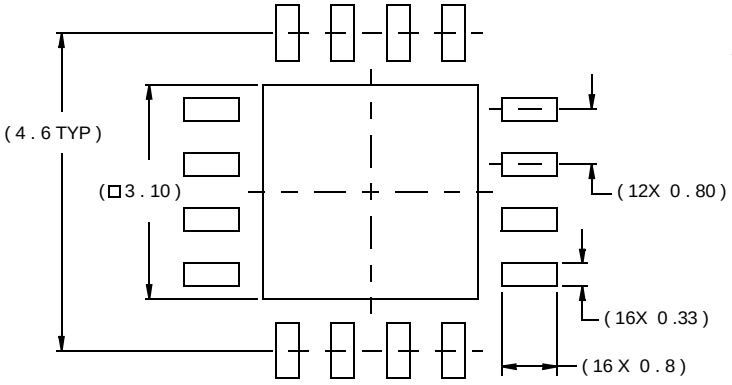
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 02/08



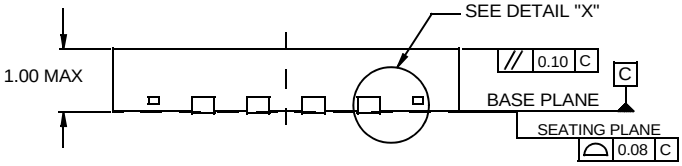
TOP VIEW



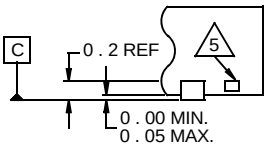
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.