

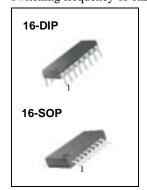
KA7500B SMPS Controller

Features

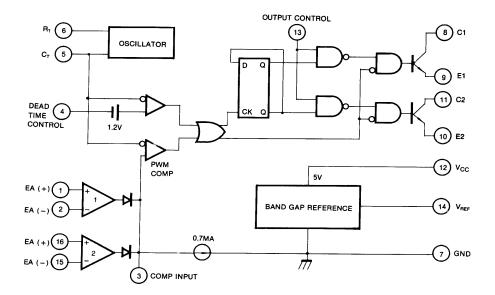
- Internal Regulator Provides a Stable 5V Reference Supply Trimmed to 5%
- Uncommitted Output TR for 200mA Sink or Source Current
- Output Control For Push-Pull or Single Ended Operation
- Variable Duty Cycle By Dead Time Control (Pin 4)
 Complete PWM Control Circuit
- On-Chip Oscillator With Master or Slave Operation
- Internal Circuit Prohibits Double Pulse at Either Output

Description

The KA7500B is used for the control circuit of the PWM switching regulator. The KA7500B consists of 5V reference voltage circuit, two error amplifiers, a flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1kHz to 300kHz.



Internal Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	42	V
Collector Supply Voltage	Vc	42	V
Output Current	lo	250	mA
Amplifier Input Voltage	VIN	Vcc +0.3	V
Power Dissipation (T _A = 25°C)	PD	1 (KA7500B) 0.9 (KA7500BD)	W
Operating Temperature Range	TOPR	0 ~ +70	°C
Storage Temperature Range	TSTG	-65 ~ +150	°C

Electrical Characteristics

(VCC = 20V, f = 10kHz, TA = 0°C to +70°C, unless otherwise specified)

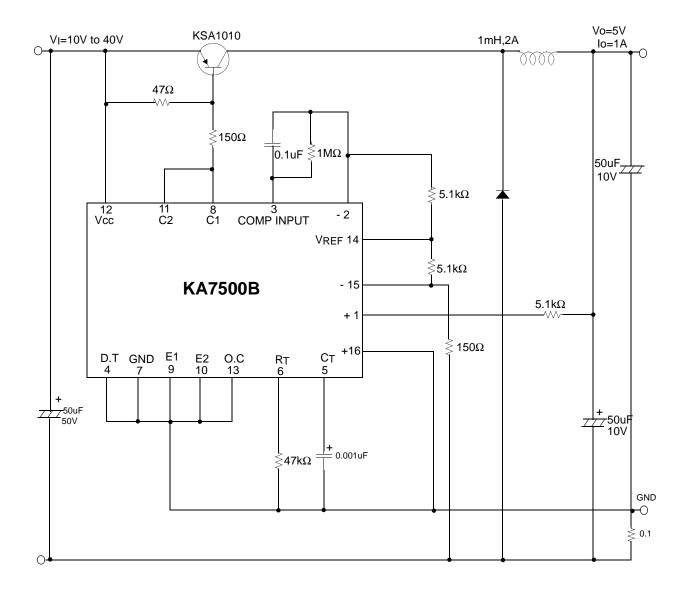
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit		
REFERENCE SECTION				•		•		
Reference Output Voltage	VREF	IREF = 1mA	4.75	5.0	5.25	V		
Line Regulation	ΔVREF	Vcc = 7V to 40V	-	2.0	25	mV		
Temperature Coefficient of VREF	ΔV _{REF} /ΔT	T _A = 0°C to 70°C	-	0.01	0.03	%/°C		
Load Regulation	ΔVREF	IREF = 1mA to 10mA	-	1.0	15	mV		
Short-Circuit Output Current	Isc	VREF = 0V	10	35	50	mA		
OSCILLATOR SECTION								
Oscillation Frequency	f	$C_T = 0.01 \mu F$, $R_T = 12 k\Omega$	-	10	-	kHz		
Frequency Change with Temperature	Δf/ΔΤ	$CT = 0.01\mu F$, $RT = 12k\Omega$	-	-	2	%		
DEAD TIME CONTROL SECTION	•		•	•	•			
Input Bias Current	IBIAS	VCC = 15V, 0V≤V4≤5.25V	-	-2.0	-10	μА		
Maximum Duty Cycle	D(MAX)	V _{CC} = 15V, V ₄ = 0V O.C Pin = V _{REF}	45	-	-	%		
land Theory and Maltana	\/	Zero Duty Cycle	-	3.0	3.3			
Input Threshold Voltage	VITH	Max. Duty Cycle	0	-	-	V		
ERROR AMP SECTION								
Input Offset Voltage	Vio	V ₃ = 2.5V	-	2.0	10	mV		
Input Offset Current	IIO	V ₃ = 2.5V	-	25	250	mA		
Input Bias Current	IBIAS	V ₃ = 2.5V	-	0.2	1.0	μА		
Common Mode Input Voltage	Vсм	7V ≤ VCC ≤ 40V	-0.3	-	Vcc	V		
Open-Loop Voltage Gain	G _{VO}	0.5V ≤ V ₃ ≤3 .5V	70	95	-	dB		
Unit-Gain Bandwidth (Note1)	BW	-	-	650	-	kHz		
PWM COMPARATOR SECTION								
Input Threshold Voltage	VITH	Zero Duty Cycle	-	4	4.5	V		
Input Sink Current	ISINK	V ₃ =0.7V	-0.3	-0.7	-	mV		
OUTPUT SECTION								
Output Saturation Voltage Common Emitter	VCE(SAT)	V _E = 0, I _C = 200mA	-	1.1	1.3			
Common Collector	VCC(SAT)	V _C = 15V, I _E = -200mA	-	1.5	2.5	V		
Collector Off-State Current	IC(OFF)	VCC = 40V, VCE = 40V	-	2	100	^		
Emitter Off-State Current	IE(OFF)	VCC = VC = 40V, VE = 0	-	-	-100	μΑ		
TOTAL DEVICE	•	•	•	•	•	•		
Supply Current	Icc	Pin 6 = VREF, VCC = 15V	-	6	10	mA		
OUTPUT SWITCHING CHARACTERIST	OUTPUT SWITCHING CHARACTERISTICS							
Rise Time	tR	-	-	-	-	-		
Common Emitter	-	-	-	100	200	no		
Common Collector	-	-	-	100	200	ns		
Fall Time	tF	-	-	-	-	-		
Common Emitter	-	-	-	25	100	ns		
Common Collector	-	-	-	40	100			

Note:

1. This parameter, although guaranteed, is not 100% tested in production.

Typical Application

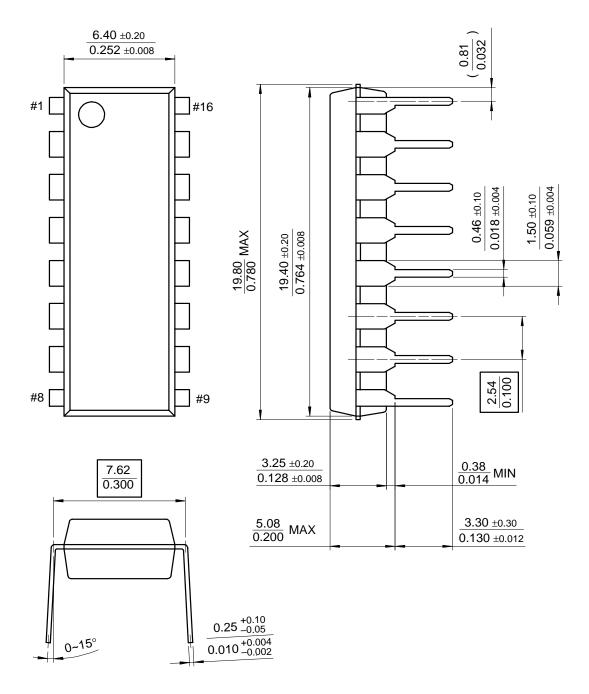
Pulse Width Modulated Step-down Converter



Mechanical Dimensions

Package

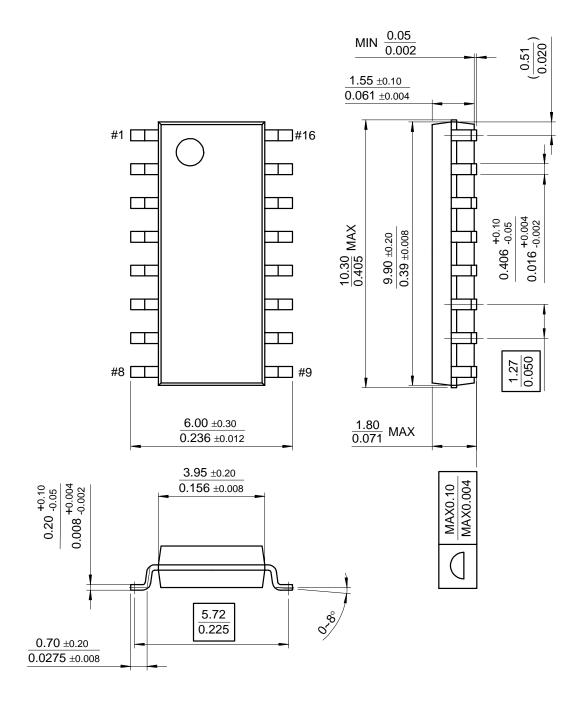
16-DIP



Mechanical Dimensions (Continued)

Package

16-SOP



Ordering Information

Product Number	Package	Operating Temperature
KA7500B	16-DIP	0 ~ +70°C
KA7500BD	16-SOP	0~ +70 C

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