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	INTEGRATED CIRCUITS GROUP SHARP CORPORATION	REPRESENTATIVE DEPARTMENT

SPECIFICATION

DEVICE SPECIFICATION FOR

16K CMOS STATIC RAM (2,048 X 8bit)

MODEL No.

LH5116NA-10

☐ CUSTOMERS APPROVAL

DATE

BY

PRESENTED
BY

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IC Engineerring Center

Integrated Circuits Group

SHARP CORPORATION

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Contents

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1. General Description

The LH5116NA-10 is a static RAM organized as 16,384(2,048 word x 8bit) fabricated with a CMOS silicon gate process.

It's main features include:

Features

- ○ Access time (MAX.) and dissipation current (MAX.)
  100ns / 40mA
- ○ Single 5V power supply (5V±10%)
- ○ Full static operation requiring no clock and refresh cycle
- ○ All input and output TTL compatible
- ○ Three state output
- ○ Pin configuration is compatible with industry standard
  16K EPROM/MASK ROM
- ○ Standard 24-pin Small-Outine Package (SOP)

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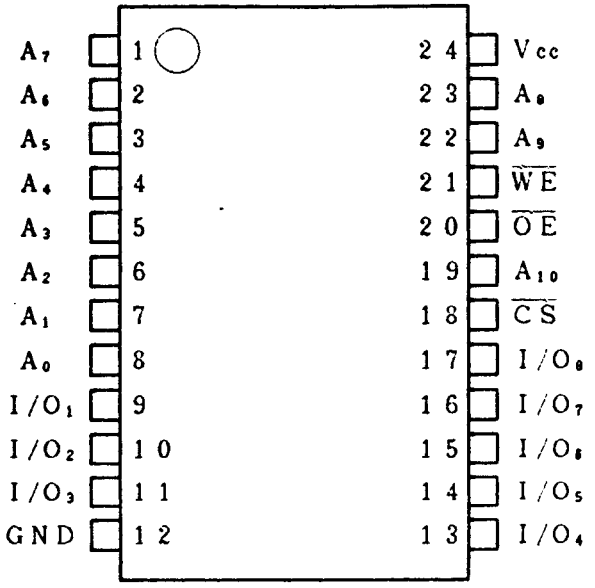
2. Pin Configuration



Pin name	Signal
$A_0 \sim A_{10}$	Address input
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$I/O_1 \sim I/O_8$	Data input/output
V_{CC}	Power supply
GND	Ground

3. Operating Mode

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	$I/O_1 \sim I/O_8$	Supply currenat
H	X	X	Deselect	High impedance	Standby (I_{CCL})
L	L	X	Write	Data input	Operating(I_{CC})
L	H	L	Read	Data output	Operating(I_{CC})
L	X	H	Output disable	High impedance	Operating(I_{CC})

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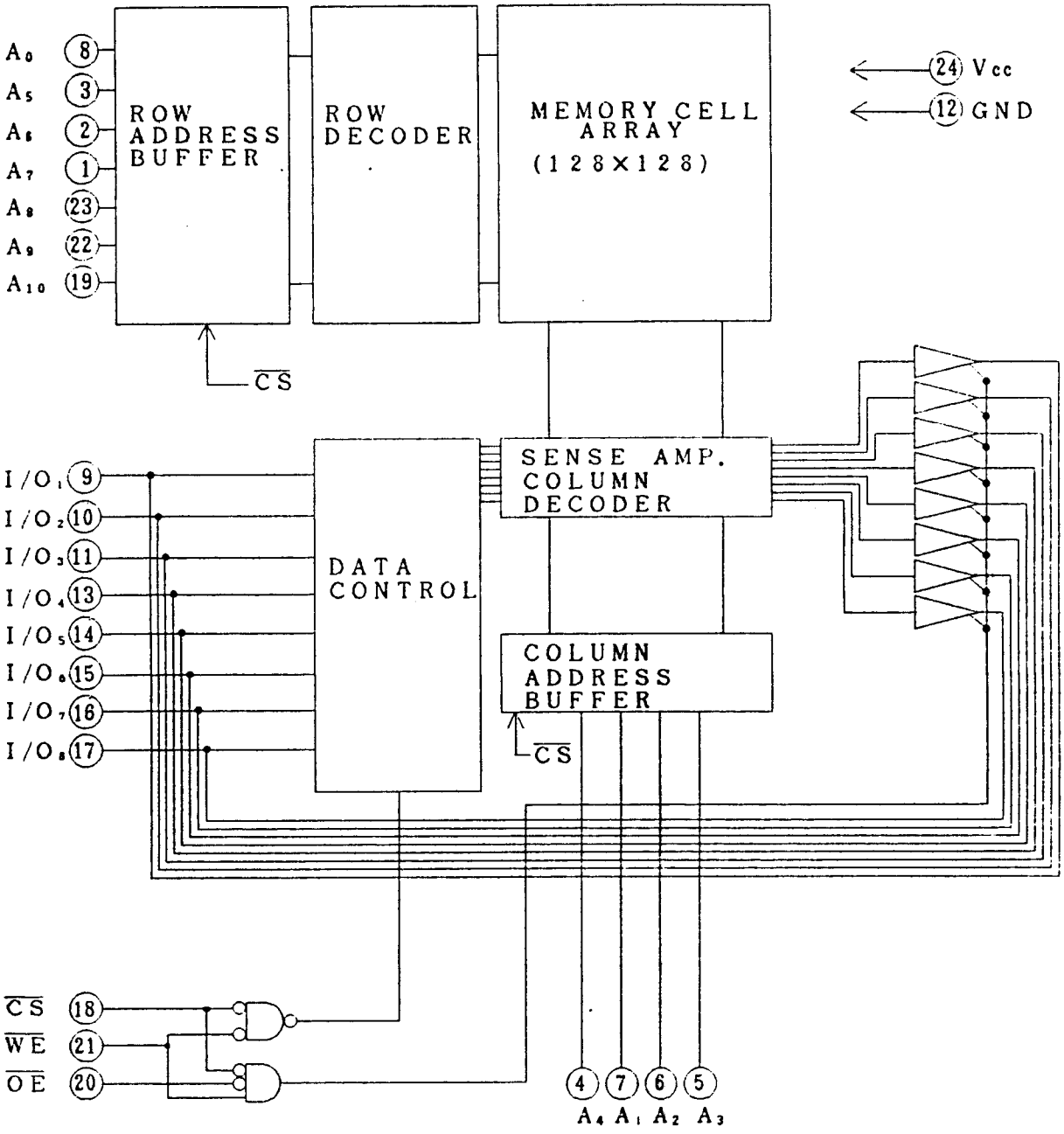
4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3～+7.0	V
Input voltage	V_{IN}	−0.3～V_{CC}+0.3	V
Operating temperature	Topr	0～+70	℃
Storage temperature	Tstr	−55～+150	℃

6. DC Electrical Characteristics

V_{CC}=5V±10%, Ta=0～+70℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input "LOW" voltage	V_{IL}		−0.3		0.8	V
Input "HIGH" voltage	V_{IH}		2.2		V_{CC}+0.3	V
Output "LOW" voltage	V_{OL}	I_{OL}= 2.1mA			0.4	V
Output "HIGH" voltage	V_{OH}	I_{OH}=−1.0mA	2.4			V
Input leakage current	$\|I_{LI}\|$	V_{IN}=0～V_{CC}			1.0	μA
Output leakage current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V～V_{CC}			1.0	μA
Dissipation current 1	I_{CC1}	$\overline{CS}$=0V, other input is 0V～V_{CC}, $I_{I/O}$=0mA, ($\overline{OE}$=V_{CC})		25	30	mA
Dissipation current 2	I_{CC2}	$\overline{CS}$=V_{IL}, other input is V_{IL}～V_{IH}, $I_{I/O}$=0mA, ($\overline{OE}$=V_{IH})		30	40	mA
Standby Dissipation current	I_{CCL}	$\overline{CS}$≧V_{CC}−0.2V			1.0	μA
		other input is 0V～V_{CC}			0.2*	μA

Note) * Ta=25℃

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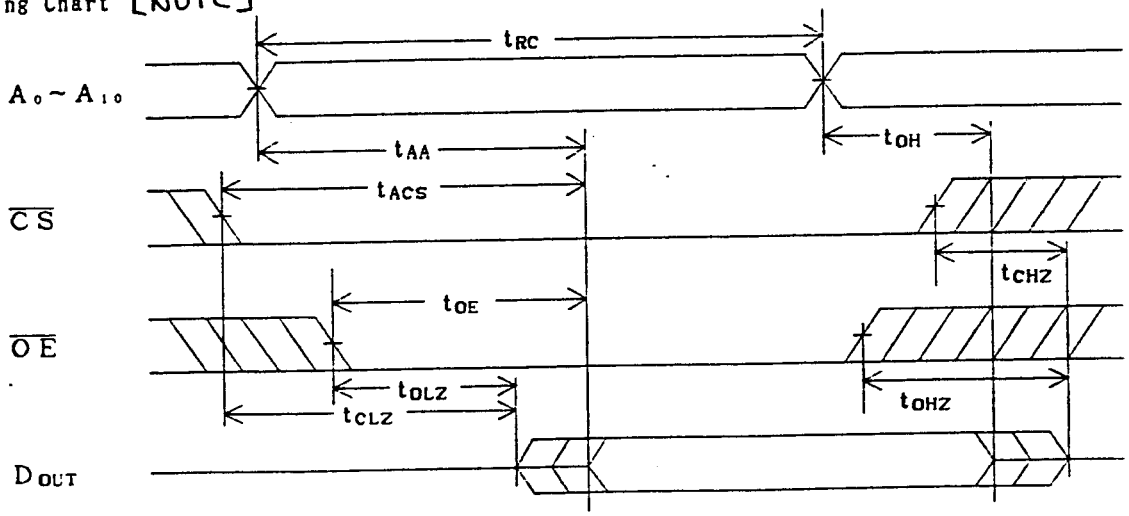
7. AC Characteristics

Read cycle

Vcc = 5 V ± 10%, Ta = 0 ~ + 70 ℃

Parameter	Symbol	MIN	MAX	Unit
Read cycle time	t_{RC}	100		ns
Address access time	t_{AA}		100	ns
Chip enable access time	t_{ACS}		100	ns
Output floating hold time with respect to chip select	t_{CLZ}	10		ns
Output enable access time	t_{OE}		40	ns
Output floating hold time with respect to output enable	t_{OLZ}	10		ns
Output floating time with respect to chip select	t_{CHZ}	0	40	ns
Output floating time with respect to output enable	t_{OHZ}	0	40	ns
Previous read data valid with respect to address change	t_{OH}	10		ns

Timing Chart [NOTE]



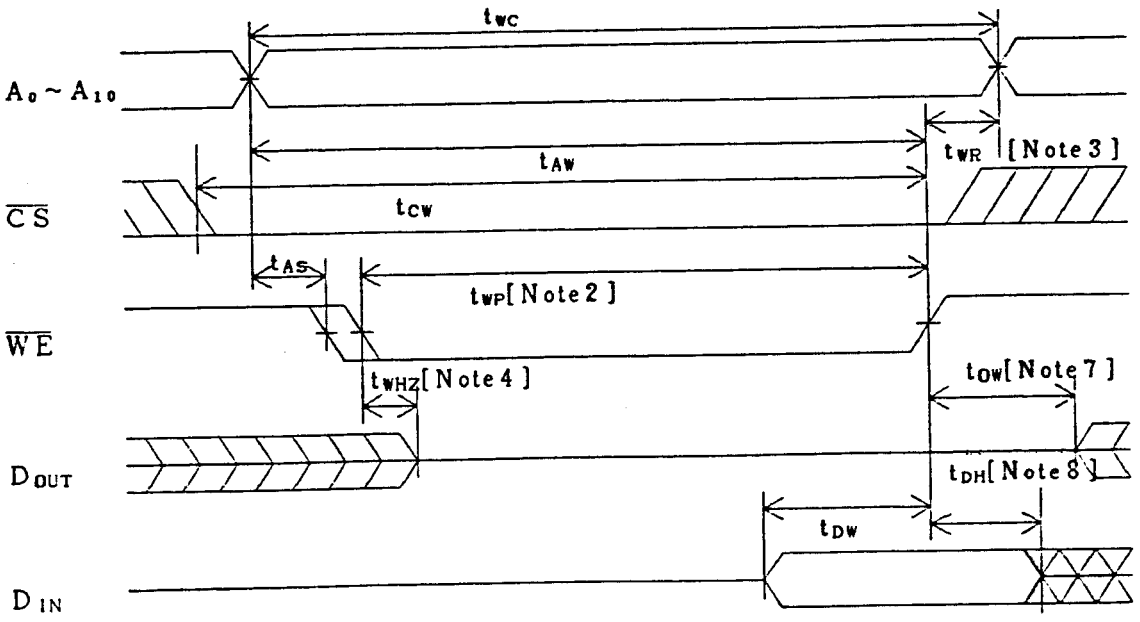
Note) $\overline{WE}$ is "High" level during the read cycle

Write Cycle

V_{CC} = 5 V ± 10 %, Ta = 0 ~ + 70 ℃

Parameter	Symbol	MIN	MAX	Unit
Write cycle	t_{WC}	100		ns
Chip enable to write	t_{CW}	80		ns
Write delay	t_{AW}	80		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	60		ns
Write recovery	t_{WR}	10		ns
Output floating time with respect to write pulse	t_{WHZ}		30	ns
Data setup time	t_{DW}	30		ns
Data hold time	t_{DH}	10		ns
Output floating time with respect to write	t_{OW}	10		ns
Output hold time with respect to output enable	t_{OHZ}		40	ns

Timing Chart(No.1)[Note 1, 6]



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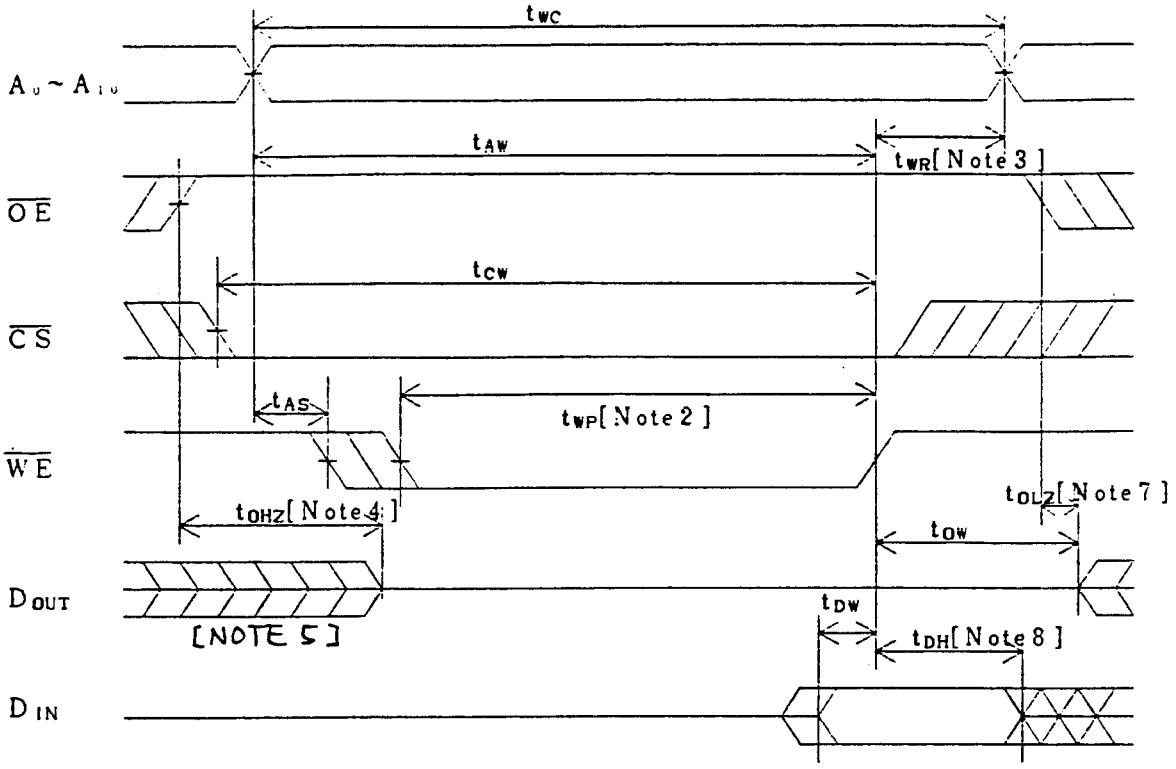
Timing Chart (No.2) [Note 1]



[NOTE]

1. $\overline{WE}$ must be High when $A_0 \sim A_{10}$ switch between high and low.
2. Write cycle occurs during a overlapping period of $\overline{CS}$ = Low an $\overline{WE}$ = Low(t_{WP}).
3. t_{WR} represents the time interval between the earliest rising edge of $\overline{CS}$ or $\overline{WE}$ and the end of write cycle.
4. Since during this period, I/O pins assume output state, no input signal 180° out of phase with an output signal is admitted.
5. If the rising edge of $\overline{CS}$ occurs simultaneously with or after the falling edge of $\overline{WE}$ the output buffer assume high impedance state.
6. $\overline{OE}$ must be kept Low level.
7. D_{OUT} generates data in phase with input data for the write cycle.
8. If both $\overline{CS}$ remain Low during this period, I/O pins assume output state. At this point, no data input signal 180° out of phase with an output signal.

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1. Package Outline Specification

Refer to drawing No. A A 9 4 1 − 0 0 1

2. Markings

2 − 1. Marking contents

(1) Product name : L H 5 1 1 6 N A − 1 0

(2) Company name : S H A R P

(3) Date code

(Example) 8 8 2 9 × × × -- Indicates the product was manufactured in the 2 9 th week of 1988.

× × × → Denotes the production ref.code (1~3)

2 9 → Denotes the production week. (01,02,03, • • • • • 52.53)

8 8 → Denotes the production year. (Lower two digit of the year.)

(4) The marking of " JAPAN " indicates the country of origin.

2 − 2. Marking position

Refer drawing No. A A 9 4 1 − 0 0 1

2 − 3. Marking color

Silver

3. Packing Specification

3 − 1. Packing materials

Material Name	Material Specification	Purpose
Magazine	Anti-static treated plastic (30devices /magazine)	Packing of device
Stopper	Plastic or rubber	Fixing of device
Label	Paper	Indication of product name,quantity and date of manufacture.
Inner case	Cardboard (1200devices/case)	Fixing of magazine
Outer case	Cardboard	Outer packing of magazine

3 − 2. External Appearance of Packing

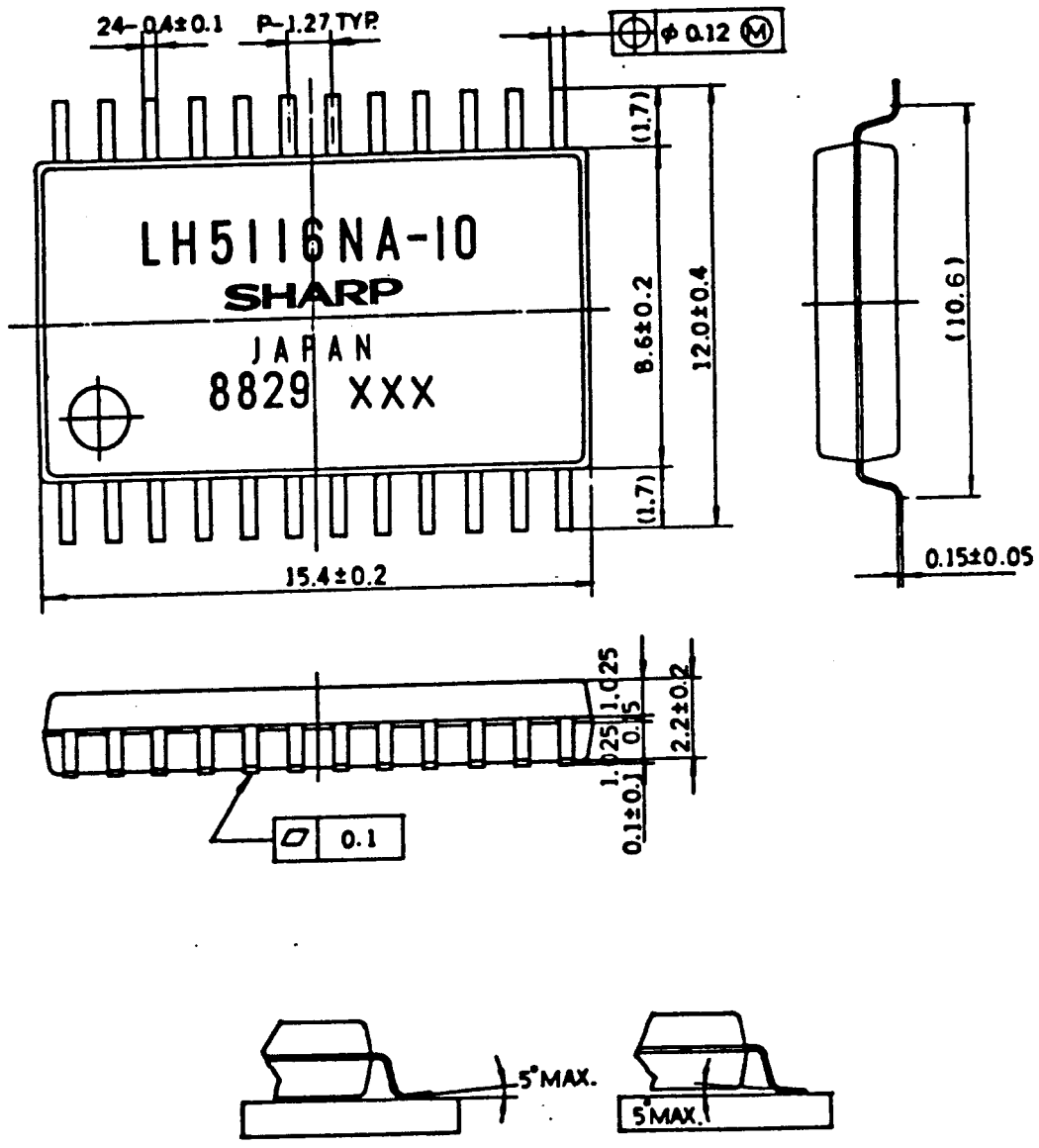
Refer to drawing No. B J 2 0 0 − 0 1 1

4. Precausion For Unpacking

(1) Unpacking should be done on the stand as well as human body treated with anti-ESD .

(2) Anti-ESD treatment is given to a magazine.
Use the equivalent magazine , if it is changed to another one.

(3) Be sure to fix two stoppers to both ends of a magazine when storage to prevent the devices from slipping.



Plastic body dimensions do not include burr of resin.

適用機種 APPLICABLE MODEL	LH5116NA	尺度 SCALE	5/1	単位 UNIT	1 = 1/1 mm	改訂日 DATE / 改訂記事 REVISE / 担当 CHARGE	
板厚 THICKNESS	員数 PIECES	材質 MATERIAL	仕上 FINISH			名称 NAME	SOT24BP
			TIN PLATING			コード CODE	
日付 DATE	'88. 7. 12						
設計 DESIGN / 製図 DRAW / 写図 TRACE / 検図 CHECK / 承認 APPROVE		ｼｬｰﾌﾟ株式会社	IC			図番 DRAWING No.	AA941-0011
		SHARP CORPORATION					

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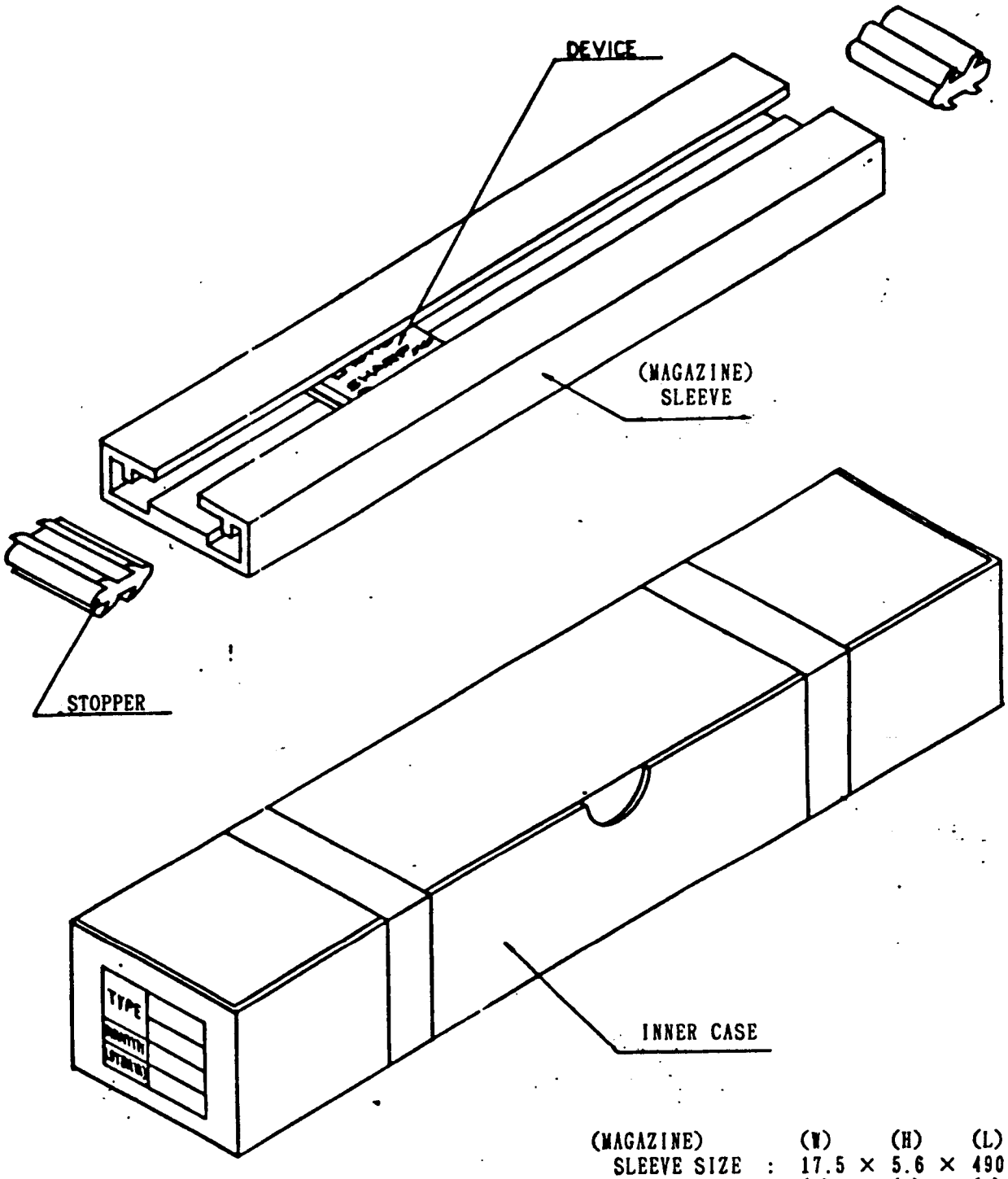
LH5116NA



(MAGAZINE) SLEEVE SIZE	:	(W) (H) (L) 17.5 × 5.6 × 490	
CASE SIZE	:	(W) (H) (L) 80 × 62 × 510	

適用機種 APPLICABLE MODEL	LH5116NA	尺度 SCALE	1/1	単位 UNIT	mm	改訂日 DATE	改訂記事 REVISE
板厚 THICKNESS	個数 PIECES	材質 MATERIAL		仕上 FINISH		名称 NAME	28SOP, 24SOP EXTERNAL APPEARANCE OF PACKING
作成日 DATE	'88. 7. 12					コード CODE	
設計 DESIGN	製図 DRAW	作図 TRACE	検図 CHECK	承認 APPROVE		図番 DRAWING No.	BJ200-011
				SHARP CORPORATION			

AC Characteristics Test Conditions

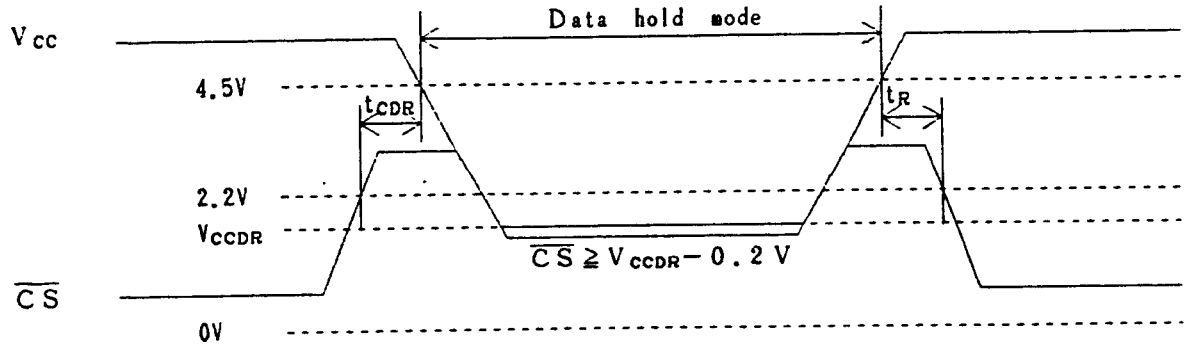
項　　目	条　　件
Input pulse level	V_{IN} = 2.2 V, V_{IL} = 0.8 V
Input rise and fall time	10 ns
I/O timing reference level	1.5 V
Output load	100 pF + 1 TTL

8. Data Hold Characteristics at Low Supply voltage

Ta = 0 ~ +70 ℃

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data hold supply voltage	V_{CCDR}	$\overline{CS} \geqq V_{CCDR} - 0.2$ V	2.0			V
Data hold supply current	I_{CCDR}	$\overline{CS} \geqq V_{CCDR} - 0.2$ V			1.0	μA
		V_{CCDR} = 2 V			0.2**	μA
Chip Select Setup time	t_{CDR}		0			ns
Chip Select Hold time	t_R		t_{RC}*			ns

Note *Read cycle time　**at Ta = 25 ℃



9. Pin Capacitances

Ta = 25 ℃, f = 1 MHz

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input capacitance	C_I	V_I = 0 V			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

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