

1,024-BIT SERIAL ELECTRICALLY ERASABLE PROM

NOVEMBER 2006

FEATURES

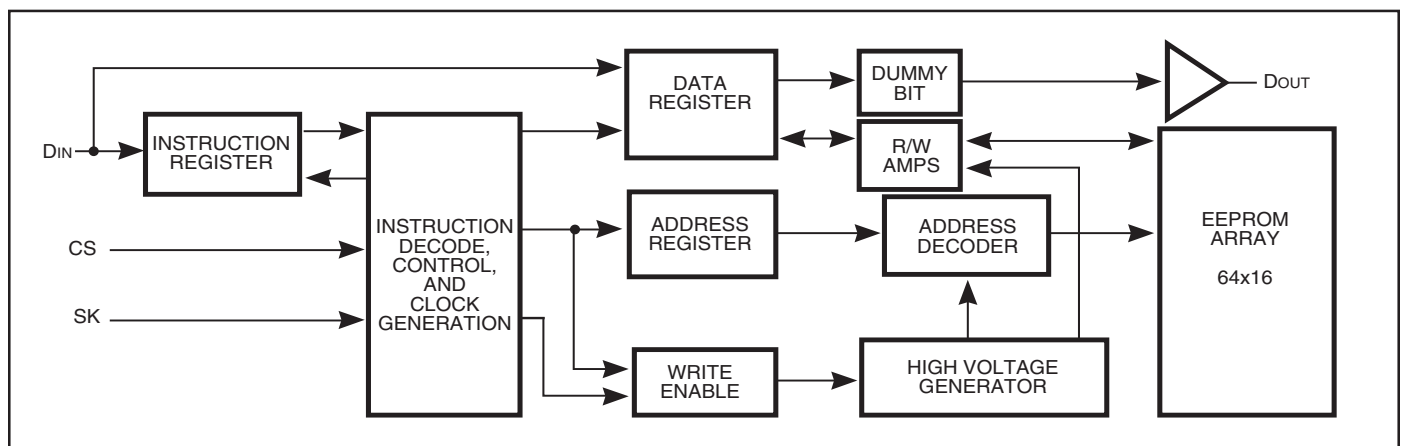
- Industry-standard Microwire Interface
 - Non-volatile data storage
 - Low voltage operation:
 - $V_{cc} = 2.5V$ to $5.5V$
 - Full TTL compatible inputs and outputs
 - Auto increment for efficient data dump
- x16 bit organization
- Hardware and software write protection
 - Defaults to write-disabled state at power-up
 - Software instructions for write-enable/disable
- Enhanced low voltage CMOS E²PROM technology
- Versatile, easy-to-use Interface
 - Self-timed programming cycle
 - Automatic erase-before-write
 - Programming status indicator
 - Word and chip erasable
 - Chip select enables power savings
- Durable and reliable
 - 40-year data retention after 1M write cycles
 - 1 million write cycles
 - Unlimited read cycles
 - Schmitt-trigger inputs
- Industrial and Automotive Temperature Grade
- Lead-free available

DESCRIPTION

The IS93C46B is a low-cost 1kb non-volatile, ISSI[®] serial EEPROM. It is fabricated using an enhanced CMOS design and process. The IS93C46B contains power-efficient read/write memory, and organization of 64 words of 16 bits. The IS93C46B is fully backward compatible with IS93C46.

An instruction set defines the operation of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all erase and write instructions are accepted only while the device is write-enabled. A selected x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the two instructions WRITE ALL or ERASE ALL can program the entire array. Once a device begins its self-timed program procedure, the data out pin (Dout) can indicate the READY/**BUSY** status by raising chip select (CS). The self-timed write cycle includes an automatic erase-before-write capability. The device can output any number of consecutive words using a single READ instruction.

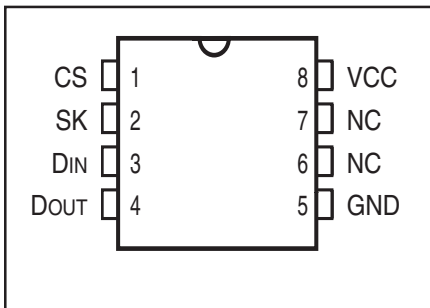
FUNCTIONAL BLOCK DIAGRAM



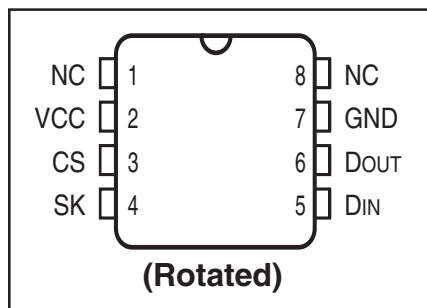
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PIN CONFIGURATIONS

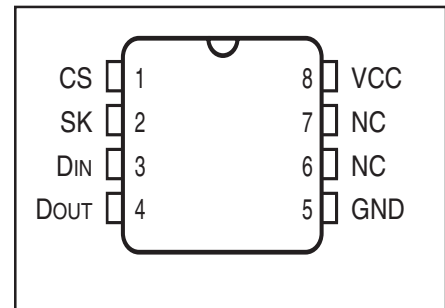
8-Pin DIP, 8-Pin TSSOP



8-Pin JEDEC SOIC "G"



8-Pin JEDEC SOIC "GR"



PIN DESCRIPTIONS

CS	Chip Select
SK	Serial Data Clock
DIN	Serial Data Input
DOUT	Serial Data Output
NC	Not Connected
Vcc	Power
GND	Ground

Applications

The IS93C46B is very popular in many high-volume applications which require low-power, low-density storage. Applications using this device include industrial controls, networking, and numerous other consumer electronics.

Endurance and Data Retention

The IS93C46B is designed for applications requiring up to 1M programming cycles (WRITE, WRALL, ERASE and ERAL). It provides 40 years of secure data retention without power after the execution of 1M programming cycles.

Device Operations

The IS93C46B is controlled by a set of instructions which are clocked-in serially on the Din pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the Din value must be stable at either LOW or HIGH. Each

instruction begins with a start bit of the logical "1" or HIGH. Following this are the opcode (2 bits), address field (6 bits), and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock-speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the DOUT pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DOUT changes during the low-to-high transitions of SK (see Figure 3).

Low Voltage Read

The IS93C46B has been designed to ensure that data read operations are reliable in low voltage environments. They provide accurate operation with Vcc as low as 2.5V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the IS93C46B has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (See Figure 4.) (Note: Chip select must remain LOW until Vcc reaches its operational value.)

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to DIN, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN).

If CS is brought HIGH, after a minimum wait of 250 ns (5V operation) after the falling edge of CS (tcs) DOUT will indicate the READY/BUSY status of the chip. Logical “0” means programming is still in progress; logical “1” means the selected register has been written, and the part is ready for another instruction (see Figure 5). The READY/BUSY status will not be available if: a) The CS input goes HIGH after the end of the self-timed programming cycle, tWP; or b) Simultaneously CS is HIGH, Din is HIGH, and SK goes HIGH, which clears the status flag.

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 250 ns (tcs), the DOUT pin indicates the READY/BUSY status of the chip (see Figure 6).

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

Erase Register (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tcs, will cause DOUT to indicate the READ/BUSY status of the chip: a logical “0” indicates programming is still in progress; a logical “1” indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical “1” (see Figure 9).

INSTRUCTION SET - IS93C46B

Instruction	Start Bit	OP Code	16-bit Organization	
			Address ⁽¹⁾	Input Data
READ	1	10	(A5-A0)	—
WEN (Write Enable)	1	00	11xxxx	—
WRITE	1	01	(A5-A0)	(D15-D0) ⁽²⁾
WRALL (Write All Registers)	1	00	01xxxx	(D15-D0) ⁽²⁾
WDS (Write Disable)	1	00	00xxxx	—
ERASE	1	11	(A5-A0)	—
ERAL (Erase All Registers)	1	00	10xxxx	—

Notes:

1. x = Don't care bit.
2. If input data is not 16 bits exactly, the last 16 bits will be taken as input data.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{GND}	Voltage with Respect to GND	-0.3to+6.5	V
T _{BIAS}	Temperature Under Bias (Industrial)	-40to+85	°C
T _{BIAS}	Temperature Under Bias (Automotive)	-40to+125	°C
T _{STG}	Storage Temperature	-65to+150	°C

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°Cto+70°C	2.5V to 5.5V
Industrial	-40°Cto+85°C	2.5V to 5.5V
Automotive	-40°Cto+125°C	2.7V to 5.5V or 4.5V to 5.5V

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5	pF

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for Commercial, -40°C to +85°C for Industrial, and -40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	V _{CC}	Min.	Max.	Unit
V _{OL}	Output LOW Voltage	I _{OL} = 100 μA	2.5V to 5.5V	—	0.2	V
V _{OL1}	Output LOW Voltage	I _{OL} = 2.1 mA	4.5V to 5.5V	—	0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = -100 μA	2.5V to 5.5V	V _{CC} - 0.2	—	V
V _{OH1}	Output HIGH Voltage	I _{OH} = -400 μA	4.5V to 5.5V	2.4	—	V
V _{IH}	Input HIGH Voltage		2.5V to 5.5V 4.5V to 5.5V	0.7xV _{CC} 0.7xV _{CC}	V _{CC} +1 V _{CC} +1	V
V _{IL}	Input LOW Voltage		2.5V to 5.5V 4.5V to 5.5V	-0.3 -0.3	0.2xV _{CC} 0.8	V
I _{LI}	Input Leakage	V _{IN} = 0V to V _{CC} (CS, SK, DIN, ORG)		0	2.5	μA
I _{LO}	Output Leakage	V _{OUT} = 0V to V _{CC} , CS = 0V		0	2.5	μA

Notes:

Automotive grade devices in this table are tested with V_{CC} = 2.7V to 5.5V and 4.5V to 5.5V.

POWER SUPPLY CHARACTERISTICST_A = 0°C to +70°C for Commercial

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
Icc1	Vcc Read Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	100	μA
			5.0V	—	500	μA
Icc2	Vcc Write Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	1	mA
			5.0V	—	3	mA
I _{SB}	Standby Current	CS = V _{IH} , SK = 0V	2.7V	—	10	μA
			5.0V	—	30	μA

POWER SUPPLY CHARACTERISTICST_A = -40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
Icc1	Vcc Read Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	100	μA
			5.0V	—	500	μA
Icc2	Vcc Write Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	1	mA
			5.0V	—	3	mA
I _{SB}	Standby Current	CS = V _{IH} , SK = 0V	2.7V	—	2	μA
			5.0V	—	4	μA

POWER SUPPLY CHARACTERISTICST_A = -40°C to +125°C for Automotive

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
Icc1	Vcc Read Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	100	μA
			5.0V	—	500	μA
Icc2	Vcc Write Supply Current	CS = V _{IH} , SK = 1 MHz CMOS input levels	2.7V	—	1	mA
			5.0V	—	3	mA
I _{SB}	Standby Current	CS = V _{IH} , SK = 0V	2.7V	—	3	μA
			5.0V	—	8	μA

AC ELECTRICAL CHARACTERISTICST_A = T_A = 0°C to +70°C for Commercial, -40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions	V _{cc}	Min.	Max.	Unit
f _{SK}	SK Clock Frequency		2.5V to 5.5V	0	1	Mhz
			2.7V to 5.5V	0	1	Mhz
			4.5V to 5.5V	0	2	Mhz
t _{SKH}	SK HIGH Time		2.5V to 5.5V	500	—	ns
			2.7V to 5.5V	350	—	ns
			4.5V to 5.5V	250	—	ns
t _{SKL}	SK LOW Time		2.5V to 5.5V	500	—	ns
			2.7V to 5.5V	350	—	ns
			4.5V to 5.5V	250	—	ns
t _{CS}	Minimum CS LOW Time		2.5V to 5.5V	500	—	ns
			2.7V to 5.5V	250	—	ns
			4.5V to 5.5V	250	—	ns
t _{CSS}	CS Setup Time	Relative to SK	2.5V to 5.5V	100	—	ns
			2.7V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t _{DIS}	Din Setup Time	Relative to SK	2.5V to 5.5V	100	—	ns
			2.7V to 5.5V	100	—	ns
			4.5V to 5.5V	100	—	ns
t _{CSH}	CS Hold Time	Relative to SK	2.5V to 5.5V	0	—	ns
			2.7V to 5.5V	0	—	ns
			4.5V to 5.5V	0	—	ns
t _{DIH}	Din Hold Time	Relative to SK	2.5V to 5.5V	100	—	ns
			2.7V to 5.5V	100	—	ns
			4.5V to 5.5V	100	—	ns
t _{PD1}	Output Delay to "1"	AC Test	2.5V to 5.5V	—	400	ns
			2.7V to 5.5V	—	350	ns
			4.5V to 5.5V	—	250	ns
t _{PD0}	Output Delay to "0"	AC Test	2.5V to 5.5V	—	400	ns
			2.7V to 5.5V	—	350	ns
			4.5V to 5.5V	—	250	ns
t _{SV}	CS to Status Valid	AC Test	2.5V to 5.5V	—	400	ns
			2.7V to 5.5V	—	250	ns
			4.5V to 5.5V	—	250	ns
t _{DF}	CS to Dout in 3-state	AC Test, CS=VIL	2.5V to 5.5V	—	200	ns
			2.7V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t _{WP}	Write Cycle Time		2.5V to 5.5V	—	10	ms
			2.7V to 5.5V	—	10	ms
			4.5V to 5.5V	—	5	ms

Notes:1. C_L = 100pF

AC ELECTRICAL CHARACTERISTICST_A = -40°C to +125°C for Automotive

Symbol	Parameter	Test Conditions	V _{CC}	Min.	Max.	Unit
f _{SK}	SK Clock Frequency		2.7V to 5.5V	0	1	Mhz
			4.5V to 5.5V	0	2	Mhz
t _{SKH}	SK HIGH Time		2.7V to 5.5V	500	—	ns
			4.5V to 5.5V	250	—	ns
t _{SKL}	SK LOW Time		2.7V to 5.5V	500	—	ns
			4.5V to 5.5V	250	—	ns
t _{CS}	Minimum CS LOW Time		2.7V to 5.5V	250	—	ns
			4.5V to 5.5V	250	—	ns
t _{CSS}	CS Setup Time	Relative to SK	2.7V to 5.5V	100	—	ns
			4.5V to 5.5V	50	—	ns
t _{DIS}	Din Setup Time	Relative to SK	2.7V to 5.5V	100	—	ns
			4.5V to 5.5V	100	—	ns
t _{CSH}	CS Hold Time	Relative to SK	2.7V to 5.5V	0	—	ns
			4.5V to 5.5V	0	—	ns
t _{DIH}	Din Hold Time	Relative to SK	2.7V to 5.5V	100	—	ns
			4.5V to 5.5V	100	—	ns
t _{PD1}	Output Delay to "1"	AC Test	2.7V to 5.5V	—	400	ns
			4.5V to 5.5V	—	250	ns
t _{PD0}	Output Delay to "0"	AC Test	2.7V to 5.5V	—	400	ns
			4.5V to 5.5V	—	250	ns
t _{SV}	CS to Status Valid	AC Test	2.7V to 5.5V	—	250	ns
			4.5V to 5.5V	—	250	ns
t _{DF}	CS to Dout in 3-state	AC Test, CS=VIL	2.7V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t _{WP}	Write Cycle Time		2.7V to 5.5V	—	10	ms
			4.5V to 5.5V	—	5	ms

Notes:1. C_L = 100pF

AC WAVEFORMS

FIGURE 2. SYNCHRONOUS DATA TIMING

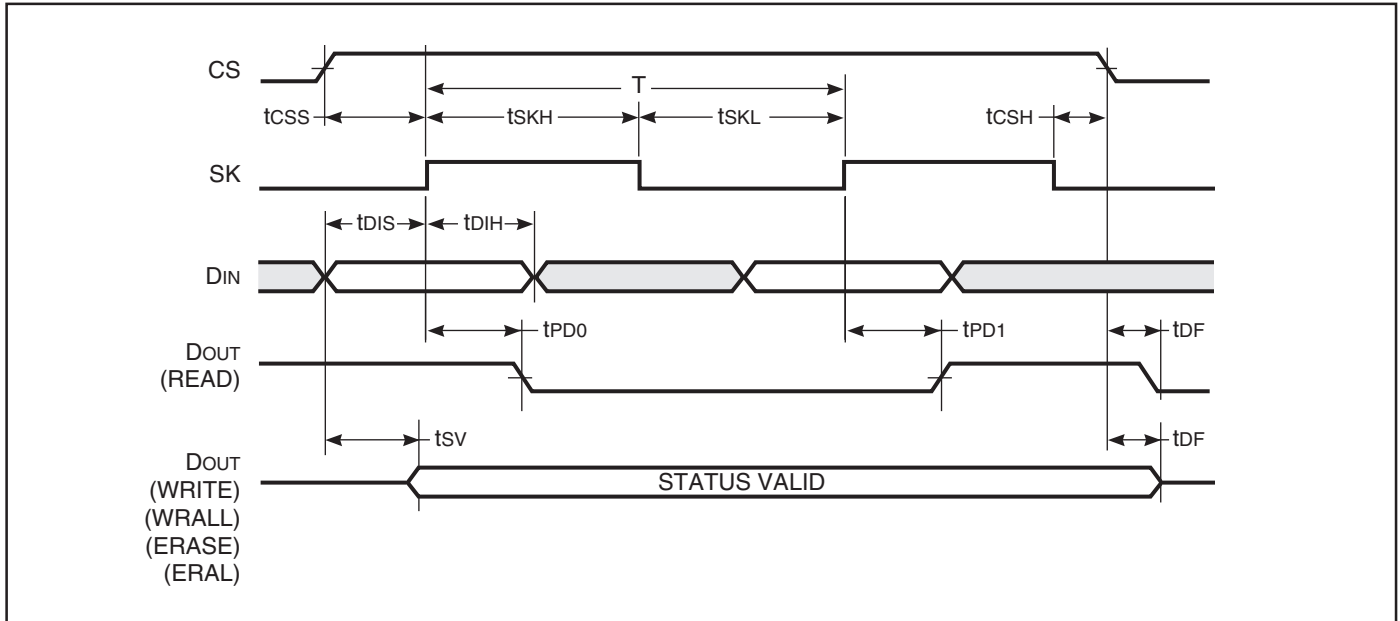
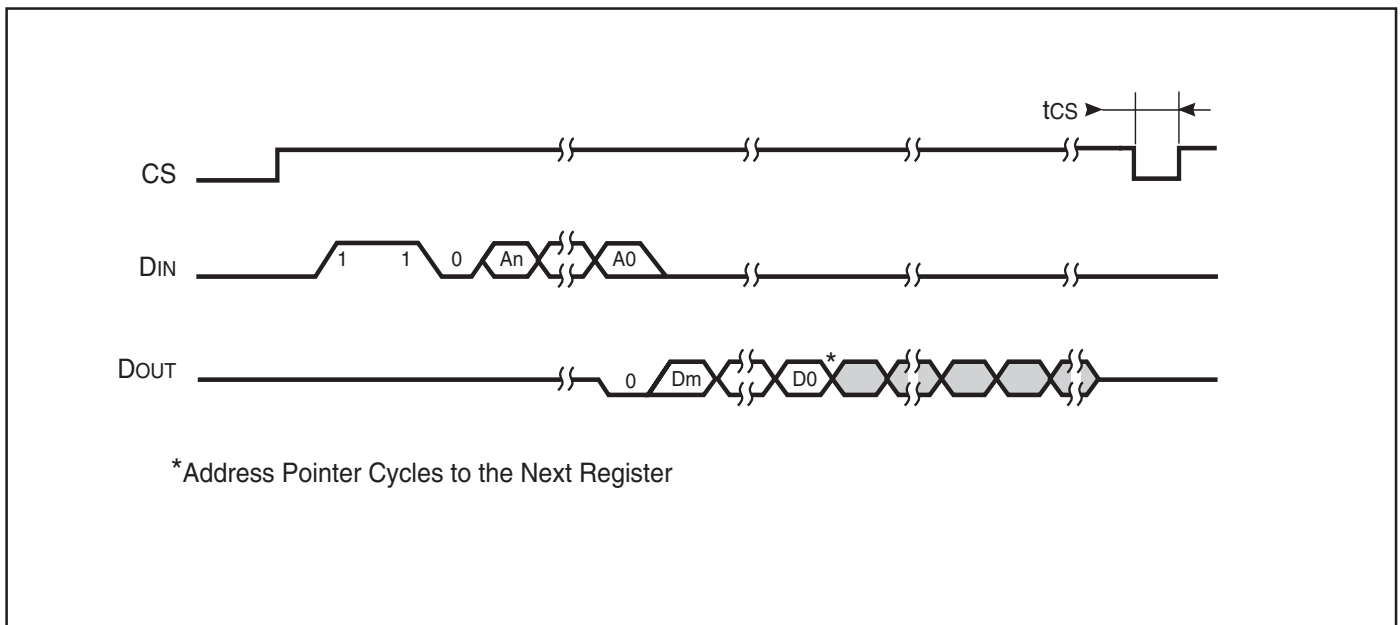


FIGURE 3. READ CYCLE TIMING



Notes:

To determine address bits A_n - A_0 and data bits D_m - D_0 , see Instruction Set.

AC WAVEFORMS

FIGURE 4. WRITE ENABLE (WEN) TIMING

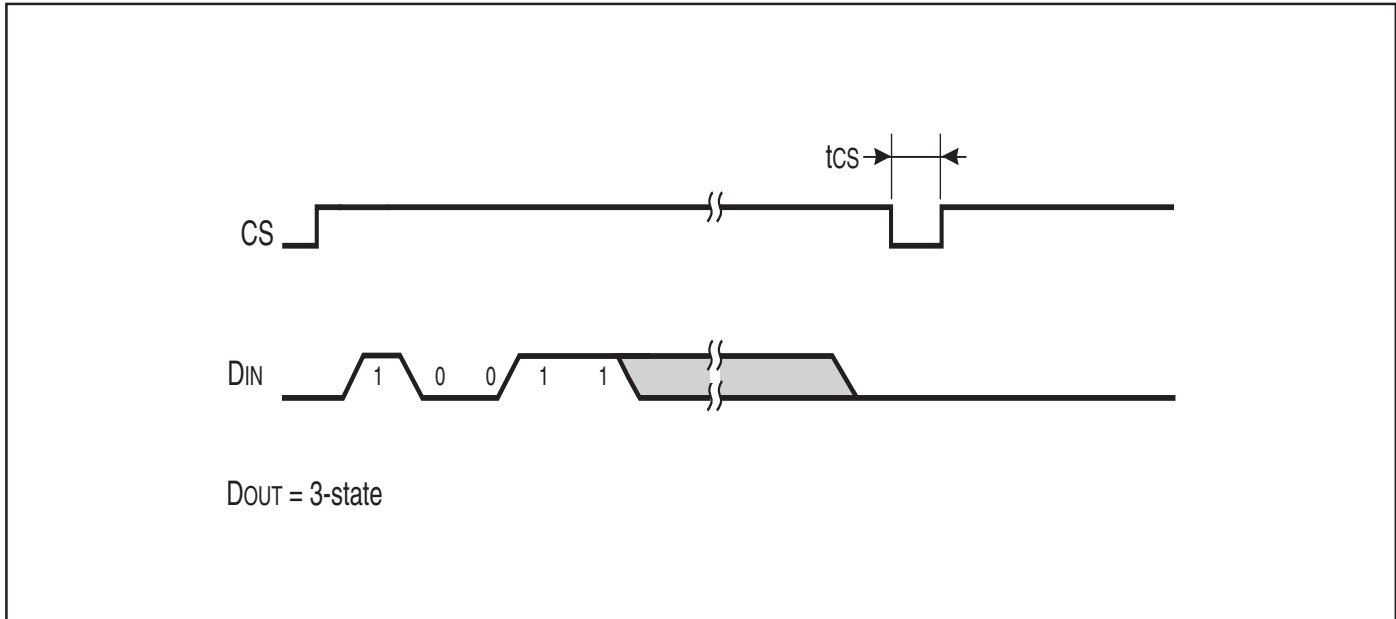
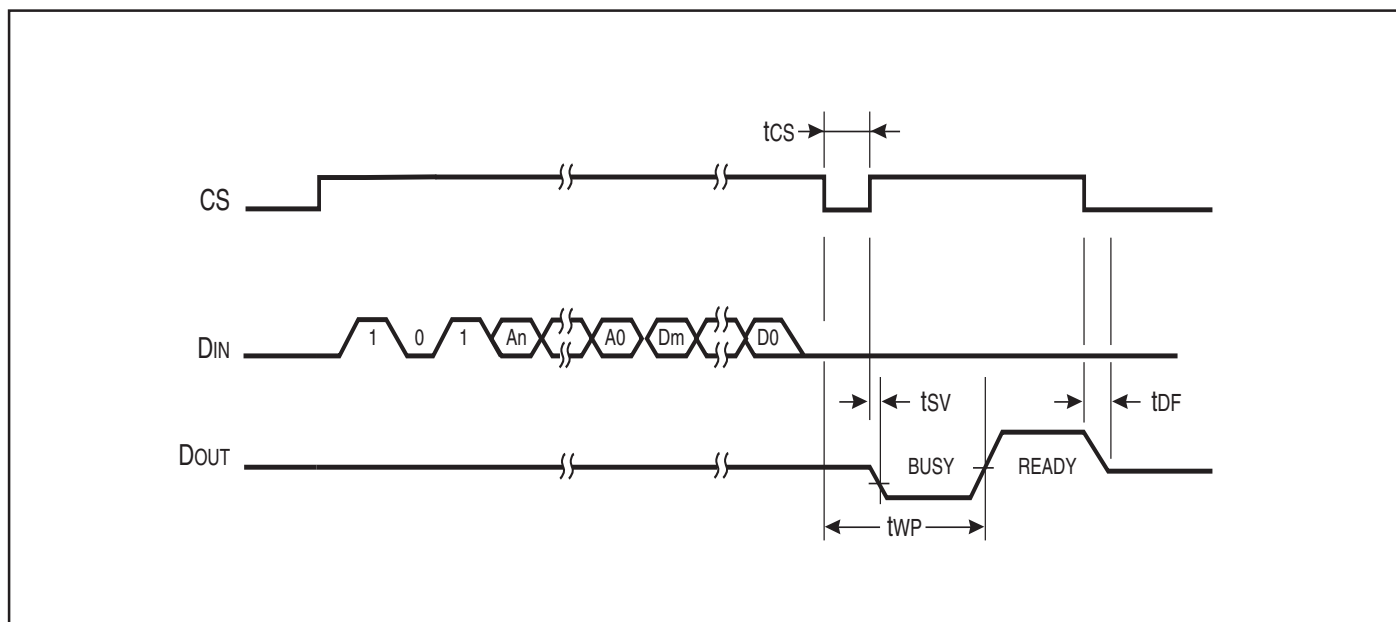


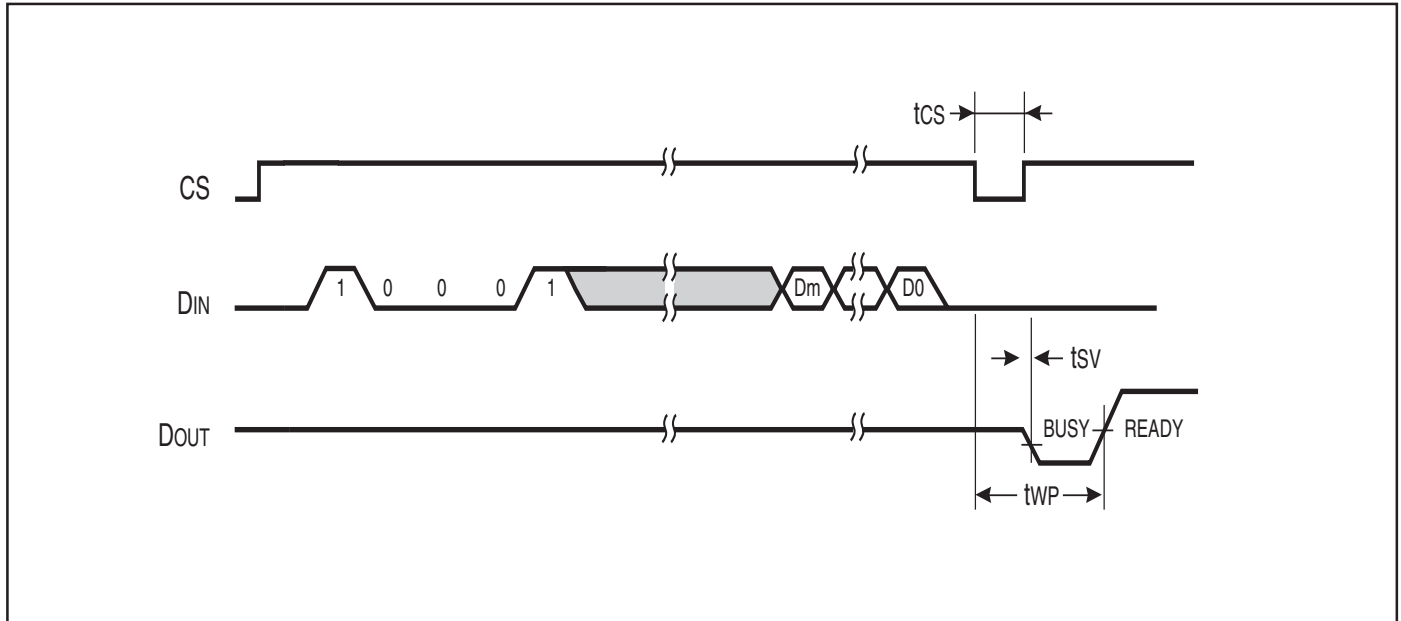
FIGURE 5. WRITE (WRITE) CYCLE TIMING

**Notes:**

1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine address bits A_n - A_0 and data bits D_m - D_0 , see Instruction Set.

AC WAVEFORMS

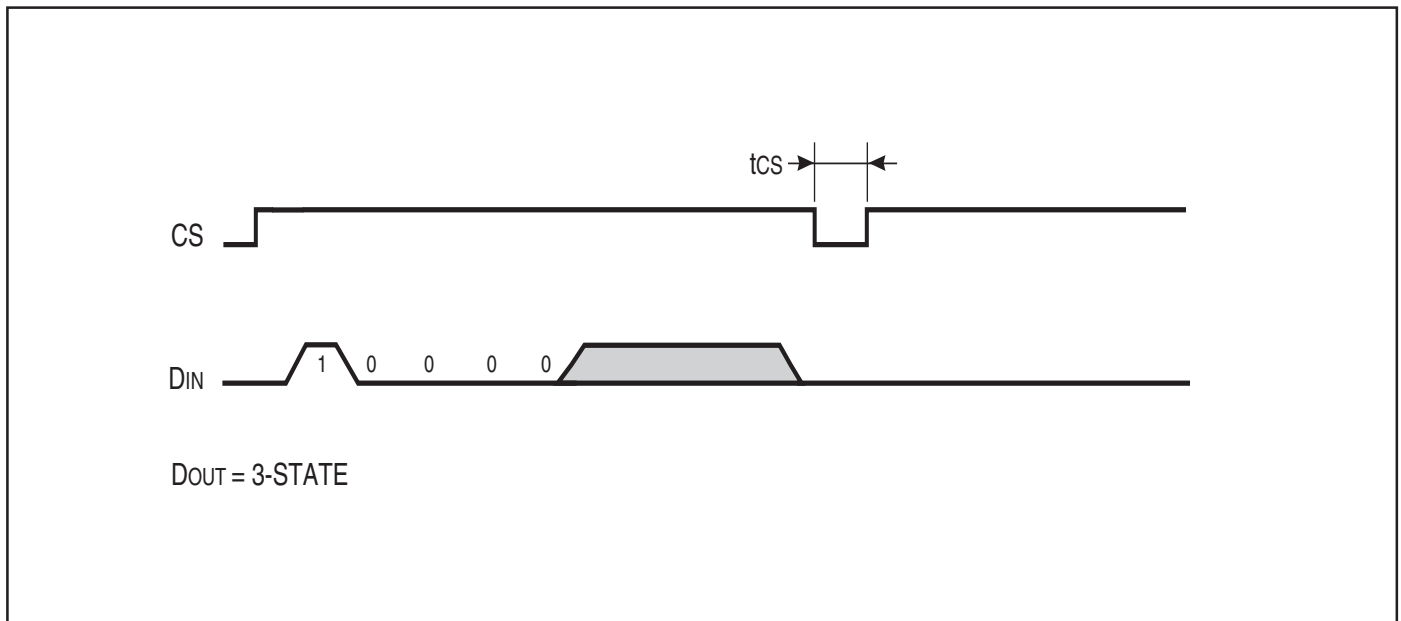
FIGURE 6. WRITE ALL (WRALL) TIMING



Notes:

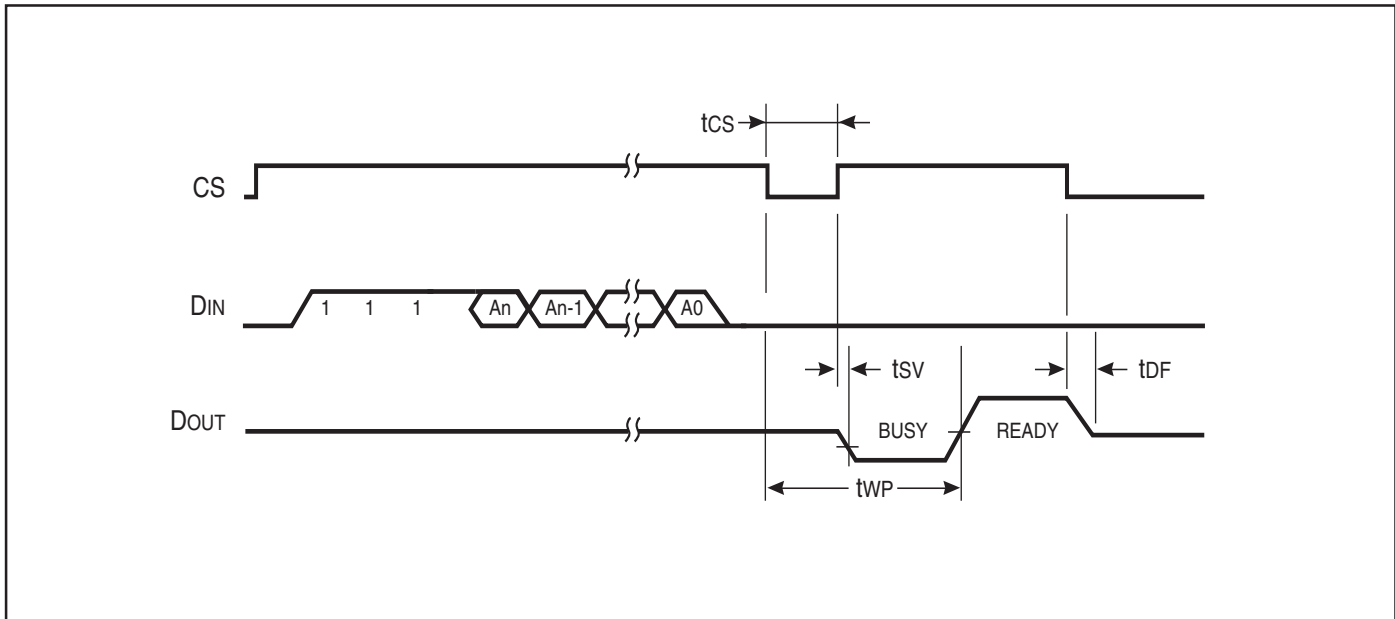
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in $\overline{\text{BUSY}}$ status (DOUT indicates $\overline{\text{BUSY}}$ status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits Dm-D0, see Instruction Set.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



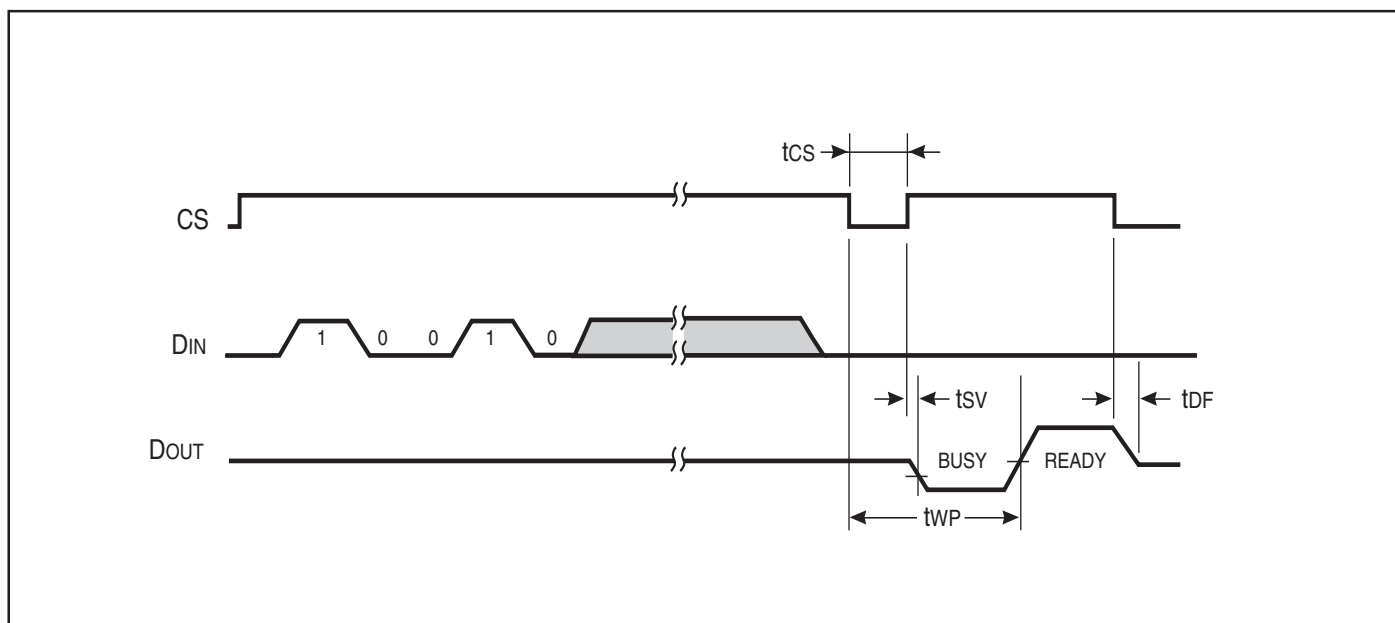
AC WAVEFORMS

FIGURE 8. ERASE (REGISTER ERASE) CYCLE TIMING

**Notes:**

To determine data bits $A_n - A_0$, see Instruction Set.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

**Note for Figures 8 and 9:**

After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (Dout indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.

ORDERING INFORMATION**Commercial: 0°C to +70°C**

Speed	Voltage Range	Order Part No.	Package
1Mhz *	2.5V to 5.5V	IS93C46B-3P	300-mil Plastic DIP
		IS93C46B-3G	SOIC (rotated) JEDEC
		IS93C46B-3GR	SOIC JEDEC
		IS93C46B-3Z	169-mil TSSOP

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

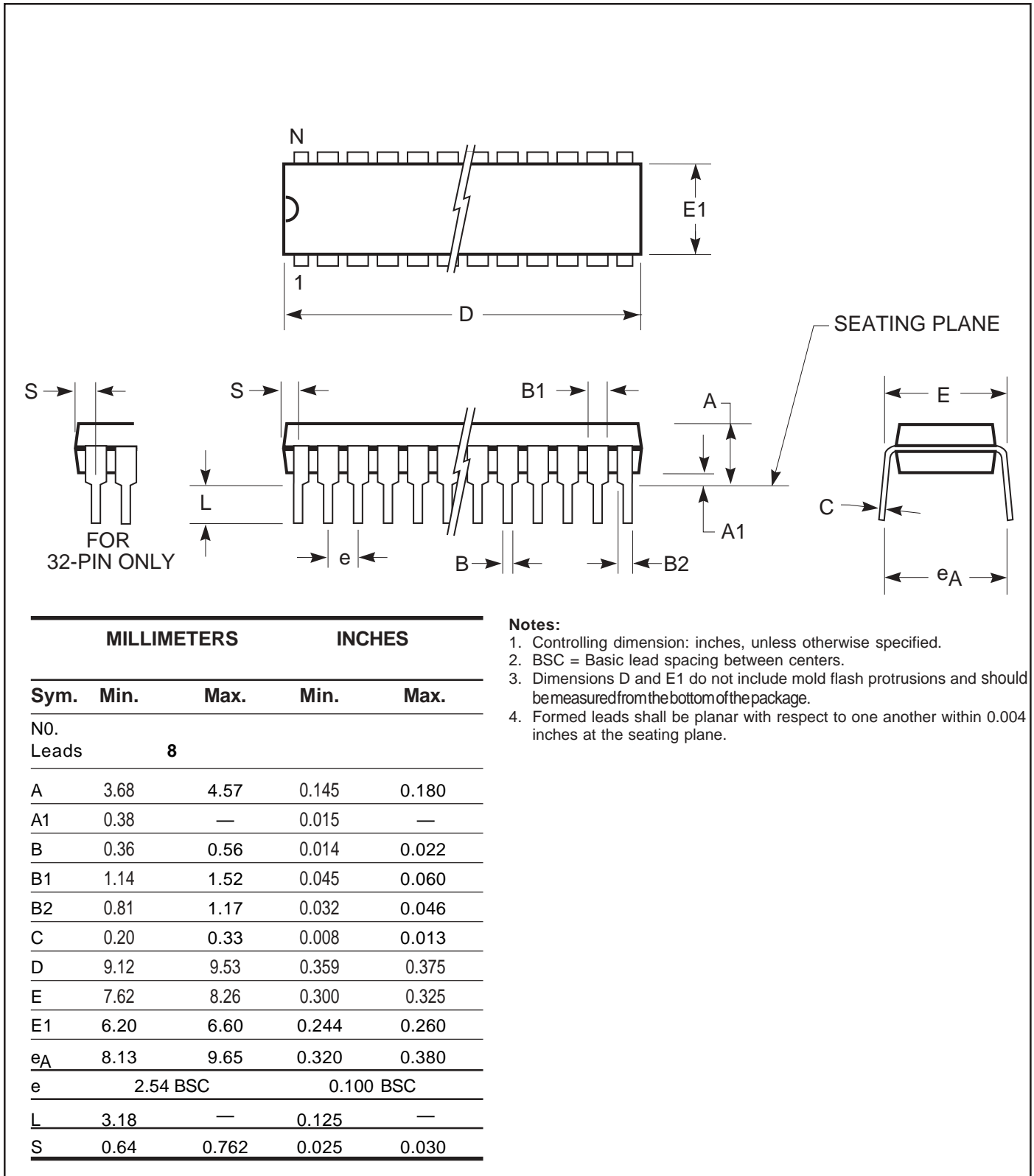
Speed	Voltage Range	Order Part No.	Package
1Mhz *	2.5V to 5.5V	IS93C46B-3PI	300-mil Plastic DIP
		IS93C46B-3PLI	300-mil Plastic DIP, Lead-free
		IS93C46B-3GI	SOIC (rotated) JEDEC
		IS93C46B-3GRI	SOIC JEDEC
		IS93C46B-3ZI	169-mil TSSOP

* The specification allows for higher speed. Please see the AC Characteristics for more information.

PACKAGING INFORMATION



300-mil Plastic DIP
Package Code: N,P



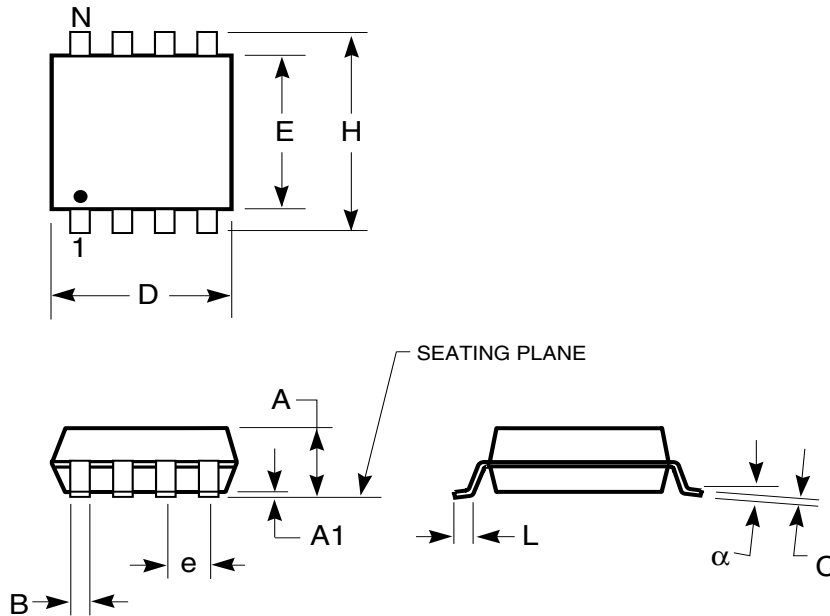
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Rev. D
 02/14/03

PACKAGING INFORMATION

150-mil Plastic SOP
 Package Code: G, GR



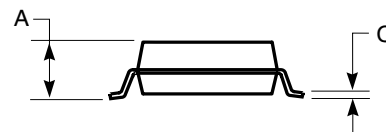
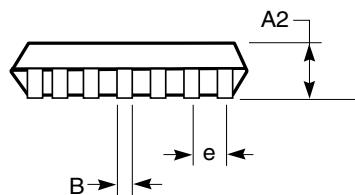
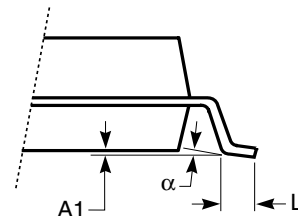
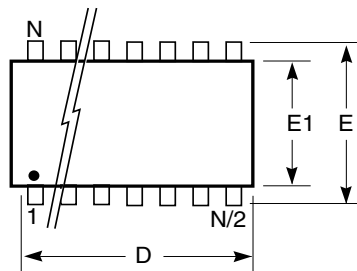
150-mil Plastic SOP (G, GR)				
Symbol	Min	Max	Min	Max
Ref. Std.	Inches		mm	
No. Leads	8		8	
A	—	0.068	—	1.73
A1	0.004	0.009	0.1	0.23
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.189	0.197	4.8	5
E	0.150	0.157	3.81	3.99
H	0.228	0.245	5.79	6.22
e	0.050 BSC		1.27 BSC	
L	0.020	0.035	0.51	0.89

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Thin Shrink Small Outline TSSOP
 Package Code: Z (8 pin, 14 pin)



TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	8			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E1	4.30	4.50	0.169	0.177
E	6.40	BSC	0.252	BSC
e	0.65	BSC	0.026	BSC
L	0.45	0.75	0.018	0.030
α	—	8°	—	8°

TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	14			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E1	4.30	4.50	0.170	0.177
E	6.40	BSC	0.252	BSC
e	0.65	BSC	0.026	BSC
L	0.45	0.75	0.0177	0.0295
α	—	8°	—	8°

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