National Semiconductor

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# LM5041
# Cascaded PWM Controller

## General Description

The LM5041 PWM controller contains all of the features necessary to implement either current-fed or voltage-fed push-pull or bridge power converters. These "Cascaded" topologies are well suited for multiple output and higher power applications. The LM5041's four control outputs include: the buck stage controls (HD and LD) and the push-pull control outputs (PUSH and PULL). Push-pull outputs are driven at 50% nominal duty cycle at one half of the switching frequency of the buck stage and can be configured for either a guaranteed overlap time (for current-fed applications) or a guaranteed both-off time (for voltage-fed applications). Push-pull stage MOSFETs can be driven directly from the internal gate drivers while the buck stage requires an external driver such as the LM5102. The LM5041 includes a high-voltage start-up regulator that operates over a wide input range of 15V to 100V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 1 MHz and total propagation delays of less than 100ns. Additional features include: line Under-Voltage Lockout (UVLO), soft-start, an error amplifier, precision voltage reference, and thermal shutdown.

## Features

- Internal Start-up Bias Regulator
- Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis
- Current Mode Control
- Internal Error Amplifier with Reference
- Dual Mode Over-Current Protection
- Leading Edge Blanking
- Programmable Push-Pull Overlap or Dead Time
- Internal 1.5A Push-Pull Gate Drivers
- Programmable Soft-start
- Programmable Oscillator with Sync Capability
- Precision Reference
- Thermal Shutdown

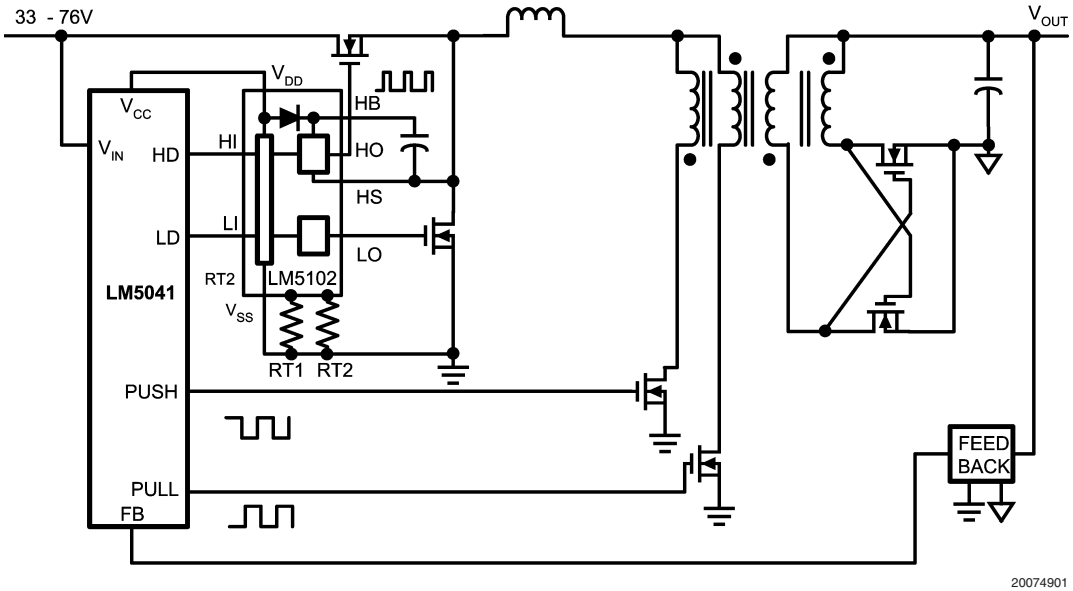
## Applications

- Telecommunication Power Converters
- Industrial Power Converters
- Multi-Output Power Converters
- +42V Automotive Systems

## Packages

- TSSOP-16
- LLP-16 (5x5 mm) Thermally Enhanced

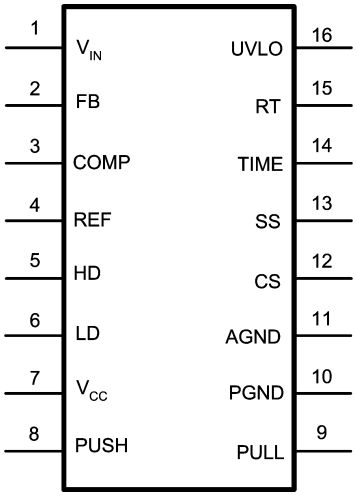
## Typical Application Circuit




**Simplified Cascaded Push-Pull Power Converter**

## Connection Diagram




**16-Lead TSSOP, LLP**

## Ordering Information

| Order Number | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|
| LM5041MTC | TSSOP-16 | MTC-16 | 92 Units per anti-static tube |
| LM5041MTCX | TSSOP-16 | MTC-16 | 2500 Units on Tape and Reel |
| LM5041SD | LLP-16 | SDA-16A | 1000 Units on Tape and Reel |
| LM5041SDX | LLP-16 | SDA-16A | 4500 Units on Tape and Reel |

## Pin Description

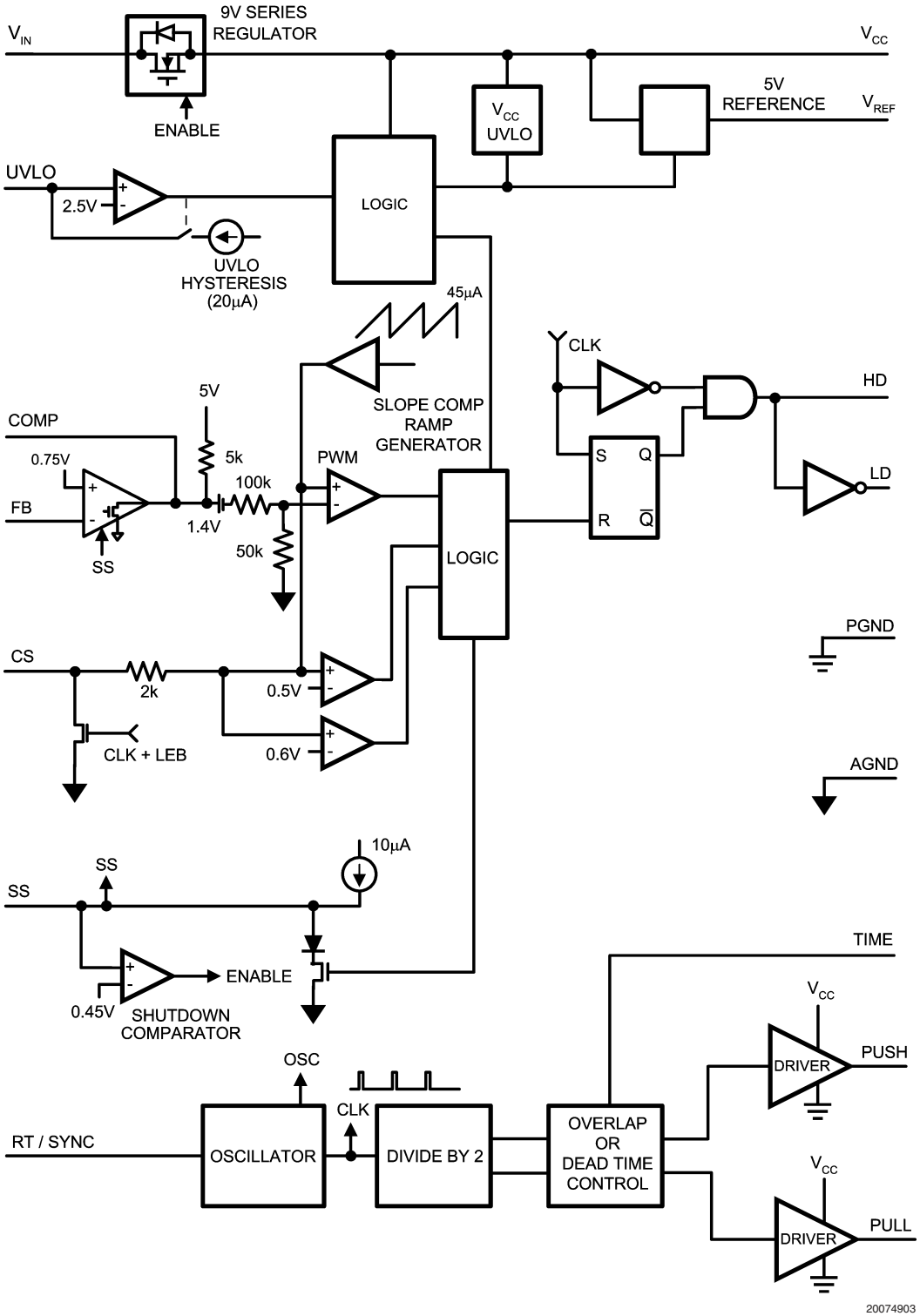
| PIN | NAME | DESCRIPTION | APPLICATION INFORMATION |
|---|---|---|---|
| 1 | $V_{IN}$ | Source Input Voltage | Input to start-up regulator. Input range 15V to 100V. |
| 2 | FB | Feedback Signal | Inverting input for the internal error amplifier. The non-inverting input is connected to a 0.75V reference. |
| 3 | COMP | Output of the Internal Error Amplifier | There is an internal 5kΩ resistor pull-up on this pin. The error amplifier provides an active sink. |
| 4 | REF | Precision 5 volt reference output | Maximum output current: 10mA. Locally decouple with a 0.1µF capacitor. Reference stays low until the line UV and the $V_{CC}$ UV are satisfied. |
| 5 | HD | Main Buck PWM control output | Buck switch PWM control output. The maximum duty cycle clamp for this output corresponds to an off time of typically 240ns per cycle. The LM5101 or LM5102 Buck stage gate driver can be used to level shift and drive the Buck switch. |
| 6 | LD | Sync Switch control output | Sync Switch control output. Inversion of HD output. The LM5101 or LM5102 lower drive can be used to drive the synchronous rectifier switch. |
| 7 | $V_{CC}$ | Output from the internal high voltage start-up regulator. Regulated to 9 volts. | If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, reducing the IC power dissipation. |
| 8 | PUSH | Output of the push-pull drivers | Output of the push-pull gate driver. Output capability of 1.5A peak . |

## Pin Description (Continued)

| PIN | NAME | DESCRIPTION | APPLICATION INFORMATION |
|---|---|---|---|
| 9 | PULL | Output of the push-pull drivers | Output of the push-pull gate driver. Output capability of 1.5A peak. |
| 10 | PGND | Power ground | Connect directly to analog ground. |
| 11 | AGND | Analog ground | Connect directly to power ground. |
| 12 | CS | Current sense input | Current sense input to the PWM comparator (CM control). There is a 50ns leading edge blanking on this pin. Using separate dedicated comparators, if CS exceeds 0.5V the outputs will go into cycle by cycle current limit. If CS exceeds 0.6V the outputs will be disabled and a soft-start commenced. |
| 13 | SS | Soft-start control | An external capacitor and an internal 10uA current source, set the soft-start ramp. The controller will enter a low power state if the SS pin is below the shutdown threshold of 0.45V |
| 14 | TIME | Push-Pull overlap and dead time control | An external resistor ($R_{SET}$) sets the overlap time or dead time for the push-pull outputs. A resistor connected between TIME and GND produces overlap. A resistor connected between TIME and REF produces dead time. |
| 15 | RT / SYNC | Oscillator timing resistor pin and sync | An external resistor sets the oscillator frequency. This pin will also accept an external oscillator. |
| 16 | UVLO | Line Under-Voltage Shutdown | An external divider from the power converter source sets the shutdown levels. Threshold of operation equals 2.5V. Hysteresis is set by a switched internal current source (20µA). |
| LLP DAP | SUB | Die substrate | The exposed die attach pad on the LLP package should be connected to a PCB thermal pad at ground potential. For additional information on using National Semiconductor's No Pull Back LLP package, please refer to LLP Application Note AN-1187. |

## Block Diagram

**Simplified Block Diagram**



## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$ to GND | 100V |
| $V_{CC}$ to GND | 16V |
| All Other Inputs to GND | -0.3 to 7V |
| Junction Temperature | 150˚C |
| Storage Temperature Range | -65˚C to +150˚C |

| | | |
|---|---|---|
| ESD Rating | 2 kV | |
| Lead temperature (Note 2) | | |
| Wave | 4 seconds | 260˚C |
| Infrared | 10 seconds | 240˚C |
| Vapor Phase | 75 seconds | 219˚C |

## Operating Ratings (Note 1)

| | |
|---|---|
| $V_{IN}$ | 15 to 90V |
| Junction Temperature | -40˚C to +125˚C |

## Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 26.7kΩ, $R_{SET}$ = 20kΩ) unless otherwise stated (Note 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Startup Regulator** | | | | | | |
| $V_{CC}$ Reg | $V_{CC}$ Regulation | open circuit | **8.7** | 9 | **9.3** | V |
| | $V_{CC}$ Current Limit | (Note 4) | **15** | 25 | | mA |
| I-$V_{IN}$ | Startup Regulator Leakage (external Vcc Supply) | $V_{IN}$ = 100V | | 145 | **500** | µA |
| | Shutdown Current (Iin) | UVLO = 0V, $V_{CC}$ = open | | 350 | **450** | µA |
| **$V_{CC}$ Supply** | | | | | | |
| | $V_{CC}$ Under-voltage Lockout Voltage (positive going $V_{cc}$) | | **$V_{CC}$ Reg - 400mV** | $V_{CC}$ Reg - 275mV | | V |
| | $V_{CC}$ Under-voltage Hysteresis | | **1.7** | 2.1 | **2.6** | V |
| | Supply Current ($I_{CC}$) | $C_L$ = 0 | | 3 | **4** | mA |
| **Error Amplifier** | | | | | | |
| GBW | Gain Bandwidth | | | 3 | | MHz |
| | DC Gain | | | 80 | | dB |
| | Input Voltage | $V_{FB}$ = COMP | **0.735** | 0.75 | **0.765** | V |
| | COMP Sink Capability | $V_{FB}$ = 1.5V, COMP= 1V | **4** | 8 | | mA |
| **Reference Supply** | | | | | | |
| $V_{REF}$ | Ref Voltage | $I_{REF}$ = 0 mA | **4.85** | 5 | **5.15** | V |
| | Ref Voltage Regulation | $I_{REF}$ = 0 to 10mA | | 25 | **50** | mV |
| | Ref Current Limit | | **15** | 20 | | mA |
| **Current Limit** | | | | | | |
| | ILIM Delay to Output | CS Step from 0 to 0.6V Time to Onset of OUT Transition (90%) $C_L$ = 0 | | 40 | | ns |
| | Cycle by Cycle Threshold Voltage | | **0.45** | 0.5 | **0.55** | V |
| | Cycle Skip Threshold Voltage | Resets SS capacitor; auto restart | **0.55** | 0.6 | **0.65** | V |
| | Leading Edge Blanking Time | | | 50 | | ns |
| | CS Sink Current (clocked) | CS = 0.3V | **2** | 5 | | mA |

## Electrical Characteristics (Continued)

Specifications with standard typeface are for $T_J$ = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 26.7kΩ, $R_{SET}$ = 20kΩ) unless otherwise stated (Note 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Soft-Start** | | | | | | |
| | Soft-start Current Source | | **7** | 10 | **13** | µA |
| | Soft-start to COMP Offset | | **0.35** | 0.55 | **0.75** | V |
| | Shutdown Threshold | | **0.25** | 0.5 | **0.75** | V |
| **Oscillator** | | | | | | |
| | Frequency1 (RT = 26.7KΩ) | $T_J$ = 25˚C | 180<br>**175** | 200 | 220<br>**225** | kHz |
| | Frequency2 (RT = 7.87KΩ) | | **515** | 600 | **685** | kHz |
| | Sync threshold | | | 3 | **3.5** | V |
| **PWM Comparator** | | | | | | |
| | Delay to Output | COMP set to 2V<br>CS stepped 0 to 0.4V,<br>Time to onset of OUT transition low | | 25 | | ns |
| | Max Duty Cycle | TS = Oscillator Period | | (Ts-240ns)/Ts) | | % |
| | Min Duty Cycle | COMP = 0V | | | 0 | % |
| | COMP to PWM Comparator Gain | | | 0.32 | | |
| | COMP Open Circuit Voltage | FB = 0V | **4.1** | 4.8 | **5.5** | V |
| | COMP Short Circuit Current | FB = 0V, COMP = 0V | **0.6** | 1 | **1.4** | mA |
| **Slope Compensation** | | | | | | |
| | Slope Comp Amplitude | Delta increase at PWM Comparator to CS | | 110 | | mV |
| **UVLO Shutdown** | | | | | | |
| | Under-voltage Shutdown | | **2.44** | 2.5 | **2.56** | V |
| | Under-voltage Shutdown Hysteresis Current Source | | **16** | 20 | **24** | µA |
| **Buck Stage Outputs** | | | | | | |
| | Output High level | | | 5 ($V_{REF}$) | | V |
| | Output High Saturation | $I_{OUT}$ = 10mA<br>REF = $V_{OUT}$ | | 0.5 | **1** | V |
| | Output Low Saturation | $I_{OUT}$ = −10mA | | 0.5 | **1** | V |
| | Rise Time | $C_L$ = 100pF | | 10 | | ns |
| | Fall Time | $C_L$ = 100pF | | 10 | | ns |
| **Push-Pull Outputs** | | | | | | |
| | Overlap Time | $R_{SET}$ = 20kΩ Connected to GND, 50% to 50% Transitions | **60** | 90 | **120** | ns |
| | Dead Time | $R_{SET}$ = 20kΩ Connected to REF, 50% to 50% Transitions | **65** | 95 | **125** | ns |

## Electrical Characteristics (Continued)

Specifications with standard typeface are for $T_J$ = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 26.7kΩ, $R_{SET}$ = 20kΩ) unless otherwise stated (Note 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Output High Saturation | $I_{OUT}$ = 50mA<br>$V_{CC}$ - $V_{OUT}$ | | 0.25 | **0.5** | V |
| | Output Low Saturation | $I_{OUT}$ = 100mA | | 0.5 | **1** | V |
| | Rise Time | $C_L$ = 1nF | | 20 | | ns |
| | Fall Time | $C_L$ = 1nF | | 20 | | ns |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Temp. | | | 165 | | ˚C |
| | Thermal Shutdown Hysteresis | | | 25 | | ˚C |
| **Thermal Resistance** | | | | | | |
| $\theta_{JA}$ | Junction to Ambient | MTC Package | | 125 | | ˚C/W |
| | | SDA Package | | 32 | | ˚C/W |

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

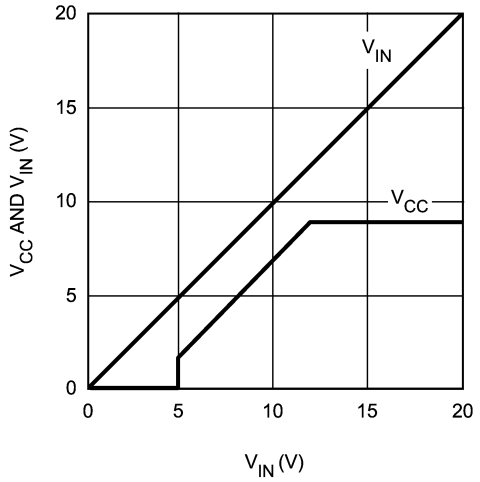
**Note 2:** For detailed information on soldering plastic TSSOP and LLP packages, refer to the Packaging Data Book available from National Semiconductor Corporation.

**Note 3:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with $T_A = T_J$ = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 4:** Device thermal limitations may limit usable range.

## Typical Performance Characteristics

**$V_{CC}$ and $V_{IN}$ vs $V_{IN}$**

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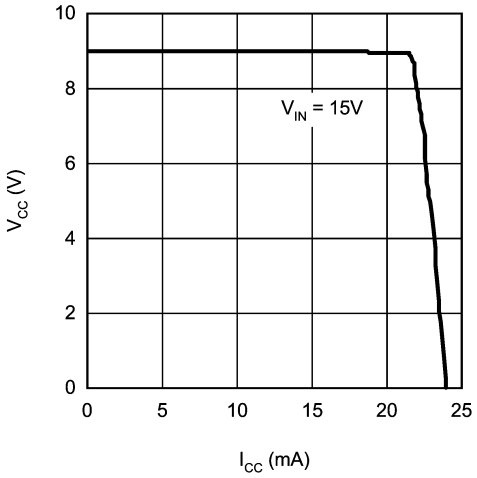
**$V_{CC}$ vs $I_{CC}$**

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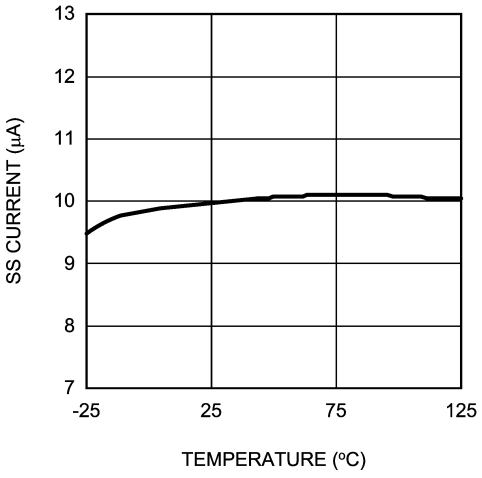
**SS Pin Current vs Temp**

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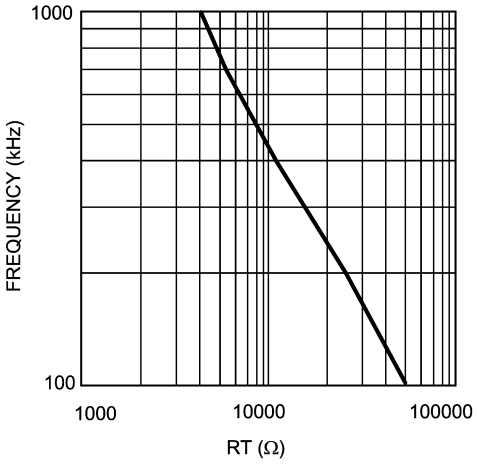
**Frequency vs RT**

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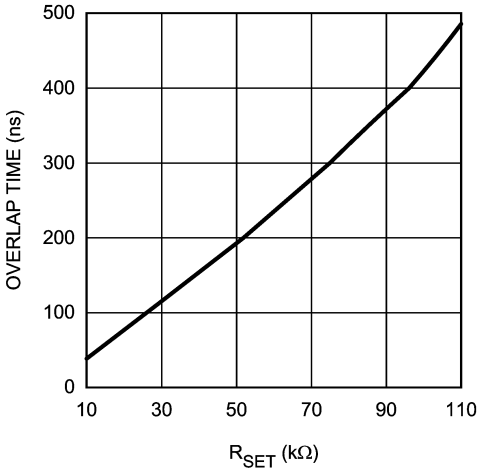
**Overlap Time vs $R_{SET}$**

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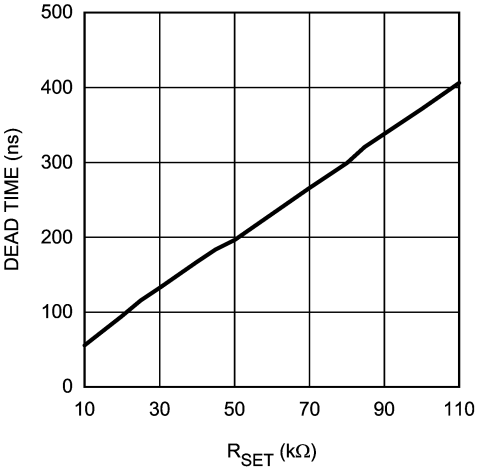
**Dead Time vs $R_{SET}$**

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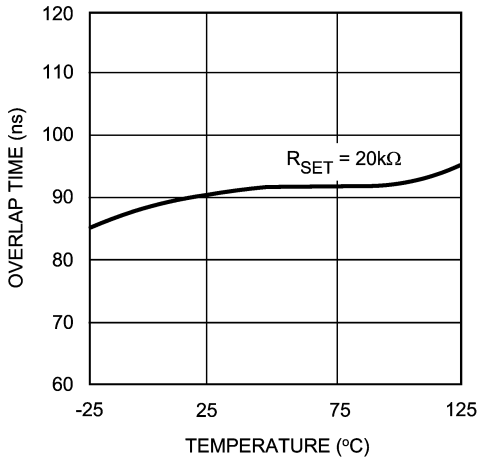
## Typical Performance Characteristics (Continued)

**Overlap Time vs Temp**

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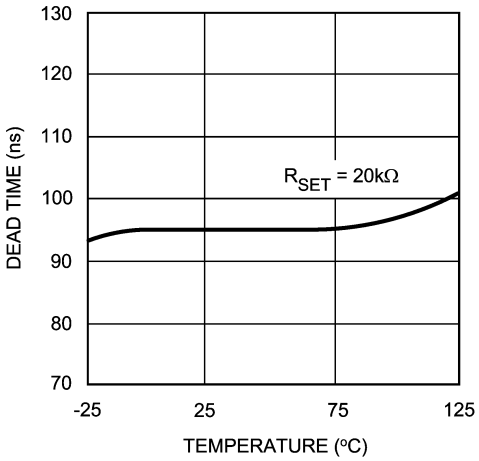
**Dead Time vs Temp**

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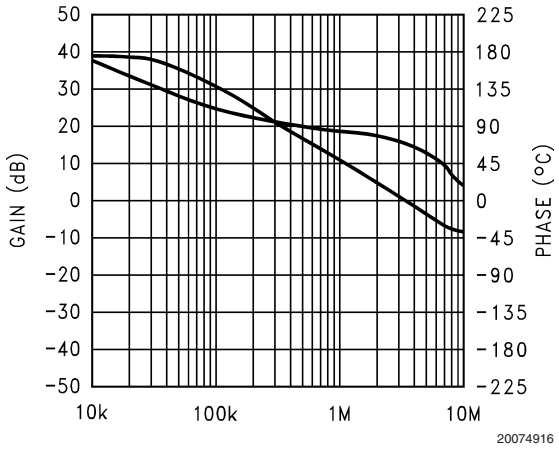
**Error Amplifier Gain Phase**

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## Detailed Operating Description

The LM5041 PWM controller contains all of the features necessary to implement either current-fed or voltage-fed push-pull or bridge power converters. These "Cascaded" topologies are well suited for multiple output and higher power applications. The LM5041's four control outputs include: the buck stage controls (HD and LD) and the push-pull control outputs (PUSH and PULL). Push-pull outputs are driven at 50% nominal duty cycle at one half of the switching frequency of the buck stage and can be configured for either a guaranteed overlap time (for current-fed applications) or a guaranteed both-off time (for voltage-fed applications). Push-pull stage MOSFETs can be driven directly from the internal gate drivers while the buck stage requires an external driver such as the LM5102. The LM5041 includes a high-voltage start-up regulator that operates over a wide input range of 15V to 100V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 1 MHz and total propagation delays of less than 100ns. Additional features include: line Under-Voltage Lockout (UVLO), soft-start, an error amplifier, precision voltage reference, and thermal shutdown.

## High Voltage Start-Up Regulator

The LM5041 contains an internal high-voltage start-up regulator, thus the input pin (Vin) can be connected directly to the line voltage. The regulator output is internally current limited to 15mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the Vcc pin. The recommended capacitance range for the Vcc regulator is 0.1uF to 100uF. When the voltage on the Vcc pin reaches the regulation point of 9V and the internal voltage reference (REF) reaches its regulation point of 5V, the controller outputs are enabled. The Buck stage outputs will remain enabled until Vcc falls below 7V or the line Under-Voltage Lockout detector indicates that Vin is out of range. The push-pull outputs continue switching until the REF pin voltage falls below approximately 3V. In typical applications, an auxiliary transformer winding is connected through a diode to the Vcc pin. This winding must raise the Vcc voltage above 9.3V to shut off the internal start-up regulator. Powering $V_{CC}$ from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The recommended capacitance range for the Vref regulator output is 0.1uF to 10uF.

The external $V_{CC}$ capacitor must be sized such that the capacitor maintains a $V_{CC}$ voltage greater than 7V during the initial start-up. During a fault mode when the converter auxiliary winding is inactive, external current draw on the $V_{CC}$ line should be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the $V_{CC}$ and the $V_{IN}$ pins together and feeding the external bias voltage into the two pins.

## Line Under-Voltage Detector

The LM5041 contains a line Under-Voltage Lockout (UVLO) circuit. An external set-point resistor divider from $V_{IN}$ to ground sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 2.5V when $V_{IN}$ is in the desired operating range. If the Under-Voltage threshold is not met, all functions of the controller are disabled and the controller will enter a low-power state with input current <300µA. ULVO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin falls below the 2.5V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. By shorting the UVLO pin to ground, the converter can be disabled. The controller can also be disabled through the soft-start pin (SS). The controller will enter a low-power off state if the SS pin is forced below the 0.45V shutdown threshold.

## Buck Stage Control Outputs

The LM5041 Buck switch maximum duty cycle clamp ensures that there will be sufficient off time each cycle to recharge the bootstrap capacitor used in the high side gate driver. The Buck switch is guaranteed to be off, and the sync switch on, for at least 250ns per switching cycle. The Buck stage control outputs (LD and HD) are CMOS buffers with logic levels of 0 to 5V.

During any fault state or Under-Voltage off state, the buck stage control outputs will default to HD low and LD high.

## Push-Pull Outputs

The push pull outputs operate continuously at a nominal 50% duty cycle. A distinguishing feature of the LM5041 is the ability to accurately configure either dead time (both-off) or overlap time (both-on) on the complementary push-pull outputs. The overlap/dead time magnitude is controlled by a resistor connected to the TIME pin on the controller. The TIME pin holds one end of the resistor at 2.5V and the other end of the resistor should be connected to either REF for dead time control setting or to GND for overlap control. The polarity of the current in the TIME is detected by the LM5041 The magnitude of the overlap/dead time can be calculated as follows:

Overlap Time (ns) = (3.66 x $R_{SET}$) + 7

Overlap Time in ns, $R_{SET}$ connected to GND, $R_{SET}$ in kΩ

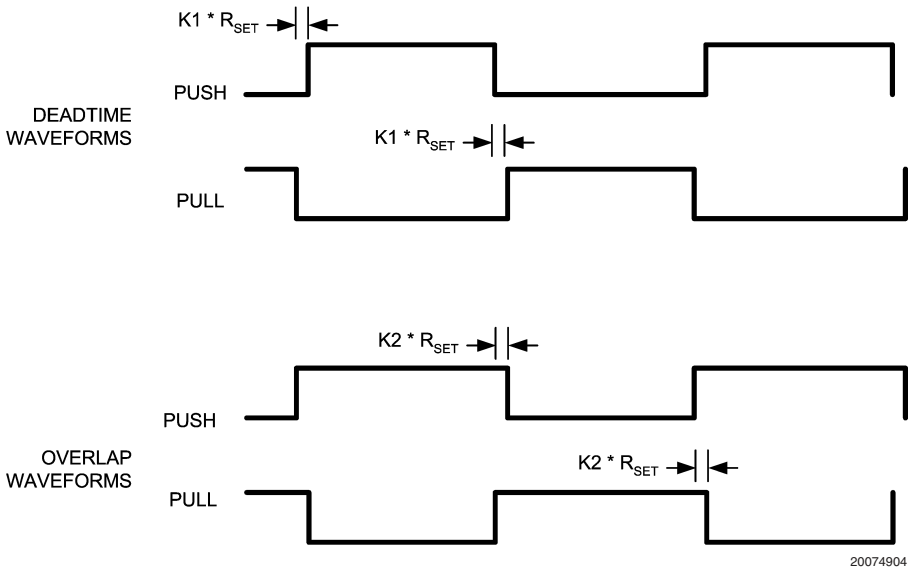
Dead Time (ns) = (3.69 x $R_{SET}$) + 21

Dead Time in ns, $R_{SET}$ connected to REF, $R_{SET}$ in kΩ

Recommended $R_{SET}$ programming range: 10kΩ to 100kΩ

Current-fed designs require a period of overlap to insure there is a continuous path for the buck inductor current. Voltage-fed designs require a period of dead time to insure there is no time when the push-pull transformer acts as a shorted turn to the low impedance sourcing node. The push-pull outputs alternate continuously under all conditions provided REF the voltage is greater than 3V.

## Push-Pull Outputs (Continued)




## PWM Comparator

The PWM comparator compares the slope compensated current ramp signal to the loop error voltage from the internal error amplifier (COMP pin). This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The comparator polarity is such that 0V on the COMP pin will produce zero duty cycle in the buck stage.

## Error Amplifier

An internal high gain wide-bandwidth error amplifier is provided within the LM5041. The amplifier's non-inverting input is tied to a 0.75V reference. The inverting input is connected to the FB pin. In non-isolated applications the power converter output is connected to the FB pin via the voltage setting resistors. Loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amp is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ground. An internal 5kΩ pull-up resistor between the 5V reference and COMP can be used as the pull-up for an opto-coupler in isolated applications.

## Current Limit/Current Sense

The LM5041 contains two levels of over-current protection. If the voltage at the CS pin exceeds 0.5V the present buck stage duty cycle is terminated (cycle by cycle current limit). If the voltage at the CS pin overshoots the 0.5V threshold and exceeds 0.6V, then the controller will terminate the present cycle and fully discharge the soft-start capacitor. A small RC filter located near the controller is recommended to filter current sense signals at the CS pin. An internal MOSFET discharges the external CS pin for an additional 50ns at the beginning of each cycle to reduce the leading edge spike that occurs when the buck stage MOSFET is turned on.

The LM5041 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed close to the device and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. A resistor may be used for current sensing instead of a transformer, located in the push-pull transistor sources, but a low inductance type of resistor is required. When designing with a sense resistor, all of the noise sensitive low power grounds should be connected together around the IC and a single connection should be made to the high current power ground (sense resistor ground point).

The second level current sense threshold is intended to protect the power converter by initiating a low duty cycle hick-up mode when abnormally high currents are sensed. If the second level threshold is reached, the soft-start capacitor will be discharged and a start-up sequence will commence when the soft-start capacitor is determined to be fully discharged. The second level threshold will only be reached when a high dV/dt is present at the current sense pin. The current sense transient must be fast enough to reach the second level threshold before the first threshold detector turns off the buck stage driver. Very high current sense dV/dt can occur with a saturated power inductor or shorted load. Excessive filtering on the CS pin such as an extremely low value current sense resistor or an inductor that does not saturate with excessive loading, may prevent the second level threshold from being reached. If the second level threshold is never exceeded during an overload condition, the first level current sense will continue cycle by cycle limiting and the output characteristic of the converter will be that of a current source. However, a sustained overload current level can cause excessive temperatures in the power train especially the output rectifiers.

## Oscillator and Sync Capability

The LM5041 oscillator is set by a single external resistor connected between the RT pin and GND. To set a desired oscillator frequency (F), the necessary RT resistor can be calculated from:

## Oscillator and Sync Capability

(Continued)

$$RT = \frac{(1/F) - 235 \times 10^{-9}}{182 \times 10^{-12}} \Omega$$

The buck stage will switch at the oscillator frequency and each push-pull output will switch at half the oscillator frequency in a push-pull configuration. The LM5041 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100pF capacitor. A peak voltage level greater than 3V is required for detection of the sync pulse. The sync pulse width should be set in the 15 to 150ns range by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to 2V. The RT resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND).

## Slope Compensation

The PWM comparator compares the current sense signal to the voltage at the COMP pin. The output stage of the internal error amplifier generally drives the COMP pin. At duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed ramp signal (slope compensation) to the current sense ramp, oscillations can be avoided. The LM5041 integrates this slope compensation by buffering the internal oscillator ramp and summing a current ramp generated by the oscillator internally with the current sense signal. Additional slope compensation may be provided by increasing the source impedance of the current sense signal.

## Soft-start and Shutdown

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses and surges. At power on, a 10uA current is sourced out of the soft-start pin (SS) to charge an external capacitor. The capacitor voltage will ramp up slowly and will limit the maximum duty cycle of the buck stage. In the event of a fault as indicated by $V_{CC}$ Under-voltage, line Under-voltage or second level current limit, the output drivers are disabled and the soft-start capacitor is discharged to ground. When the fault condition is no longer present, a soft-start sequence will begin again and buck stage duty cycle will gradually increase as the soft-start capacitor is charged. The SS pin also serves as an enable input. The controller will enter a low power state if the SS pin is forced below the 0.45V threshold.

## Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low-power standby state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

## Typical Application

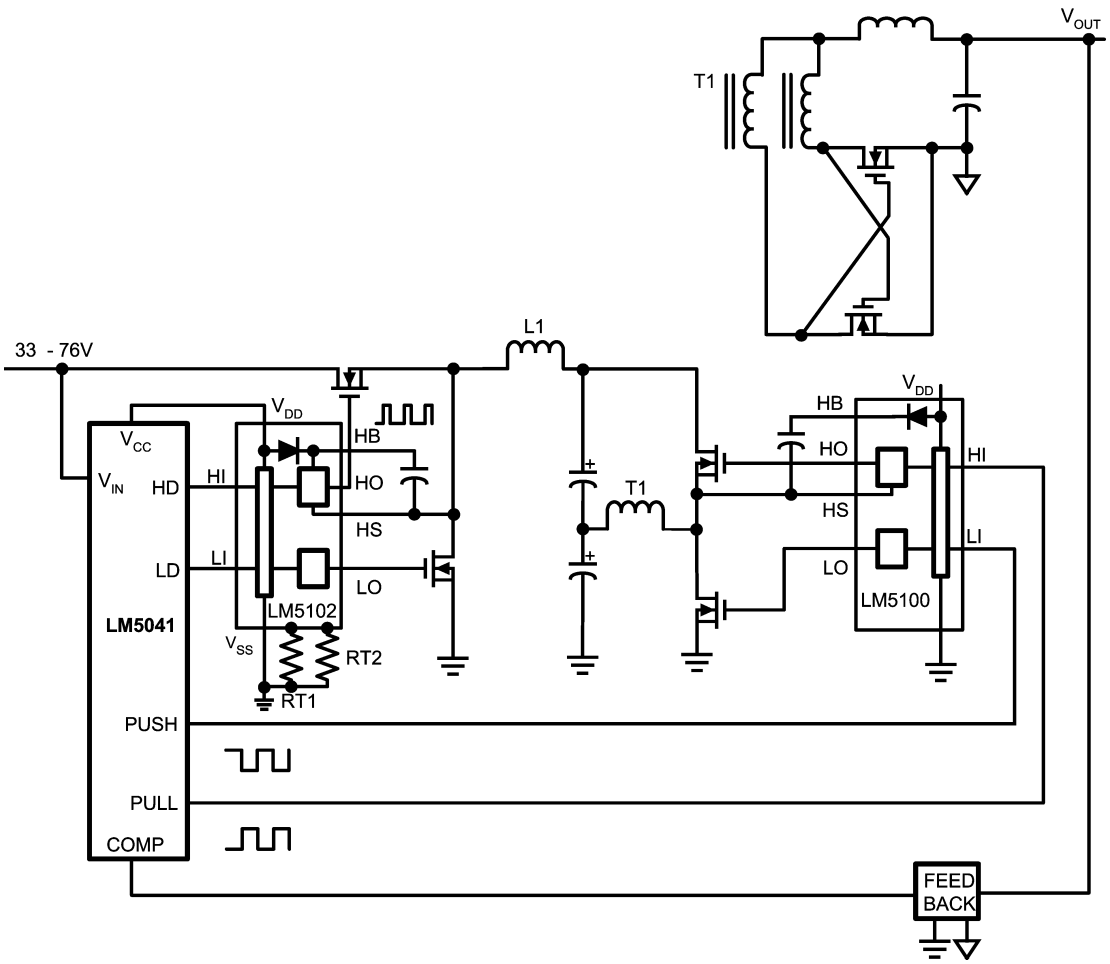
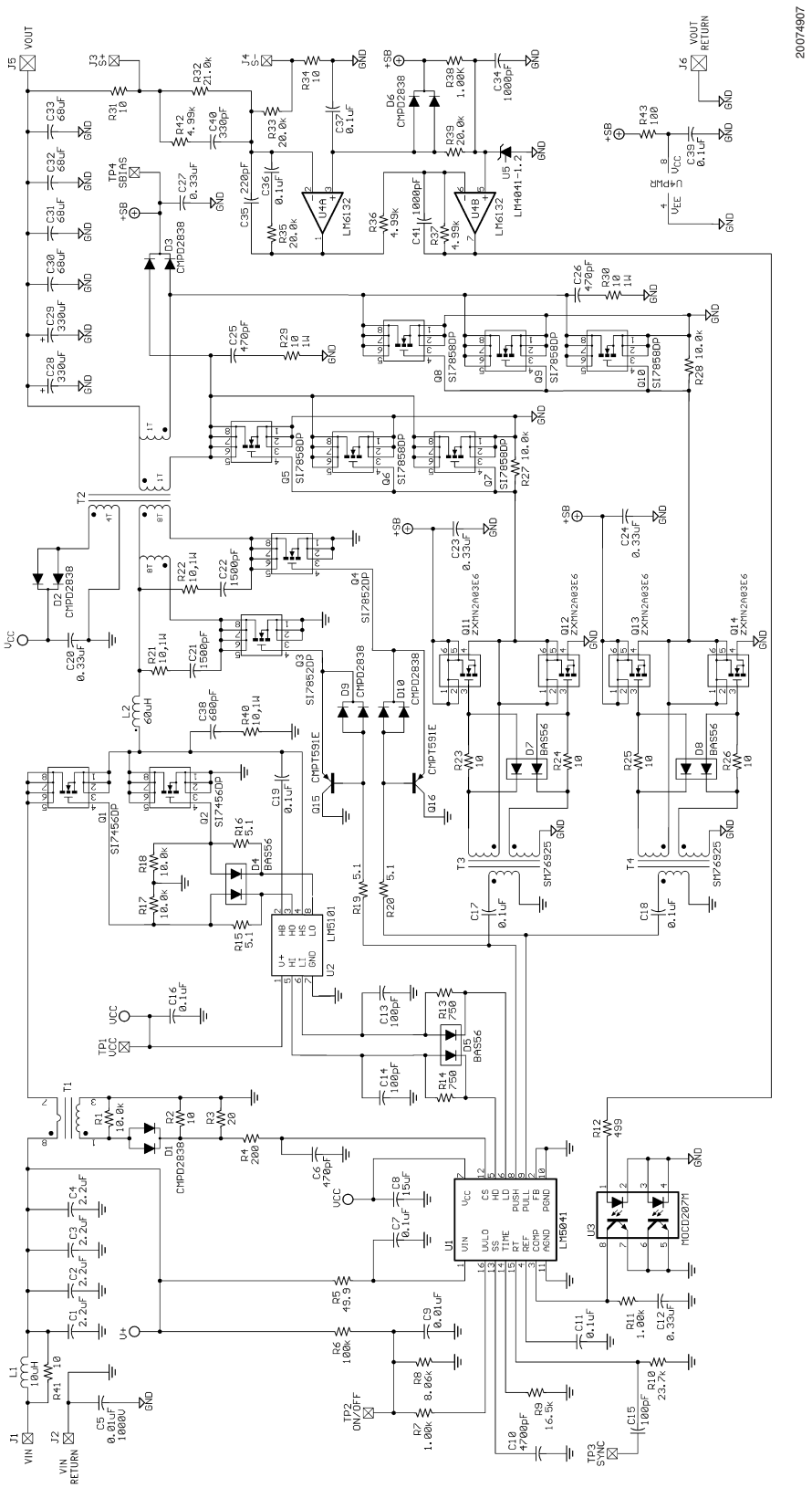
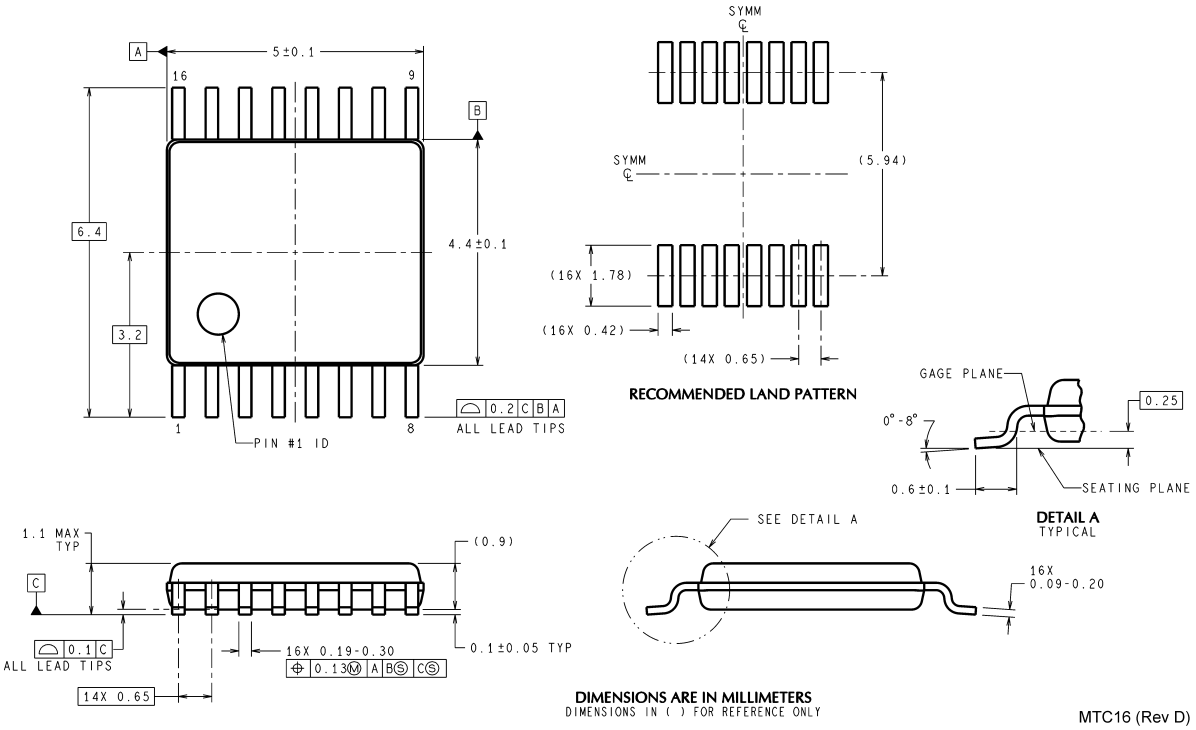



**FIGURE 1. Simplified Cascaded Half-Bridge**

## Application Circuit: Input 35-80V, Output 2.5V, 50A

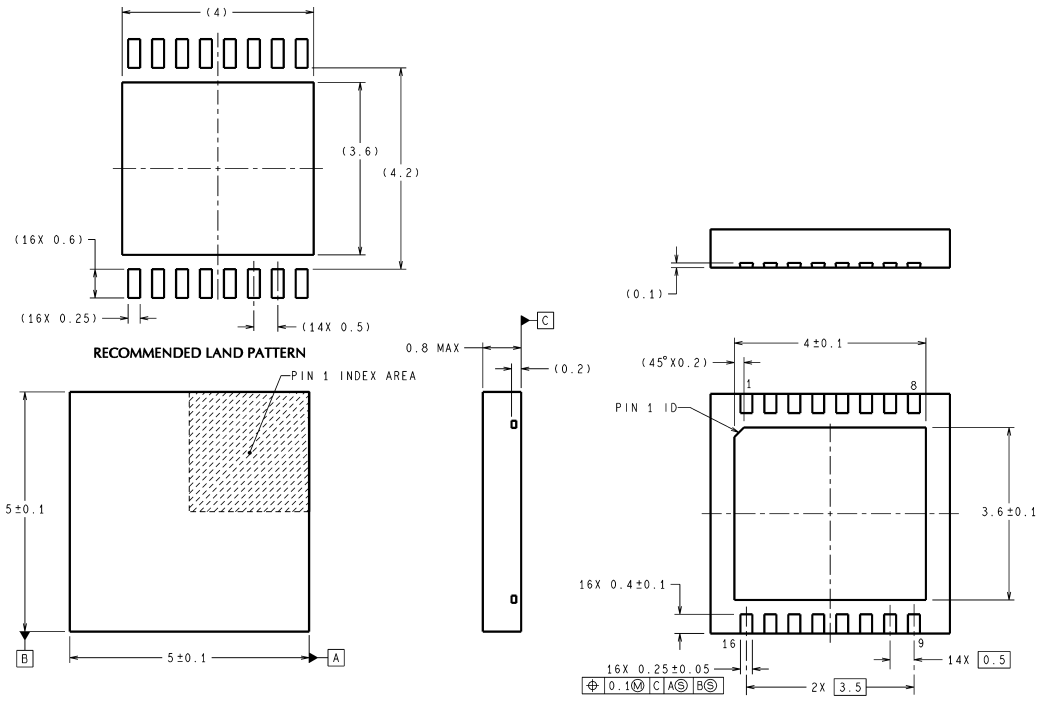


## Physical Dimensions inches (millimeters)
unless otherwise noted




MTC16 (Rev D)

**Molded TSSOP-16**
**NS Package Number MTC16**




SDA16A (Rev A)

**16-Lead LLP Surface Mount Package**
**NS Package Number SDA16A**

## Notes

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