National Semiconductor

April 8, 2008

LM3881
Power Sequencer

General Description

The LM3881 Power Sequencer offers the easiest method to control power up and power down of multiple power supplies (switching or linear regulators). By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in MSOP-8 package, the Power Sequencer contains a precision enable pin and three open drain output flags. Upon enabling the LM3881, the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch conditions. Time delays are defined using an external capacitor and the output flag states can be inverted by the user.

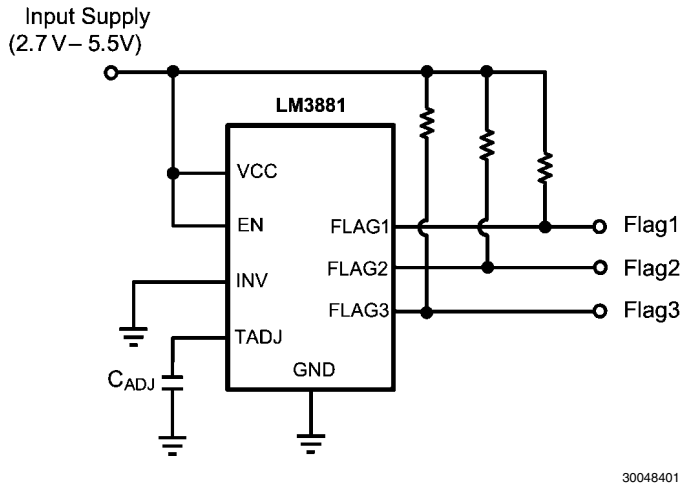
Features

- Easiest method to sequence rails
- Power up and power down control
- Input voltage range of 2.7V to 5.5V
- Small footprint MSOP-8 package
- Low quiescent current of 80 µA
- Output invert feature
- Timing controlled by small value external capacitor

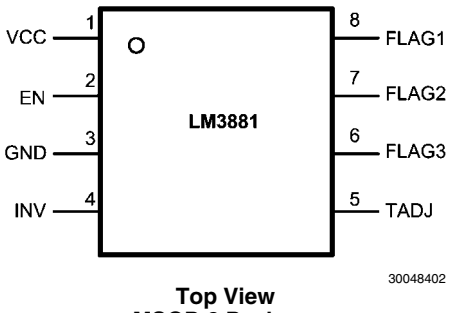
Applications

- Multiple Supply Sequencing
- Microprocessor / Microcontroller Sequencing
- FPGA Sequencing

Typical Application Circuit



Connection Diagram



Top View
MSOP-8 Package

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3881MM	MSOP-8	MUA08A	1000 Units on Tape and Reel
LM3881MMX			3500 Units on Tape and Reel
LM3881MME			250 Units on Tape and Reel

Pin Descriptions

Pin #	Name	Function
1	VCC	Input Supply
2	EN	Precision Enable
3	GND	Ground
4	INV	Output Logic Invert
5	TADJ	Timer Adjust
6	FLAG3	Open Drain Output #3
7	FLAG2	Open Drain Output #2
8	FLAG1	Open Drain Output #1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VCC, EN, INV, TADJ, FLAG1, FLAG2, FLAG3 to GND	-0.3V to +6.0V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 5 sec.)	260°C
Minimum ESD Rating (Note 2)	2 kV

Operating Ratings (Note 1)

VCC to GND	2.7V to 5.5V
EN, INV, TADJ, FLAG1, FLAG2, FLAG3 to GND	-0.3V to VCC + 0.3V
Junction Temperature	-40°C to +125°C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in bold face type apply over the full Operating Temperature Range (T_J = -40°C to +125°C). Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. V_{CC} = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 3)	Typ (Note 4)	Max (Note 3)	Unit
I_Q	Operating Quiescent Current			80	**110**	µA
Open Drain Flags						
I_{FLAG}	FLAGx Leakage Current	V_{FLAGx} = 3.3V		0.001	**1**	µA
V_{OL}	FLAGx Output Voltage Low	I_{FLAGx} = 1.2 mA			**0.4**	V
Time Delays						
I_{TADJ_SRC}	TADJ Source Current		**4**	12	**20**	µA
I_{TADJ_SNK}	TADJ Sink Current		**4**	12	**20**	µA
V_{HTH}	High Threshold Level		**1.0**	1.22	**1.4**	V
V_{LTH}	Low Threshold Level		**0.3**	0.5	**0.7**	V
T_{CLK}	Clock Cycle	C_{ADJ} = 10 nF		1.2		ms
T_{D1}, T_{D4}	Flag Time Delay		**9**		**10**	Clock Cycles
T_{D2}, T_{D3}, T_{D5}, T_{D6}	Flag Time Delay			8		Clock Cycles
ENABLE Pin						
V_{EN}	EN Pin Threshold		**1.0**	1.22	**1.5**	V
I_{EN}	EN Pin Pull-up Current	V_{EN} = 0V		7		µA
INV Pin						
V_{IH_INV}	Invert Pin V_{IH}		**90% VCC**			V
V_{IL_INV}	Invert Pin V_{IL}				**10% VCC**	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

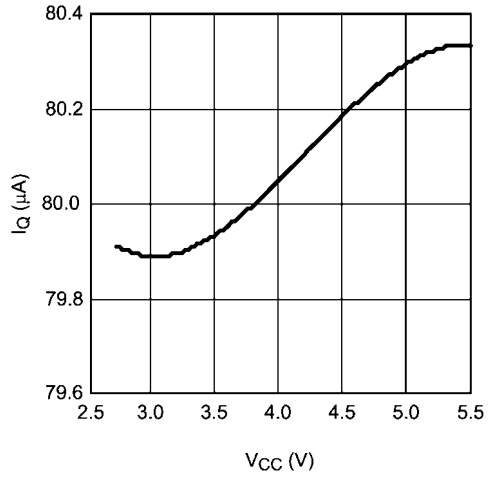
Note 3: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

Typical Performance Characteristics

V_{CC} = 3.3V unless otherwise specified.

Quiescent Current vs V_{CC}



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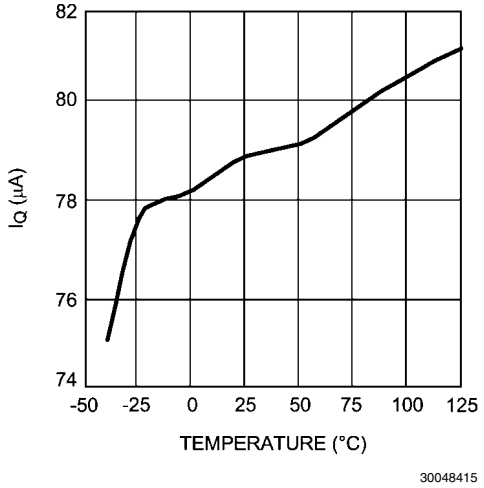
Quiescent Current vs Temperature



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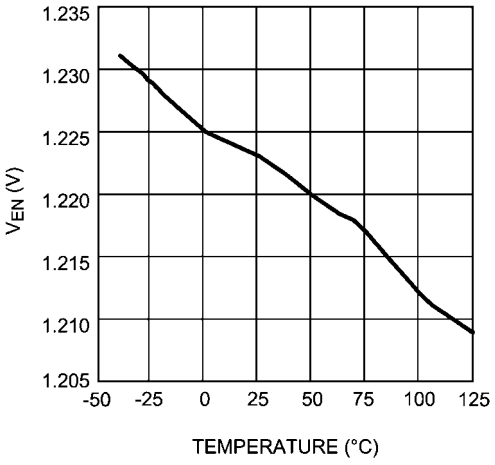
Enable Threshold vs Temperature



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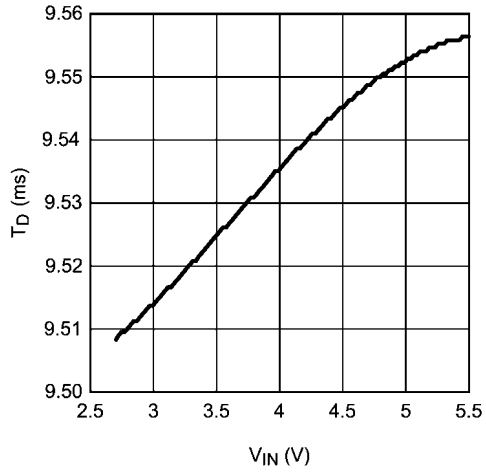
Time Delay vs V_{IN} (C_{ADJ} = 10 nF Nominal)



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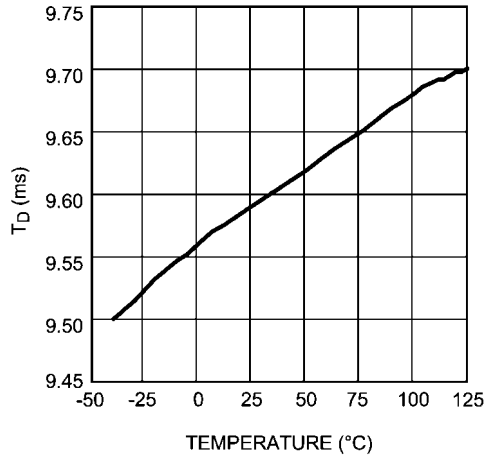
Time Delay vs Temperature (C_{ADJ} = 10 nF Nominal)



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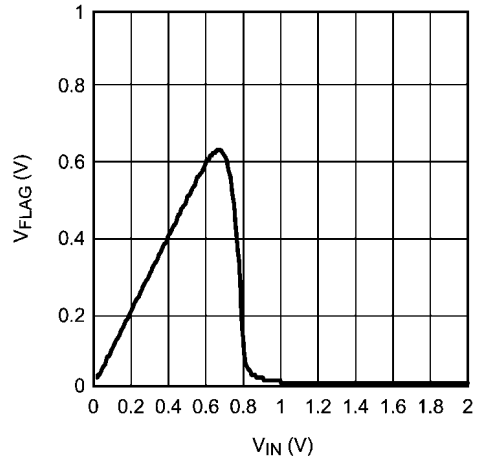
V_{FLAG} vs V_{IN} (INV Low, R_{FLAG} = 100 kΩ)



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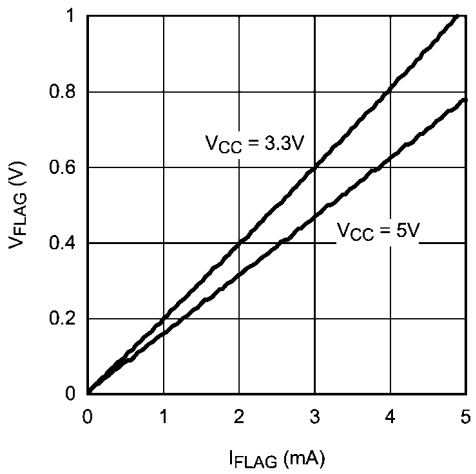
FLAG Voltage vs Current



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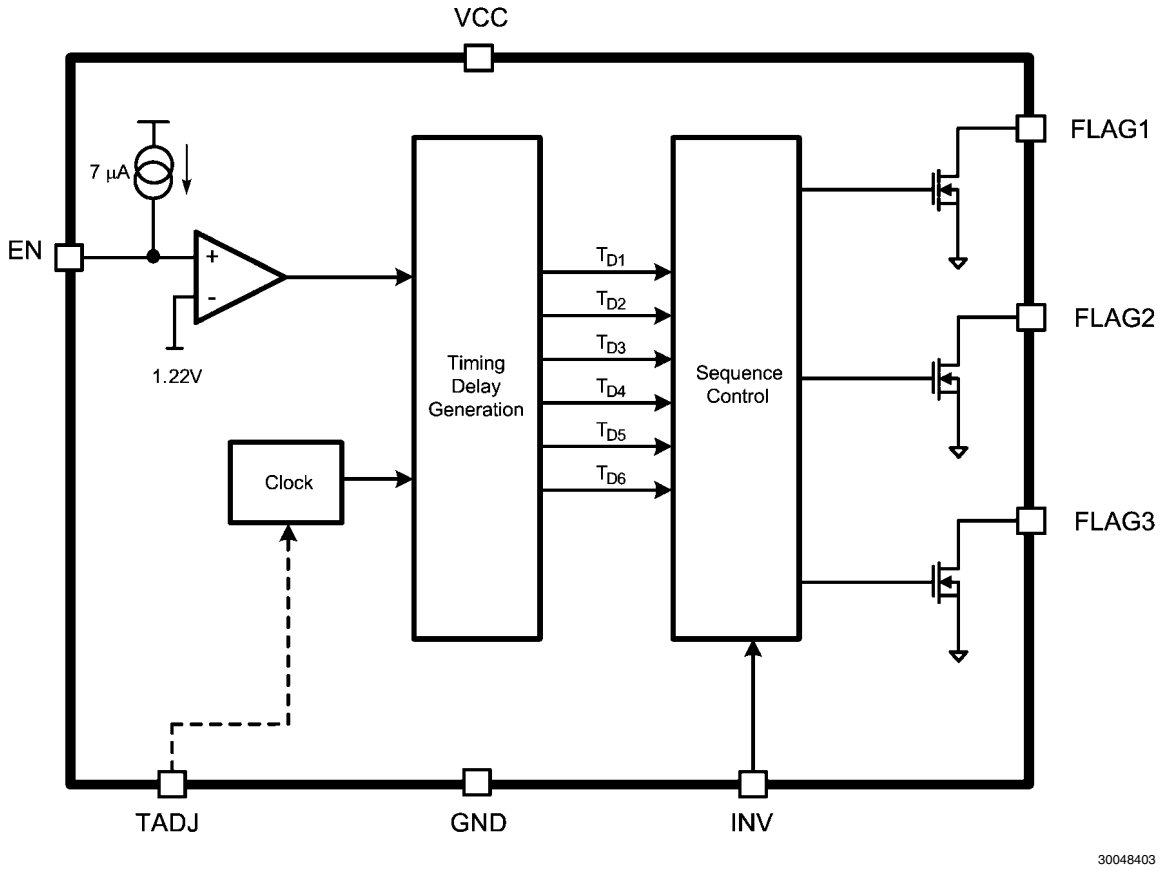
Block Diagram



Application Information

OVERVIEW

The LM3881 Power Sequencer provides a simple solution for sequencing multiple rails in a controlled manner. A clock signal is established that facilitates control of the power up and power down of three open drain FET output flags. These flags permit connection to shutdown or enable pins of linear regulators and/or switching regulators to control the power supplies' operation. This allows a complete power system to be designed without worrying about large in-rush currents or latch-up conditions that can occur during an uncontrolled startup. An invert (INV) pin is provided that reverses the logic of the output flags. This pin should be tied to a logic output high or low and not allowed to remain open circuit. The following discussion assumes the INV pin is held low such that the flag output is active high.

A small external timing capacitor is connected to the TADJ pin that establishes the clock waveform. This capacitor is linearly charged/discharged by a fixed current source/sink, denoted I_{TADJ_SRC} / I_{TADJ_SNK}, of magnitude 12 µA between predefined voltage threshold levels, denoted V_{LTH} and V_{HTH}, to generate the timing waveform as shown in the following diagram.

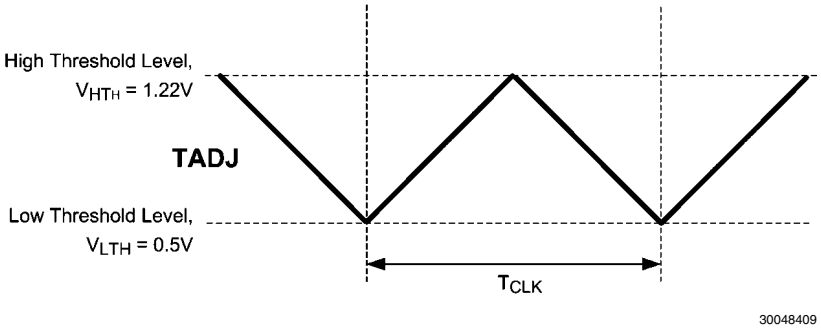


FIGURE 1. TADJ Pin Timing Waveform

Thus, the clock cycle duration is directly proportional to the timing capacitor value. Considering the TADJ voltage threshold levels and the charge/discharge current magnitude, it can be shown that the timing capacitor-clock period relationship is typically 120 µs/nF. For example, a 10 nF capacitor sets up a clock period of 1.2 ms.

The timing sequence of the LM3881 is controlled by the enable (EN) pin. Upon power up, all the flags are held low until the precision enable pin exceeds its threshold. After the EN pin is asserted, the power up sequence will commence and the open-drain flags will be sequentially released.

An internal counter will delay the first flag (FLAG1) from rising until a fixed time period, denoted by T_{D1} in the following timing diagram, elapses. This corresponds to at least nine, maximum ten, clock cycles depending on where EN is asserted relative to the clock signal. Upon release of the first flag, another timer will begin to delay the release of the second flag (FLAG2). This time delay, denoted T_{D2}, corresponds to exactly eight clock periods. Similarly, FLAG3 is released after time delay T_{D3}, again eight clock cycles, has expired. Accordingly, a TADJ capacitor of 10 nF generates typical time delays T_{D2} and T_{D3} of 9.6 ms and T_{D1} of between 10.8 ms and 12.0 ms.

The power down sequence is the same as power up, but in reverse order. When the EN pin is de-asserted, a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate time delays. These time delays, denoted T_{D4}, T_{D5}, T_{D6}, are equal to T_{D1}, T_{D2}, T_{D3}, respectively.

For robustness, the pull down FET associated with each flag is designed such that it can sustain a short circuit to VCC.

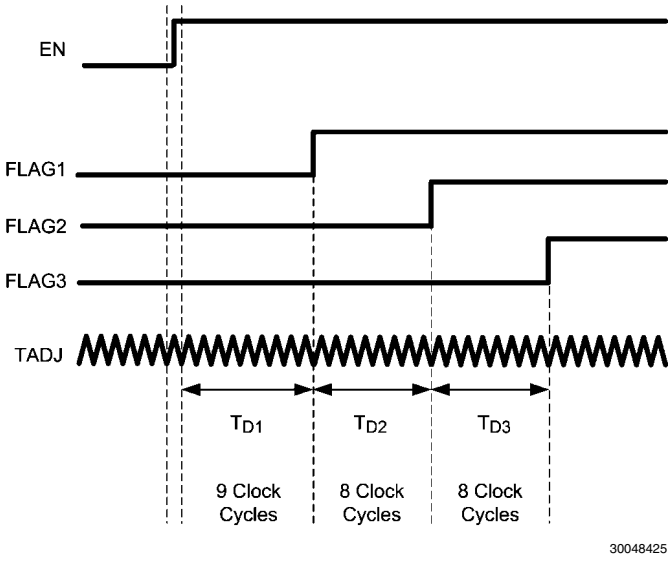


FIGURE 2. Power Up Sequence, INV Low

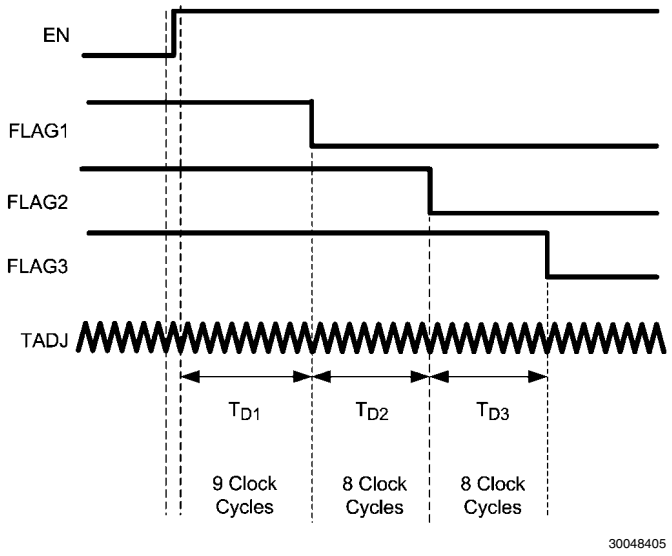


FIGURE 3. Power Up Sequence, INV High

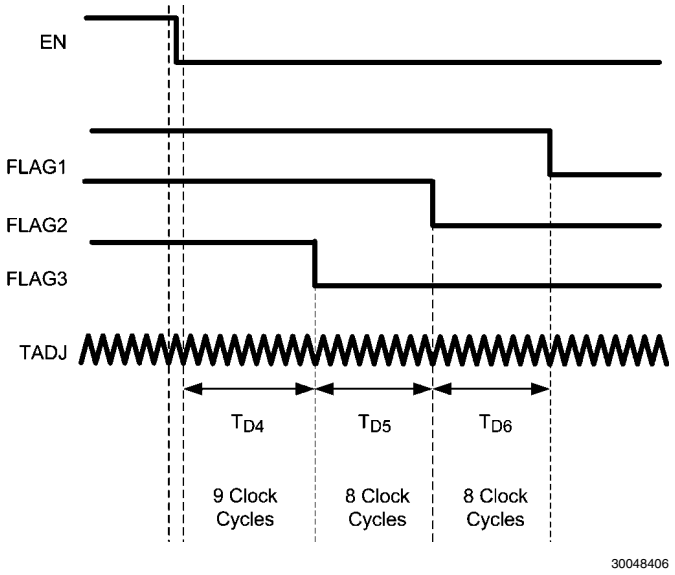


FIGURE 4. Power Down Sequence, INV Low

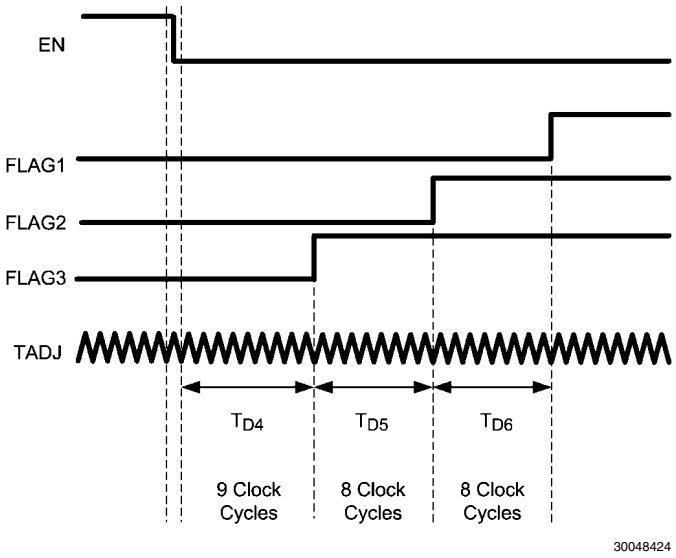


FIGURE 5. Power Down Sequence, INV High

ENABLE CIRCUIT

The enable circuit is designed with an internal comparator, referenced to a bandgap voltage (1.22V), to provide a precision threshold. This allows the timing to be set externally using a capacitor as shown in the diagram below. Alternatively, sequencing can be based on a certain event such as a line voltage reaching 90% of its nominal value by employing a resistor divider from VCC to Enable.

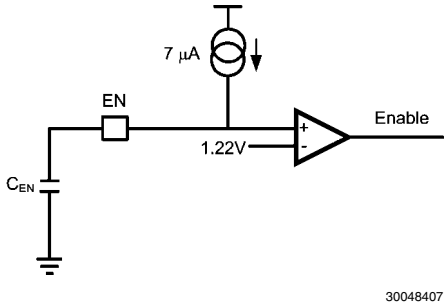


FIGURE 6. Precision Enable Circuit

Using the internal pull-up current source to charge the external capacitor C_{EN}, the time delay while the enable voltage reaches the required threshold, assuming EN is charging from 0V, can be calculated by the equation as follows.

$$T_{enable\_delay} = \frac{1.22V \times C_{EN}}{7\ \mu A}$$

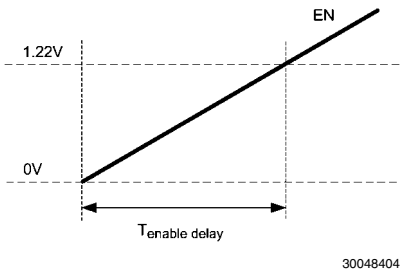


FIGURE 7. Enable Delay Timing

A resistor divider can also be used to enable the LM3881 based on exceeding a certain VCC supply voltage threshold. Care needs to be taken when sizing the resistor divider to include the effects of the internal EN pull-up current source. The supply voltage for which EN is asserted is given by

$$VCC_{ENABLE} = 1.22V\left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - 7\ \mu A\ (R_{EN1} \| R_{EN2})$$

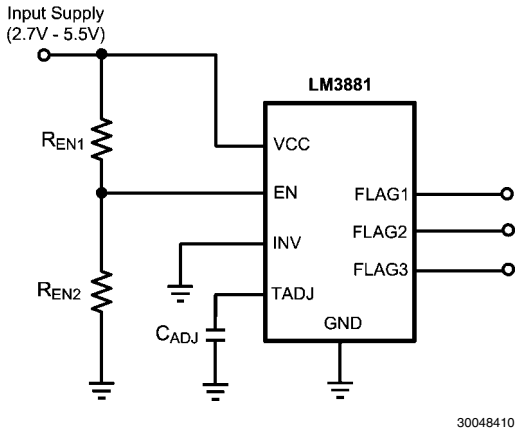


FIGURE 8. Enable Based On Input Supply Level

One of the features of the enable pin is that it provides glitch free operation. The timer will start counting at a rising threshold, but will always reset if the enable pin is de-asserted before the first output flag is released. This is illustrated in the timing diagram below, assuming INV is low.

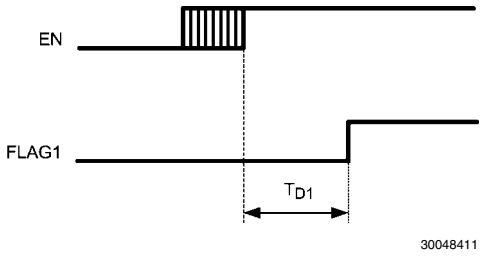


FIGURE 9. Enable Glitch Timing, INV Low

If the EN pin remains high for the entire power up sequence, then the part will operate as shown in the standard timing diagrams. However, if the EN signal is de-asserted before the power-up sequence is completed, the part will enter a controlled shutdown. This allows the system to initiate a controlled power sequence, preventing any latch conditions to occur. The following timing diagrams describe the flag sequence if the EN pin is de-asserted after FLAG1 releases, but before the entire power-up sequence is completed. INV is assumed low.

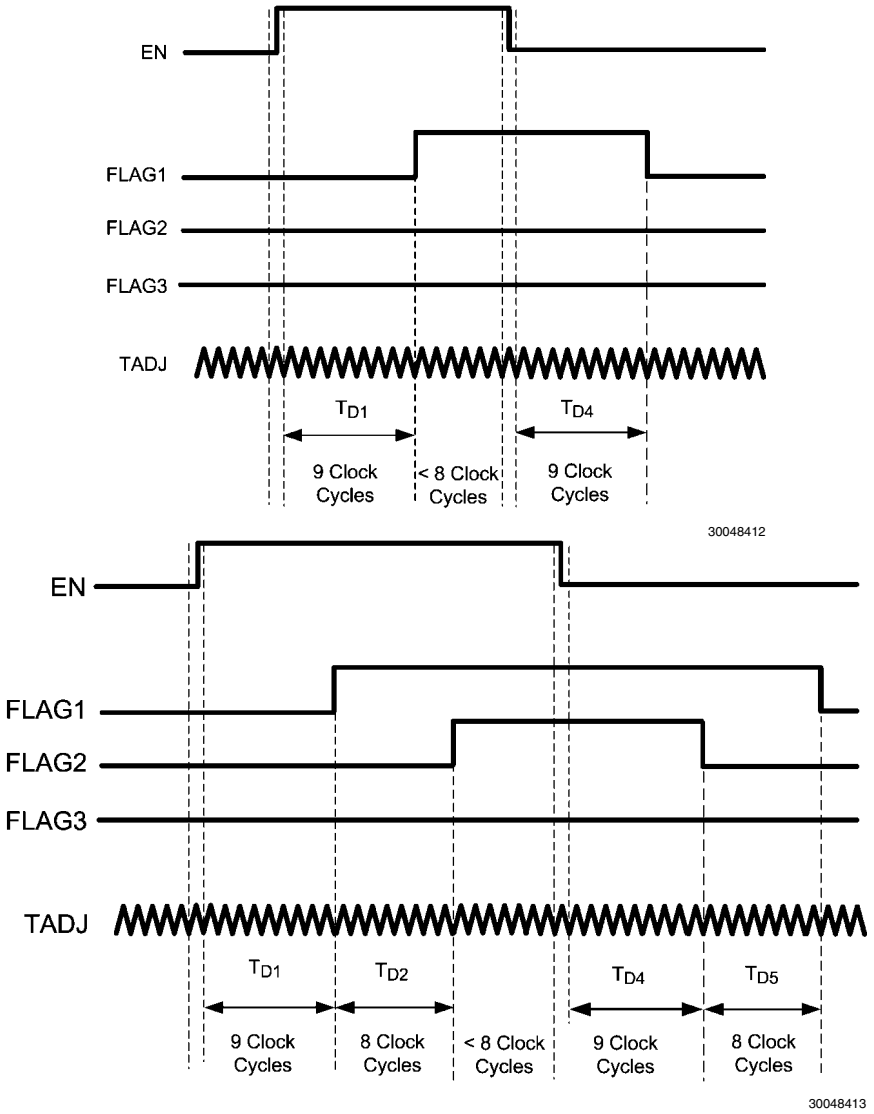
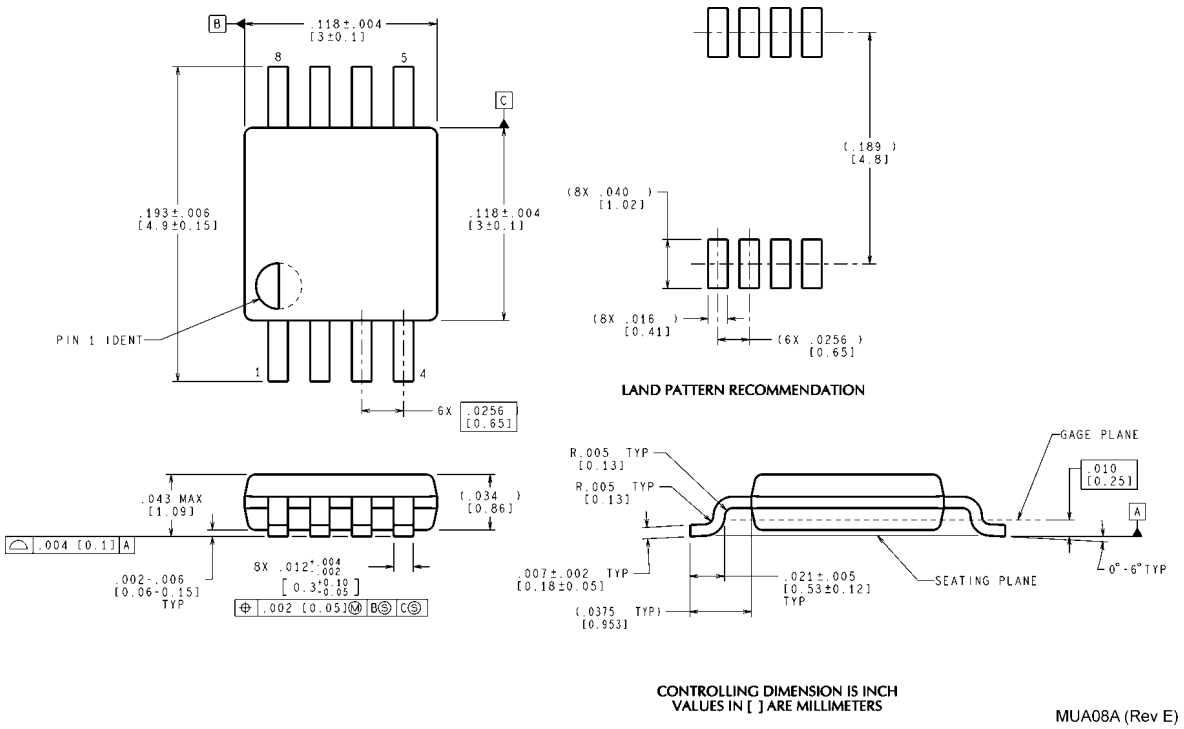


FIGURE 10. Incomplete Sequence Timing, INV Low

Physical Dimensions inches (millimeters) unless otherwise noted



MSOP-8 Package
NS Package Number MUA08A

Notes

Notes

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