Mobile DDR SDRAM

MT46H8M16LF – 2 Meg x 16 x 4 Banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

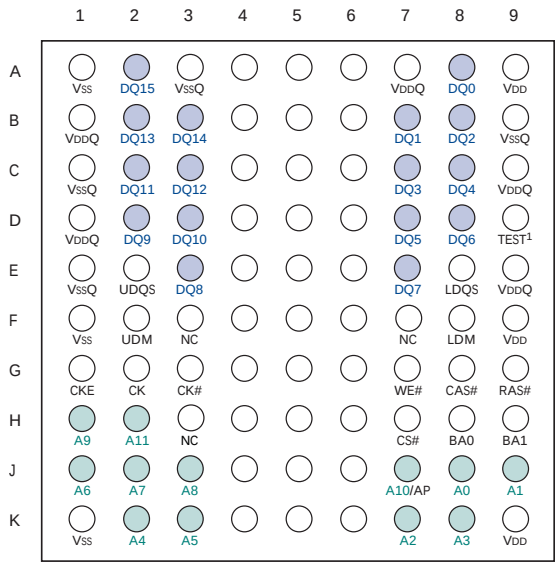
Features

- VDD/VDDQ = +1.8V ±0.1V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data–one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control refresh rate
- Partial array self refresh (PASR)
- Selectable output drive (DS)
- Clock stop capability

Options / Marking

- VDD/VDDQ
  - 1.8V/1.8V — H
- Configuration
  - 8 Meg x 16 (2 Meg x 16 x 4 banks) — 8M16
- Plastic package
  - 60-Ball VFBGA (lead-free) 8mm x 10mm — CF
- Timing – cycle time
  - 7.5ns @ CL = 3 — -75
  - 10ns @ CL = 3 — -10
- Operating temperature range
  - Commercial (0° to +70°C) — None
  - Industrial (-40°C to +85°C) — IT

Figure 1: 60-Ball VFBGA Assignment (Top View)



Notes:1.D9 should be connected to VSS or VSSQ in normal operations.

Table 1: Configuration Addressing

Architecture	8 Meg x 16
Configuration	2 Meg x 16 x 4
Refresh count	4K
Row addressing	4K (A0–A11)
Bank addressing	4 (BA0, BA1)
Column addressing	512K (A0–A8)

Table 2: Key Timing Parameters

Speed Grade	Clock Rate		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-75	83 MHz	133 MHz	6.5ns	6.0ns
-10	67 MHz	104 MHz	7.0ns	7.0ns

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Table 3: 128Mb Mobile DDR SDRAM Part Numbers

Part Number	Configuration	I/O Drive Level	Temperature Option
MT46H8M16LFCF-75	8 Meg x 16	Programmable drive	0°C to +70°C
MT46H8M16LFCF-75IT	8 Meg x 16	Programmable drive	-40°C to +85°C
MT46H8M16LFCF-10	8 Meg x 16	Programmable drive	0°C to +70°C
MT46H8M16LFCF-10IT	8 Meg x 16	Programmable drive	-40°C to +85°C

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's new FBGA Part Marking Decoder makes it easier to understand this part marking. Visit the Web site at www.micron.com/decoder.

General Description

The 128Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,271,728 bits. It is internally configured as a quad-bank DRAM. Each of the 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

The 128Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 128Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 128Mb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

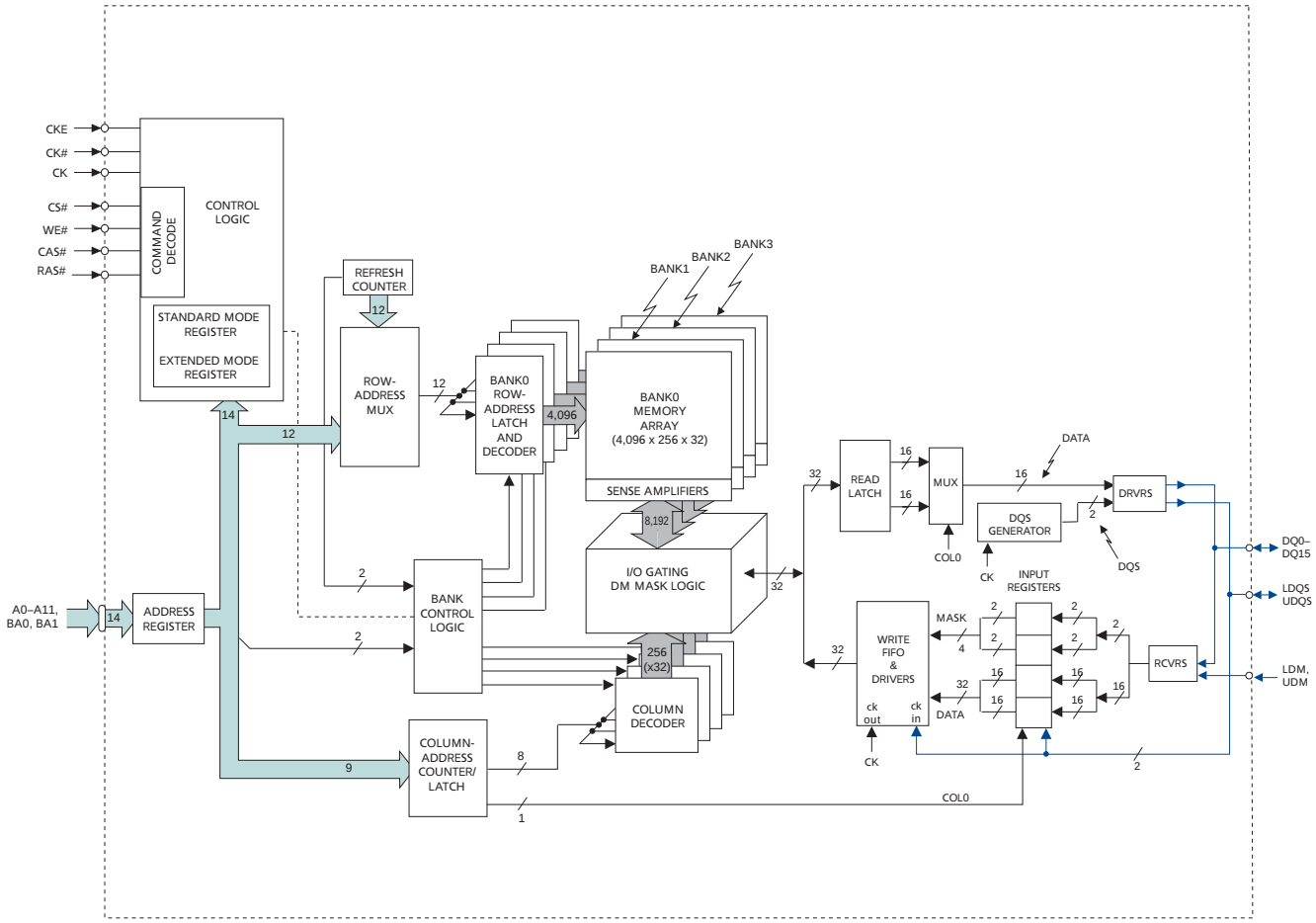
The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Mobile DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Notes:
1. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes—the lower byte and upper byte. For the lower byte (DQ0–DQ7) DM refers to LDM and DQS refers to LDQS; and for the upper byte (DQ8–DQ15) DM refers to UDM and DQS refers to UDQS.
2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

Figure 2: Functional Block Diagram (8 Meg x 16)



Ball Description

Table 4: 60-Ball VFBGA Ball Description

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions expect SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F2, F8	UDM, LDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15.
H8, H9	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K8, K2, K3, J1, J2, J3, J7, H1, H2	A0–A11	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B7, B8, C7, C8, D7, D8, E7 E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ15	I/O	Data input/output: Data bus for x16.
E2, E7	UDQS, LDQS	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.
A7, B1, C9, D1, E9	$V_{DD}Q$	Supply	DQ power supply.
A3, B9, C1, E1	$V_{SS}Q$	Supply	DQ ground: Isolated on the die for improved noise immunity.
A9, F9, K9	V_{DD}	Supply	Power supply.
A1, F1, K1	V_{SS}	Supply	Ground.
F3, F7, H3	NC	Input	No connect. These pins should be left unconnected.
D9	TEST	Input	Test pin: Must be tied to V_{SS} or $V_{SS}Q$ in normal operations.

Functional Description

The 128Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,271,728-bits. It is internally configured as a quad-bank DRAM. Each of the 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

The 128Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. single read or write access for the 128Mb Mobile DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Mobile DDR SDRAM.

To properly initialize the Mobile DDR SDRAM, the following sequence must be followed:

1. It is recommended the core power (V_{DD}) and I/O power ($V_{DD}Q$) be from the same power source and brought up simultaneously. If separate power sources are used, V_{DD} must lead $V_{DD}Q$.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs minimum delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least ^{t}RP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued after step 10.

7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least ^{t}MRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least ^{t}MRD time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all SDRAM devices, and the extended mode register, which is exists on all Mobile SDRAM devices.

Standard Mode Register

The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 3 on page 10. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again.

Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3 on page 10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap until a boundary is reached. The block is uniquely selected by A1–A*i* when BL = 2, by A2–A*i* when BL = 4, by A3–A*i* when BL = 8 (where A*i* is

the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See Table 5 on page 11 for more information.

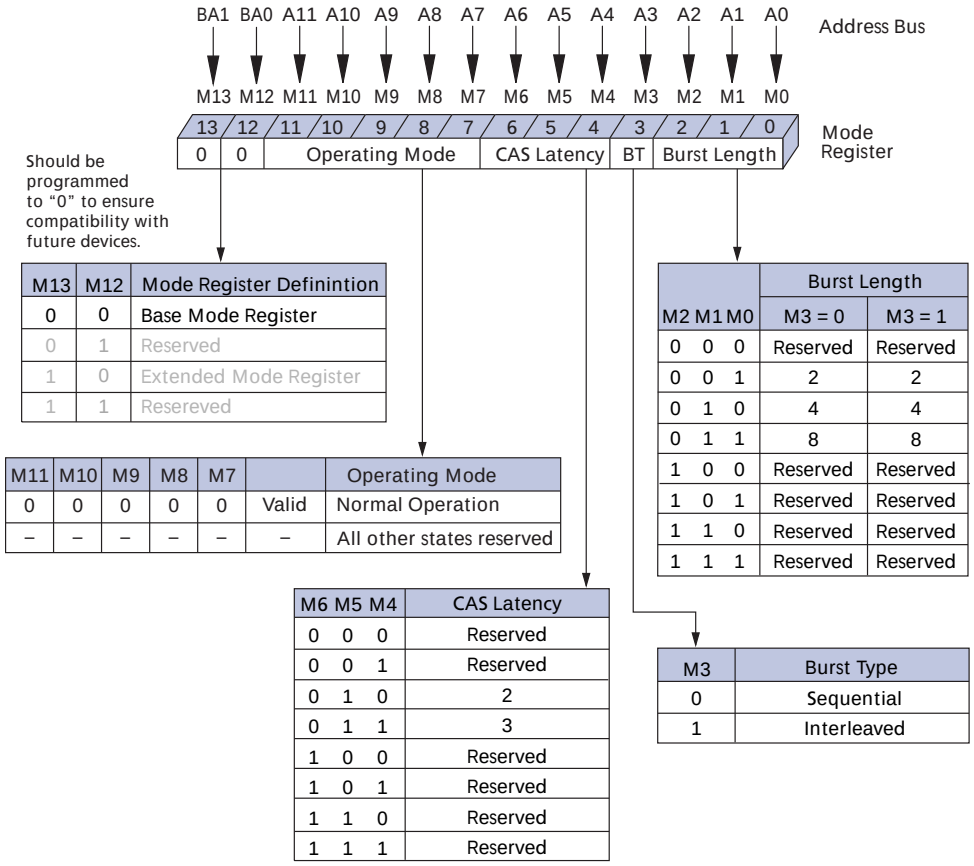
READ Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in Figure 3 on page 10.

For CL = 3, if the READ command is registered at clock edge *n*, then the data will nominally be available at (*n* + 2 clocks + ^{t}AC). For CL = 2, if the READ command is registered at clock edge *n*, then the data will be nominally be available at (*n* + 1 clock + ^{t}AC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 3: Standard Mode Register Definition



M13	M12	Mode Register Definintion
0	0	Base Mode Register
0	1	Reserved
1	0	Extended Mode Register
1	1	Resereved

M11	M10	M9	M8	M7		Operating Mode
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

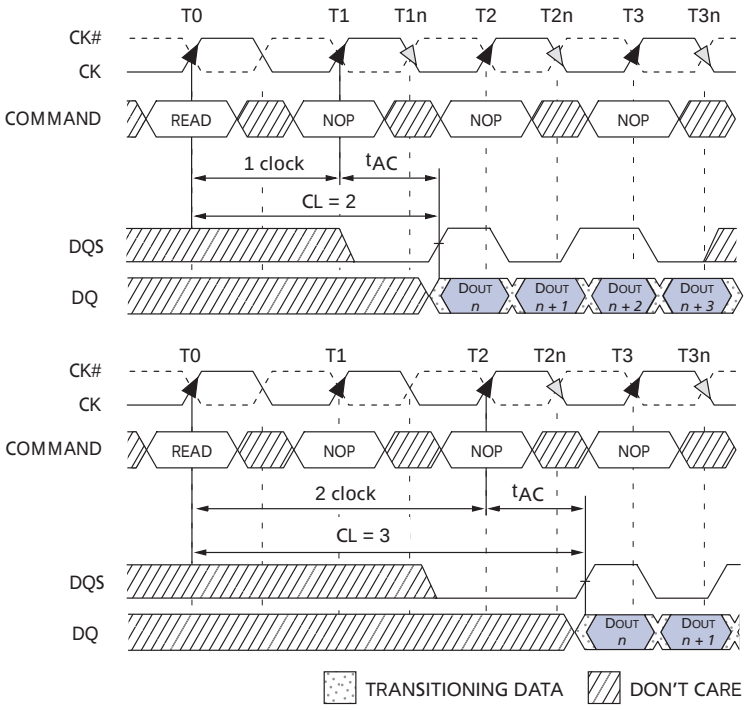
M2 M1 M0	Burst Length	
	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Table 5: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Figure 4: CAS Latency



Notes: 1. BL = 4 in the cases shown.
2. Shown with nominal ^{t}AC and nominal ^{t}DSDQ.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7–A11 each set to zero, and bits A0–A6 set to the desired values.

All other combinations of values for A7–A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh.

Temperature Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

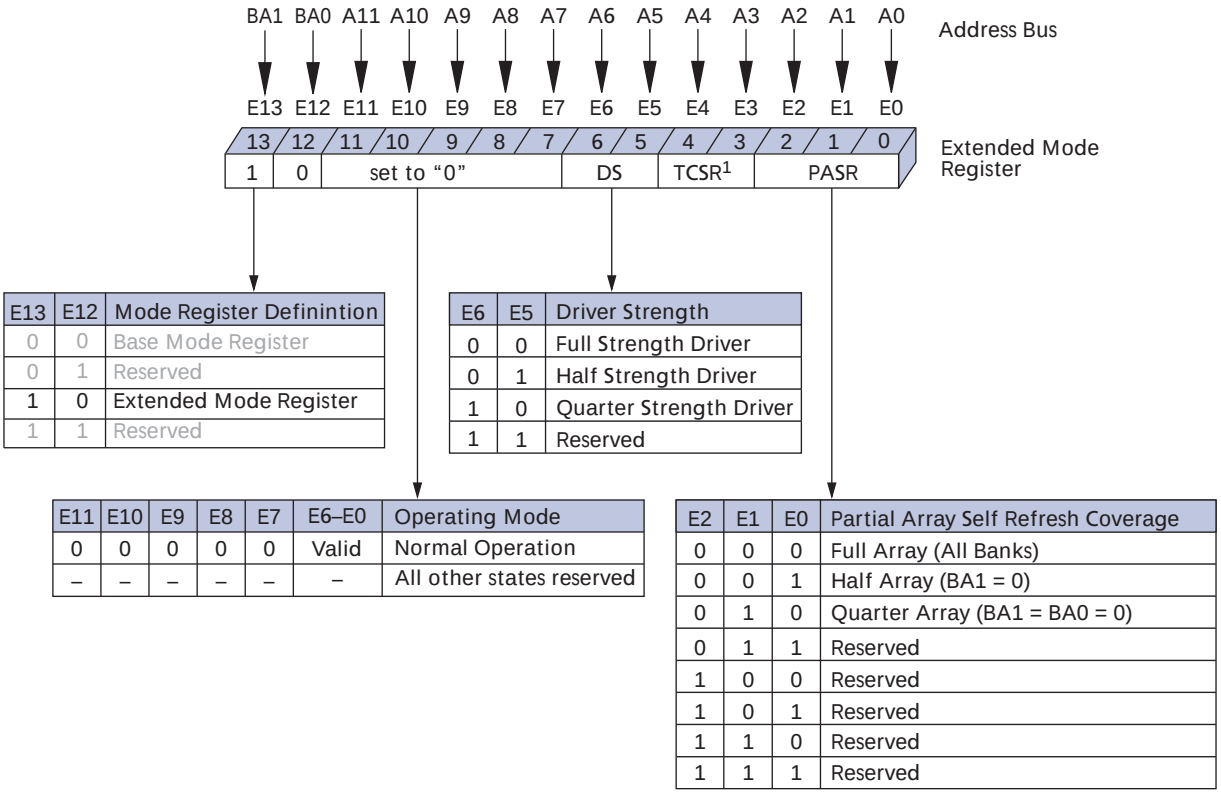
- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 and 1
- Quarter array: bank 0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs. There are three allowable settings for the output drivers (25 ohm internal impedance, 55 ohm internal impedance, and 80 ohm internal impedance).

Figure 5: Extended Mode Register



E13	E12	Mode Register Definintion
0	0	Base Mode Register
0	1	Reserved
1	0	Extended Mode Register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full Strength Driver
0	1	Half Strength Driver
1	0	Quarter Strength Driver
1	1	Reserved

E11	E10	E9	E8	E7	E6–E0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial Array Self Refresh Coverage
0	0	0	Full Array (All Banks)
0	0	1	Half Array (BA1 = 0)
0	1	0	Quarter Array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes: 1. On-chip temperature sensor is used in place of TCSR. Setting these bits will have no effect.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency.
2. Stop the clock.

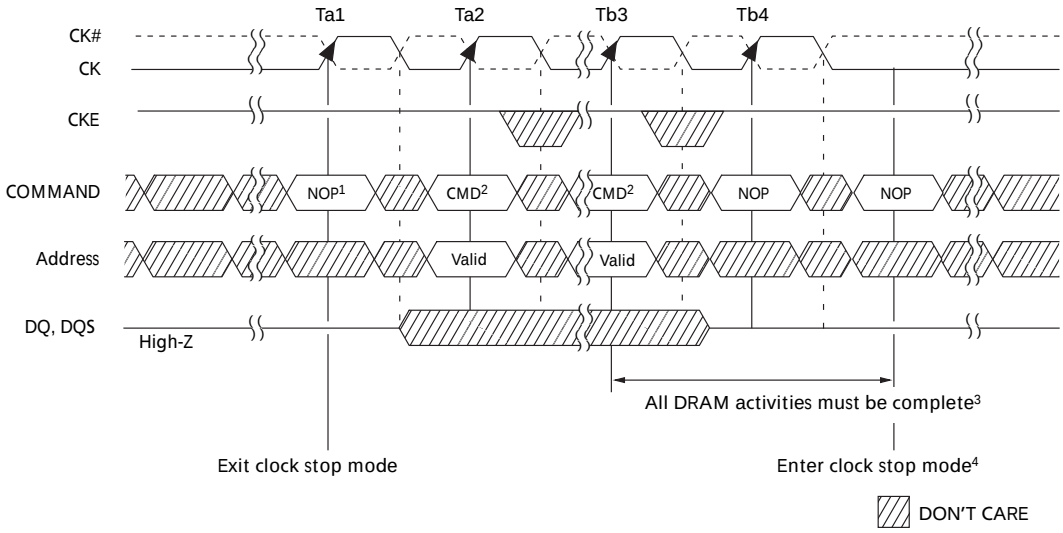
Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Mobile DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped if there are no data accesses in progress, either WRITEs or READs that would be affected by this change. If a WRITE or a READ is in progress the entire data burst must be complete prior to stopping the clock.

For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied. CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued. Figure 6 on page 14 illustrates the clock stop mode.

Figure 6: Clock Stop Mode



Notes:
1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is allowed, device is not in clock suspend mode.
3. Any DRAM operation already in process must be completed before entering clock stop mode. This includes ^{t}RCD, ^{t}RP, ^{t}RFC, ^{t}MRD, ^{t}WR, all data-out for READ bursts.
4. To enter and maintain a clock stop mode: CK = LOW, CK# = HIGH, CKE = HIGH.

Commands

Table 6 and Table 7 provide quick references of available commands. This is followed by a written description of each command. Three additional Truth Tables (Table 8 on page 42, Table 9 on page 43, and Table 10 on page 45) provide CKE commands and current/next state information.

Table 6: Truth Table – Commands

Note 1 applies to all commands; All states and sequences not shown are reserved and/or illegal.

Name (Function)	CS#	RAS#	CAS#	WE#	ADDR	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code	2

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 provide the op-code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A11 provide row address.
4. BA0–BA1 provide bank address; A0–A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.

Table 7: Truth Table – DM Operation

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

Note: Used to mask write data; provided coincident with corresponding data.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# = LOW, RAS# = CAS# = WE# = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A11. See mode register descriptions in "Register Definition" on page 9. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 8 for x16) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Except in the case of

concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in "Operations" on page 19. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 19. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 128Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 15.625µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting).

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued for ^{t}XSR is required for the completion of any internal refresh in progress.

Operations

Bank/row Activation

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 7.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 8 on page 20,which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$. (Figure 8 also shows the same case for ^{t}RCD; the same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 7: Activating a Specific Row in a Specific Bank

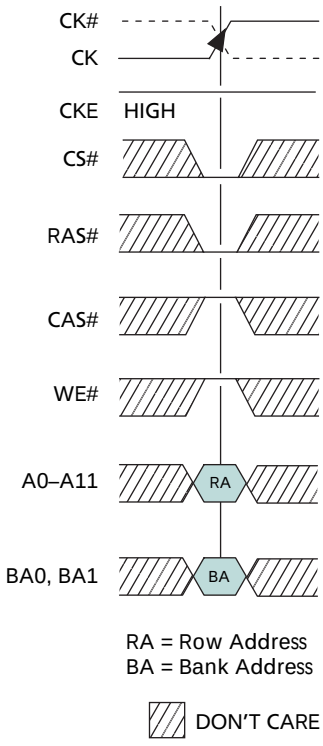
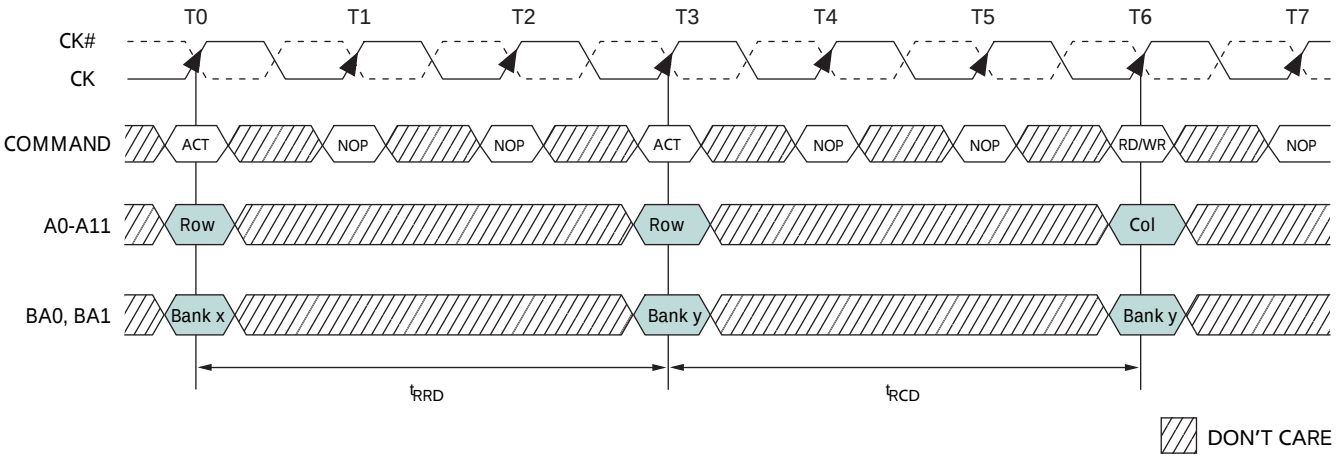


Figure 8: Example: Meeting ^{t}RCD (^{t}RRD) MIN When 2 < ^{t}RCD (^{t}RRD) MIN/^{t}CK ≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 9 on page 21.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

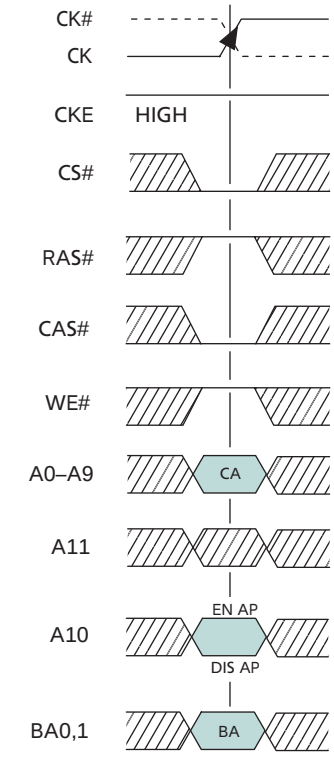
During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 10 on page 22 shows general timing for each possible CAS latency setting. DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 31 on page 55. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 32 on page 56.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued ***x*** cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 11 on page 23.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 12 on page 24. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 13 on page 25.

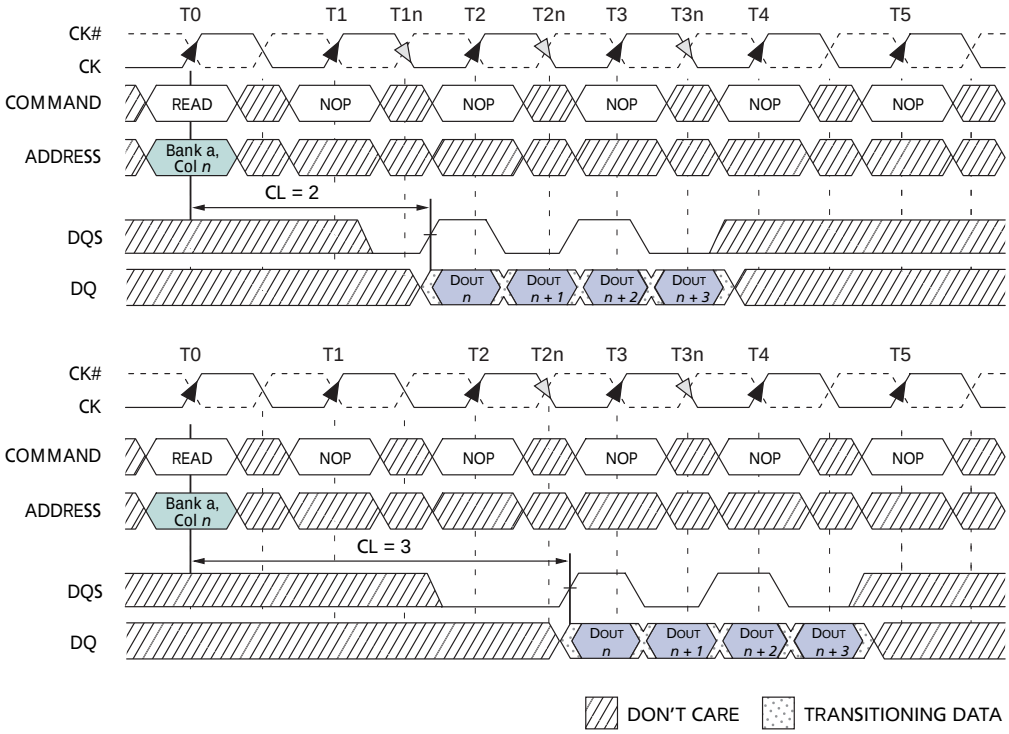
Figure 9: READ Command



CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

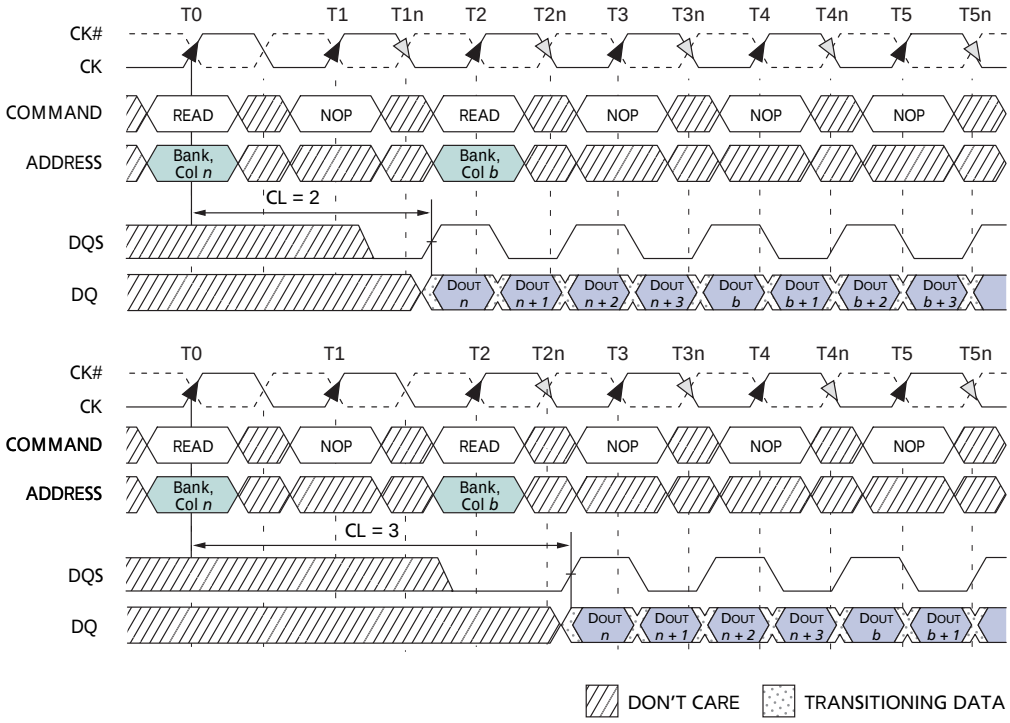
DON'T CARE

Figure 10: READ Burst



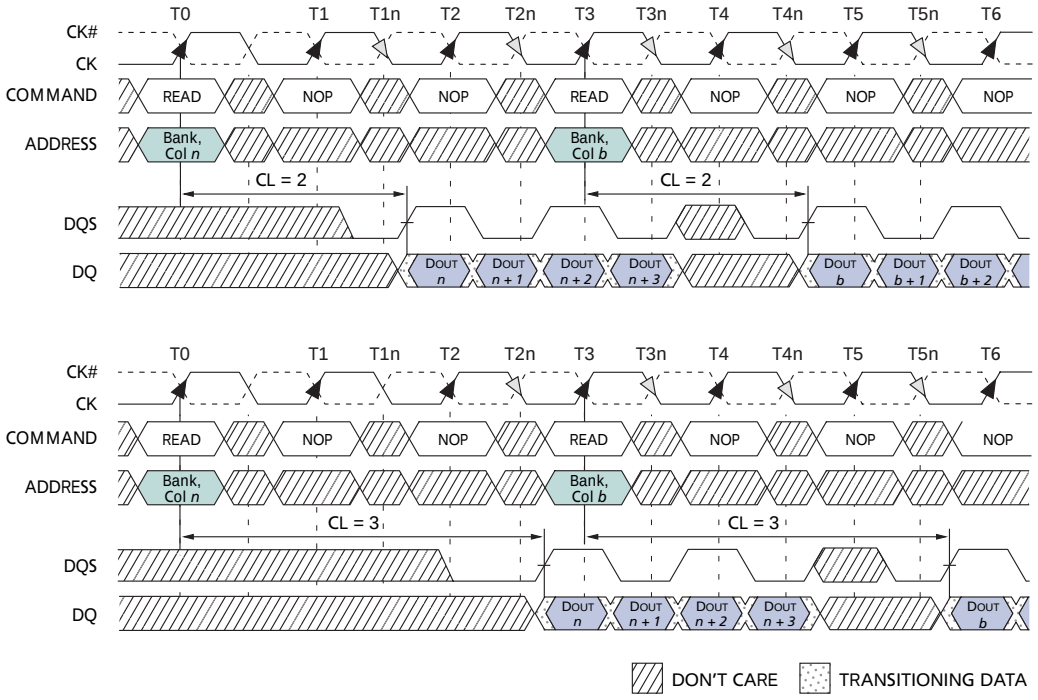
Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 11: Consecutive READ Bursts



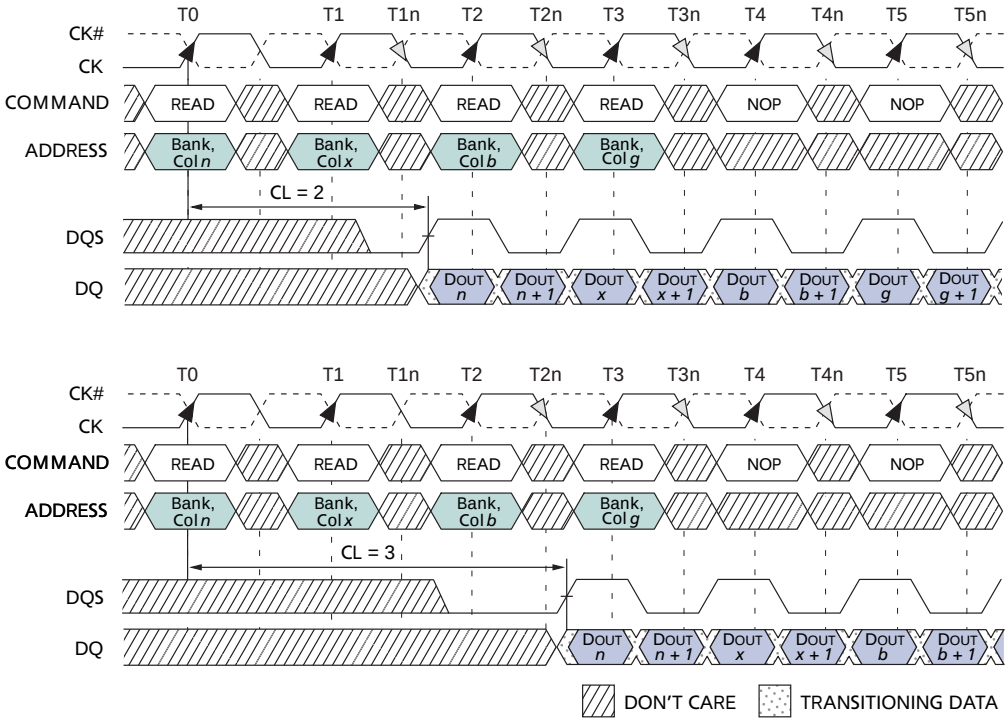
Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. This example represents consecutive READ commands issued to the device.

Figure 12: Nonconsecutive READ Bursts



Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. This example represents nonconsecutive READ commands issued to the device.

Figure 13: Random READ Accesses



Notes:
1. DOUT *n* (or *x*, b, *g*) = data-out from column *n* (or column *x*, column *b*, column *g*).
2. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
3. READs are to an active row in any bank.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Truncated READs

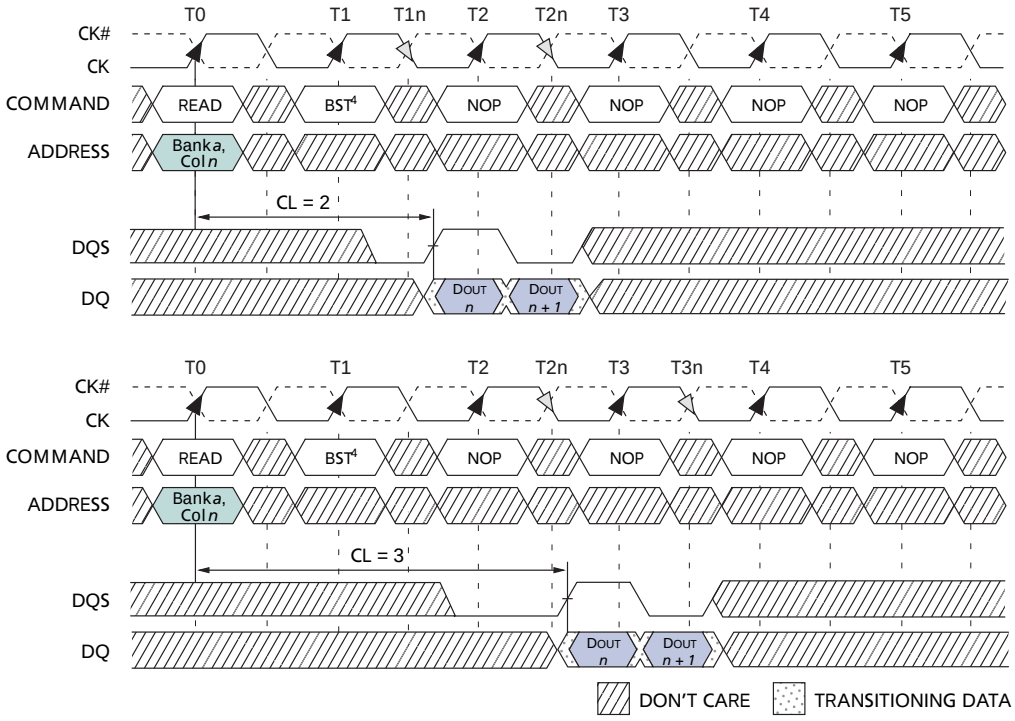
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 14 on page 26. The burst terminate latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 15 on page 27. The ^{t}DQSS (MIN) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the *n*-prefetch architecture). This is shown in Figure 16 on page 28. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

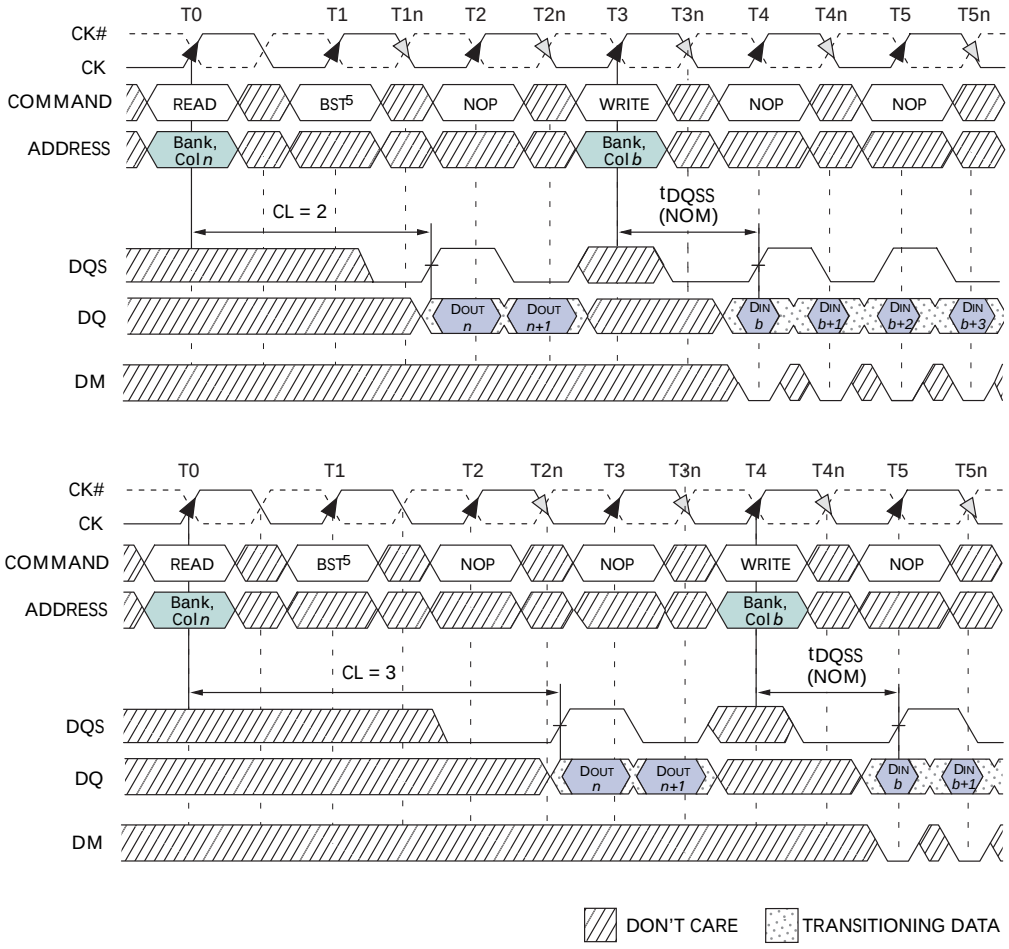
Note: Part of the row precharge time is hidden during the access of the last data elements.

Figure 14: Terminating a READ Burst



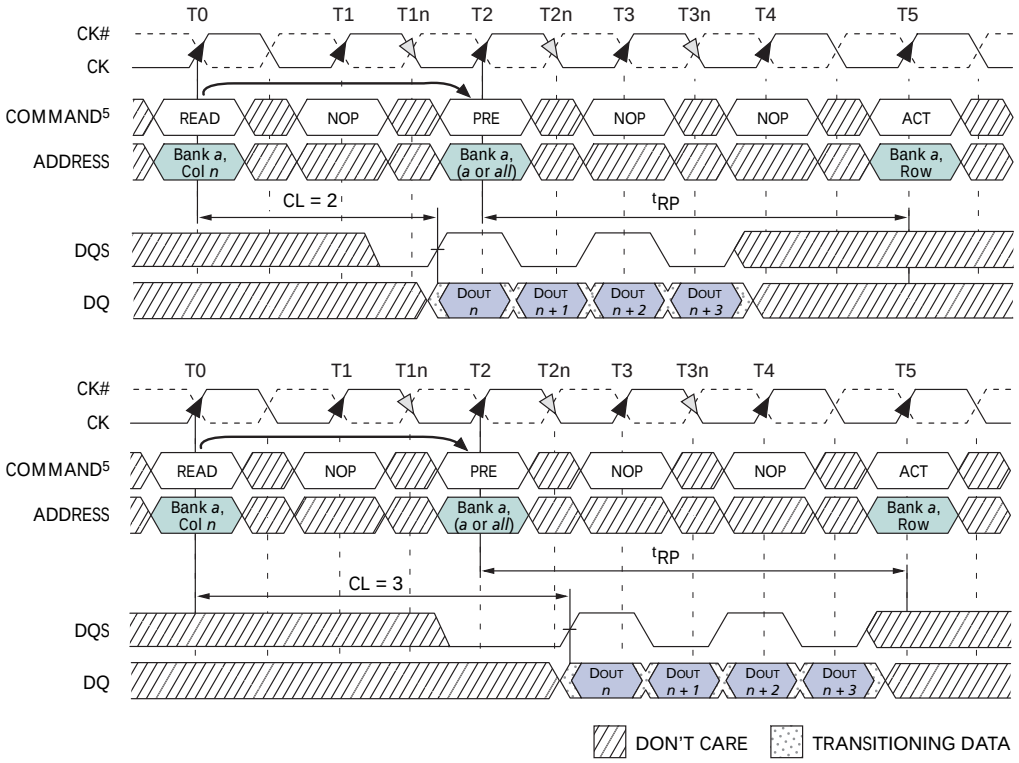
Notes:
1. DOUT *n* = data-out from column *n*.
2. Only valid for BL = 4 and BL = 8.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

Figure 15: READ-to-WRITE



Notes:
1. DOUT *n* = data-out from column *n*.
2. DIN *b* = data-in from column *b*.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.

Figure 16: READ-to-PRECHARGE



Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided ^{t}RAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL / 2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 17 on page 30.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 18 on page 31 shows the nominal case and the extremes of ^{t}DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Figure 19 on page 32 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 20 on page 32. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 21 on page 33.

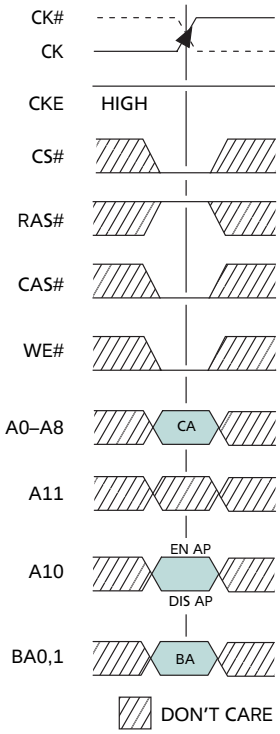
Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, ^{t}WTR should be met, as shown in Figure 22 on page 34.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 23 on page 35. Note that only the data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 24 on page 36.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, ^{t}WR should be met, as shown in Figure 25 on page 37.

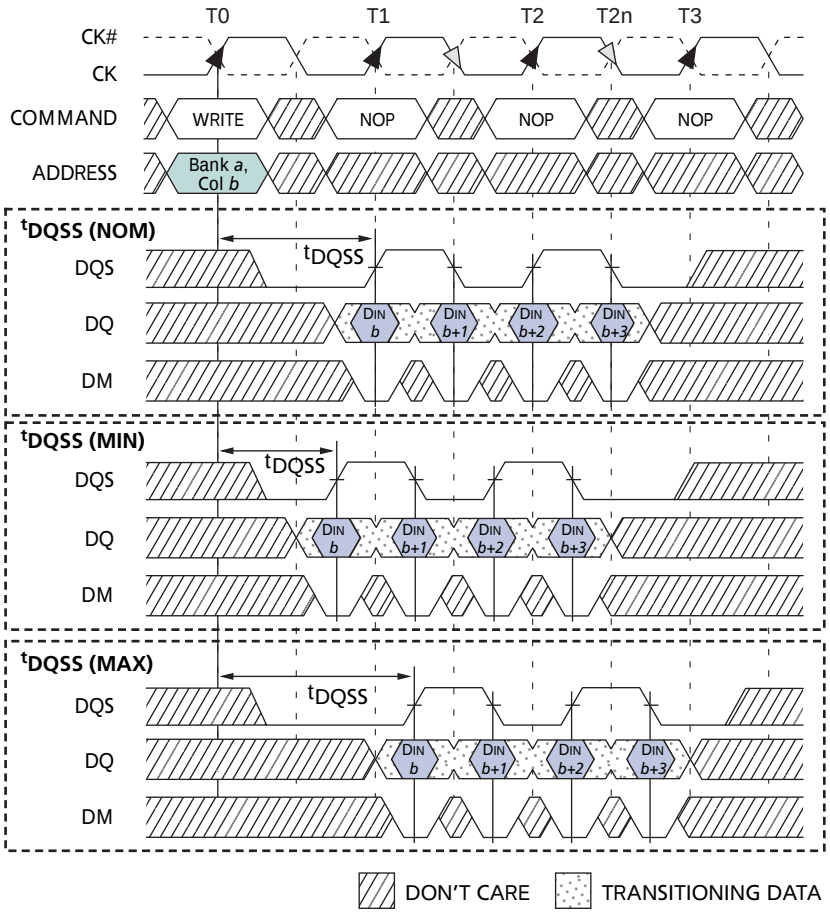
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 26 on page 38 and Figure 27 on page 39. Note that only the data-in pairs that are registered prior to the ^{t}WR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 26 on page 38 and Figure 27 on page 39. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

Figure 17: WRITE Command



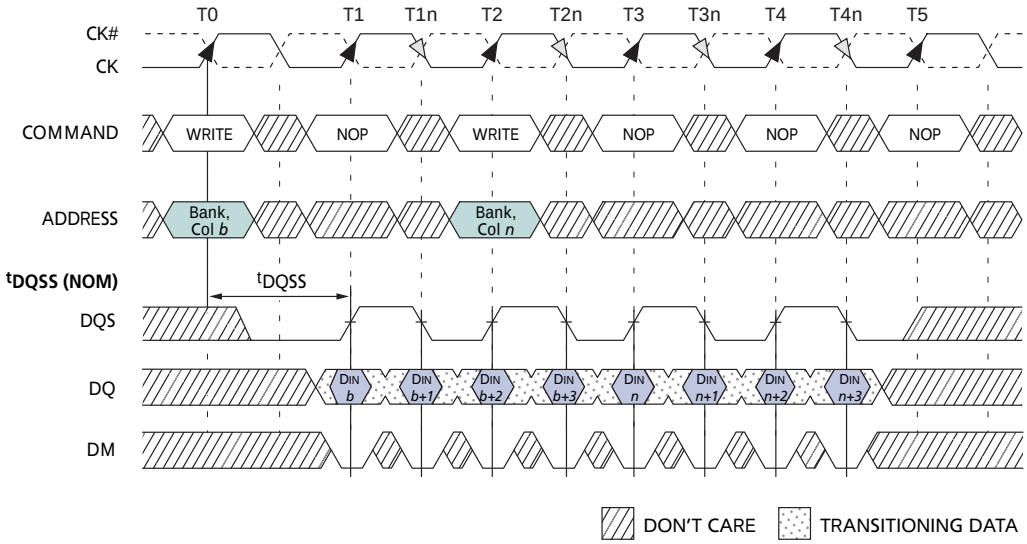
Note: DIS AP = Disable Auto Precharge
EN AP = Enable Auto Precharge
BA = Bank Address
CA = Column Address

Figure 18: WRITE Burst



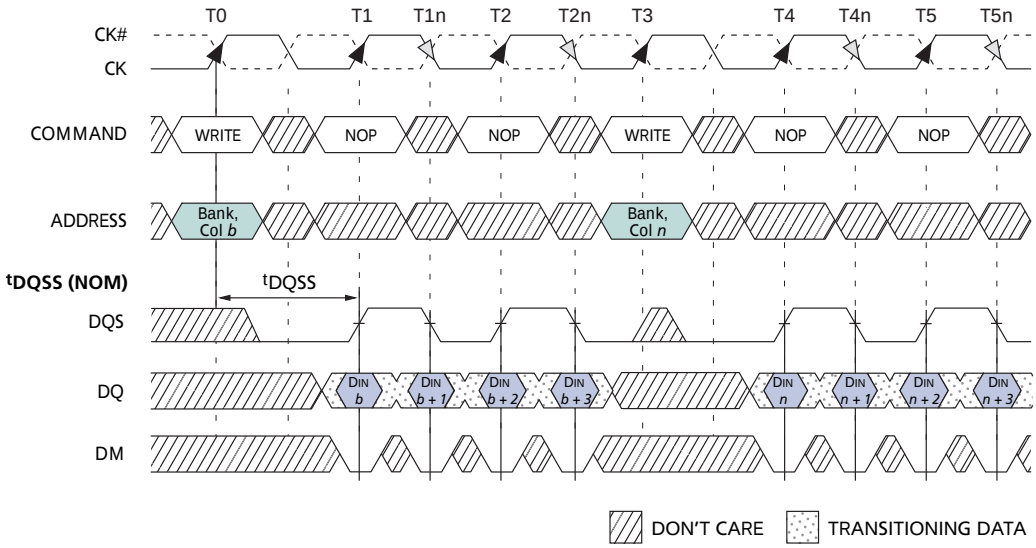
Notes:
1. DIN *b* = data-in for column *b*.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 19: Consecutive WRITE-to-WRITE



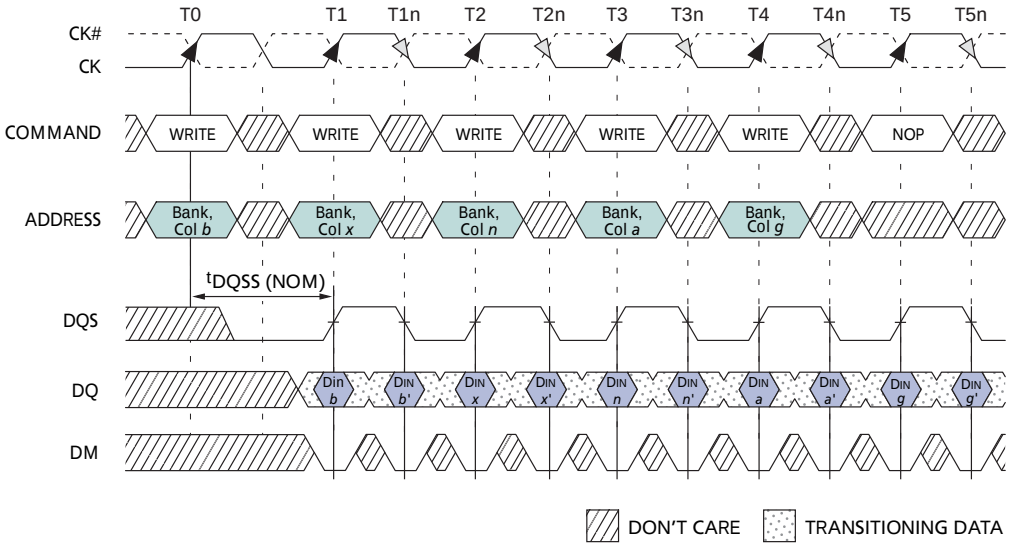
Notes:
1. DIN *b* (*n*) = data-in for column *b* (*n*).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

Figure 20: Nonconsecutive WRITE-to-WRITE



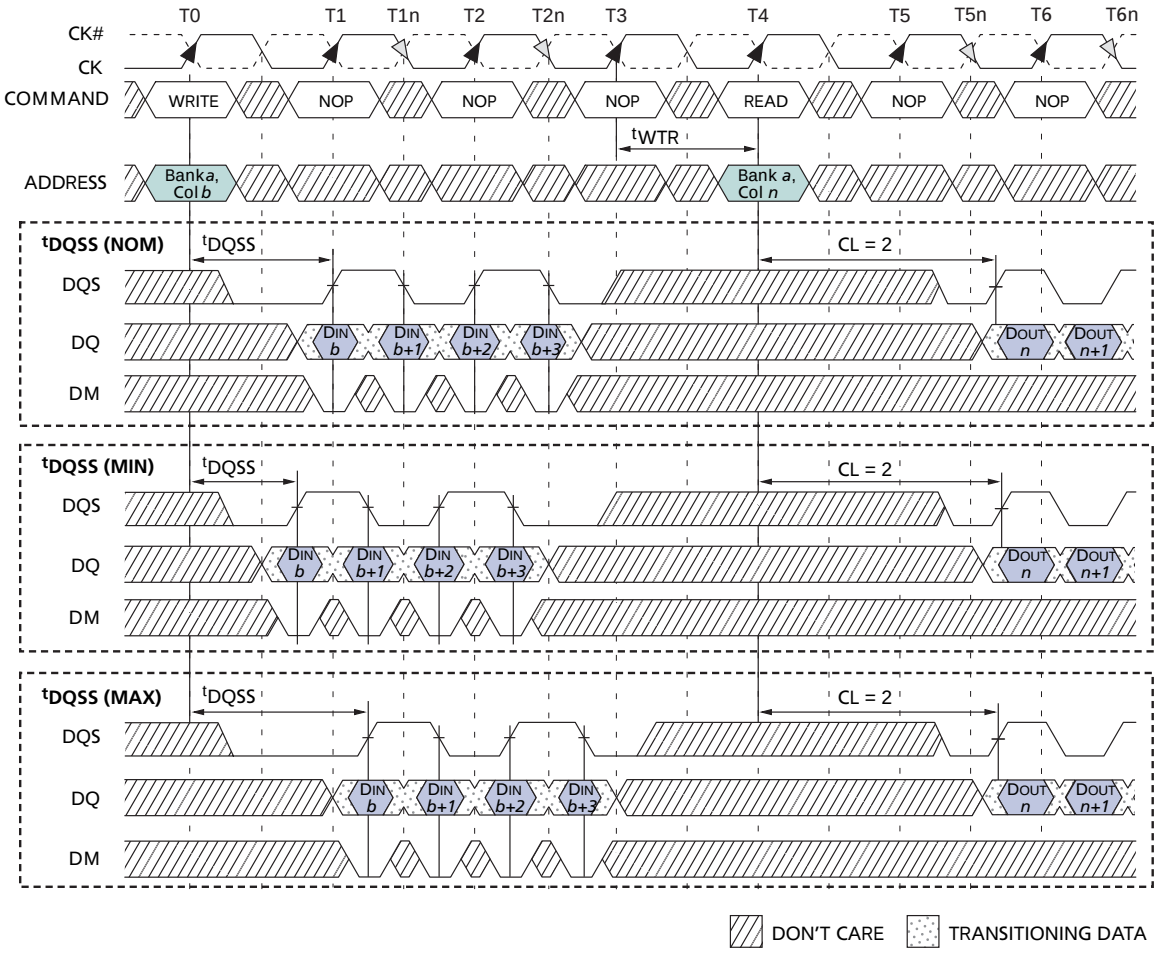
Notes:
1. DIN *b* (*n*) = data-in for column *b* (*n*).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

Figure 21: Random WRITE Cycles



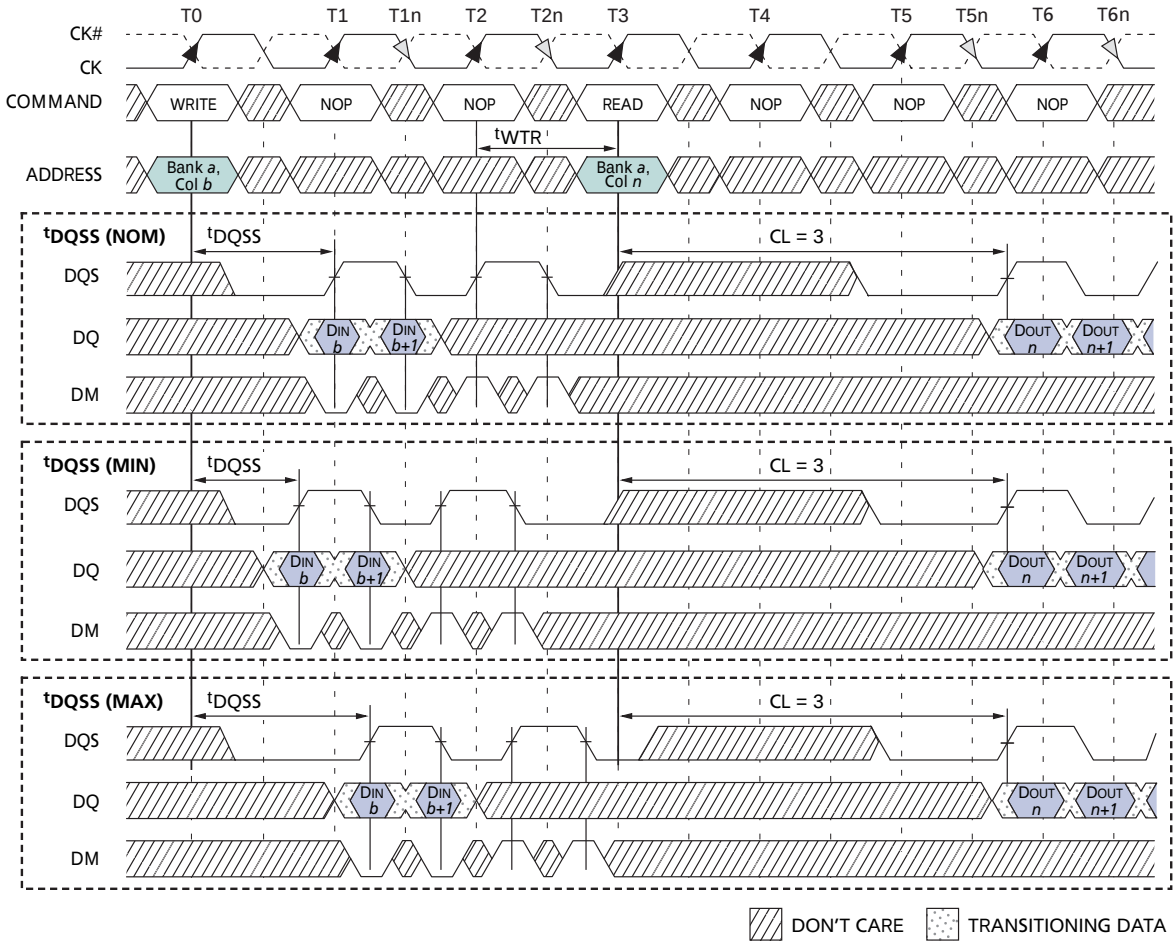
Notes:
1. DIN *b* (*or x*, *n*, *a*, *g*) = data-in for column *b* (or *x, n, q, g*)
2. b' (or *x, n, a, g*) = the next data-in following DIN *b* (*x, n, a, g*), according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.

Figure 22: WRITE-to-READ – Uninterrupting



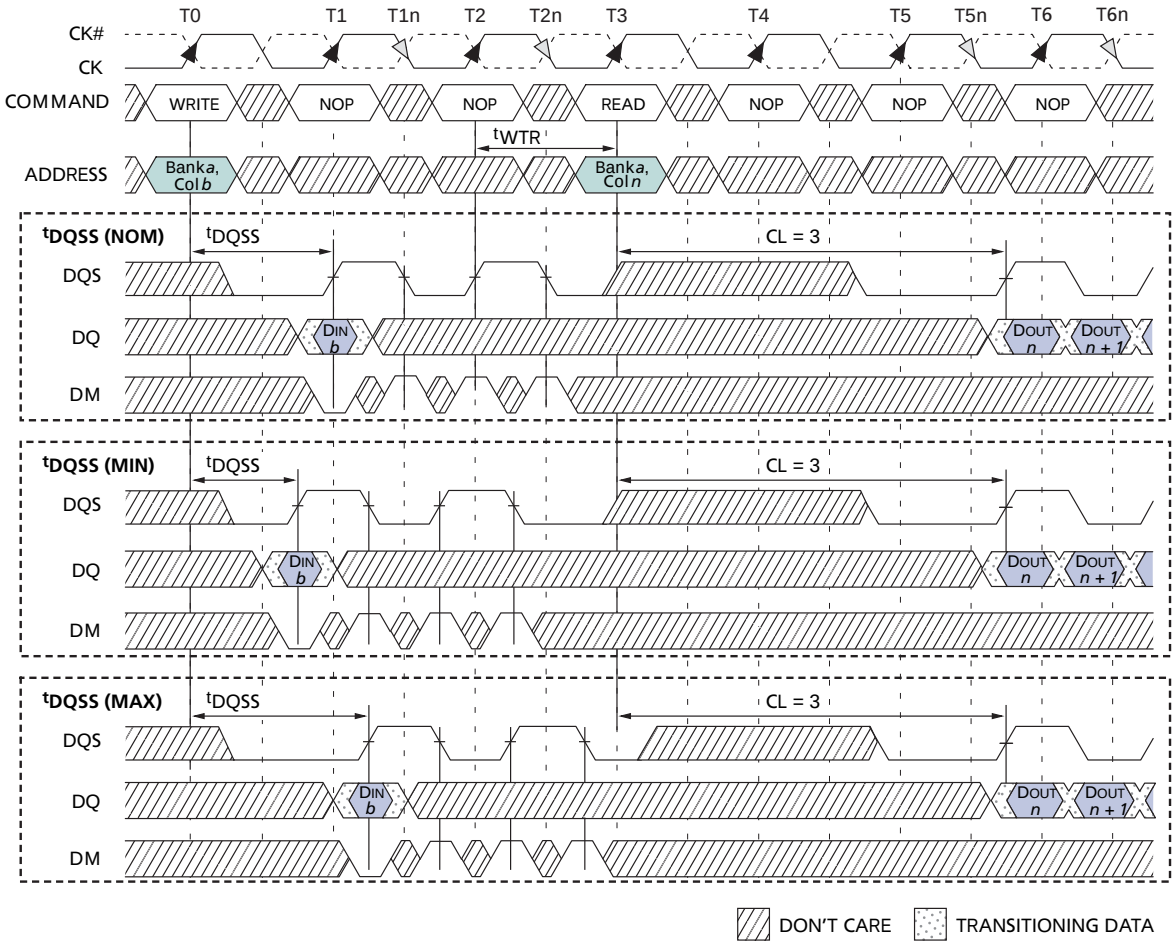
Notes:
1. DIN *b* = data-in for column *b*; DOUT *n* = data-out for column *n*.
2. An uninterrupted burst of 4 is shown.
3. tWTR is referenced from the first positive CK edge after the last data-in pair.
4. The READ and WRITE commands are to same device. However, the READ and WRITE commands may be to different devices, in which case tWTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 23: WRITE-to-READ – Interrupting



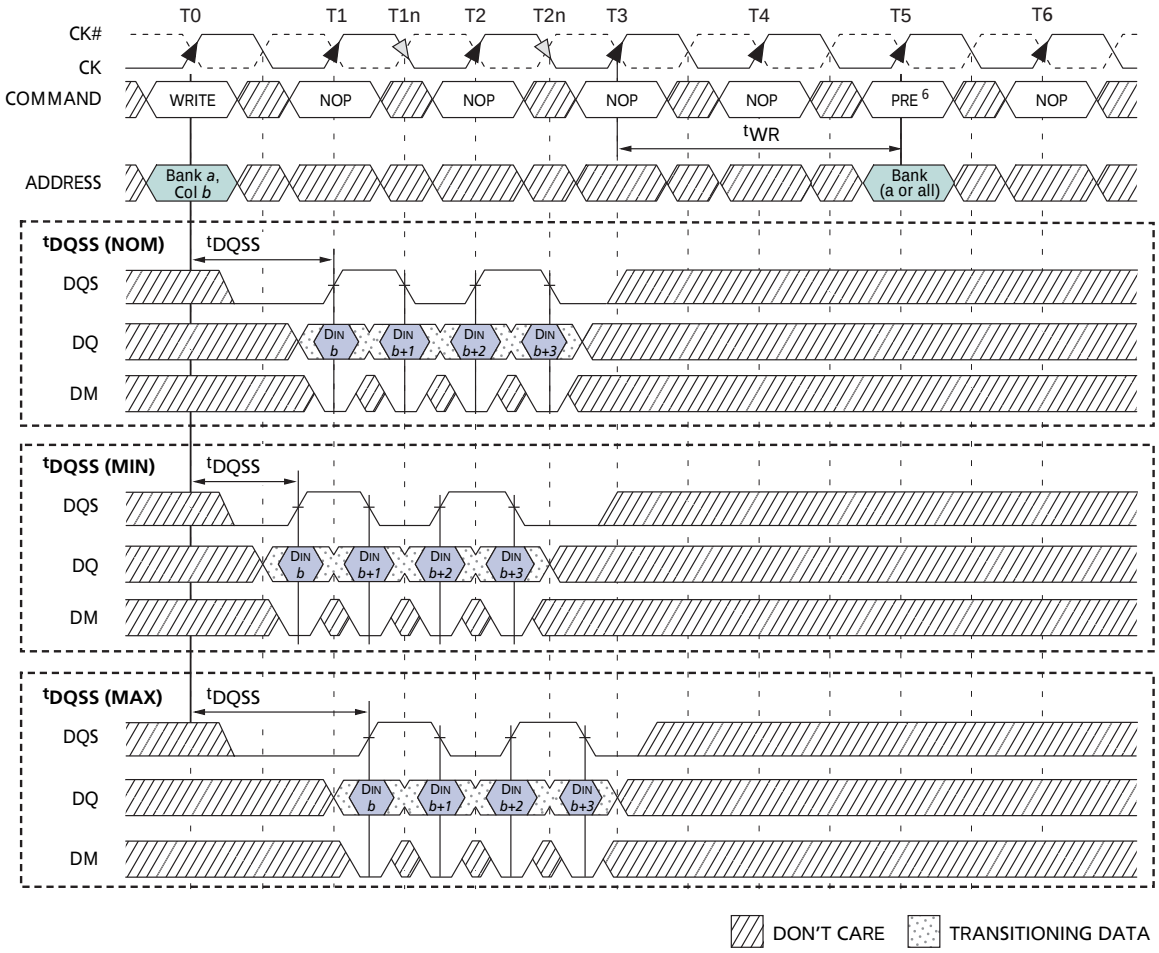
Notes:
1. DIN *b* = data-in for column *b*; DOUT *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; two data elements are written.
3. tWTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 24: WRITE-to-READ – Odd Number of Data, Interrupting



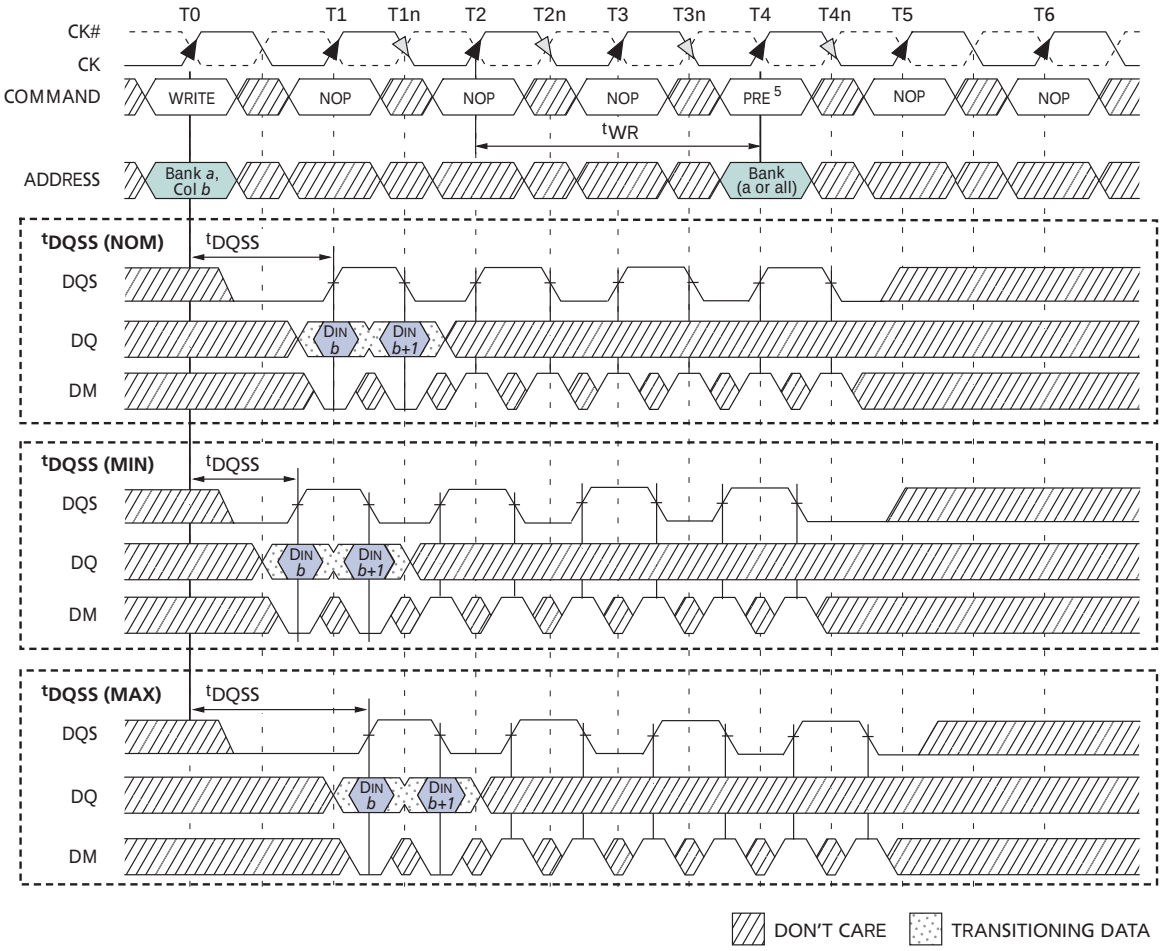
Notes:
1. DIN *b* = data-in for column *b*; DOUT *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; one data element is written, three are masked.
3. tWTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 25: WRITE-to-PRECHARGE – Uninterrupting



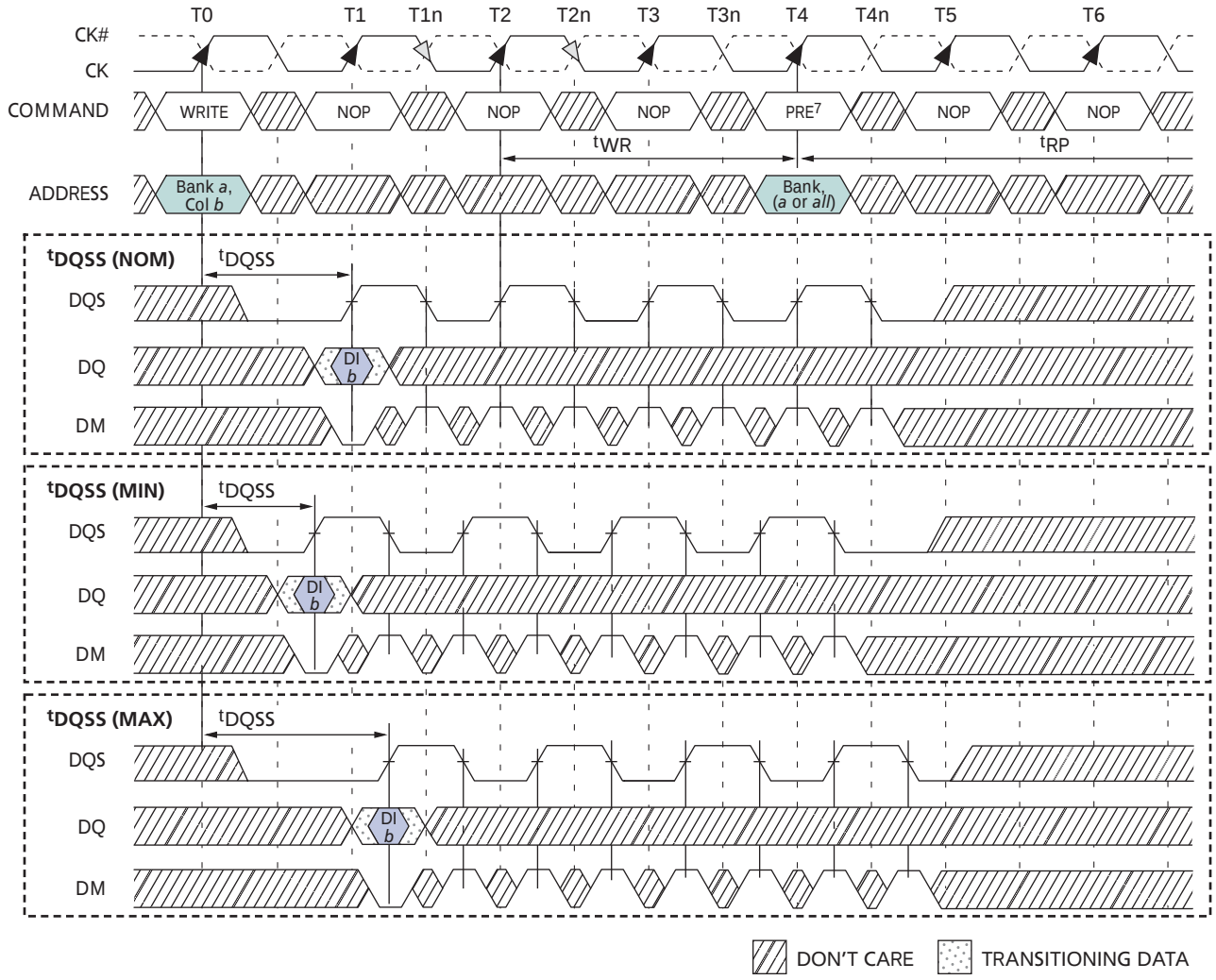
Notes:
1. DIN *b* = data-in for column *b*.
2. An uninterrupted burst of 4 is shown.
3. tWR is referenced from the first positive CK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the PRECHARGE command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

Figure 26: WRITE-to-PRECHARGE – Interrupting



Notes:
1. DIN *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. PRE = PRECHARGE command.
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If a burst of 4 was used, DQS and DM would not be required at T3, T3n, T4, and T4n.

Figure 27: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting

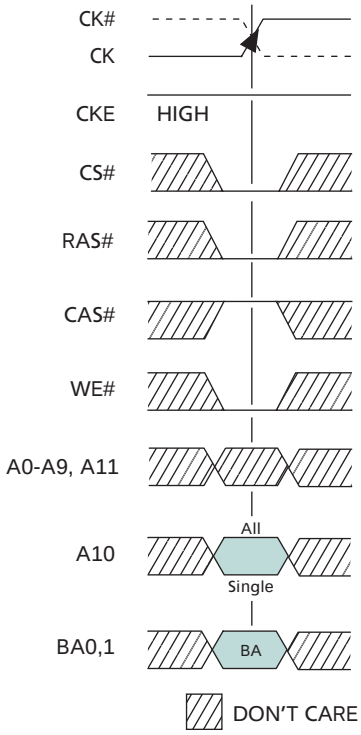


Notes:
1. DIN *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. PRE = PRECHARGE command.
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If a burst of 4 was used, DQS and DM would not be required at T3, T3n, T4, and T4n.

PRECHARGE

The PRECHARGE command (Figure 28) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 28: PRECHARGE Command



Notes: 1. BA = Bank Address.
All = All banks to be Precharged, BA1, BA0 are "Don't Care."
Single = Only bank selected by BA1 and BA0 will be precharged.

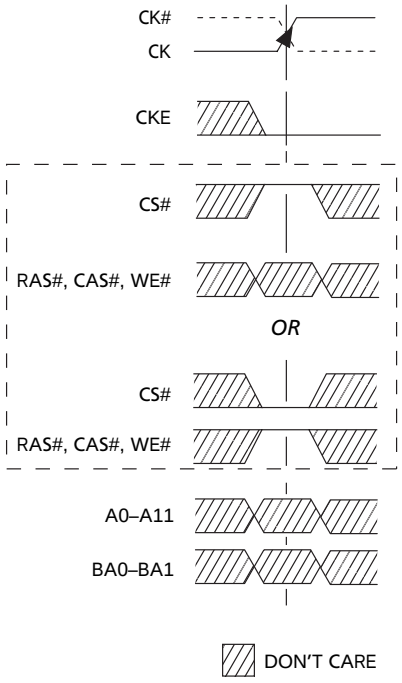
Power-Down

Power-down is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, including CK and CK#. Exiting power-down requires the device to be at the same voltage as when it entered power-down and a stable clock.

Note: The power-down duration is limited by the refresh requirements of the device.

While in power-down, CKE LOW must be maintained at the inputs of the Mobile DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until ^{t}XP is satisfied.

Figure 29: Power-Down Command (Active or Precharge)



Truth Tables

Table 8: Truth Table – CKE
Notes: 1–5

CKE_{n-1}	CKE_n	Current State	$COMMAND_n$	$ACTION_n$	Notes
L	L	(Active) Power-Down	X	Maintain (active) power-down	
L	L	(Precharge) Power-Down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	(Active) Power-Down	DESELECT or NOP	Exit (active) power-down	6, 7
L	H	(Precharge) Power-Down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	(Active) power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 10 on page 45		
H	H		See Table 10 on page 45		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n,* and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. ^tCKE pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the ^tXP period.
7. The clock must toggle at least once during the ^tXP period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the ^tXSR period.
9. The clock must toggle at least once during the ^tXSR period.

Table 9: Truth Table – Current State Bank *n* - Command to Bank *n*

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH and after ^tXSR has been met (if the previous state was self refresh) and after ^tXP has been met (if the previous state was power-down).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 9, and according to Table 10.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. Once ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the row active state.

   Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

   Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR SDRAM will be in the all banks idle state.

   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the Mobile DDR SDRAM will be in the all banks idle state.

   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 10: Truth Table – Current State Bank *n* - Command to Bank *m*
Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH and after ^tXSR has been met (if the previous state was self refresh) or after ^tXP has been met (if the previous state was power-down).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^tRP has been met.
   - Row Active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

Read with auto precharge enabled: See following text – 3a
Write with auto precharge enabled: See following text – 3a

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto

precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.

This device supports concurrent auto precharge such that when a read with auto precharge enabled or a write with auto precharge is enabled any command to other banks is allowed, long as that command does not interrupt the read or write data transfer already in process. either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	[1 + (BL/2)] ^{t}CK + ^{t}WTR
	WRITE or WRITE w/AP	(BL/2) ^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK
READ w/AP	READ or READ w/AP	(BL/2) × ^{t}CK
	WRITE or WRITE w/AP	[CL_{RU} + (BL/2)] ^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK

CL_{RU} = CAS latency (CL) rounded up to the next integer
BL = Bust length

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
Vdd supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V	1
VddQ supply voltage relative to $V_{SS}Q$	$V_{DD}Q$	–0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	2

Notes: 1. V_{DD}, $V_{DD}Q$, and $V_{DD}L$ must be within 300mV of each other at all times.
2. Voltage on any I/O may not exceed voltage on $V_{DD}Q$.

Table 12: AC/DC Electrical Characteristics and Operating Conditions
Notes: 1–5; notes appear on pages 52–54; V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.9	V	31
I/O supply voltage	$V_{DD}Q$	1.7	1.9	V	31
Address and Command Inputs					
Input voltage high	V_{IH}	0.8 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	25, 32
Input voltage low	V_{IL}	–0.3	0.2 × $V_{DD}Q$	V	25, 32
Clock Inputs (CK, CK#)					
DC input voltage	V_{IN}	–0.3	$V_{DD}Q$ + 0.3	V	27
DC input differential voltage	$V_{ID(DC)}$	0.4 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	8, 27
AC input differential voltage	$V_{ID(AC)}$	0.6 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	8, 27
AC differential crossing voltage	V_{IX}	0.4 × $V_{DD}Q$	0.6 × $V_{DD}Q$	V	9, 27
Data Inputs					
DC input high voltage	$V_{IH(DC)}$	0.7 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	25, 28, 32
AC input high voltage	$V_{IH(AC)}$	0.8 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	25, 28, 32
DC input low voltage	$V_{IL(DC)}$	–0.3	0.3 × $V_{DD}Q$	V	25, 28, 32
AC input low voltage	$V_{IL(AC)}$	–0.3	0.2 × $V_{DD}Q$	V	25, 28, 32
Data Outputs					
DC output high voltage: Logic 1 (I_{OH} = -0.1mA)	V_{OH}	0.9 × $V_{DD}Q$	–	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	–	0.1 × $V_{DD}Q$	V	
Leakage Current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)	II	–1	1	µA	
Output leakage current (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)	IOZ	–5	5	µA	

Table 13: Capacitance
Notes: 13; notes appear on pages 52–54

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQs, DQS, DM	CDIO	–	1.00	pF	21
Delta input capacitance: Command and address	CDI	–	1.75	pF	26
Delta input capacitance: CK, CK#	CDCK	–	0.25	pF	26
Input/output capacitance: DQs, DQS, DM	CIO	3.0	5.5	pF	
Input capacitance: Address	CI	1.5	4.0	pF	
Input capacitance: Command	CI	1.5	5.0	pF	
Input capacitance: CK, CK#	CCK	1.5	4.5	pF	

Table 14: IDD Specifications and Conditions
Notes: 1–5, 7, 10, 12, 14 notes appear on pages 52–54; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

Parameter/Condition	Symbol	Max		Units	Notes
		-75	-10		
Operating one bank active precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable	IDD0	80	75	mA	19
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD2P	200	200	µA	20, 28
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD2PS	200	200	µA	20, 28
Precharge non power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD2N	25	25	mA	34
Precharge non power-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD2NS	15	15	mA	34
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD3P	3	3	mA	20, 28
Active power-down standby current: Clock stopped; One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD3PS	3	3	mA	20, 28
Active non power-down standby: One bank active; CKE = HIGH; CS = HIGH; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are switching every two cycles; Data bus inputs are stable	IDD3N	25	25	mA	19
Active non-power-down standby: Clock stopped; One bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching every two clock cycles; Data bus inputs are stable	IDD3NS	20	20	mA	19
Operating burst read: One bank active; BL = 4; $^{t}CK = {}^{t}CK$ (MIN); Continuous read bursts; IOUT = 0mA; Address inputs are switching; 50% data changing each burst	IDD4R	95	90	mA	19
Operating burst write: One bank active; BL = 4; $^{t}CK = {}^{t}CK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst	IDD4W	95	90	mA	19

Table 14: IDD Specifications and Conditions (continued)

Notes: 1–5, 7, 10, 12, 14 notes appear on pages 52–54; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

Parameter/Condition		Symbol	Max		Units	Notes
			-75	-10		
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	tRC = tRC (MIN)	IDD5	105	100	mA	35
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH; tCK = tCK (MIN); address and data bus inputs are stable	tRC = 15.625µs	IDD5a	5	5	mA	24, 35
Self refresh: CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full Array, 85°C	IDD6a	300		µA	11, 36
	Full Array, 70°C	IDD6b	220		µA	11, 36
	Full Array, 45°C	IDD6c	180		µA	11, 36
	Full Array 15°C	IDD6d	160		µA	11, 36
	Half Array, 85°C	IDD6a	220		µA	11, 36
	Half Array, 70°C	IDD6b	180		µA	11, 36
	Half Array, 45°C	IDD6c	160		µA	11, 36
	Half Array, 15°C	IDD6d	150		µA	11, 36
	1/4 Array, 85°C	IDD6a	180		µA	11, 36
	1/4 Array, 70°C	IDD6b	160		µA	11, 36
	1/4 Array, 45°C	IDD6c	150		µA	11, 36
	1/4 Array, 15°C	IDD6d	145		µA	11, 36

Figure 30: Typical Self-Refresh Current vs. Temperature

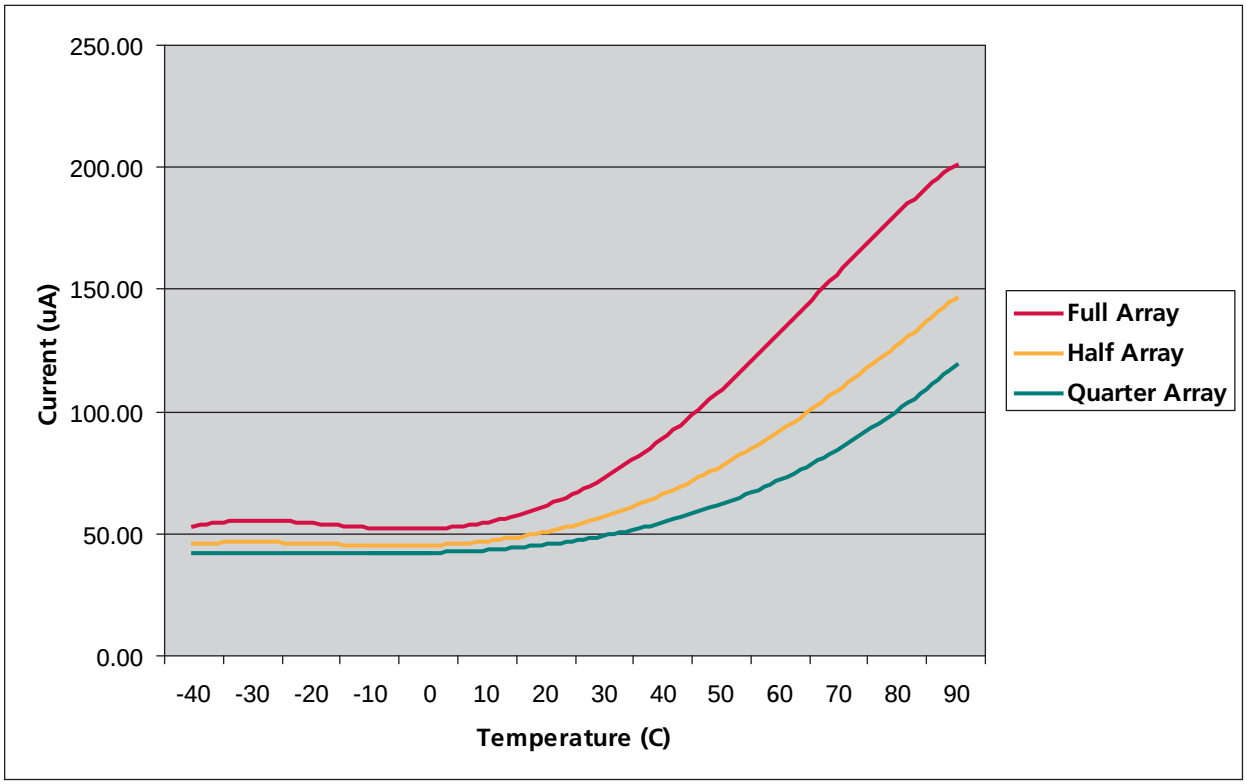


Table 15: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–6, 27; notes appear on pages 52–54; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

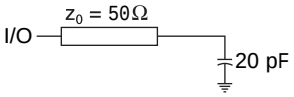
AC Characteristics			-75		-10			
Parameter		Symbol	Min	Max	Min	Max	Units	Notes
Access window of DQs from CK/CK#	CL = 3	$^tAC(3)$	2.5	6.0	2.0	7.0	ns	7
	CL = 2	$^tAC(2)$	2.0	6.5	2.0	7.0		
Clock cycle time	CL = 3	$^tCK(3)$	7.5	–	9.6	–	ns	7
	CL = 2	$^tCK(2)$	12	–	15	–		
CK high-level width		^tCH	0.45	0.55	0.45	0.55	^tCK	
CK low-level width		^tCL	0.45	0.55	0.45	0.55	^tCK	
Minimum ^tCKE HIGH/LOW time		^tCKE	2	–	2	–	^tCK	
Auto precharge write recovery + precharge time		^tDAL	–	–	–	–		38
DQ and DM input hold time relative to DQS		^tDH	0.75	–	1.1	–	ns	23, 28, 37
DQ and DM input setup time relative to DQS		^tDS	0.75	–	1.1	–	ns	23, 28, 37
DQ and DM input pulse width (for each input)		^tDIPW	$^tDS + ^tDH$		$^tDS + ^tDH$		ns	39
Access window of DQS from CK/CK#		^tDQSCK	2.5	6.0	2.5	7.0	ns	
DQS input high-pulse width		^tDQSH	0.4	0.6	0.4	0.6	^tCK	
DQS input low-pulse width		^tDQSL	0.4	0.6	0.4	0.6	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.6	–	0.7	ns	22, 23
WRITE command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	0.2	–	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	0.2	–	^tCK	
Data valid output window (DVW)		na	$^tQH - ^tDQSQ$		$^tQH - ^tDQSQ$		ns	22
Half-clock period		^tHP	$^tCH, ^tCL$	–	$^tCH, ^tCL$	–	ns	29
Data-out High-Z window from CK/CK#	CL = 3	$^tHZ(3)$	–	6.0	–	7.0	ns	15, 33
	CL = 2	$^tHZ(2)$	–	6.5	–	7.0	ns	
Data-out Low-Z window from CK/CK#		^tLZ	1.0	–	1.0	–	ns	15
Address and control input hold time (fast slew rate)		^tIH_F	1.3	–	1.5	–	ns	14, 37
Address and control input hold time (slow slew rate)		^tIH_S	1.5	–	1.7	–	ns	14, 37
Address and control input setup time (fast slew rate)		^tIS_F	1.3	–	1.5	–	ns	14, 37
Address and control input setup time (slow slew rate)		^tIS_S	1.5	–	1.7	–	ns	14, 37
Address and control input pulse width		^tIPW	3.0	–	3.4	–	ns	39
LOAD MODE REGISTER command cycle time		^tMRD	2	–	2	–	^tCK	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	$^tHP - ^tQHS$	–	$^tHP - ^tQHS$	–	ns	22, 23
Data hold skew factor		^tQHS	–	0.75	–	1	ns	
ACTIVE-to-PRECHARGE command		^tRAS	45	70,000	50	70,000	ns	30
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^tRC	75	–	80	–	ns	
ACTIVE-to-READ or WRITE delay		^tRCD	22.5	–	30	–	ns	
Average periodic refresh interval		^tREFI	–	15.6	–	15.6	µs	20
AUTO REFRESH command period		^tRFC	97.5	–	80	–	ns	35
PRECHARGE command period		^tRP	22.5	–	30	–	ns	

Table 15: Electrical Characteristics and Recommended AC Operating Conditions (continued)
Notes: 1–6, 27; notes appear on pages 52–54; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

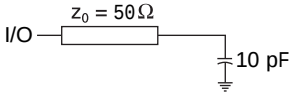
AC Characteristics			-75		-10			
Parameter		Symbol	Min	Max	Min	Max	Units	Notes
DQS read preamble	CL = 3	^{t}RPRE(3)	0.9	1.1	0.9	1.1	^{t}CK	33
	CL = 2	^{t}RPRE(2)	0.5	1.1	0.5	1.1	^{t}CK	33
DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	^{t}CK	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	15	–	15	–	ns	
DQS write preamble		^{t}WPRE	0.25	–	0.25	–	^{t}CK	
DQS write preamble setup time		^{t}WPRES	0	–	0	–	ns	17, 18
DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	^{t}CK	16
Write recovery time		^{t}WR	15	–	15	–	ns	
Internal WRITE to READ command delay		^{t}WTR	1	–	1	–	^{t}CK	
Exit power-down mode to first valid command		^{t}XP	8.8	–	25	–	ns	41
Exit SELF REFRESH to first valid command		^{t}XSR	120	–	120	–	ns	40

Notes

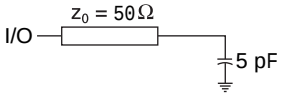
1. All voltages referenced to Vss.
2. All parameters assume proper device initialization.
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load:



Full-drive strength



Half-drive strength



Quarter-drive strength

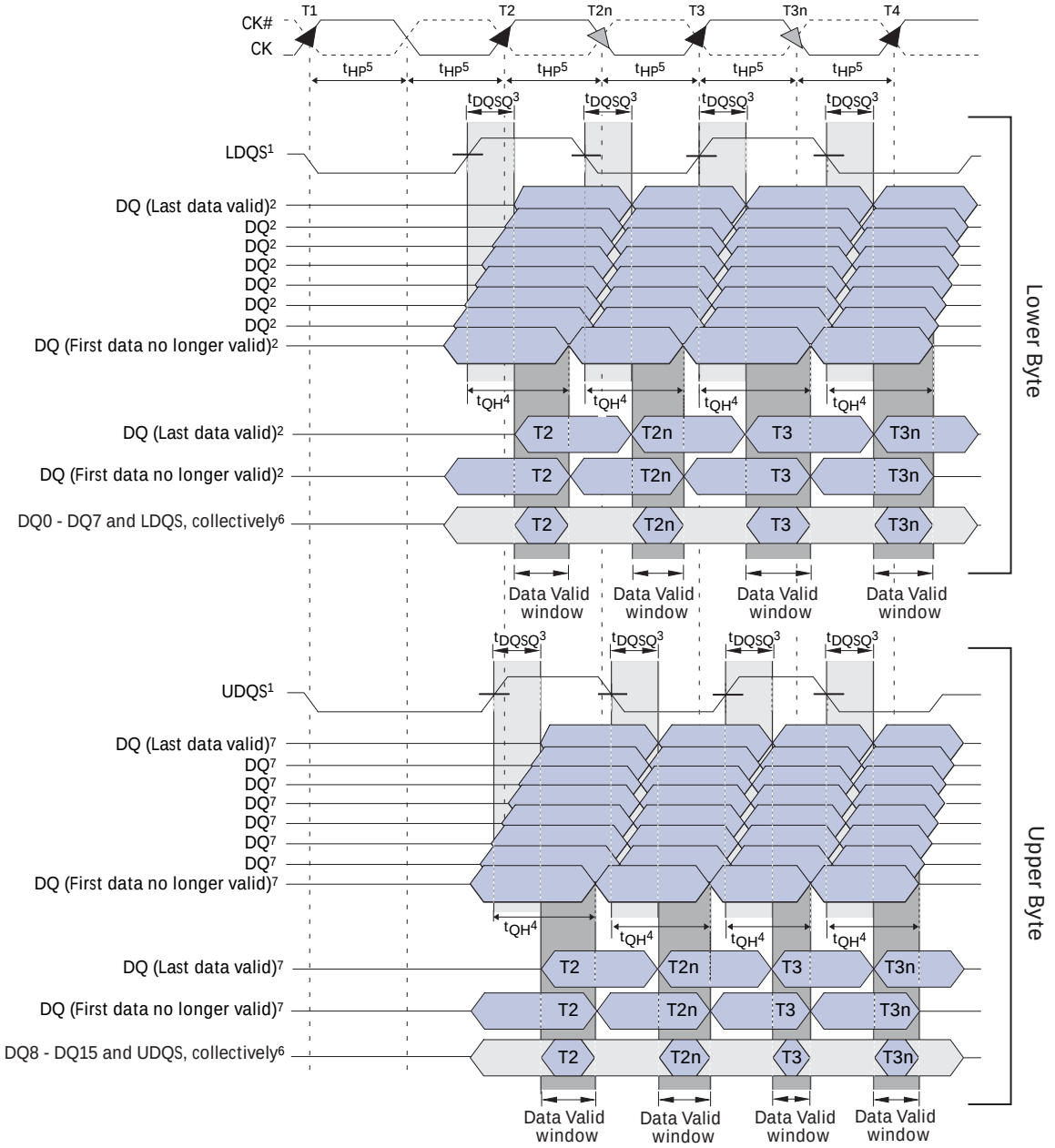
5. Timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VDDQ/2 (or to the crossing point for CK/CK#). The output timing reference voltage level is VDDQ/2.
6. All AC timings assume an input slew rate of 1V/ns.
7. CAS latency definition: for CL = 2, the first data element is valid at (^{t}CK + ^{t}AC) after the clock at which the READ command was registered; for CL = 3, the first data element is valid at (2 × ^{t}CK + ^{t}AC) after the first clock at which the READ command was registered.
8. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of VIX is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
10. IDD is dependent on cycle rate, and may be affected by output loading if VDD and VDDQ are supplied from the same source. Specified values are obtained with minimum cycle time for CL = 3 with the outputs open.
11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly.
13. This parameter is sampled. VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, f = 100 MHz, T_A = 25°C, VOUT(DC) = VDDQ/2, VOUT (peak-to-peak) = 0.2V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
14. Fast command/address input slew rate ≥ 1V/ns. Slow command/address input slew rate ≥ 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 0.5V/ns. ^{t}IH remains constant.
15. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
17. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
18. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command.
19. MIN (^{t}RC or ^{t}RFC) for IDD measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
20. The refresh period equals 64ms. This equates to an average refresh rate of 15.625µs.
21. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
22. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}HP - ^{t}QHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
23. Referenced to each output group: LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
24. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC), or VIH(AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
26. The input capacitance per ball group will not differ by more than this maximum amount for any given device.
27. CK and CK# input slew rate must be ≥ 1V/ns (2V/ns if measured differentially).
28. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
29. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively.
30. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
31. Any positive glitch must be less than 1/3 of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -150mV or 1.6V, whichever is more positive.
32. VIH overshoot: VIH (MAX) = VDDQ + 0.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = -0.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
33. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
34. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
35. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC later.

36. Values for IDD6 85°C are guaranteed for the entire temperature range. All other IDD6 values are estimated.
37. The transition time for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between VIL(DC) to VIH(AC) for rising input signals and VIH(DC) to VIL(AC) for falling input signals.
38. ^{t}DAL = (^{t}WR/^{t}CK) + (^{t}RP/^{t}CK): for each term, if not already an integer, round to the next higher integer.
39. These parameters guarantee device timing but they are not necessarily tested on each device.
40. Clock must be toggled a minimum of two times during this period.
41. Clock must be toggled a minimum of one time during this period.

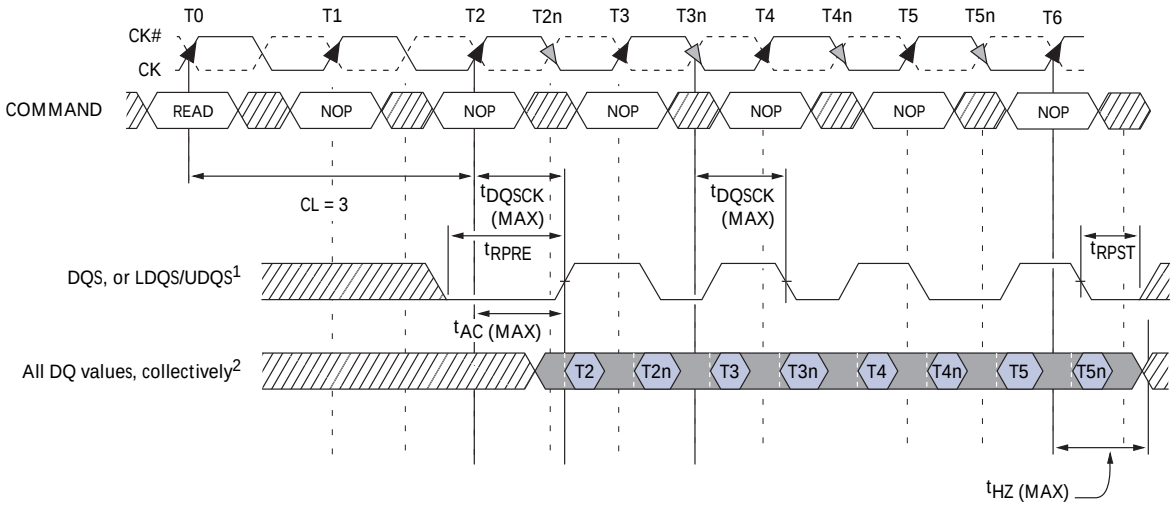
Timing Diagrams

Figure 31: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



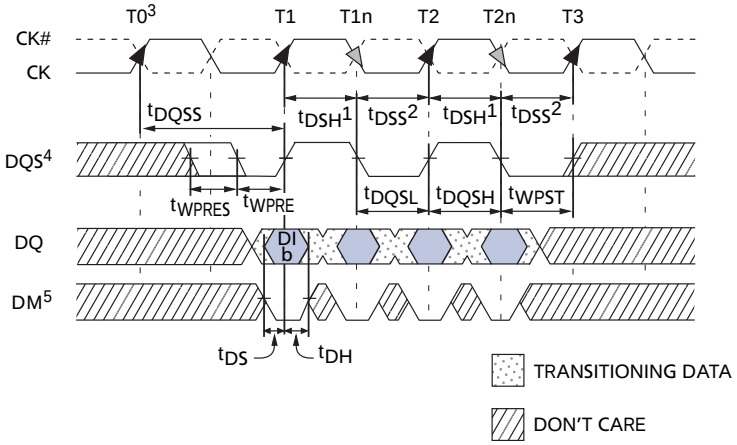
Notes:
1. DQ transitioning after DQS transition define ^{t}DQSQ window. LDQS defines the lower byte and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is ^{t}QH minus ^{t}DQSQ.
7. DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.

Figure 32: Data Output Timing – ^{t}AC and ^{t}DQSCK



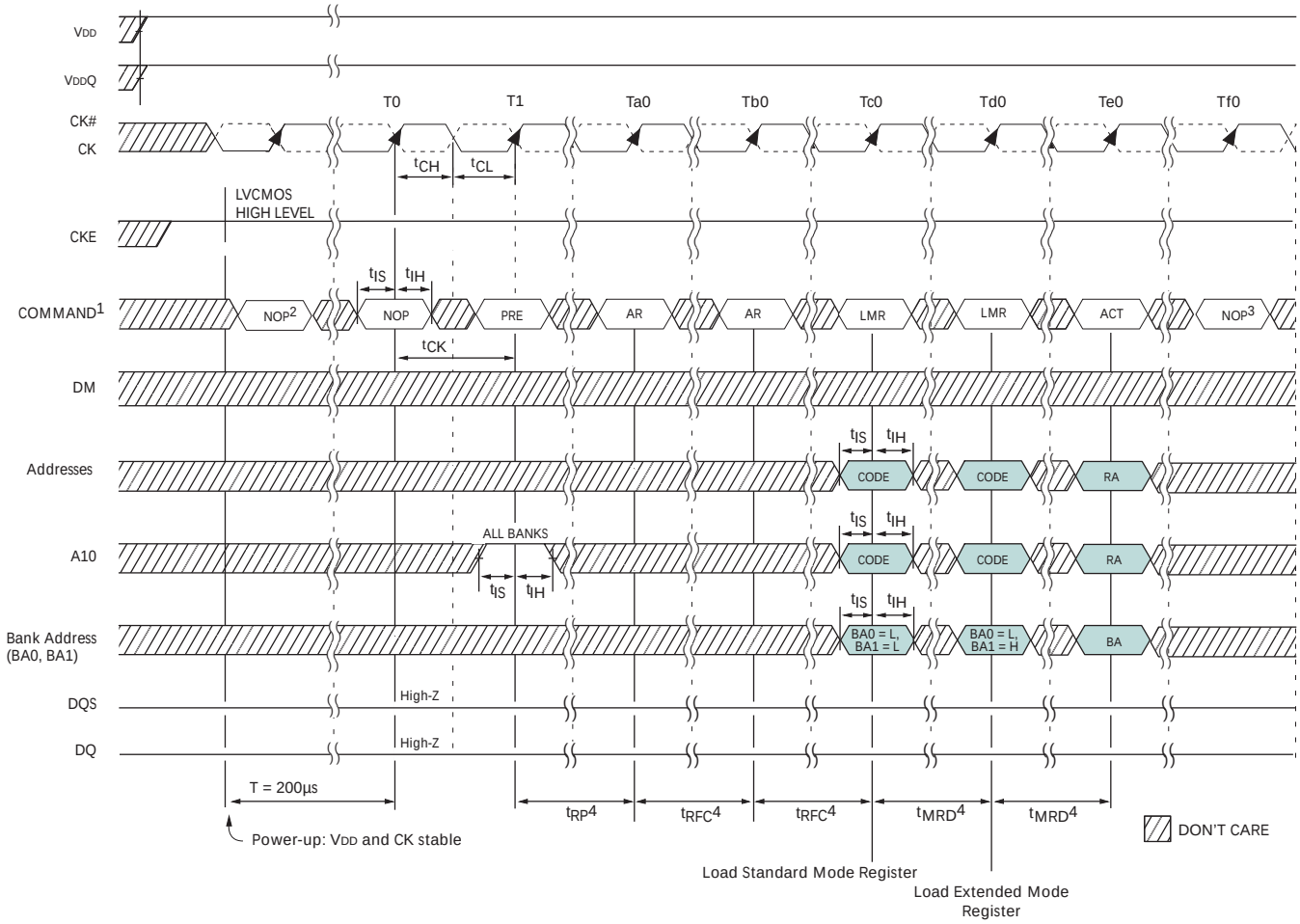
Notes:
1. DQ transitioning after DQS transition define ^{t}DQSQ window.
2. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
3. ^{t}AC is the DQ output window relative to CK, and is the "long term" component of DQ skew.

Figure 33: Data Input Timing



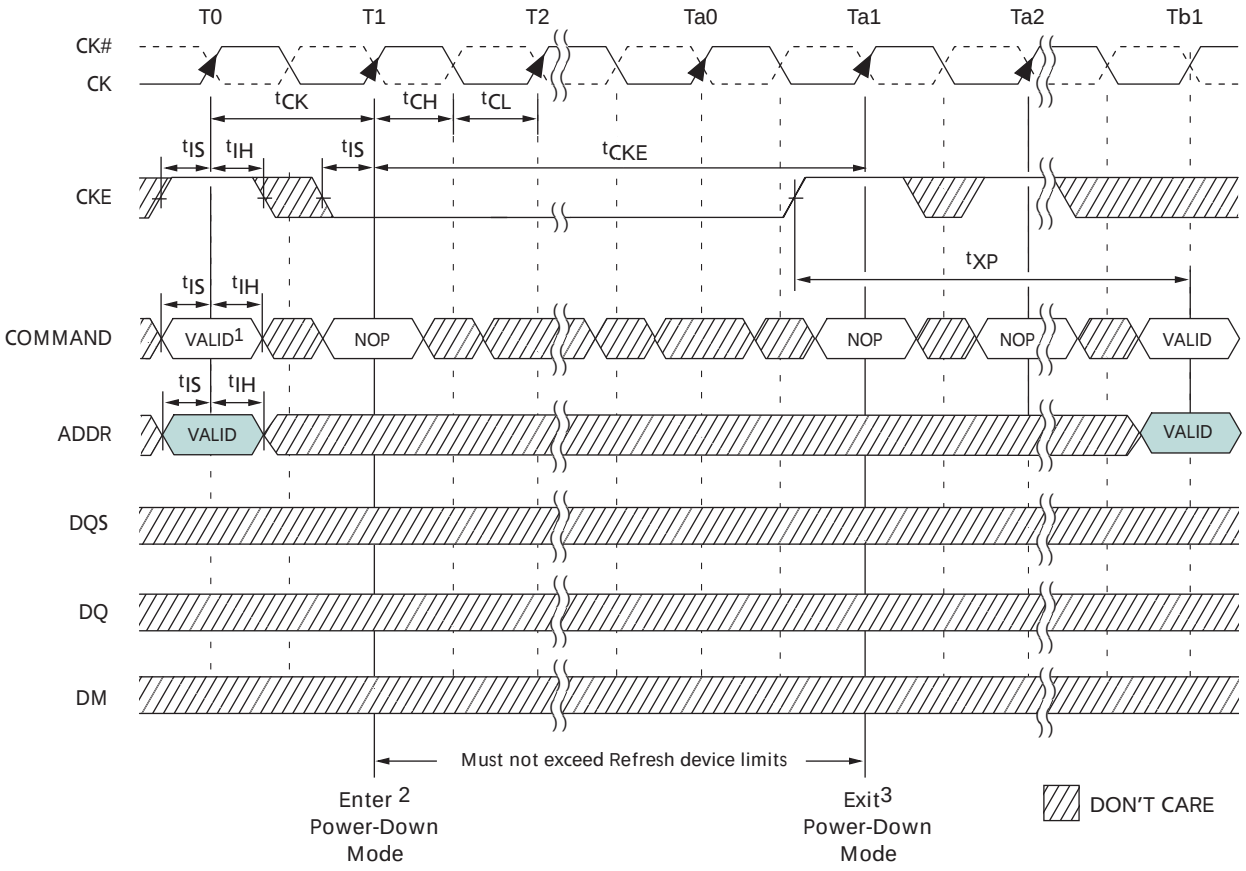
Notes:
1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. WRITE command issued at T0.
4. LDQS controls the lower byte and UDQS controls the upper byte.
5. LDM controls the lower byte and UDM controls the upper byte.

Figure 34: Initialize and Load Mode Registers



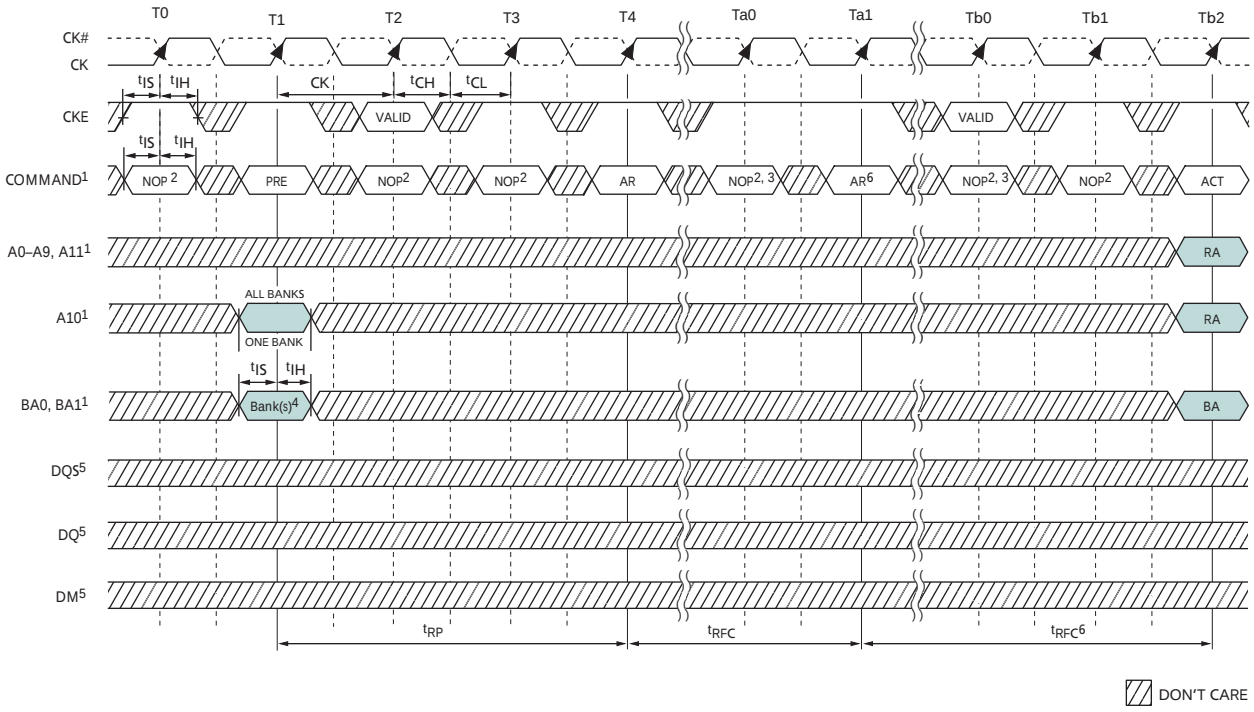
Notes:
1. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row address, BA = Bank address.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

Figure 35: Power-Down Mode (Active or Precharge)



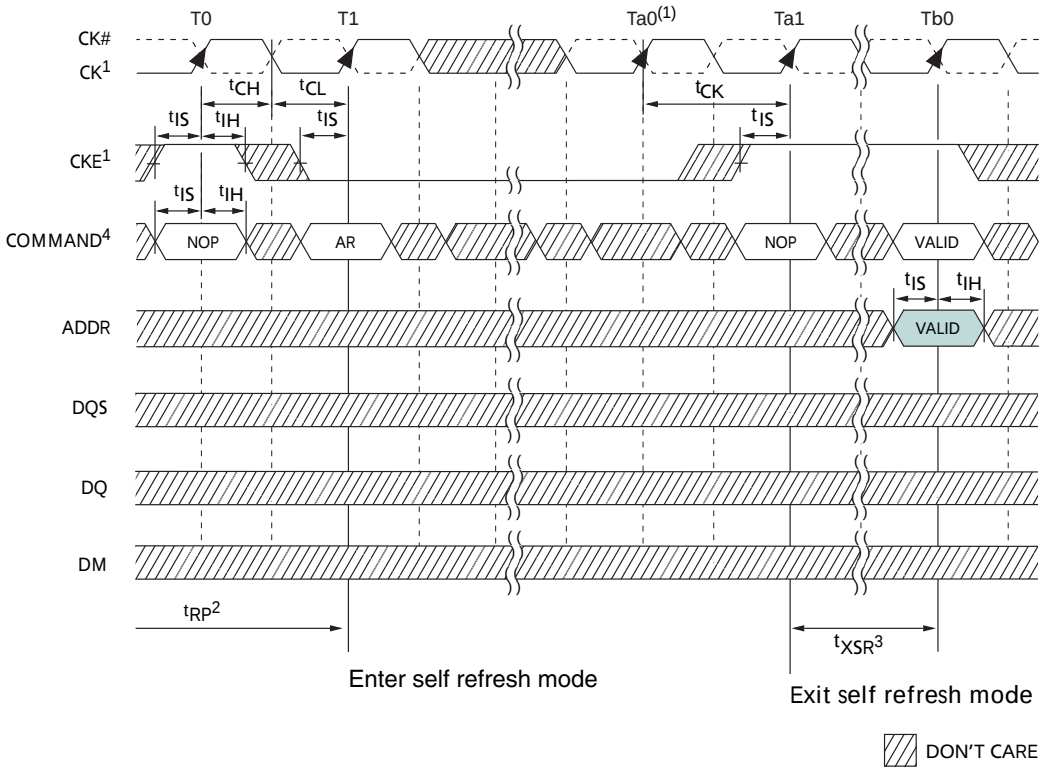
Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during ^{t}XP time.

Figure 36: Auto Refresh Mode



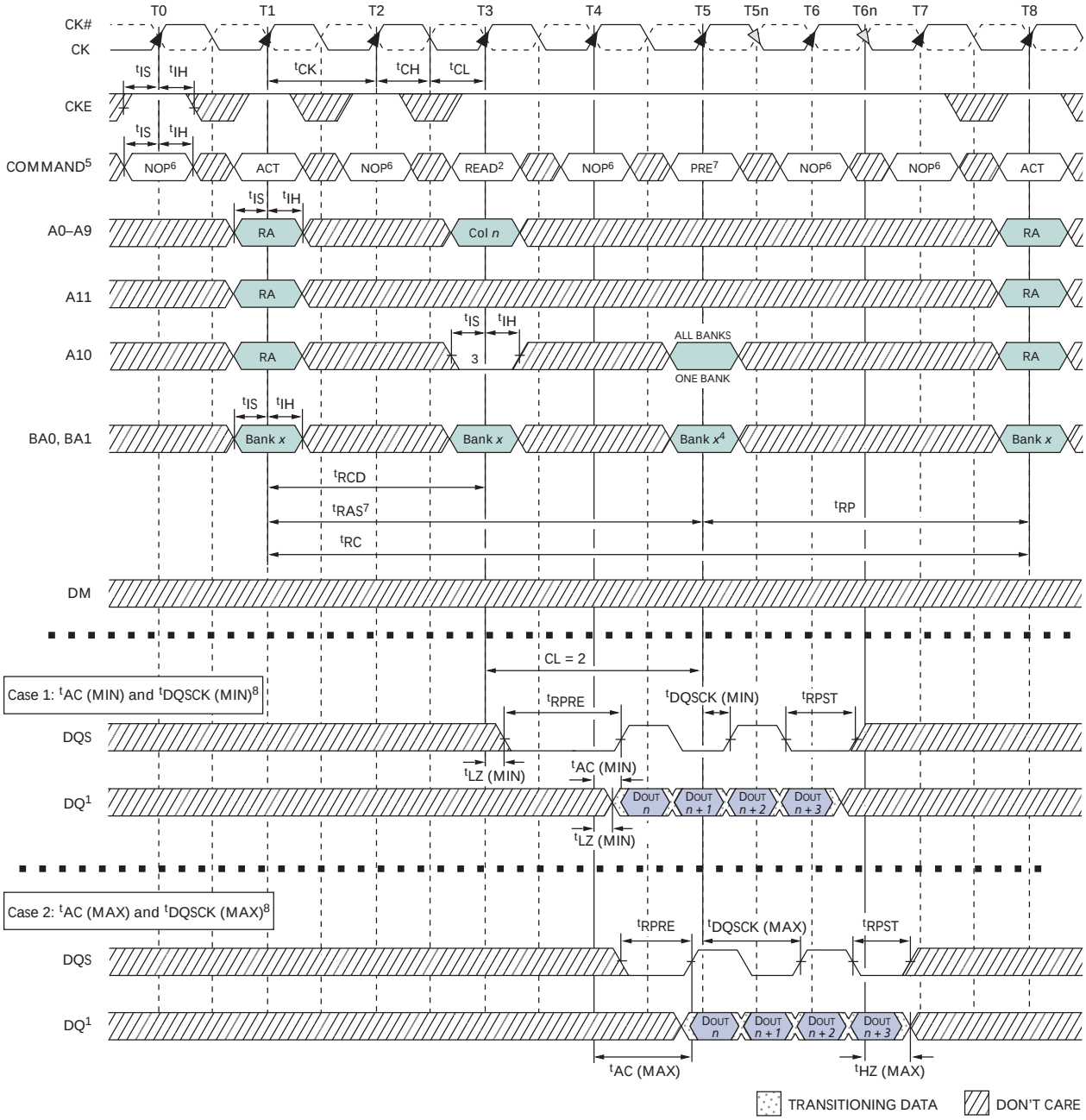
Notes:
1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row address, BA = Bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after ^{t}RFC time, CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

Figure 37: Self Refresh Mode



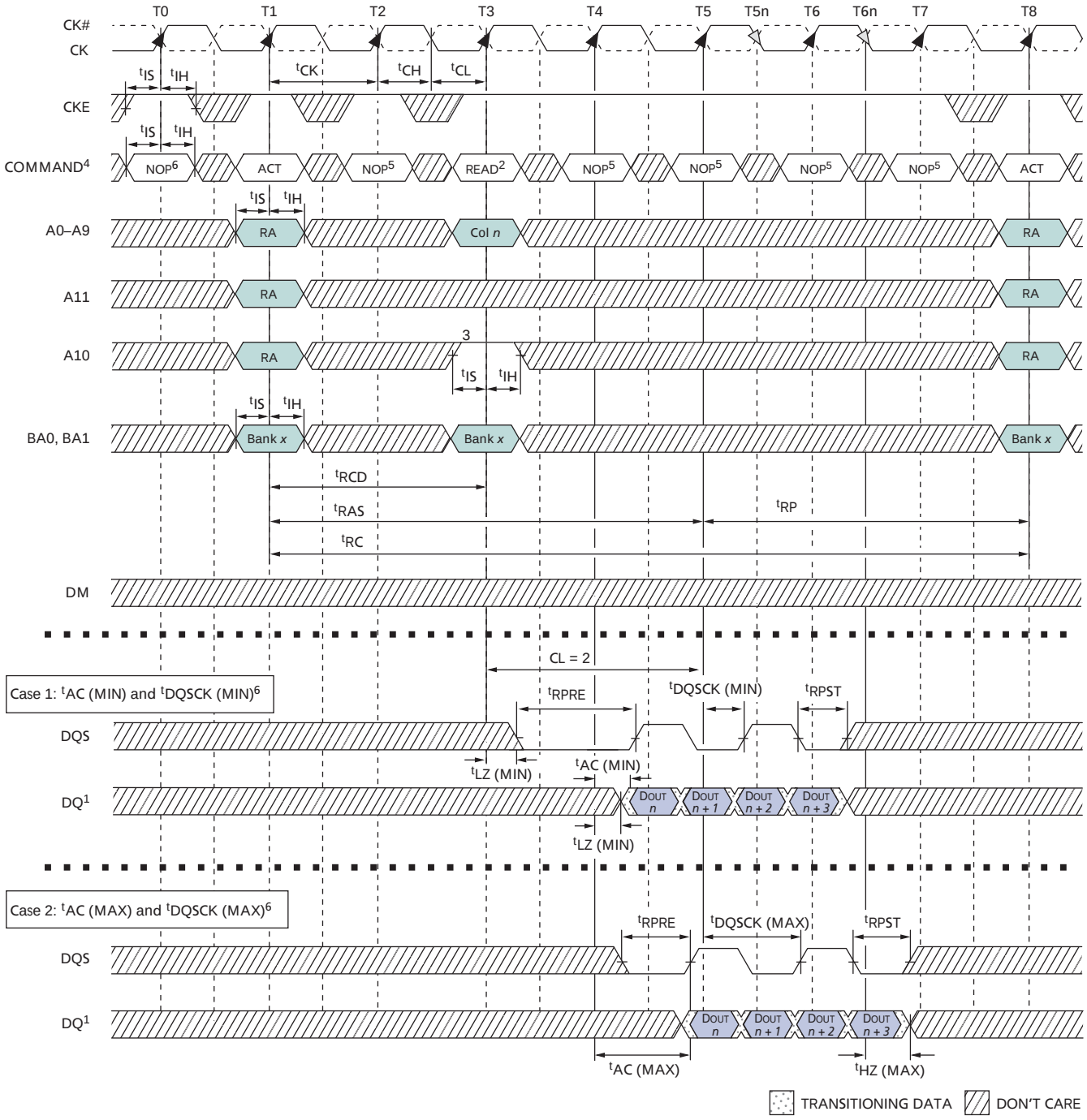
Notes:
1. Clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT are required for ^{t}XSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.

Figure 38: Bank Read – Without Auto Precharge



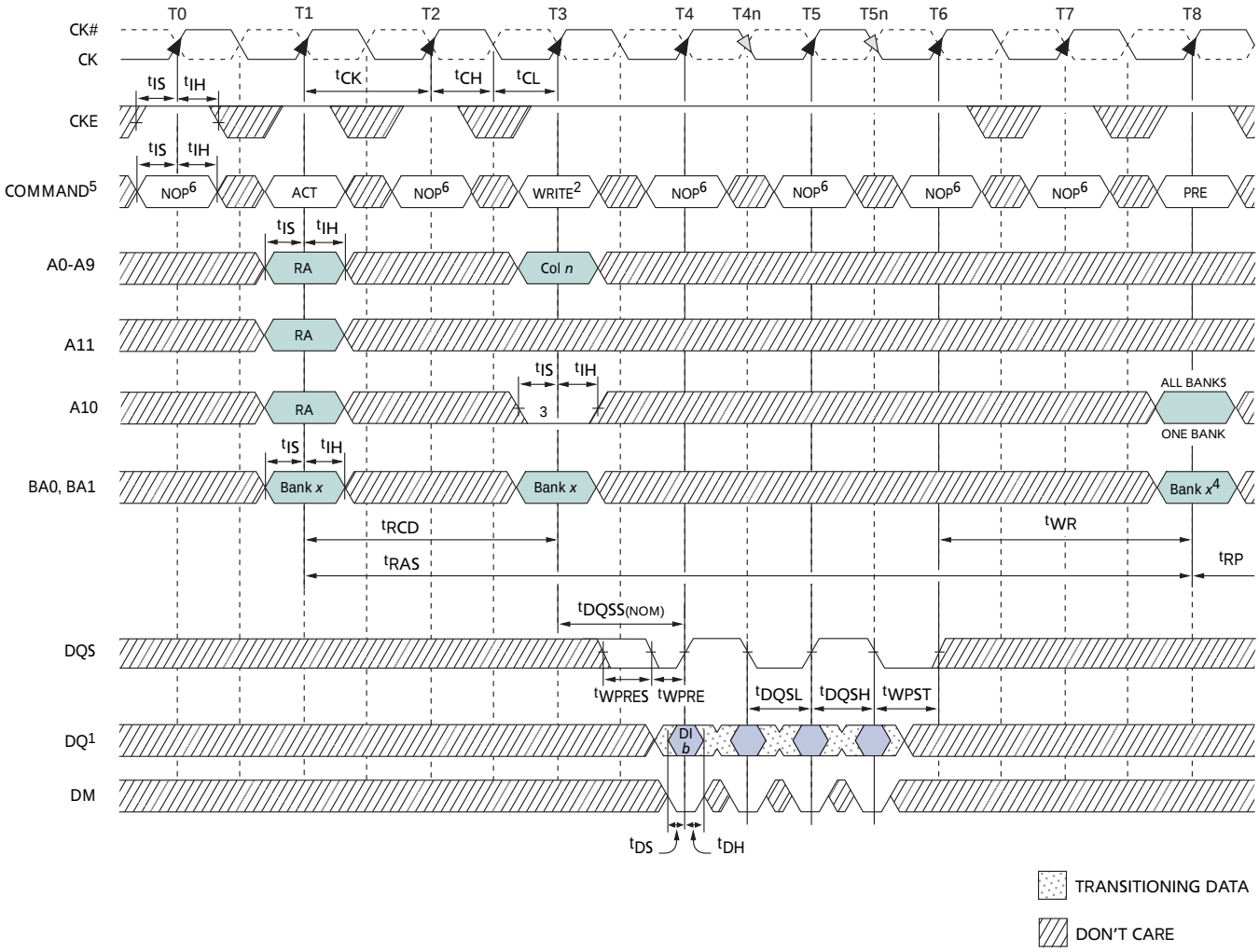
Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "don't care" if A10 is HIGH at T5.
5. RA = row address, BA = bank address, PRE = PRECHARGE, ACT = ACTIVE.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T5 if tRAS minimum is met.
8. Refer to Figure 31 on page 55 and Figure 32 on page 56 for detailed DQS and DQ timing.

Figure 39: Bank Read – with Auto Precharge



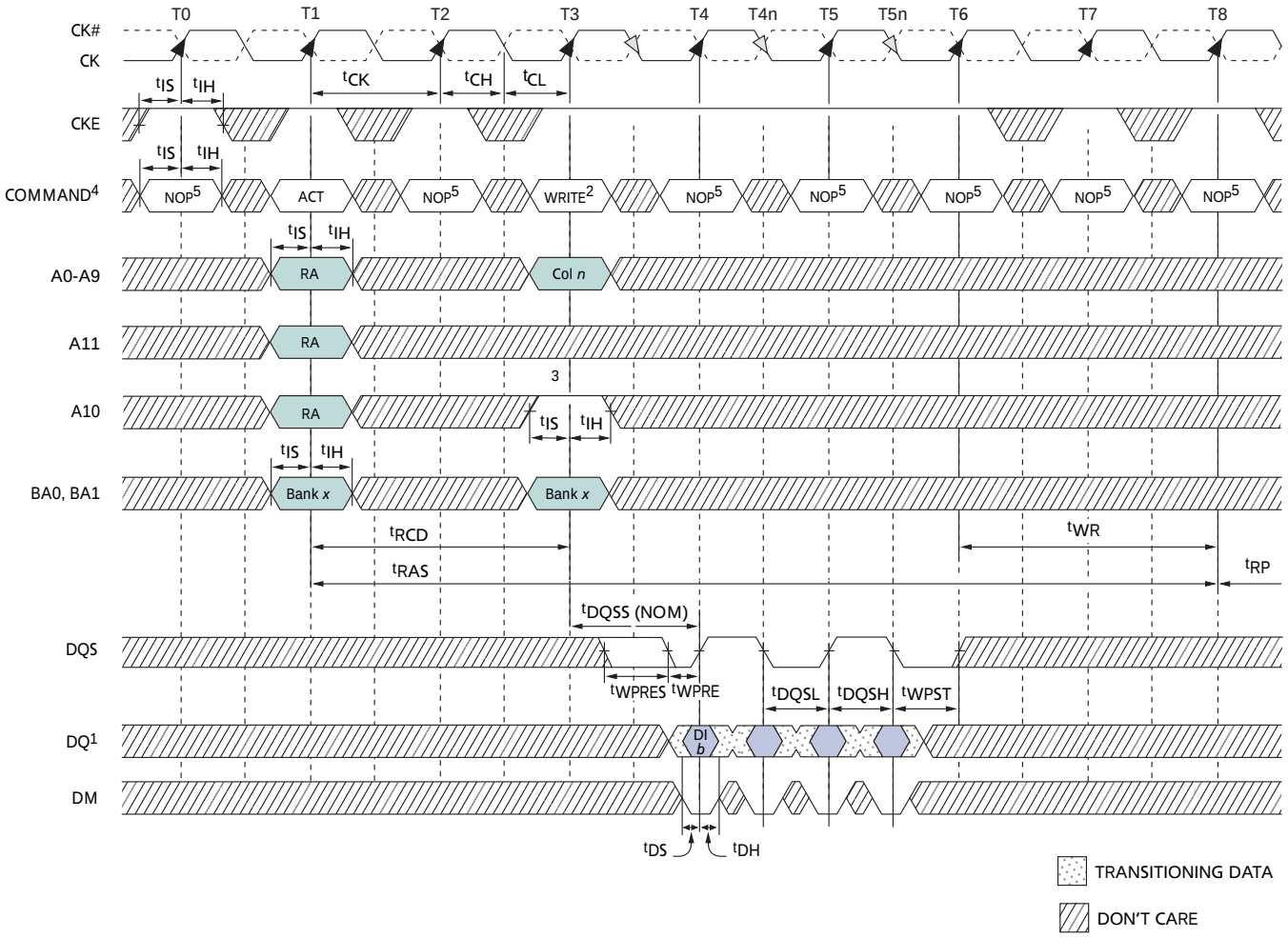
Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. Refer to Figure 31 on page 55 and Figure 32 on page 56 for detailed DQS and DQ timing.

Figure 40: Bank Write – Without Auto Precharge



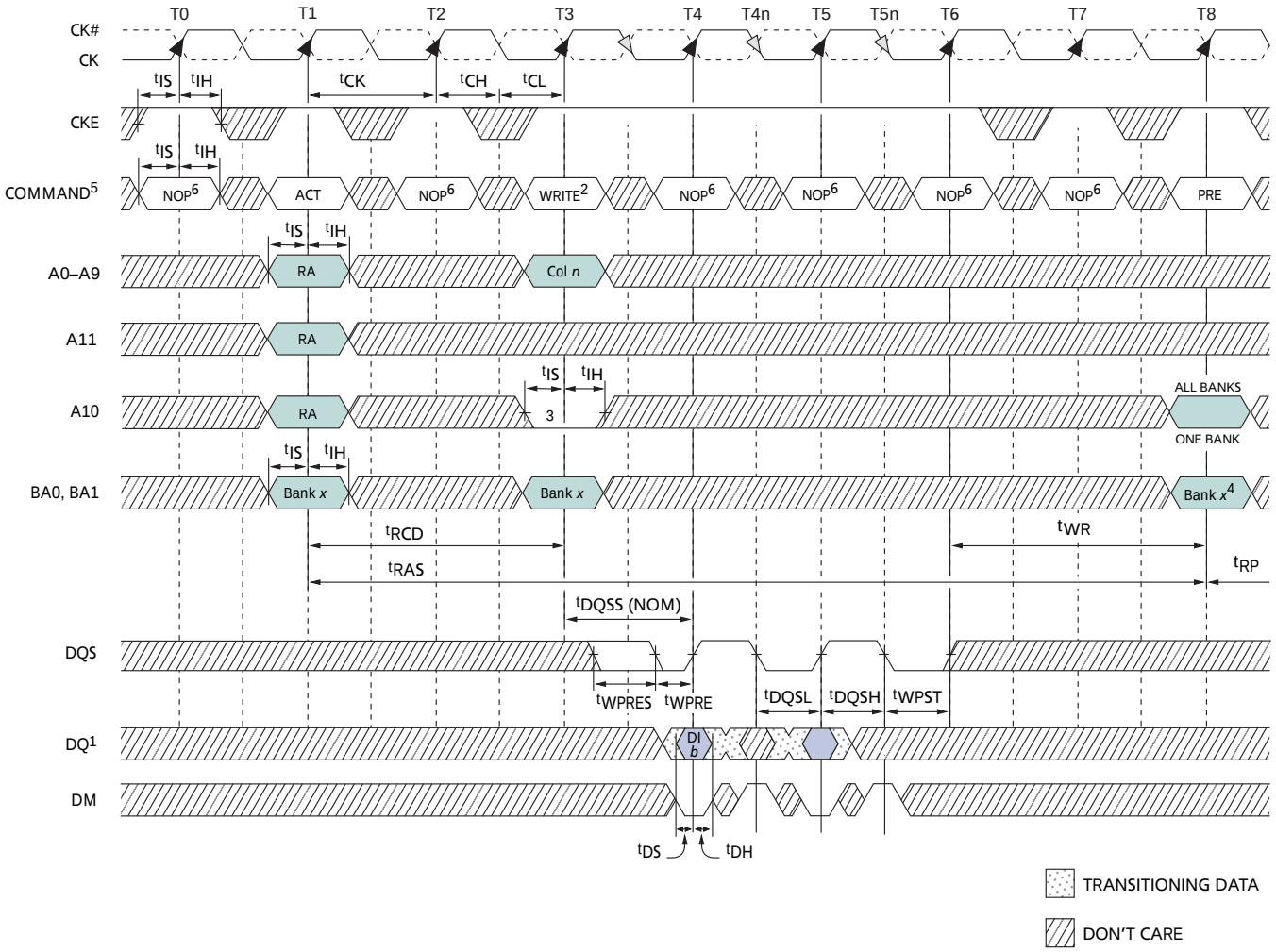
Notes:
1. DI *b* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T4 or T5.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.

Figure 41: Bank Write – with Auto Precharge



Notes:
1. DI *b*= data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T4 or T5.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.

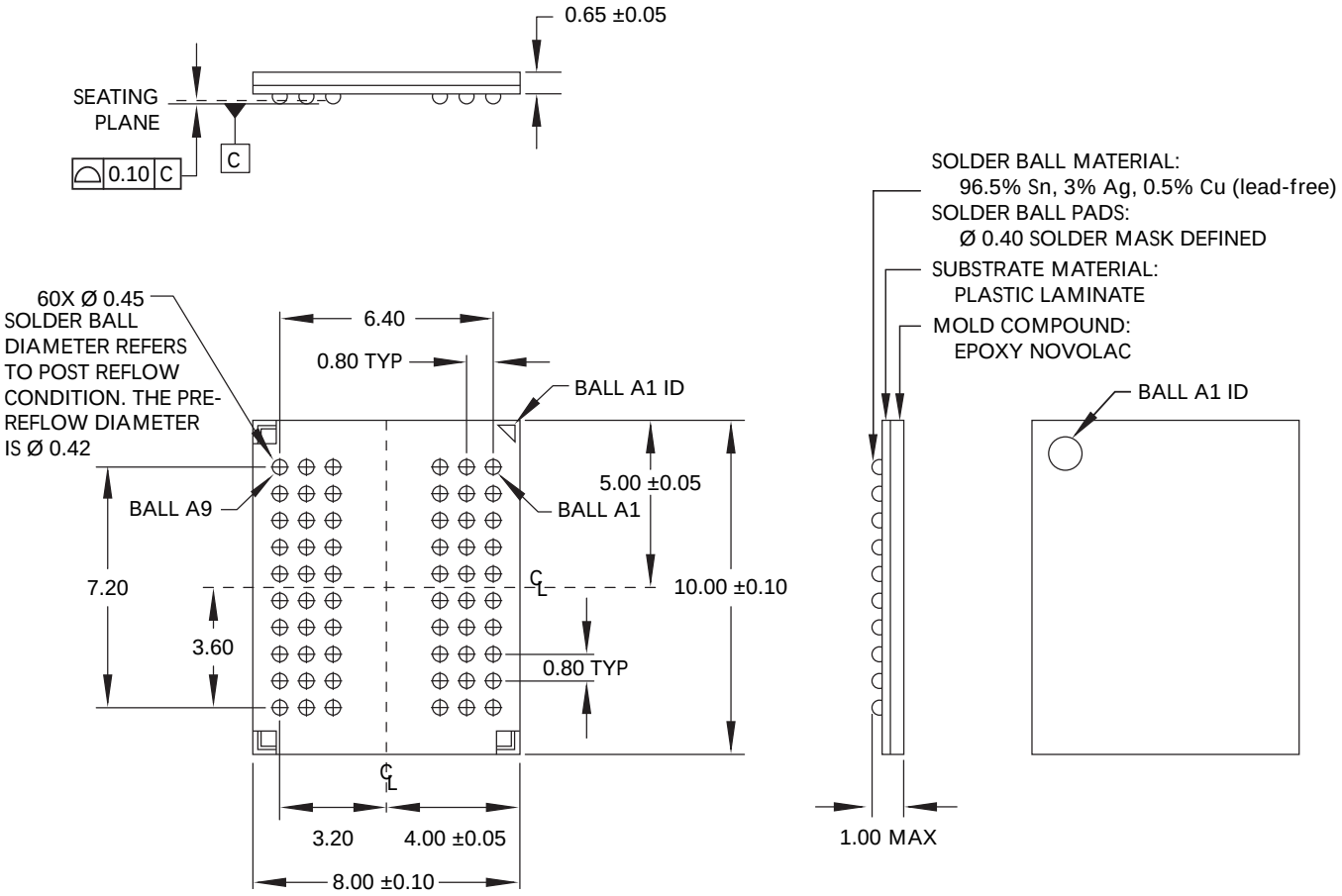
Figure 42: Write – DM Operation



Notes:
1. DI *b* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T4 or T5.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.

Package Dimensions

Figure 43: 60-Ball VFBGA Package



Notes: 1. Dimensions are in millimeters.

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