Data Sheet | March 9, 2006 | FN6110.1

14-Channel Programmable Switchable I²C TFT-LCD Reference Voltage Generator with Integrated 4-Channel Static Gamma Drivers

The ISL24006 is a 14-channel programmable switchable reference voltage generator with four channels of static gamma drivers integrated, for a complete 18-channel total gamma solution for TFT-LCD displays. The 14-channel programmable switchable configuration allows switching between two gamma curves.

The ISL24006 is divided into two banks of seven generators: one designed to cover the range from V_{REFL_L} to V_{REFL_H}; the remaining seven channels covering the range from V_{REFU_L} to V_{REFU_H}. Each bank has its own separate high and low reference inputs, with integrated buffers (four static gamma drivers) to drive the column driver internal DAC resistor string to within 0.2V from the top and bottom rails. An output MUX is used to switch between the two curves in less than 1µs. Switching is controlled using an external select pin.

ISL24006 includes an I²C interface for programming the offset values.

ISL24006 is available in the 38-pin QFN package and is specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL24006IRZ (See Note)	ISL24006IRZ	-	38-Pin QFN (Pb-Free)	MDP0046
ISL24006IRZ-T7 (See Note)	ISL24006IRZ	7”	38-Pin QFN (Pb-Free)	MDP0046
ISL24006IRZ-T13 (See Note)	ISL24006IRZ	13”	38-Pin QFN (Pb-Free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

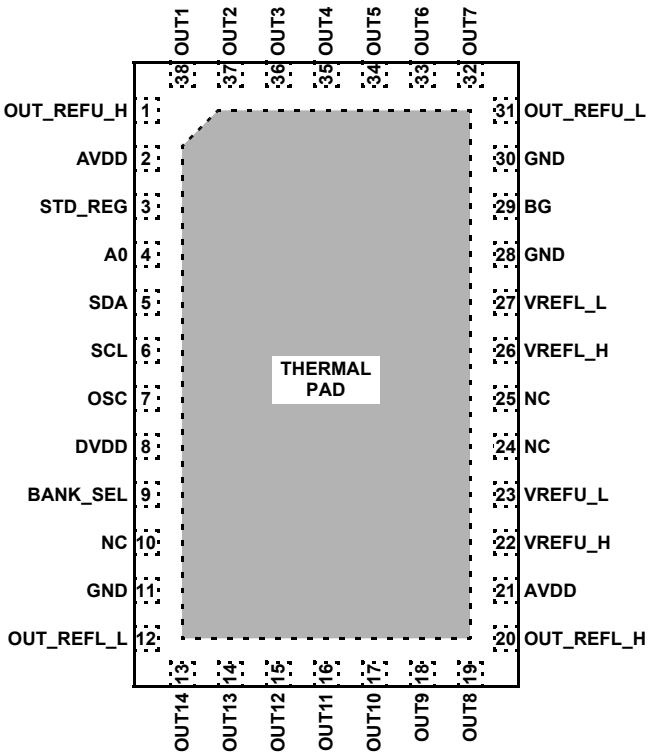
- 14-channel programmable switchable
- 4-channel static
- Fast switch time (< 1µs)
- Programmable with 20mV resolution
- Digital supply 3.3V to 5V
- Supply current of 32mA (without load)
- Rail-to-Rail capability
- I²C interface
- Pb-free plus anneal available (RoHS compliant)

Applications

- TFT-LCD drive circuits
- Reference voltage generators

Pinout

ISL24006
(38-PIN QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between A_{VDD} and GND . . . . . +18V
Supply Voltage between D_{VDD} and GND lesser of V_S or +7V (max)
Maximum Continuous Output Current
[V_{REFU_H}, V_{REFU_L}, V_{REFL_H}, V_{REFL_L}] 60mA
[OUT1 to OUT14] 30mA
Total Sourcing/Sink [Upper/Lower] 180mA
Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . +125°C
Lead Temperature . . . . . +260°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. The device outputs cannot withstand short-circuit condition for extended periods of time. To avoid damage, do not exceed absolute maximum rating of 20mA/channel.

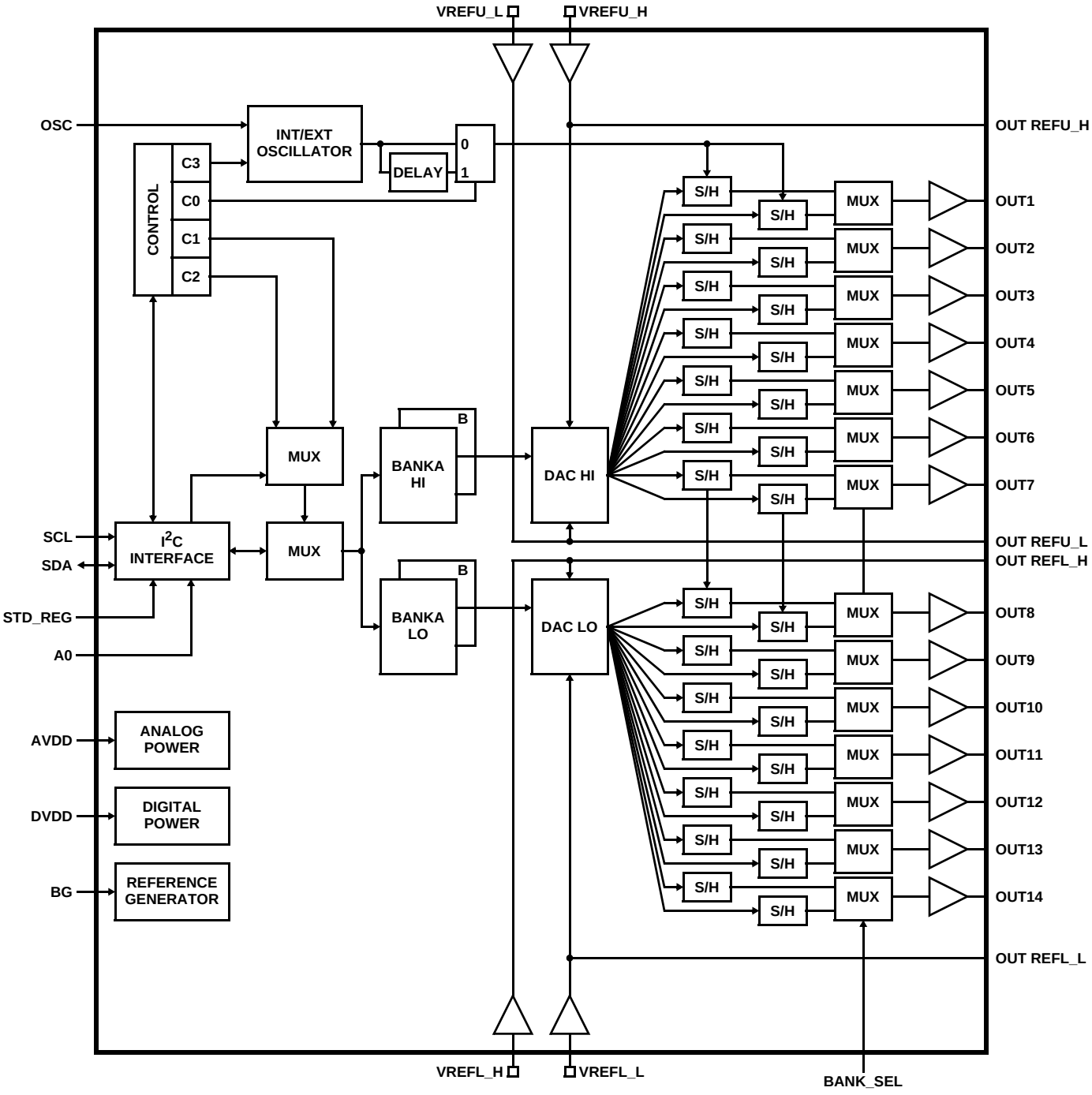
IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

A_{VDD} = 15V, D_{VDD} = 5V, V_{REFU_H} = 14V, V_{REFU_L} = 8.5V, V_{REFL_H} = 6.5V, V_{REFL_L} = 1V, R_L = 1kΩ and C_L = 10pF to 1/2 A_{VDD}, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{AVDD}	Supply Current	No load		30	38	mA
I_{DVDD}	Digital Supply Current			2.75	4	mA
ANALOG						
V_{OH}	OUT1 to OUT7	V_{REFU_H} = 14V, A_{VDD} = 15V	13.94	13.98	14.02	V
V_{OL}	OUT1 to OUT7	V_{REFU_L} = 8.5V, A_{VDD} = 15V	8.47	8.51	8.55	V
V_{OH}	OUT8 to OUT14	V_{REFL_H} = 6.5V, A_{VDD} = 15V	6.44	6.48	6.52	V
V_{OL}	OUT8 to OUT14	V_{REFL_L} = 1.0V, A_{VDD} = 15V	0.96	1.00	1.04	V
PSRR	Power Supply Rejection Ratio	A_{VDD} is moved from 14V to 16V	42	50		dB
V_{AC}	Accuracy		-50	0	+50	mV
I_B	Input Bias Current, $V_{REF(U\_H, U\_L, L\_H, L\_L)}$	V_{REF} = 1/2 A_{VDD}		2	50	nA
REG	Load Regulation	I_{OUT} = 5mA step		0.5		mV/mA
BG	Band Gap		1.1	1.3	1.4	V
SR	Slew Rate		8	15		V/µs
t_S	Settling Time	±1/2 LSB		1		µs
DIGITAL						
V_{IH}	Logic 1 Input Voltage		D_{VDD}-20%			V
V_{IL}	Logic 0 Input Voltage				20%* D_{VDD}	V
F_{CLK}	Clock Frequency				400	kHz
R_{SDIN}	S_{DIN} Input Resistance	SCL, SDA, STD_REG		1		GΩ
t_S	Setup Time			40		ns
t_H	Hold Time			40		ns

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN FUNCTION
1	OUT REFU_H	Analog Output	Analog output of V_{REFU_H}
2, 21	AVDD	Analog Power	Power supply for analog circuit
3	STD_REG	Logic Input	Selects mode, high = standard, low = register
4	A0	Logic Input	I^2C device address input, bit 0; when LO, hex address = 74; when HI, hex address = 75
5	SDA	Input/Output	I^2C data
6	SCL	Logic Input	I^2C clock
7	OSC	Input/Output	Input clock reference
8	DVDD	Digital Power	Power supply for digital circuit
9	BANK_SEL	Digital Signal	Select one of two sets of gamma voltages
10, 24, 25	NC		Not connected
28, 30, 11	GND	GND	Ground
12	OUT REFL_L	Analog Output	Analog output of V_{REFL_L}
13, 14, 15, 16, 17, 18, 19	OUT8 - OUT14	Analog Output	Analog output voltages in lower range
20	OUT REFL_H	Analog Output	Analog output of V_{REFL_H}
22	VREFU_H	Reference	High reference for upper seven output voltages
23	VREFU_L	Reference	Low reference for upper seven output voltages
26	VREFL_H	Reference	High reference for lower seven output voltages
27	VREFL_L	Reference	Low reference for lower seven output voltages
29	BG	Analog Bypass Pin	Decoupling capacitor for internal reference generator
31	OUT REFU_L	Analog Output	Analog output of V_{REFU_L}
32, 33, 34, 35, 36, 37, 38	OUT1 - OUT7	Analog Output	Analog output voltages in upper range

Typical Performance Curves

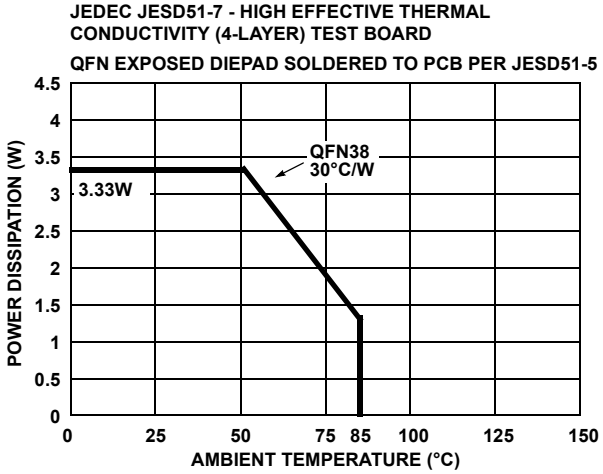


FIGURE 1. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

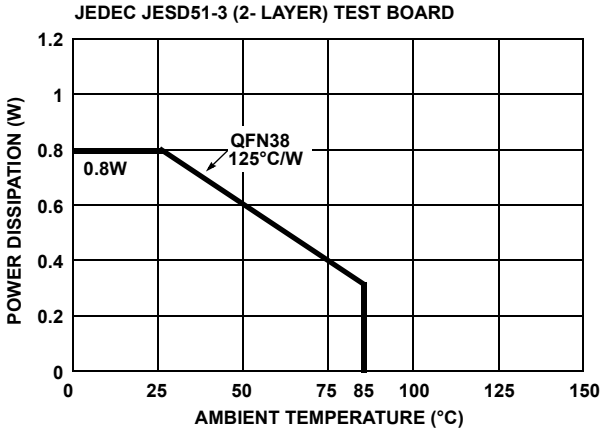


FIGURE 2. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

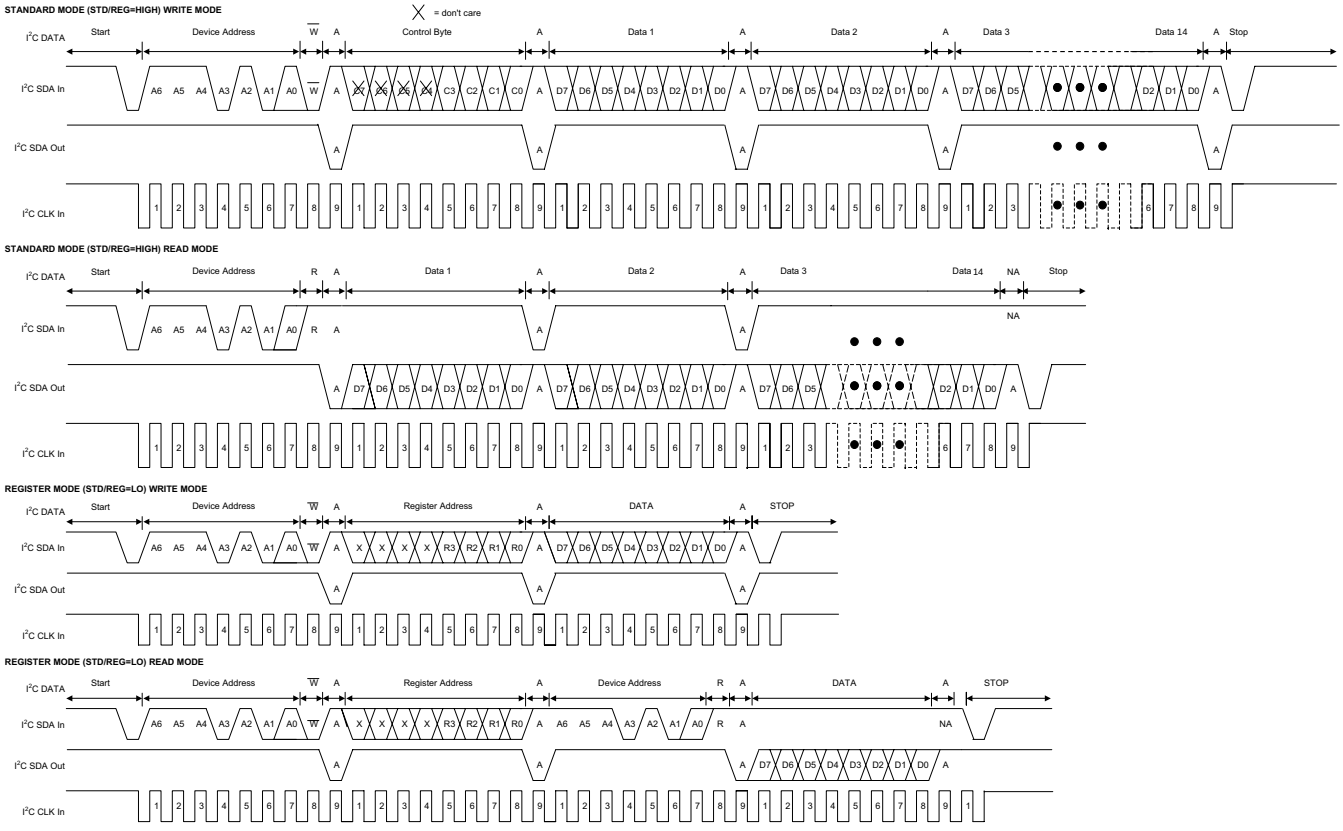


FIGURE 3. I²C TIMING DIAGRAM 1

General Description

The ISL24006 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear. However, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the ISL24006, the V/T curve can be changed to optimize its characteristics according to the required application of the display product.

Each of the 14 reference voltage outputs can be set with a 8-bit resolution. The first half of the output buffers, OUT1 to OUT7 can be operated from V_{REFU_L} to V_{REFU_H}. The second half OUT8 to OUT14 can swing from V_{REFL_L} to V_{REFL_H}.

It is also possible to use the ISL24006 for applications other than LCDs where multiple voltage references are required that can be set to 8-bit accuracy.

Digital Interface

The ISL24006 uses a simple two-wire I^2C interface to program all 14 outputs. The bus line SCLK is the clock signal line and bus SDA is the bi-directional data information signal line. The ISL24006 can support a clock rate up to 400kHz. An external pull up typically 1kΩ resistor is required for each bus line.

Start and Stop Condition

A Start condition is a high to low transition on the serial data line (SDA) line while the serial clock line (SCLK) holds high. The Stop condition is a low to high transition on the SDA line while SCLK is high. The master device always generates Start and Stop conditions. The bus is considered to be busy after the Start condition and to be free at a certain time interval after the Stop condition. The two bus lines must be high when the buses are not in use. The I^2C Timing Diagram 2 (Figure 2) shows the format.

Data Validity

The data on the SDA line must be stable (clearly defined as HI or LO) during the HI period of the clock signal. SDA transition can only change when the clock signal on the SCLK line is LO.

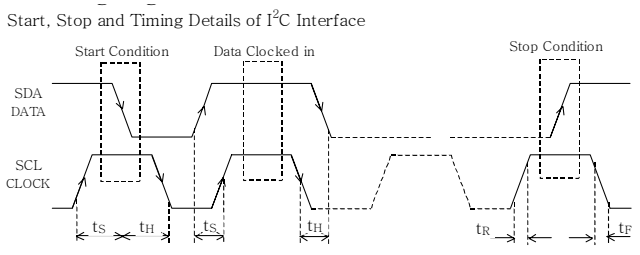


FIGURE 4. I^2C TIMING DIAGRAM 2

Byte Format

Every byte put along the SDA line must be eight bits long. The number of bytes that can be transmitted between a Start and Stop condition is unrestricted. Data is always transferred with the most significant bit (MSB) first.

Acknowledge

Each byte is followed by an acknowledge bit.

When a master device is sending data (WRITE) the master puts a resistive high level on the SDA line during the acknowledge clock pulse. The peripheral that acknowledges, which is the receiver, has to pull down the SDA line during the acknowledge pulse.

When a master device is receiving data (READ) the slave puts a resistive high level on the SDA line during the acknowledge clock pulse. The master will acknowledge by pulling down the SDA line during the acknowledge pulse.

Not Acknowledge

A Not Acknowledge (NA) is when the receiver does not pull down the SDA line during the acknowledge pulse: SDA line remains in the HI or in a high impedance state.

A Not Acknowledge is the master device's signal to the slave device to release the SDA line so the master device can generate a Stop signal on the same line. The NA indicates that data just received is the last byte of the data transfer.

Standard Mode

When pin #6 (STD_REG) is pulled high, the part operates in Standard Mode, which is more commonly used than the Register Mode. In the Standard Mode, the user can program all outputs in one data stream or transfer frame.

For the Standard Mode in a WRITE transfer, a master device sends data to program all the output buffers of the ISL24006. The input data byte (DATA 1) to the first channel (OUT1) is the third byte following the control byte. The second channel (OUT2) is programmed by the fourth byte (DATA 2), and so on. Each byte is followed by an acknowledge bit.

TABLE 1. STANDARD MODE WRITE TRANSFER

S	ISL24006 ADDRESS + W	A	CONTROL BYTE	A	DATA 1	A	DATA 2	A	...	DATA 14	A	P

S = Start condition

P = Stop condition

A = Acknowledge bit

CONTROL BYTE = multifunction control

DATA 1 = 8-bit input to DAC OUT1

DATA 2 = 8-bit input to DAC OUT2

DATA 14 = 8-bit input to DAC OUT14

For the Standard mode in a READ transfer, a master device accepts data from the ISL24006. The output data byte (DATA 1) of the first channel (OUT1) is the second byte of the transfer. OUT2 output data byte is the third byte of the transfer, and so forth and so on. The ISL24006 sends an acknowledge bit after every eighth bit to tell the master device that the ISL24006 is ready to send another byte. Consequently, the master must send a Not Acknowledge, (NA) at the end of the 14th data byte to tell ISL24006 to release the SDA bus.

TABLE 2. Standard Mode READ Transfer

S	ISL24006 ADDRESS + R	A	DATA 1	A	DATA 2	A	...	DATA 14	P

S = Start condition

P = Stop condition

A = Acknowledge

NA = Not Acknowledge

DATA 1 = 8-bit input to DAC OUT1

DATA 2 = 8-bit input to DAC OUT2

DATA 14 = 8-bit input to DAC OUT14

See Timing Diagram 1 (Figure 1) for detailed formats.

Devices Address and W/R Bit

Data transfers follow the format shown in Timing Diagram 1. After the Start condition, a first byte is sent which contains the Device Address and write/read bit. This address is a 7-bit long device address and only two device addresses hex (74) and hex (75) in binary, bin (111010) and bin (111011) are allowed for the ISL24006. The first 6 bits (A6 to A1, MSBs) of the device address have been factory programmed and are always 111010. Only the least significant bit (LSB) A0 is allowed to change the logic state. This LSB is controlled externally on the pin #4, A0. When pulled high to D_{VDD}, the LSB of the device address is high and thus the address is hex (75) or in binary bin (1110101). When pulled low to GND, the LSB of the device address low and thus the address is hex (74) or in binary 1110100. Since the device address has to be unique in the I^2C bus line, a maximum of two ISL24006 may be used on the same bus at one time.

The ISL24006 monitors the bus continuously and waiting for the Start condition followed by the device address. When the device recognizes its device address, it will start to accept data. The eighth bit (W/R) following the device address indicates the data direction. A "0" is a Write transmission; a master device will send data to the ISL24006 to set or program a desired reference voltage. A "1" indicates a Read transmission; the master device will receive data from the ISL24006 to read the previous data the voltage reference was set or programmed.

Control Byte

The multi-function control byte contains information that selects the memory bank (bankA, or bankB), and operation (output, read, or write). It also controls the OSC pin function (external or internal).

TABLE 3. Control Byte

C7	C6	C5	C4	C3	C2	C1	C0
X	X	X	X	0	0	0	0

C0 = "0" bypass oscillator

= "1" 3.5µs lagging

C1 = "0" write data to bankA (default)

= "1" write data to bankB

C2 = "0" read data from bankA (default)

= "1" read data from bankB

C3 = "0" internal oscillator (default)

= "1" external oscillator

The second bit, C1, selects which bank to write to. A "**0**" selects **bankA**. A "**1**" selects **bankB**. C1 is a "don't care" on a read mode.

The third bit, C2, selects which bank to read from. A "**0**" selects **bankA**. A "**1**" selects **bankB**. C2 is a "don't care" on a write mode.

The fourth bit, C3, selects the function of the OSC pin. A "**0**" selects the internal oscillator. When the internal oscillator is selected, the OSC pin acts as an output pin. It generates a square wave with a frequency of typically 20kHz where multiple chips can be synchronized. A "**1**" selects an external oscillator. When the external oscillator is selected, the OSC pin acts an input pin. Multiple chips can be synchronized to an external oscillator. The external frequency or refresh rate can be synchronized up to 200kHz typically.

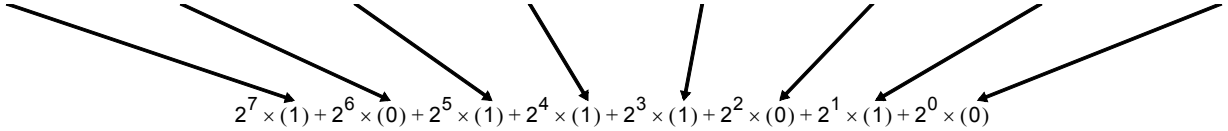
The rest of the bits (C4-C7) in the control byte are "don't cares".

Data Byte

Data Bytes are the input code data to the 8-bit DACs. Most significant bits are clocked in first. These data bytes determine the output voltages of the ISL24006.

TABLE 4.

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
1	0	1	1	1	0	1	0



$$2^7 \times (1) + 2^6 \times (0) + 2^5 \times (1) + 2^4 \times (1) + 2^3 \times (1) + 2^2 \times (0) + 2^1 \times (1) + 2^0 \times (0)$$

Ideal Transfer Function Example

Given a typical voltage applied to V_{REFU_H} and V_{REFU_L}:

$V_{REF\ U\_H} = 14V$ $\quad$ $V_{REF\ L\_H} = 6.5V$

$V_{REF\ U\_L} = 8.5V$ $\quad$ $V_{REF\ L\_L} = 1V$

$R = \frac{14V - 8.5V}{256} = 21.5mV$ $\quad$ $R = \frac{6.5V - 1V}{256} = 21.5mV$

TABLE 5.

BINARY INPUT	DECIMAL	VOUT1 (V)	VOUT14 (V)
00000000	0	8.5	1
00000001	1	8.521484	1.021484
00000011	3	8.564453	1.064453
00000111	7	8.650391	1.150391
00001111	15	8.822266	1.322266
00011111	31	9.166016	1.666016
00111111	63	9.853516	2.353516
01111111	127	11.22852	3.728516
11111111	255	13.97852	6.478516

Clock Oscillator

The ISL24006 require an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labelled OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the OSC pin. In a two-chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect.

The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits. After power on, the chip will default with the internal oscillator mode. At this time, the OSC pin will be in a high impedance condition to prevent contention.

Channel Outputs

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle. The time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

Power-On Sequencing

At power-on, make sure that $A_{VDD} \geq D_{VDD}$ - 0.5V to prevent the ESD diode between A_{VDD} and D_{VDD} from driving too much current. If D_{VDD} comes on first, leave A_{VDD} floating. Do **not** ground A_{VDD}.

Power Dissipation

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = A_{VDD} \times I_{AVDD} + \Sigma[(A_{VDD} - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = A_{VDD} \times I_{AVDD} + \Sigma(V_{OUT}i \times I_{LOAD}i)$$

when sinking.

Where:

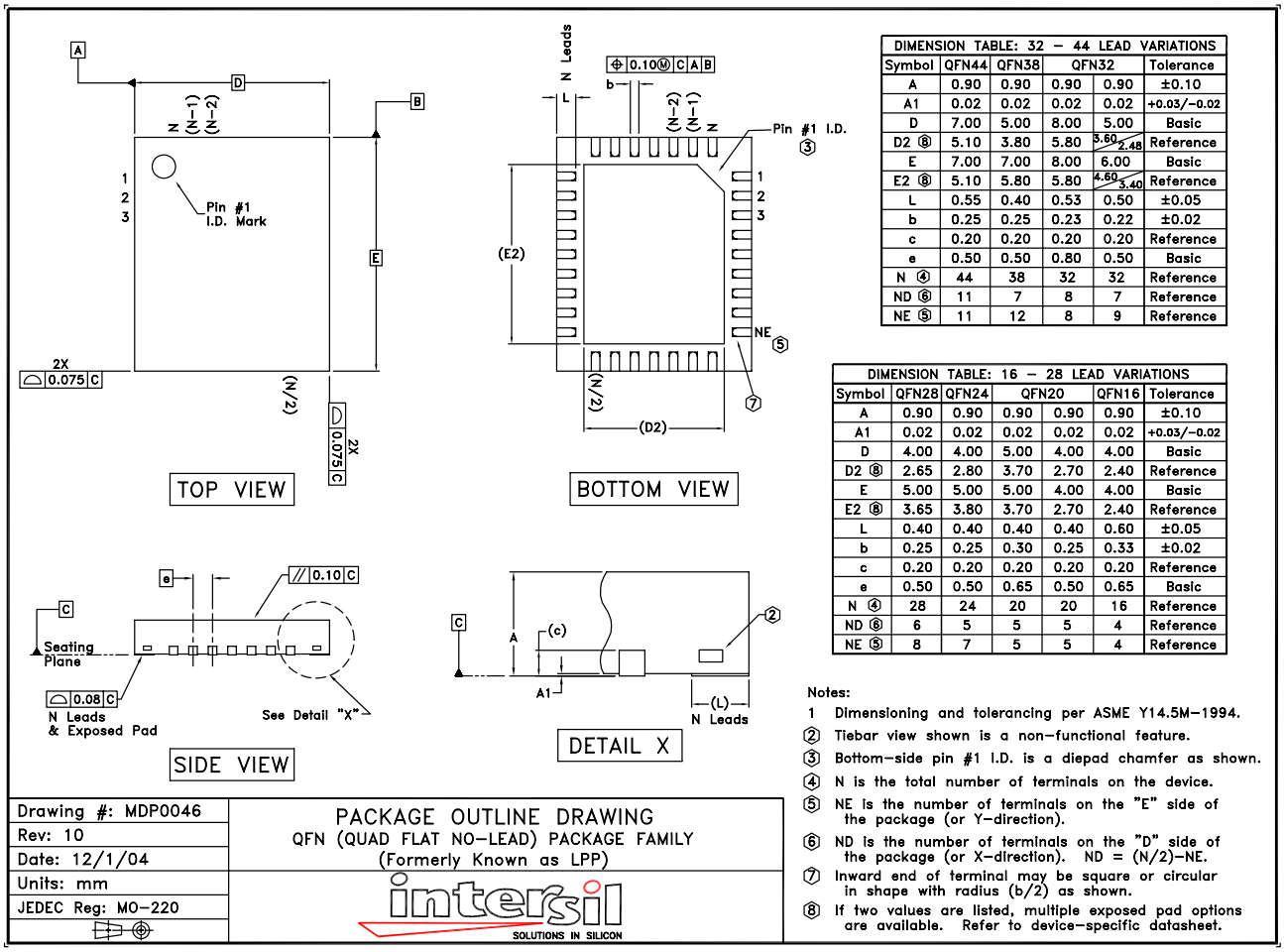
- i = 1 to total 14
- A_{VDD} = Supply voltage
- I_{AVDD} = Quiescent current
- $V_{OUT}i$ = Output voltage of the i channel
- $I_{LOAD}i$ = Load current of the i channel

By setting the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}s to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

Power Supply Bypassing and Printed Circuit Board Layout

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the ISL24006. The traces from the two ground pins to the ground plane must be very short. The thermal pad should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1µF ceramic capacitor must be placed very close to the A_{VDD}, V_{REFU_H}, V_{REFU_L}, V_{REFL_H}, V_{REFL_L}, and BG pins. A 4.7µF local bypass ceramic capacitor should be placed to the A_{VDD}, V_{REFU_H}, V_{REFU_L}, V_{REFL_H}, V_{REFL_L} pins.

Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/-0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60/2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60/3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (6)	11	7	8	7	Reference
NE (5)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/-0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N (4)	28	24	20	20	16	Reference
ND (6)	6	5	5	5	4	Reference
NE (5)	8	7	5	5	4	Reference

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp