Data Sheet | December 13, 2006 | FN7445.0

4-Channel TFT-LCD Supply

The ISL97522 represents a 4-channel supply control IC for use in large panel TFT-LCD displays. Supporting inputs from 4.5V to 13V, the ISL97522 includes a boost controller to achieve the required A_{VDD} output voltage. Both V_{ON} and V_{OFF} are generated using off-chip charge-pumps which are then post regulated using on-board LDO controllers.

The logic supply is generated using an internal non-synchronous buck controller. This controller runs at 180° out of phase with the A_{VDD} supply to minimize input noise.

The A_{VDD}, V_{OFF}, and V_{ON} outputs are automatically sequenced as A_{VDD}, V_{OFF}, and V_{ON}. By using an optional external series transistor with A_{VDD} (Q1), the start-up sequence can be adjusted to VOFF, A_{VDD} and then V_{ON}. A V_{ON} slicing circuit is also included to reduce LCD flicker.

The ISL97522 also incorporates a fault protection circuit that can disable the IC and turn off all outputs when an output short is detected. (Note that to protect A_{VDD} a single external transistor is required).

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97522IRZ-TK	ISL 97522IRZ	13” (1k pcs)	38 Ld QFN	L38.5x7B
ISL97522IRZ-T	ISL 97522IRZ	13” (4k pcs)	38 Ld QFN	L38.5x7B

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

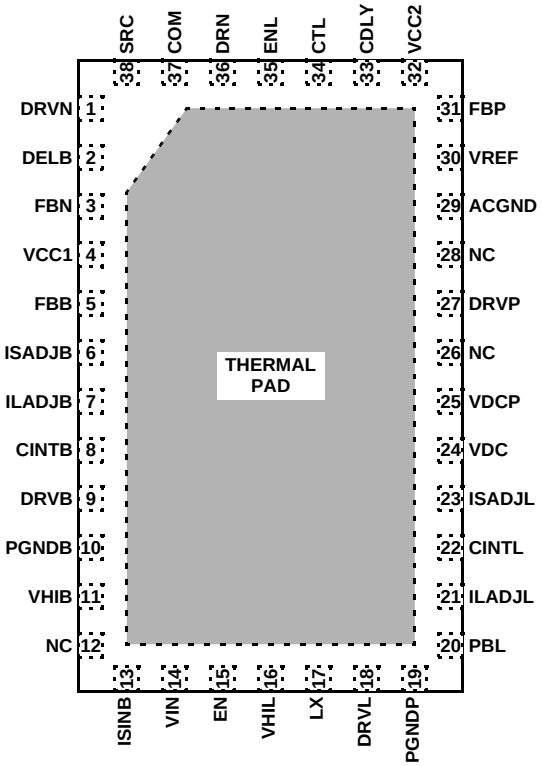
- 4.5V to 13V input
- Boost controller for A_{VDD}
- Regulated LDOs for V_{OFF} and V_{ON}
- Buck controller for logic output
- V_{ON} slicing circuit
- Fully fault-protected
- Programmable sequence
- 1MHz switching frequency
- 38 Ld QFN package
- Pb-free plus anneal available (RoHS compliant)

Applications

- LCD-TVs (up to 50”+)
- LCD monitors (15”+)
- Industrial/medical LCD displays

Pinout

ISL97522
(38 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Maximum Pin Voltages, all pins except below 6.5V
VIN,EN,ENL,LX,VHIL. 25V
VDELB 36V
VDRVP, VSINB, SRC, COM, DRN 36V
VDRVN . . . . . -20V

Operating Conditions

Input Voltage Range, V_{IN}. . . . . 4.5V to 13V
Boost Output Voltage Range, A_{VDD} . . . . . +15V to +25V
V_{ON} Output Range, V_{ON}. . . . . +15V to +32V
V_{OFF} Output Range, V_{ON} . . . . . -15V to -5V
Input Capacitance, C_{IN} 2x10µF
Boost Inductor, L1 . . . . . 3.3µH to 10µH
Output Capacitance, C_{OUT} 4x10µF
Buck Inductor, L2 . . . . . 3.3µH to 10µH
Operating Ambient Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
38 Ld QFN Package (Notes 1, 2).	33	4.5

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{IN} = 5V, A_{VDD} = 15V, V_{ON} = 20V, V_{OFF} = -9V, V_{LOGIC} = 3V, Over Temperature from -40°C to +85°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
GENERAL						
V_{IN}	Input Voltage		4.5		13.2	V
I_S	Sum Quiescent Current into Vin	EN = 0, ENL = 0		3		mA
		EN = ENL = 1, switching		15		mA
F_{OSC}	Oscillator Frequency		850	1000	1100	kHz
V_{REF}	Reference Voltage	T_A = +25°C	1.192	1.215	1.235	V
			1.190	1.215	1.237	V
A_{VDD}						
V_{FBB}	Feedback Reference Voltage	T_A = +25°C	1.195	1.208	1.221	V
			1.193	1.208	1.223	V
V_{F_FBB}	FBB Fault Trip Point	V_{FBB} falling	0.85	0.9	0.95	V
D_{MIN}	Minimum Duty Cycle			19	25	%
D_{MAX}	Maximum Duty Cycle		80	86		%
Eff	Boost Efficiency			90		%
I_{FBB}	FBB Input Bias Current			25		nA
R_{LINEB}	Line Regulation	C_{INT} = 2.2nF, V_{IN} = 4.5V to12V, I_O =100mA		0.01	0.25	%/V
R_{LOADB}	Load Regulation	C_{INT} = 2.2nF, V_{IN} = 5V, I_{AVDD} = 100mA to 350mA		0.03	0.25	%
R_{ONB}	Gate Drive on Resistance	Pull-up		3.6		Ω
		Pull-down		1.9		Ω

Electrical Specifications V_{IN} = 5V, A_{VDD} = 15V, V_{ON} = 20V, V_{OFF} = -9V, V_{LOGIC} = 3V, Over Temperature from -40°C to +85°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
I_{PEAKB}	Peak Drive Current	Source		600		mA
		Sink		900		mA
I_{ISADJB}	I_{SADJB} Output Current	R_{SADJB} = 30kΩ	10	15	25	µA
I_{ILADJB}	I_{LADJB} Output Current	R_{LADJB} = 30kΩ	10	17	25	µA
V_{ON} LDO						
V_{FBP}	FBP Regulation Voltage	I_{DRVP} = 0.2mA,T_A = +25°C	1.176	1.2	1.224	V
		I_{DRVP} = 0.2mA	1.174	1.2	1.226	V
V_{F_FBP}	FBP Fault Trip Point	V_{FBP} falling	0.82	0.87	0.92	V
I_{FBP}	FBP Input Bias Current	V_{FBP} = 1.35V		150		nA
R_{LOADP}	V_{ON} Load Regulation	I(V_{ON}) = 0mA to 20mA		0.5	0.75	%
I_{DRVP}	DRVP Sink Current Max	V_{FBP} = 1.1V, V_{DRVP} = 25V	2	4		mA
I_{L_DRVP}	DRVP Leakage Current	V_{FBP} = 1.5V, V_{DRVP} = 35V		0.3	2	µA
V_{OFF} LDO						
V_{FBN}	FBN Regulation Voltage	I_{DRVN} = 0.2mA,T_A = +25°C	0.186	0.213	0.24	V
		I_{DRVN} = 0.2mA	0.183	0.213	0.243	V
V_{F_FBN}	FBN Fault Trip Point	V_{FBN} rising	0.45	0.5	0.55	V
I_{FBN}	FBNInput Bias Current	V_{FBN} = 0.2V		40		nA
R_{LOADN}	V_{OFF} Load Regulation	I(V_{OFF}) = 0mA to 20mA		0.4	0.85	%
I_{DRVN}	DRVN Source Current Max	V_{FBN} = 0.3V, V_{DRVN} = -6V	2	4		mA
I_{L_DRVN}	DRVN Leakage Current	V_{FBN} = 0V, V_{DRVN} = -20V		0.4	5	µA
V_{LOGIC}						
V_{FBL}	FBL Regulation Voltage	T_A = 25°C	1.178	1.2	1.222	V
			1.176	1.2	1.224	V
D_{MIN}	Minimum Duty Cycle			20		%
D_{MAX}	Maximum Duty Cycle			85		%
EFF_L	Logic Buck Efficiency			90		%
IFBL	FBL Input Bias Current			20		nA
I_{LINEL}	V_{LOGIC} Line Regulation	C_{INT} = 2.2nF, V_{IN} = 5V to 12V		0.03	0.25	%/V
I_{LOADL}	V_{LOGIC} Load Regulation	C_{INT} = 2.2nF, I_{LOGIC} = 100mA to 450mA		0.1	0.5	%
R_{ONL}	Gate Drive on Resistance	Pull-up		3.6		Ω
		Pull-down		1.9		Ω
I_{PEAKL}	Peak Drive Current	Source		600		mA
		Sink		900		mA
I_{ISADJL}	I_{SADJB} Output Current	R_{SADJB} = 30kΩ		15		µA
I_{ILADJL}	I_{LADJB} Output Current	R_{LADJB} = 30kΩ		17		µA
V_{ON}-SLICE CIRCUIT						
I_{LEAK}CTL	CTL Input Leakage Current	CTL = A_{GND} or V_{IN}	-1		1	µA
$t_D$rise	CTL to OUT Rising Prop Delay	1kΩ from DRN to 8V, V_{CTL} = 0V to 3V step, no load on OUT, measured from V_{CTL} = 1.5V to OUT = 20%		100		ns

Electrical Specifications V_{IN} = 5V, A_{VDD} = 15V, V_{ON} = 20V, V_{OFF} = -9V, V_{LOGIC} = 3V, Over Temperature from -40°C to +85°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
$t_D$fall	CTL to OUT Falling Prop Delay	1kΩ from DRN to 8V, V_{CTL} = 3V to 0V step, no load on OUT, measured from V_{CTL} = 1.5V to OUT = 80%		100		ns
V_{SRC}	SRC Input Voltage Range				30	V
ISRC	SRC Input Current	Start-up sequence not completed		0.2	1.25	mA
		Start-up sequence completed		150	250	µA
R_{ON}SRC	SRC On Resistance	Start-up sequence completed		5	14	Ω
R_{ON}DRN	DRN On Resistance	Start-up sequence completed		30	60	Ω
R_{ON}COM	COM to GND On Resistance	Start-up sequence not completed	400	1000	1800	Ω
SEQUENCING						
t_{ON}	Turn On Delay	C_{DLY} = 0.22µF		30		ms
t_{SS}	Soft-start Time	C_{DLY} = 0.22µF		2		ms
t_{DEL1}	Delay Between A_{VDD} and V_{OFF}	C_{DLY} = 0.22µF		10		ms
t_{DEL2}	Delay Between V_{ON} and V_{OFF}	C_{DLY} = 0.22µF		17		ms
t_{DEL3}	Delay Between V_{OFF} and Delayed V_{BOOST}	C_{DLY} = 0.22µF		10		ms
I_{DELB_ON}	DELB Pull-Down Current or Resistance when Enabled by the Start-Up Sequence	V_{DELB} > 0.9V	35	50	65	µA
		V_{DELB} < 0.9V	1.2	1.6	2	KΩ
I_{DELB_OFF}	DELB Pull-Down Current or Resistance when Disabled	VDELB < 20V			500	nA
FAULT DETECTION						
T_{FAULT}	Fault Time Out	C_{DLY} = 0.22µF		50		ms
OT	Over-temperature Threshold			140		°C
LOGIC						
V_{HI}	Logic High Threshold		2.2			V
V_{LO}	Logic Low Threshold				0.8	V
I_{LOW}	Logic Low Bias Current			0.1		µA
I_{HIGH}	Logic High Bias Current		16	23	30	µA

Typical Performance Curves

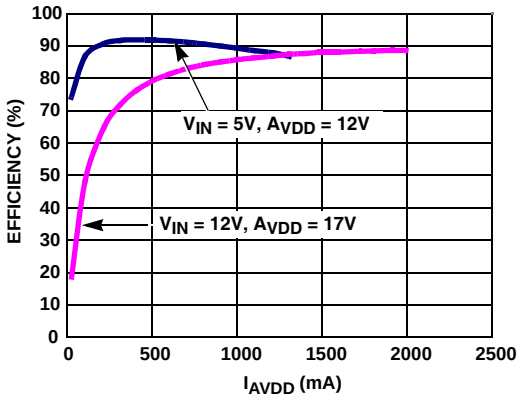


FIGURE 1. BOOST AVDD EFFICIENCY

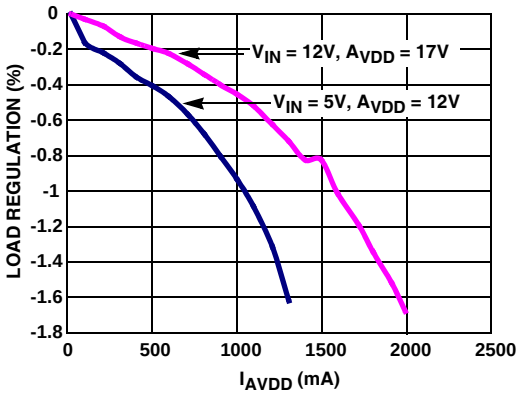


FIGURE 2. BOOST AVDD LOAD REGULATION

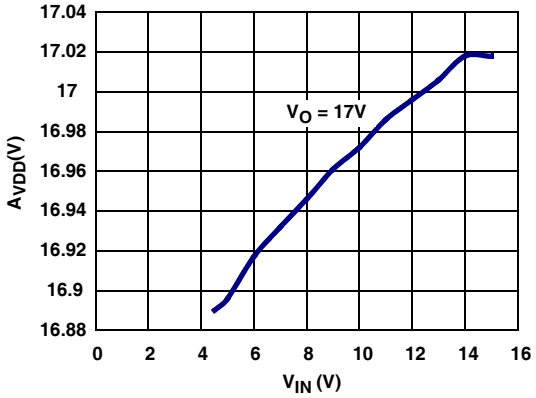


FIGURE 3. BOOST AVDD LINE REGULATION

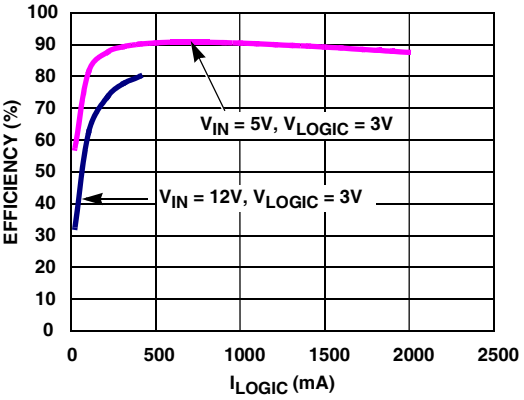


FIGURE 4. BUCK V_{LOGIC} EFFICIENCY

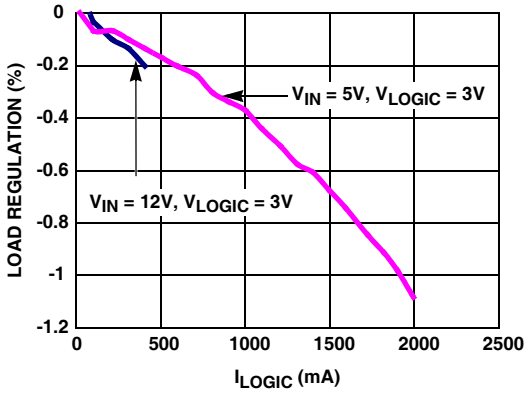


FIGURE 5. BUCK V_{LOGIC} LOAD REGULATION

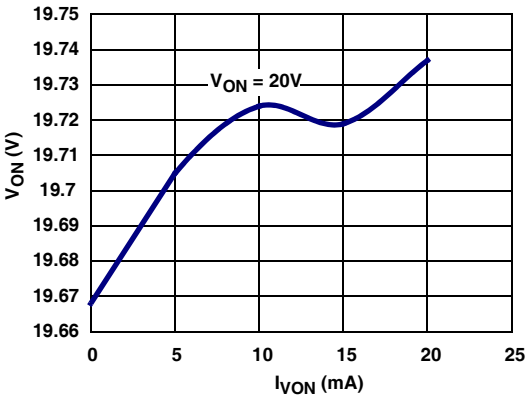


FIGURE 6. V_{ON} LOAD REGULATION

Typical Performance Curves (Continued)

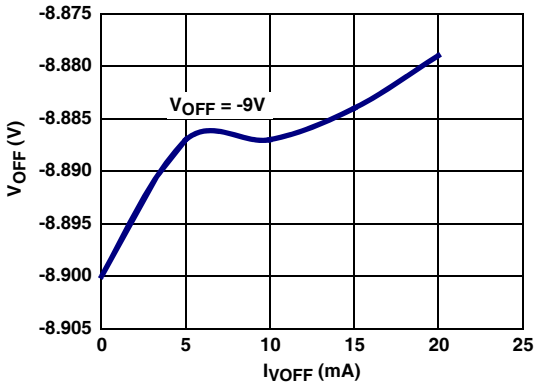


FIGURE 7. V_{OFF} LOAD REGULATION

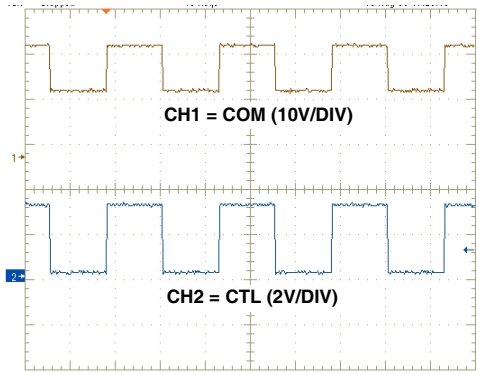


FIGURE 8. 4ms/DIV V_{ON} SLICE CIRCUIT OPERATION

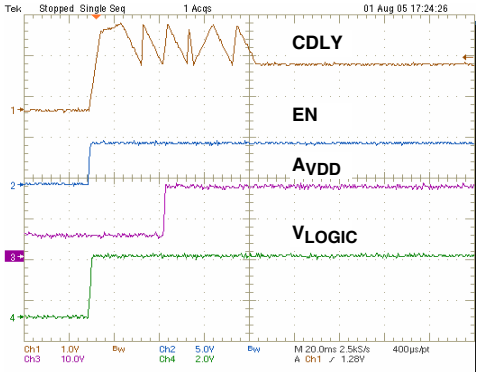


FIGURE 9. START-UP SEQUENCE

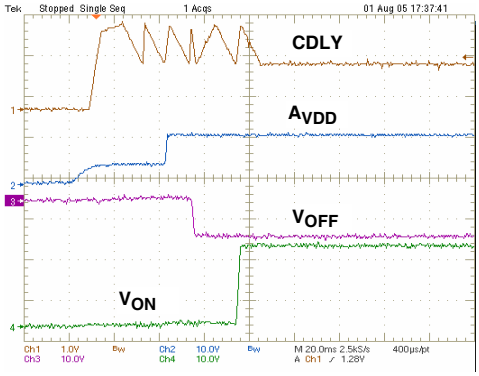


FIGURE 10. START-UP SEQUENCE

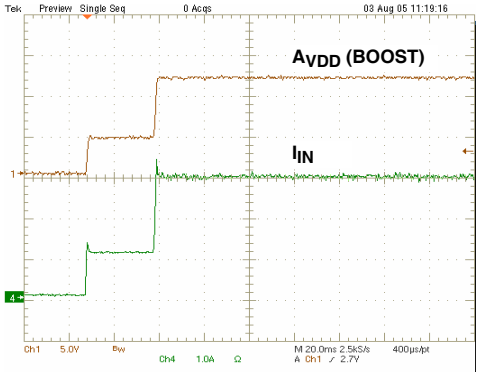


FIGURE 11. IN RUSH CURRENT

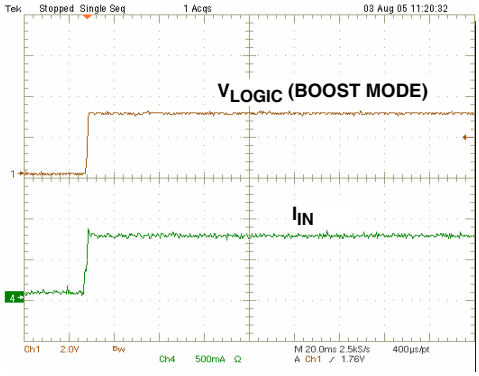


FIGURE 12. IN RUSH CURRENT

Typical Performance Curves (Continued)

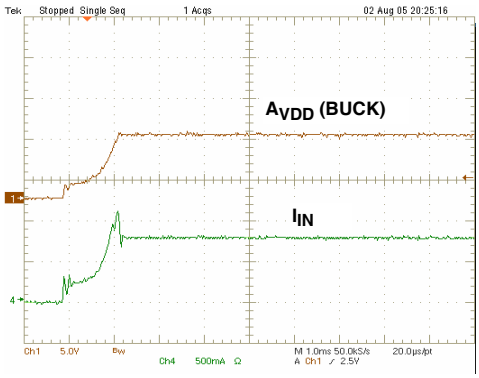


FIGURE 13. IN RUSH CURRENT

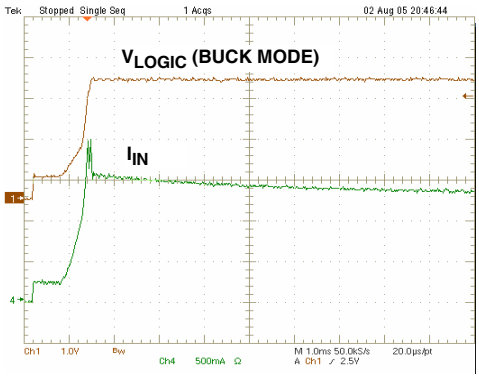
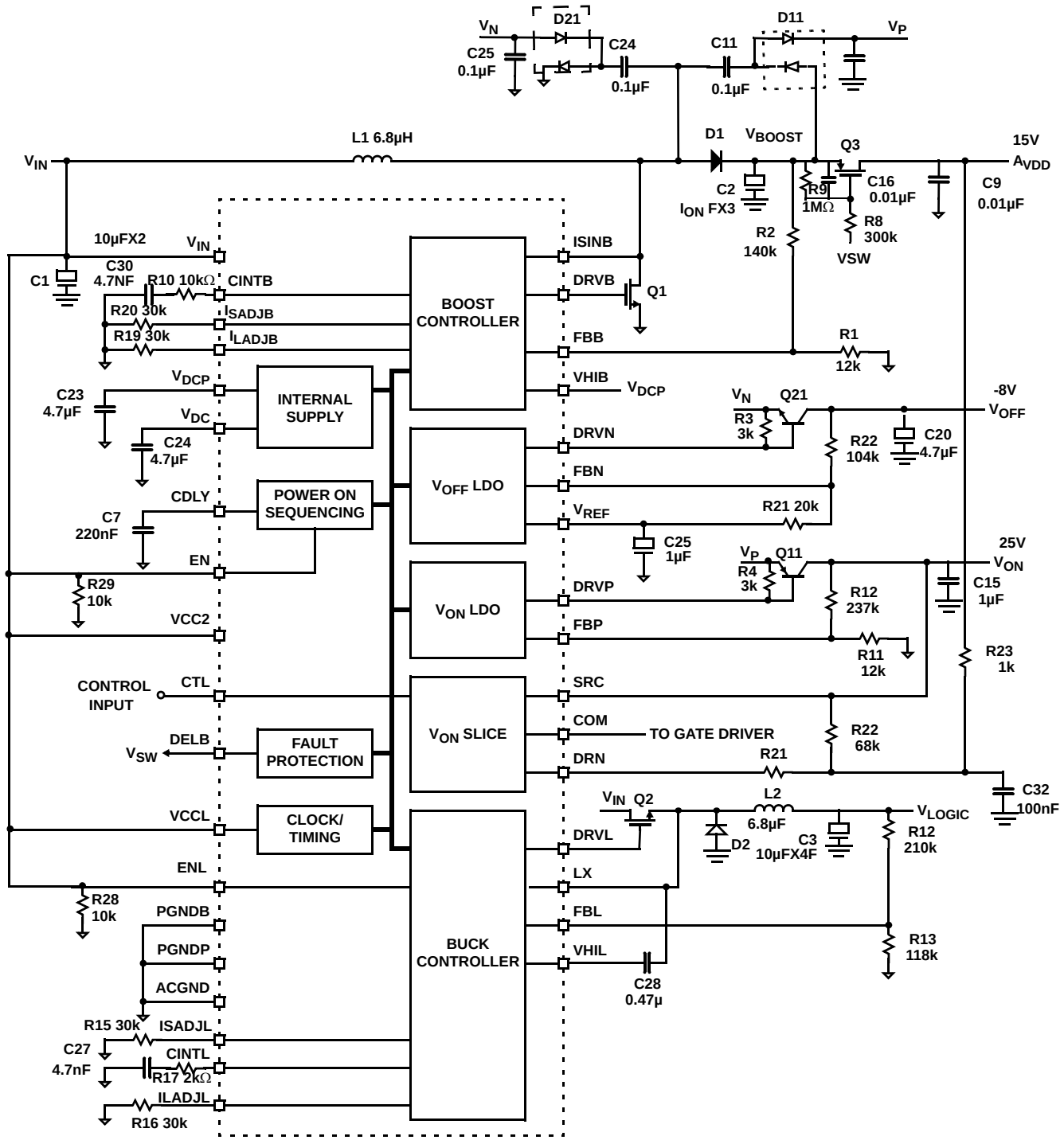


FIGURE 14. IN RUSH CURRENT

Pin Descriptions

PIN #	PIN NAME	PIN DESCRIPTION
1	DRVN	Negative LDO base drive; open drain of an internal P-Channel MOSFET.
2	DELB	Active low control output for optional delay control for external A_{VDD} P-Channel FET; when fault is detected, this pin goes to high.
3	FBW	Negative LDO voltage feedback input pin; regulates to 0.2V nominal.
4	VCC1	Supply input, connect to V_{IN}.
5	FBB	A_{VDD} regulator voltage feedback input pin; regulates to 1.2V nominal.
6	ISADJB	Current feedback adjust for A_{VDD}.
7	ILADJB	With a resistor connected from this pin to GND sets the current limit of the external N-channel FET for A_{VDD}.
8	CINTB	A_{VDD} integrator output, connect 2.2nF to analog GND.
9	DRVB	Gate driver output for the external N-Channel switch.
10	PGNDB	Power GND for A_{VDD}.
11	VHIB	Internal Drive of Boost controller, Connect to VDCP.
12	NC	
13	ISINB	Sense the drain voltage of the external N-channel FET and connected to the internal current limit comparator.
14	VIN	Main supply input.
15	EN	Enable pin; high enable, low disabled.
16	VHIL	V_{LOGIC} boost strap mode.
17	LX	V_{LOGIC} switch connection.
18	DRVL	Gate driver output for external N-channel switch.
19	PGNDP	Power GND.
20	FBL	V_{LOGIC} regulator voltage feedback pin; regulates to 1.2V nominal.
21	ILADJL	With resistor connected from this pin to GND sets the current limit of the external N-channel FET.
22	CINTL	V_{LOGIC} integrator output, connect 2.2nF to analog GND.
23	ISADJL	Current feedback adjust for V_{LOGIC}.
24	VDC	Positive supply for all internal analog circuits.
25	VDCP	Positive supply for external N-Channel FET gate drives.
26	NC	
27	DRVP	Positive LDO base drive; open drain of an internal N-Channel MOSFET.
28	NC	
29	ACGND	Low noise signal ground.
30	VREF	Bandgap voltage bypass terminal; bypass with a 0.1µF to analog GND; can be used as charge pump reference.
31	FBP	Positive LDO voltage feedback input pin; regulates to 1.2V nominal.
32	CC2	Supply input, connect to V_{IN}.
33	CDLY	With a capacitor connect from this pin to GND, sets the delay time for start-up sequence and fault detection timeout.
34	CTL	Input control for switch output.
35	ENL	Enable pin for V_{LOGIC} high enable; low disabled.
36	DRN	Lower reference voltage for switch output.
37	COM	Switch output; when CTL = 1, COM is connected to SRC through a 15Ω resistor, when CT: = 0, COM is connected to DRN through a 30Ω resistor.
38	SRC	Upper reference voltage for switch output.

Typical Application Diagram



Applications Information

The ISL97522 provides a multiple output power supply solution for TFT-LCD applications. The system consists of a high efficiency boost controller, two low cost linear-regulator controllers (V_{ON} and V_{OFF}) and a buck reglator (V_{LOGIC}).

Table 1 below lists the recommended components.

TABLE 1. RECOMMENDED COMPONENTS

DESIGNATION	DESCRIPTION
C1, C2, C3	10µF, 16V, X7R ceramic capacitor (1206) TDK C3216X7R1C106M
C20	4.7µF, 16V X5R ceramic capacitor (1206) TDK C3216X5R1A475K
C15	1µF, 25V X7R ceramic capacitor (1206) TDK C3216X7R1E105K
D1	1A 20V low leakage schottky rectifier (CASE 457-04) ON SEMI MBRM120ET3
D11, D12, D21	200mA 30V schottky barrier diode (SOT-23) Fairchild BAT54S
L1	6.8mH 4.6A inductor Coilcraft DO3316P-682ML
Q1,Q2	6.3A 30V single N-Channel logic level PowerTrench MOSFET (SOT-23) Fairchild FDC655AN
Q3	-2A -30V single P-Channel logic level PowerTrench MOSFET (SuperSOT-3) Fairchild FDN360P
Q11	200mA 40V PNP amplifier (SOT-23) Fairchild MMBT3906
Q21	200mA 40V NPN amplifier (SOT-23) Fairchild MMBT3904

A_{VDD} Converter

The main boost converter is a current mode PWM controller operating at a fixed frequency. The 1MHz switching frequency enables the use of low profile inductor and multilayer ceramic capacitors, which results in a compact, low-cost power system for LCD panel design.

The A_{VDD} converter can operate in continuous or discontinuous inductor current mode. The ISL97522 is designed for continuous current mode, but it can also operate in discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by (in boost mode):

$$\frac{A_{VDD}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

where D is the duty cycle of switching MOSFET.

Figure 15 shows the function diagram of the boost controller. It uses a summing amplifier architecture consisting of GM stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 200kΩ is recommended. The boost converter output voltage is determined by the following equation:

$$A_{VDD} = \frac{R_1 + R_2}{R_1} \times V_{FBB} \quad \text{(EQ. 2)}$$

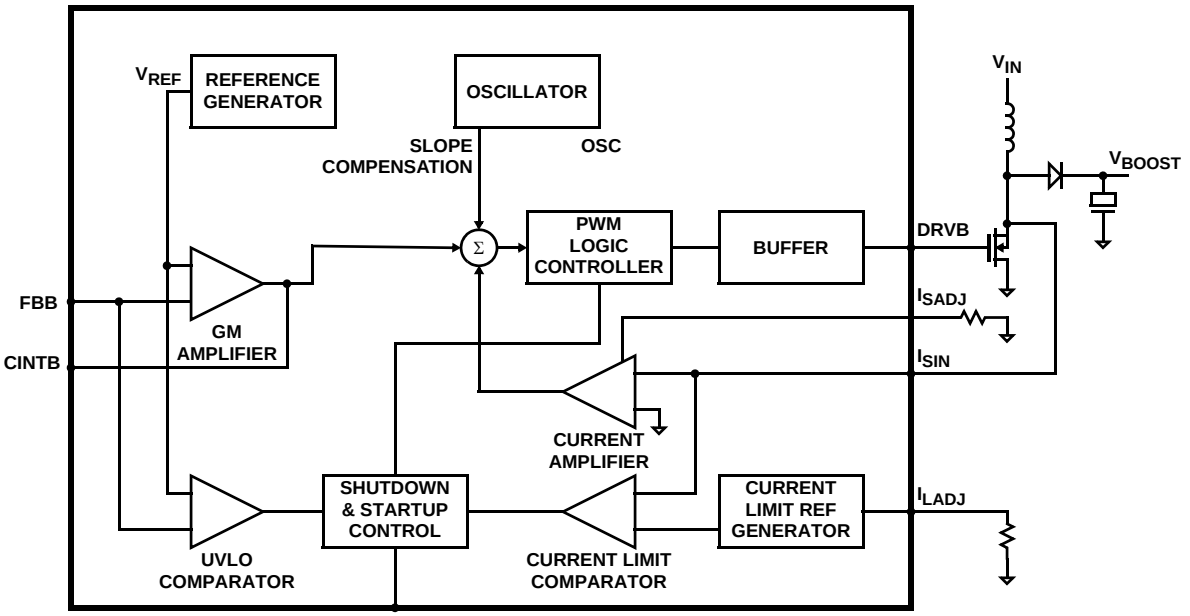


FIGURE 15. FUNCTION DIAGRAM OF THE BOOST CONTROLLER

The internal current limit circuitry is shown in Figure 16. The circuit senses the voltage across the $R_{DS(ON)}$ when the MOSFET is on; then compare it to the internal voltage reference to realize the current limit. The internal voltage reference is generated by a 10mA current and any additional current set at I_{LADJB} pin flowing through an 8kΩ resistor. The voltage reference is based on the following equation:

$$V_{THRESHOLD} = \left(\frac{V_{ILADJB}}{R_1} + 10\mu A\right) \times 8K \quad \text{(EQ. 3)}$$

Where V_{ILADJB} is the voltage at pin I_{LADJ}.

Where V_{ISAD} is the voltage at pin I_{SAD}.

$$V_{ISAD} = V_{REF} - V_{BE} - 1K \times I_{SAD}$$

$$I_{SAD} = \frac{V_{ISAD}}{R1} \quad \text{(EQ. 4)}$$

Where $V_{BE} \approx 0.7V$

The external resistor R_1 should be chosen in the order of 100K to generate µA of current.

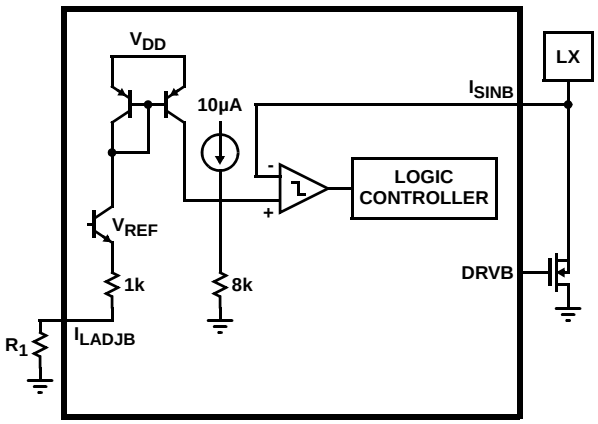


FIGURE 16. CURRENT LIMIT BLOCK DIAGRAM

Hence the maximum output current is determined by the following equation:

$$I_{OMAX} = \left(\frac{V_{THRESHOLD}}{R_{DSON}} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 5)}$$

Where ΔI_L is the peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 6)}$$

f_S is the switching frequency; D is the duty cycle.

$$D = \frac{V_O - V_{IN}}{V_O} \quad \text{(EQ. 7)}$$

To overcome the variation in external LX driver $R_{DS(ON)}$, an input is provided (ILADJ) to accommodate 5 different bands of $R_{DS(ON)}$ by using 5 different selection resistors. Internally, the ILADJ resistor adjusts two things:

1.the current limit;

2.the current feedback being used.

This keeps the dc-dc loop stable and the current limit the same over a wide range of external drive FETs.

Alternatively, the current limit can be changed for the same FET by varying the resistor. This would affect the stability of the system somewhat (because the current feedback changes) but be selected appropriately to accommodated the change. The integrator loop should keep the load regulation within limits as long as it doesn't run out of dynamic adjustment range when current feedback gets larger than intended. This could be determined by measuring how close to the upper clamp limit the voltage on the Cint pin voltage gets under maximum load current.

Here are the resistor settings on ILADJ which select the five $R_{DS(ON)}$ ranges:

1/ 0ohms (Cfb factor 1, "Cfb" are the relative current feedback factors)

2/ 30K (Cfb factor 1/1.8)

3/ 83K (Cfb factor 1/3.3)

4/ 182K (Cfb factor 1/5.7)

5/ >370K (Cfb factor 1/10)

1/ sets maximum internal current feedback and minimum ILimit, used for low Ron fets.

5/ sets minimum internal current feedback and maximum ILimit, used for large Ron fets.

The Current limit factors should be the inverse of the Cfb values.

Input Capacitor

The input capacitor is used to supply the current to the converter. It is recommended that C_{IN} be larger than 10µF. The reflected ripple voltage will be smaller with larger C_{IN}. The voltage rating of input capacitor should be larger than maximum input voltage.

Boost Inductor

A 6.8µH inductor is recommended. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1 - D} \quad \text{(EQ. 8)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 9)}$$

BOOST MOSFET

Due to the parasitic inductance of the trace, the MOSFET will experience spikes higher that the output voltage when the MOSFET turns off. Thus, a MOSFET with enough voltage margin is needed.

The $R_{DS(ON)}$ of the MOSFET is critical for power dissipation and current limit. A MOSFET with low $R_{DS(ON)}$ is desired to get high efficiency and output current, but very low $R_{DS(ON)}$ will reduce the loop stability. A MOSFET with 20mΩ to 50mΩ $R_{DS(ON)}$ is recommended. Some recommended MOSFETs are shown in Table 2.

TABLE 2. RECOMMENDED MOSFETs

PART NUMBER	MANUFACTURER	FEATURE
FDC655AN	Fairchild Semiconductor	6.3A, 30V, $R_{DS(ON)}$ = 23mΩ
FDS4488	Fairchild Semiconductor	7.9A, 30V, $R_{DS(ON)}$ = 22mΩ
Si7844DP	Vishay	10A, 30V, $R_{DS(ON)}$ = 22mΩ
SI6928DQ	Vishay	20A, 30V, $R_{DS(ON)}$ = 30mΩ

Rectifier Diode

A high-speed diode is desired due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S} \quad \text{(EQ. 10)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

PI mode C_{INT} (C_{23}) and R_{INT} (R_{10})

The IC is designed to operate with a minimum C_{23} capacitor of 4.7nF and a minimum C_2 (effective) = 10µF.

Note that, for high voltage A_{VDD}, the voltage coefficient of ceramic capacitors (C_2) reduces their effective capacitance greatly; a 16V 10µF ceramic can drop to around 3µF at 15V.

To improve the transient load response of A_{VDD} in PI mode, a resistor may be added in series with the C_{23} capacitor. The larger the resistor the lower the overshoot but at the expense of stability of the converter loop - especially at high currents.

With L = 10µH, A_{VDD} = 15V, C_{23} = 4.7nF, C_2 (effective) should have a capacitance of greater than 10µF. R_{INT} (R_7) can have values up to 5kΩ for C_2 (effective) up to 20µF and up to 10K for C_2 (effective) up to 30µF.

Larger values of R_{INT} (R_7) may be possible if maximum A_{VDD} load currents less than the current limit are used. To ensure A_{VDD} stability, the IC should be operated at the maximum desired current and then the transient load response of A_{VDD} should be used to determine the maximum value of R_{INT}

Operation of the DELB Output Function

An open drain DELB output is provided to allow the boost output voltage, developed at C_2 (see application diagram), to be delayed via an external switch (Q3) to a time after the V_{BOOST} supply and negative V_{OFF} charge pump supply have achieved regulation during the start-up sequence shown in Figure 21. This then allows the A_{VDD} and V_{ON} supplies to start-up from 0V instead of the normal offset voltage of V_{IN}-V_{DIODE} (D_1) if Q3 were not present.

When DELB is activated by the start-up sequencer, it sinks 50µA allowing a controlled turn-on of Q3 and charge-up of C_9. C_{16} can be used to control the turn-on time of Q3 to reduce inrush current into C_9. The potential divider formed by R_9 and R_8 can be used to limit the V_{GS} voltage of Q3 if required by the voltage rating of this device. When the voltage at DELB falls to less than 0.6V, the sink current is increased to ~1.2mA to firmly pull DELB to 0V.

The voltage at DELB is monitored by the fault protection circuit so that if the initial 50µA sink current fails to pull DELB below ~0.6V after the start-up sequencing has completed, then a fault condition will be detected and a fault time-out ramp will be initiated on the C_{DEL} capacitor (C_7).

Linear-Regulator Controllers (V_{ON}, V_{OFF})

The ISL97522 includes two independent linear-regulator controllers, in which one is a positive output voltage (V_{ON}), and one is negative. The V_{ON} and V_{OFF} linear-regulator controller function diagrams are shown in Figures 17, and 18, respectively.

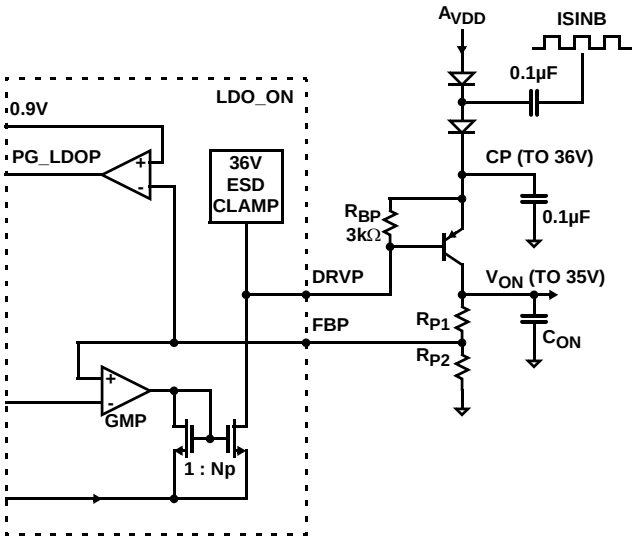


FIGURE 17. V_{ON} FUNCTION BLOCK DIAGRAM

Calculation of the Linear Regulator Base-Emitter Resistors (R_{BP} and R_{BN})

For the pass transistor of the linear regulator, low frequency gain (Hfe) and unity gain freq. (f_T) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/Hfe$. Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high frequency low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor R_{BE} (R_{BP}, R_{BL}, R_{BN} in the Functional Block Diagram), which increase the pole frequency to: $f_p = f_T*(1+ Hfe *re/R_{BE})/Hfe$, where re = KT/qIc. So choose the lowest value R_{BE} in the design as long as there is still enough base current (I_B) to support the maximum output current (I_C).

We will take as an example the V_{ON} linear regulator. If a Fairchild MMBT3906 PNP transistor is used as the external pass transistor, Q11 in the application diagram, then for a maximum V_{ON} operating requirement of 50mA the data sheet indicates HFE_min = 30.
The base-emitter saturation voltage is: Vbe_max = 0.7V.

For the ISL97522, the minimum drive current is:
I_DRVP_min = 2mA.

The minimum base-emitter resistor, R_{BP}, can now be calculated as:

R_{BP}_min = V_{BE}_max/(I_DRVP_min - Ic/Hfe_min) = 0.7V/(2mA - 50mA/30) = 2.1kΩ

This is the minimum value that can be used - so, we now choose a convenient value greater than this minimum value; say 3KΩ. Larger values may be used to reduce quiescent current, however, regulation may be adversely affected, by supply noise if R_{BP} is made too high in value.

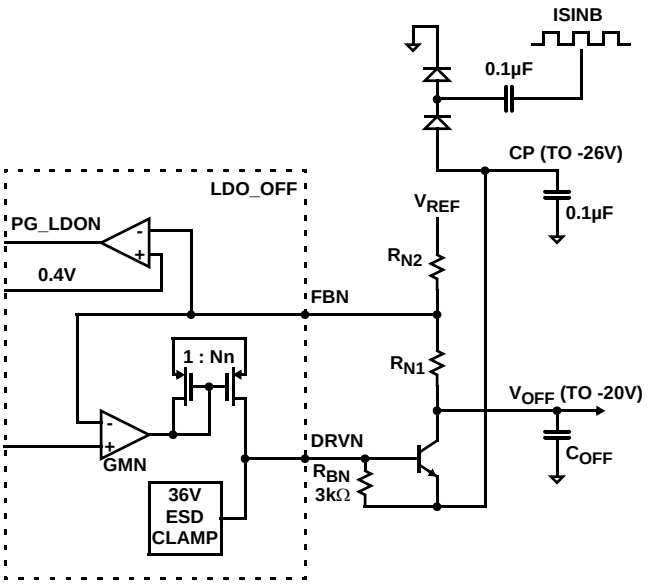


FIGURE 18. V_{OFF} FUNCTION BLOCK DIAGRAM

The V_{ON} power supply is used to power the positive supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the switch node (LXB) of the A_{VDD} converter, followed by a low dropout linear regulator (LDO_ON). The LDO_ON regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V_{ON} voltage supported by the ISL97522 ranges from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 16.7% below the 1.2V reference.

The V_{OFF} power supply is used to power the negative supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the switch node (LXB) of the A_{VDD} converter, followed by a low dropout linear regulator (LDO_OFF). The LDO_OFF regulator uses an external NPN transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V_{OFF} voltage supported by the ISL97522 ranges from -5V to -25V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 20% above the 1.0V reference level.Set-Up LDOs Output Voltage.

Set-Up LDOs Output Voltage

Refer to Typical Application Diagram, the output voltages of V_{ON}, V_{OFF}, and V_{LOGIC} are determined by Equations 11 and 12:

$$V_{ON} = V_{FBP} \times \left(1 + \frac{R_{12}}{R_{11}}\right) \quad \text{(EQ. 11)}$$

$$V_{OFF} = V_{FBN} + \frac{R_{22}}{R_{21}} \times (V_{FBN} - V_{REF}) \quad \text{(EQ. 12)}$$

Charge Pump

To generate an output voltage higher than A_{VDD}, single or multi stages of charge pumps are needed. The number of stage is determined by the input and output voltage. For positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{OUT} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \times V_F} \quad \text{(EQ. 13)}$$

where V_{CE} is the dropout voltage of the pass component of the linear regulator. It ranges from 0.3V to 1V depending on the transistor. V_F is the forward-voltage of the charge pump rectifier diode.

The number of negative charge pump stages is given by:

$$N_{NEGATIVE} \geq \frac{|V_{OUTPUT}| + V_{CE}}{V_{INPUT} - 2 \times V_F} \quad \text{(EQ. 14)}$$

To achieve high efficiency and low material cost, the lowest number of charge pump stages, which can meet the above requirements, is always preferred.

Charge Pump Output Capacitors

A ceramic capacitor with low ESR is recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by Equation 15.

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}} \quad \text{(EQ. 15)}$$

Where f_{SOC} is the switching frequency.

High Charge Pump Output Voltage (>36V) Applications

In the applications where the charge pump output voltage is over 36V, an external npn transistor need to be inserted into between DRVP pin and base of pass transistor Q3 as shown in Figure 19; or the linear regulator can control only one stage charge pump and regulate the final charge pump output as shown in Figure 20.

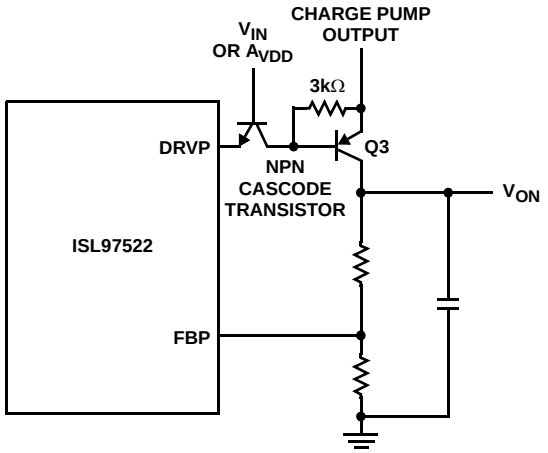


FIGURE 19. CASCODE NPN TRANSISTOR CONFIGURATION FOR HIGH CHARGE PUMP OUTPUT VOLTAGE (>36V)

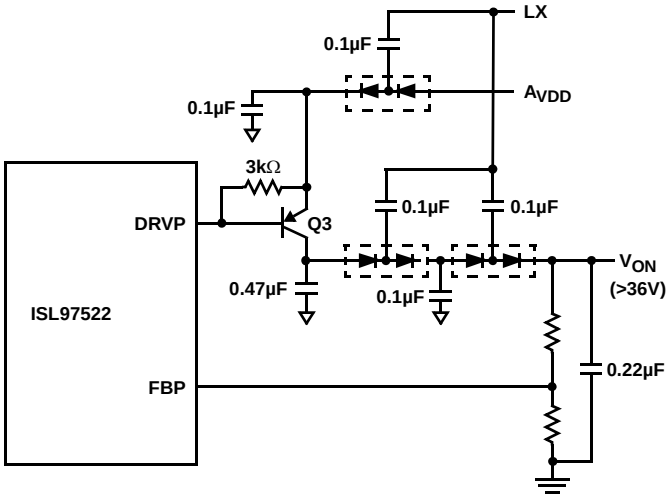


FIGURE 20. THE LINEAR REGULATOR CONTROLS ONE STAGE OF CHARGE PUMP

Discontinuous/Continuous Boost Operation and its Effect on the Charge Pumps

The ISL97522 V_{ON} and V_{OFF} architecture uses LX switching edges to drive diode charge pumps from which LDO regulators generate the V_{ON} and V_{OFF} supplies. It can be appreciated that should a regular supply of LX switching edges be interrupted, for example during discontinuous operation at light A_{VDD} boost load currents, then this may affect the performance of V_{ON} and V_{OFF} regulation - depending on their exact loading conditions at the time.

To optimize V_{ON}/V_{OFF} regulation, the boundary of discontinuous/continuous operation of the boost converter can be adjusted, by suitable choice of inductor given V_{IN}, V_{OUT}, switching frequency and the A_{VDD} current loading, to be in continuous operation.

The following equation gives the boundary between discontinuous and continuous boost operation. For continuous operation (LX switching every clock cycle) we require that:

$I(A_{VDD}\_load) > D*(1-D)*V_{IN}/(2*L*F_{OSC})$

where the duty cycle, $D = (A_{VDD} - V_{IN})/A_{VDD}$

For example, with V_{IN} = 5V, F_{OSC} = 1.0MHz and A_{VDD} = 12V we find continuous operation of the boost converter can be guaranteed for:

L = 10µH and $I(A_{VDD}) > 61mA$

L = 6.8µH and $I(A_{VDD}) > 89mA$

L = 3.3µH and $I(A_{VDD}) > 184mA$

Buck Converter

The buck converter is the step down converter, which supplies the current to the logic circuit of the LCD system. In the continuous current mode, the relationship between input voltage and output voltage is as following:

$$\frac{LOGIC}{V_{IN}} = D \qquad \text{(EQ. 16}$$

Where D is the duty cycle of the switching MOSFET. Because D is always less than 1, the output voltage of buck converter is lower than input voltage.

The Feedback Resistors

The buck converter output voltage is determined by the following equation:

$$V_{LOGIC} = \frac{R_{12} + R_{13}}{R_{13}} \times V_{FBL} \qquad \text{(EQ. 17)}$$

Where R12 and R13 are the feedback resistors of buck converter to set the output voltage Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 300Ω is recommended.

Buck Converter Input Capacitor

The capacitor should support the maximum AC RMS current which happens when D = 0.5 and maximum output current.

$$I_{acrms}(C_{IN}) = \sqrt{D \cdot (1-D)} \cdot I_O \qquad \text{(EQ. 18)}$$

Where I_O is the output current of the buck converter.

Buck Inductor

An inductor value in the range 3.3-10µH is recommended for the buck converter. Besides the inductance, the DC resistance and the saturation current should also be considered when choosing buck inductor. Low DC resistance can help maintain high efficiency, and the saturation current rating should be at least maximum output current plus half of ripple current.

Buck MOSFET

The principle to select Buck MOSFET is similar to that of Boost. The voltage of stress of buck converter should be maximum input voltage plus reasonable margin, and the current rating should be over the maximum output current. The $r_{DS(ON)}$ of this MOSFET should be in the range from 20mΩ to 50mΩ.

Rectifier Diode (Buck Converter)

A Schottky diode is recommended due to fast recovery and low forward voltage. The reverse voltage rating should be higher than the maximum input voltage. The average current should be as the following equation,

$$I_{AVG} = (1 - D) * I_O \quad \text{(EQ. 19)}$$

Where I_O is the output current of buck converter.

Output Capacitor (Buck Converter)

Four 10µF or two 22µF ceramic capacitors are recommended for this part. The overshoot and undershoot will be reduced with more capacitance, but the recovery time will be longer.

PI Loop Compensation (Buck Converter)

The buck converter of ISL97522 can be compensated by a RC network connected from CINTL pin to ground. C27 = 4.7nF and R17= 2k RC network is used in the demo board. The larger value resistor can lower the transient overshoot, however, at the expense of stability of the loop.

The stability can be optimized in a similar manner to that described in the section on "PI Loop Compensation (Boost Converter)".

Bootstrap Capacitor (C28)

This capacitor is used to provide the supply to the high driver circuitry for the buck MOSFET. The bootstrap supply is formed by an internal diode and capacitor combination. A 1µF is recommended for ISL97522. A low value capacitor can lead to overcharging and in turn damage the part.

If the load is too light, the on-time of the low side diode may be insufficient to replenish the bootstrap capacitor voltage. In this case, if V_{IN}-V_{BUCK} < 1.5V, the internal MOSFET pull-up device may be unable to turn-on until V_{LOGIC} falls. Hence, there is a minimum load requirement in this case. The minimum load can be adjusted by the feedback resistors to FBL.

The bootstrap capacitor can only be charged when the higher side MOSFET is off. If the load is too light which can not make the on time of the low side diode be sufficient to replenish the boot strap capacitor, the MOSFET can't turn on. Hence there is minimum load requirement to charge the bootstrap capacitor properly.

Start-Up Sequence

Figure 21 shows a detailed start-up sequence waveform. For a successful power-up, there should be six peaks at V_{CDLY}. When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

If EN is L, the device is powered down. If EN is H, and the input voltage (V_{IN}) exceeds 2.5V, an internal current source starts to charge C_{DLY} to an upper threshold using a fast ramp followed by a slow ramp. If EN is low at this point, the C_{DLY} ramp will be delayed until EN goes high.

The first four ramps on C_{DLY} (two up, two down) are used to initialize the fault protection switch and to check whether there is a fault condition on C_{DLY} or V_{REF}. If a fault is detected, the outputs and the input protection will turn off and the chip will power down.

If no fault is found, C_{CDLY} continues ramping up and down until the sequence is completed.

During the second ramp, the device checks the status of V_{REF} and over temperature.

Initially the boost is not enabled so V_{BOOST} rises to V_{IN}-V_{DIODE} through the output diode. Hence, there is a step at V_{BOOST} during this part of the start-up sequence. If this step is not desirable, an external PMOS FET can be used to delay the output until the boost is enabled internally. The delayed output appears at A_{VDD}.

V_{BOOST} soft-starts at the beginning of the third ramp. The soft-start ramp depends on the value of the C_{DLY} capacitor. For C_{DLY} of 220nF, the soft-start time is ~2ms.

V_{OFF} turns on at the start of the fourth peak. At the fifth peak, the open drain o/p DELB goes low to turn on the external PMOS Q3 to generate a delayed V_{BOOST} output.

V_{ON} is enabled at the beginning of the sixth ramp. A_{VDD}, V_{OFF}, DELB and V_{ON} are checked at end of this ramp.

Vlogic's start-up is controlled by ENL. When ENL is L, Vlogic is off, and when ENL is H, V_{LOGIC} is on.

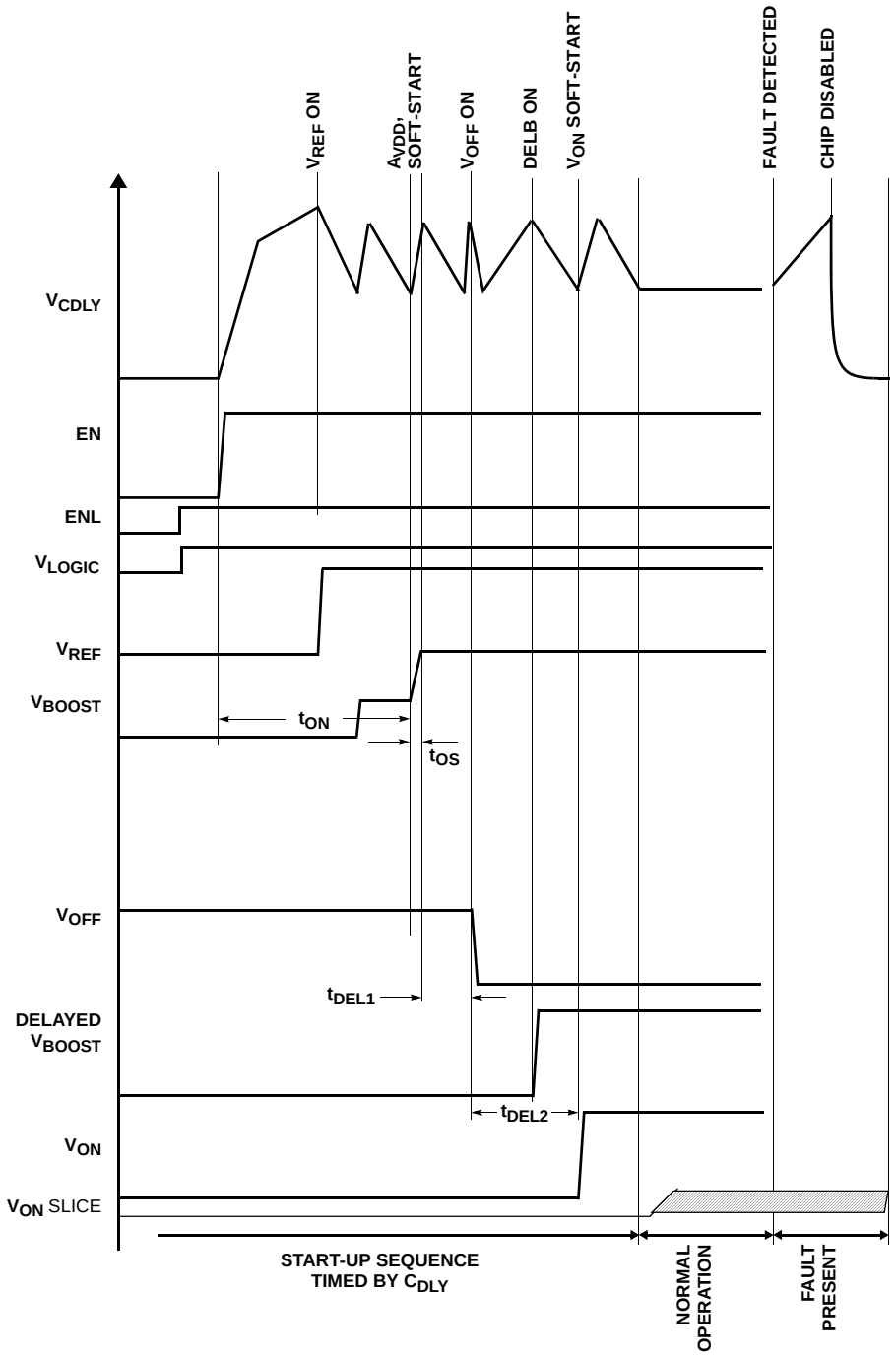


FIGURE 21. ISL97522 START-UP SEQUENCE

Fault Protection

During the startup sequence, prior to BOOST soft-start, V_{REF} is checked to be within ±20% of its final value and the device temperature is checked. If either of these are not within the expected range, the part is disabled until the power is recycled or EN is toggled.

If C_{DELAY} is shorted low, then the sequence will not start, while if C_{DELAY} is shorted H, the first down ramp will not occur and the sequence will not complete.

Once the start-up sequence is completed, the chip continuously monitors C_{DLY}, DELB, FBP, FBL, FBN, V_{REF} and FBB for faults. During this time, the voltage on the C_{DLY} capacitor remains at 1.15V until either a fault is detected, or the EN pin is pulled low.

A fault on C_{DELAY}, V_{REF} or temperature will shut down the chip immediately. If a fault on any other output is detected, C_{DELAY} will ramp up linearly with a 5µA (typical) current to the upper fault threshold (typically 2.4V), at which point the chip is disabled until the power is recycled or EN is toggled. If the fault condition is removed prior to the end of the ramp, the voltage on the C_{DLY} capacitor returns to 1.15V.

Typical fault thresholds for FBP, FBL, FBN and FBB are included in the tables. DELB fault threshold is typically 0.6V.

C_{INTB} and C_{INTL} have an internal current-limited clamp to keep the voltage within their normal ranges. If they are shorted low, the regulators will attempt to regulate to 0V.

If any of the regulated outputs (AVDD, V_{ON}, V_{OFF} or V_{LOGIC}) are driven above their target levels the drive circuitry will switch off until the output returns to its expected value.

If AVDD and V_{LOGIC} are excessively loaded, the current limit will prevent damage to the chip. While in current limit, the part acts like a current source and the regulated output will drop. If the output drops below the fault threshold, a ramp will be initiated on C_{DELAY} and, provided that the fault is sustained, the chip will be disabled on completion of the ramp.

In some circumstances, (depending on ambient temperature and thermal design of the board), continuous operation at current limit may result in the over-temperature threshold being exceeded, which will cause the part to disable immediately.

All I/O also have ESD protection, which in many cases will also provide overvoltage protection, relative to either ground or V_{DD}. However, these will not generally operate unless abs max ratings are exceeded.

Component Selection for Start-Up Sequencing and Fault Protection

The C_{REF} capacitor is typically set at 220nF and is required to stabilize the V_{REF} output. The range of C_{REF} is from 22nF to 1µF and should not be more than five times the capacitor on C_{DEL} to ensure correct start-up operation.

The C_{DEL} capacitor is typically 220nF and has a usable range from 47nF minimum to several microfarads - only limited by the leakage in the capacitor reaching µA levels.

C_{DEL} should be at least 1/5 of the value of C_{REF} (See above). Note with 220nF on C_{DEL} the fault time-out will be typically 50ms and the use of a larger/smaller value will vary this time proportionally (e.g. 1µF will give a fault time-out period of typically 230ms).

Fault Sequencing

The ISL97522 has an advanced fault detection system which protects the IC from both adjacent pin shorts during operation and shorts on the output supplies.

A high quality layout/design of the PCB, in respect of grounding quality and decoupling is necessary to avoid falsely triggering the fault detection scheme - especially during start-up. The user is directed to the layout guidelines and component selection sections to avoid problems during initial evaluation and prototype PCB generation.

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that the die temperature exceeds the thermal trip point of 140°C, the device will shut down.

Layout Recommendation

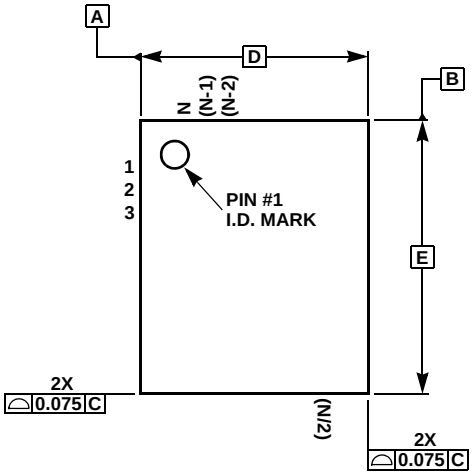
The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

There are some general guidelines for layout:

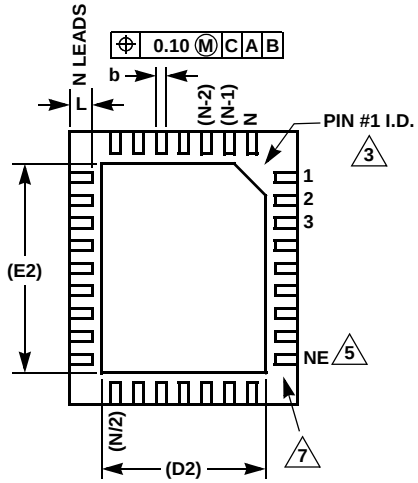
1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF}, V_{DC} and V_{DCP} bypass capacitors close to the pins.
3. Minimize the length of traces carrying fast signals and high current.
4. All feedback networks should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point near the main decoupling capacitors.

6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separate from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for feedback resistor networks (R_1, R_{11}, R_{41}) and the V_{REF} capacitor, C_{25}, the C_{DELAY} capacitor C_7 and the integrator capacitor C_{30}, C_{27}.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

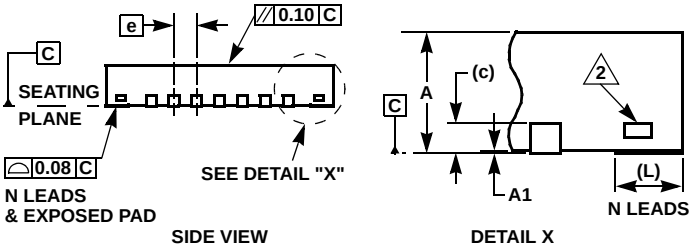
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



TOP VIEW



BOTTOM VIEW



SIDE VIEW DETAIL X

L38.5x7B (One of 10 Packages in MDP0046)

38 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
D		5.00 BSC		-
D2		3.50 REF		-
E		7.00 BSC		-
E2		5.50 REF		-
L	0.35	0.40	0.45	-
b	0.23	0.25	0.27	-
c		0.20 REF		-
e		0.50 BSC		-
N		38 REF		4
ND		7 REF		6
NE		12 REF		5

Rev 0 5/06

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.