International
IOR Rectifier

IR3521

DATA SHEET

XPHASE3™ AMD SVID CONTROL IC

DESCRIPTION

The IR3521 Control IC combined with an *xPHASE3*™ Phase IC provides a full featured and flexible way to implement a complete AMD SVID power solution. It provides outputs for both the VDD core and VDDNB auxiliary planes required by the CPU. The IR3521 provides overall system control and interfaces with any number of Phase ICs each driving and monitoring a single phase. The *xPHASE3*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- 2 converter outputs for the AMD processor VDD core and VDDNB auxiliary planes
- Supports High Speed (HS) I^2C Serial communications
- PSI_L serial commands are communicated to a programmable number of phase ICs
- 0.5% overall system set point accuracy
- High speed error amplifiers with wide bandwidth of 20MHz and fast slew rate of 10V/us
- Remote sense amplifiers provide differential sensing and require less than 50uA bias current
- Programmable Dynamic VID Slew Rates
- Programmable VID Offset (VDD output only)
- Programmable output impedance (VDD output only)
- Programmable Dynamic OC for IDD_Spike
- Programmable per phase switching frequency of 250kHz to 1.5MHz
- Hiccup over current protection with delay during normal operation
- Central over voltage detection and communication to phase ICs through IIN (ISHARE) pin
- OVP disabled during dynamic VID down to prevent false triggering
- Over voltage signal to system with over voltage detection during powerup and normal operation
- Detection and protection of open remote sense lines
- Gate Drive and IC bias linear regulator control with programmable output voltage and UVLO
- Small thermally enhanced 32L MLPQ (5mm x 5mm) package

ORDERING INFORMATION

Device	Package	Order Quantity
IR3521MTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
IR3521MPBF (Samples Only)	32 Lead MLPQ (5 x 5 mm body)	100 piece strips

APPLICATION CIRCUIT

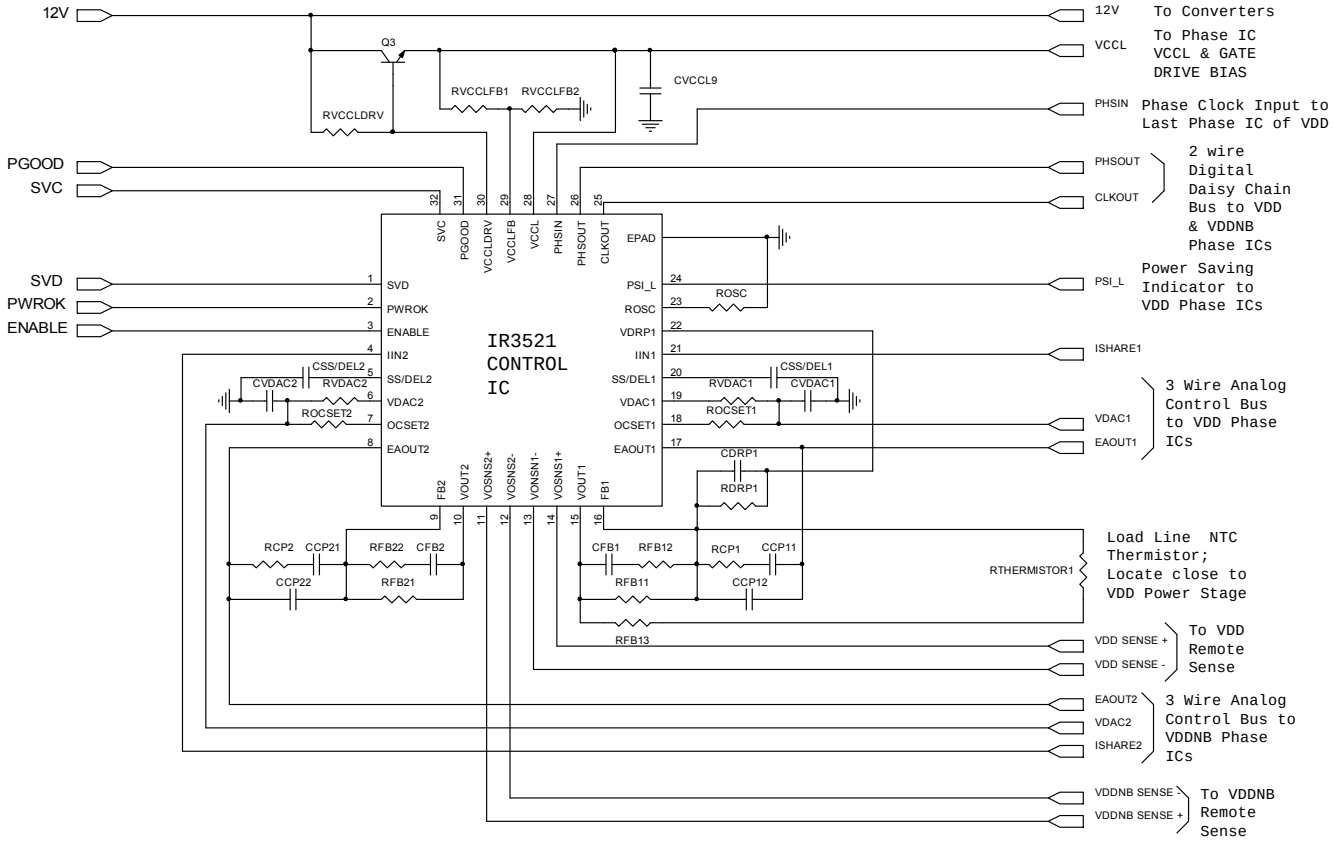


Figure 1 – IR3521 Application Circuit

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	SVD	SVD (Serial VID Data) is a bidirectional signal that is an input and open drain output for both master (AMD processor) and slave (IR3521), requires an external bias voltage and should not be floated
2	PWROK	System wide Power Good signal and input to the IR3521. When asserted, the IR3521 output voltage is programmed through the SVID interface protocol. Connecting this pin to VCCL enables VFIX mode.
3	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. A logic high on the pin enables the converter and causes the SVC and SVD input states to be decoded and stored, determining the 2-bit Boot VID. Do not float this pin as the logic state will be undefined.
4	IIN2	Output 2 average current input from the output 2 phase IC(s). This pin is also used to communicate over voltage condition to the output 2 phase ICs.
5	SS/DEL2	Programs output 2 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
6	VDAC2	Output 2 reference voltage programmed by the SVID inputs and error amplifier non-inverting input. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.
7	OCSET2	Programs the output 2 constant converter output current limit and hiccup over-current threshold through an external resistor tied to VDAC2 and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC2 to program the threshold higher than the possible signal into the IIN2 pin from the phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
8	EAOUT2	Output of the output 2 error amplifier.
9	FB2	Inverting input to the Output 2 error amplifier.
10	VOUT2	Output 2 remote sense amplifier output.
11	VOSEN2+	Output 2 remote sense amplifier input. Connect to output at the load.
12	VOSEN2-	Output 2 remote sense amplifier input. Connect to ground at the load.
13	VOSEN1-	Output 1 remote sense amplifier input. Connect to ground at the load.
14	VOSEN1+	Output 1 remote sense amplifier input. Connect to output at the load.
15	VOUT1	Output 1 remote sense amplifier output.
16	FB1	Inverting input to the output 1 error amplifier. Converter output voltage can be increased from the VDAC1 voltage with an external resistor connected between VOUT1 and this pin (there is an internal current sink at this pin).
17	EAOUT1	Output of the output 1 error amplifier.
18	OCSET1	Programs the output 1 constant converter output current limit and hiccup over-current threshold through an external resistor tied to VDAC1 and an internal current source from this pin. Over-current protection can be disabled by connecting a resistor from this pin to VDAC1 to program the threshold higher than the possible signal into the IIN1 pin from the phase ICs but no greater than 5V (do not float this pin as improper operation will occur).
19	VDAC1	Output 1 reference voltage programmed by the SVID inputs and error amplifier non-inverting input. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.

PIN#	PIN SYMBOL	PIN DESCRIPTION
20	SS/DEL1	Programs output 1 startup and over current protection delay timing. Connect an external capacitor to LGND to program.
21	IIN1	Output 1 average current input from the output 1 phase IC(s). This pin is also used to communicate over voltage condition to phase ICs.
22	VDRP1	Output 1 Buffered IIN1 signal. Connect an external RC network to FB1 to program converter output impedance.
23	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency and OCSET1, OCSET2, FB1, FB2, VDAC1, and VDAC2 bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation and higher than 1.6V if over-voltage condition is detected.
24	PSI_L	Digital output to communicate the systems power state to phase ICs PSI_L pin.
25	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
27	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
28	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND. No external power rail connection is allowed.
29	VCCLFB	Non-inverting input of the voltage regulator error amplifier. Output voltage of the regulator is programmed by the resistor divider connected to VCCL.
30	VCCLDRV	Output of the VCCL regulator error amplifier to control external transistor. The pin senses 12V power supply through a resistor.
31	PGOOD	Open collector output that drives low during startup and under any external fault condition. And it monitors output voltages, if any of the voltage planes fall out of spec, it will drive low. Connect external pull-up. (Output voltage out of spec is defined as 350mV to 240mV below VDAC voltage)
32	SVC	SVC (Serial VID Clock) is an open drain output of the processor and input to IR3521, requires an external bias voltage and should not be floated
EPAD	LGND	Local ground for internal circuitry and IC substrate connection.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. All voltages are absolute voltages referenced to the LGND pin.

Operating Junction Temperature……..0 to 150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	SVD	8V	-0.3V	1mA	10mA
2	PWROK	8V	-0.3V	1mA	1mA
3	ENABLE	3.5V	-0.3V	1mA	1mA
4	IIN2	8V	-0.3V	5mA	1mA
5	SS/DEL2	8V	-0.3V	1mA	1mA
6	VDAC2	3.5V	-0.3V	1mA	1mA
7	OCSET2	8V	-0.3V	1mA	1mA
8	EAOUT2	8V	-0.3V	25mA	10mA
9	FB2	8V	-0.3V	1mA	1mA
10	VOUT2	8V	-0.3V	5mA	25mA
11	VOSEN2+	8V	-0.5V	5mA	1mA
12	VOSEN2-	1.0V	-0.5V	5mA	1mA
13	VOSEN1-	1.0V	-0.5V	5mA	1mA
14	VOSEN1+	8V	-0.5V	5mA	1mA
15	VOUT1	8V	-0.3V	5mA	25mA
16	FB1	8V	-0.3V	1mA	1mA
17	EAOUT1	8V	-0.3V	25mA	10mA
18	OCSET1	8V	-0.3V	1mA	1mA
19	VDAC1	3.5V	-0.3V	1mA	1mA
20	SS/DEL1	8V	-0.3V	1mA	1mA
21	IIN1	8V	-0.3V	5mA	1mA
22	VDRP1	8V	-0.3V	35mA	1mA
23	ROSC/OVP	8V	-0.3V	1mA	1mA
24	PSI_L	VCCL+ 0.3V	-0.3V	1mA	20mA
25	CLKOUT	8V	-0.3V	100mA	100mA
26	PHSOUT	8V	-0.3V	10mA	10mA
27	PHSIN	8V	-0.3V	1mA	1mA
28	VCCL	8V	-0.3V	1mA	20mA
29	VCCLFB	3.5V	-0.3V	1mA	1mA
30	VCCLDRV	10V	-0.3V	1mA	50mA
31	PGOOD	VCCL + 0.3V	-0.3V	1mA	20mA
32	SVC	8V	-0.3V	1mA	1mA
EPAD	LGND	n/a	n/a	20mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN
4.75V ≤ VCCL ≤ 7.5V, -0.3V ≤ VOSEN-x ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, 7.75 kΩ ≤ R_{OSC} ≤ 50 kΩ, $C_{SS/DELx}$ = 0.1uF

ELECTRICAL CHARACTERISTICS

The electrical characteristics table shows the spread of values guaranteed within the recommended operating conditions (unless otherwise specified). Typical values (TYP) represent the median values, which are related to 25°C.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SVID Interface					
SVC & SVD Input Thresholds	Threshold Increasing	0.8025	0.90	**0.9975**	V
	Threshold Decreasing	**570**	650	750	mV
	Threshold Hysteresis	**150**	250	400	mV
Bias Current	0V ≤ V(x) ≤ 3.5V, SVD not asserted	-5	0	5	uA
SVD Low Voltage	I(SVD)= 3mA		20	300	mV
SVD Fall Time, C_{SVD}=400 pF	70-30% VDDIO, 1.425V ≤ VDDIO ≤ 1.9V, 1.7MHz operation, Note 1	**20**	**40**	**160**	ns
SVD Fall Time, C_{SVD}=100 pF	3.4MHz operation		**20**	**80**	ns
Pulse width input filter	Note 1	**10**	20	20 <100	ns
PSI_L OUTPUT					
Output Voltage	I(PSI_L) = 3mA		150	300	mV
Pull-up Resistance (to VCCL)		6	10	20	kΩ
Oscillator					
PHSOUT Frequency		**-10%**	**See Figure 2**	**+10%**	kHz
ROSC Voltage		0.57	0.600	0.630	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
VDRP1 Buffer Amplifier					
Input Offset Voltage	V(VDRP1) – V(IIN1), 0.5V ≤ V(IIN) ≤ 3.3V	**-8**	**0**	**8**	mV
Source Current	0.5V ≤ V(IIN1) ≤ 3.3V	2		30	mA
Sink Current	0.5V ≤ V(IIN1) ≤ 3.3V	0.2	0.4	0.6	mA
Unity Gain Bandwidth	Note 1		8		MHz
Slew Rate	Note 1		4.7		V/μs
IIN Bias Current		-2	-0.2	1	μA
Remote Sense Differential Amplifiers					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V, Note 2	-3	0	3	mV
Source Current	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V	0.5	1	1.7	mA
Sink Current	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V	2	12	18	mA
Slew Rate	0.5V≤ V(VOSENx+) - V(VOSENx-) ≤ 1.6V	2	4	8	V/us
VOSEN+ Bias Current	TBS V < V(VOSENx+) < 1.6V		30	50	uA
VOSEN- Bias Current	-0.3V ≤ VOSENx- ≤ 0.3V, All VID Codes		30	50	uA
VOSEN+ Input Voltage Range	V(VCCL)=7V			5.5	V
Low Voltage	V(VCCL) =7V			250	mV
High Voltage	V(VCCL) – V(VOUTx)		0.5	1	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Delay					
Start Delay	Measure Enable to EAOUTx activation	1	2.9	3.5	ms
Start-up Time	Measure Enable activation to PGOOD	3	8	13	ms
OC Delay Time	V(IINx) – V(OCSETx) = 500 mV	85	170	325	us
SS/DELx to FBx Input Offset Voltage	With FBx = 0V, adjust V(SS/DELx) until EAOUTx drives high	0.7	1.4	1.9	V
Charge Current		-30	-50	-70	µA
OC Delay/VID Off Discharge Currents	Note 1		47		µA
Fault Discharge Current		2.5	4.5	6.5	µA
Hiccup Duty Cycle	I(Fault) / I(Charge)	7	10	12	uA/uA
Charge Voltage		3.5	3.9	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx rising Note 1		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx falling Note 1		120		mV
Delay Comparator Hysteresis	Note 1		40		mV
Discharge Comp. Threshold		150	200	300	mV
Over-Current Comparators					
Input Offset Voltage	1V ≤ V(OCSETx) ≤ 3.3V	-35	0	35	mV
OCSET Bias Current		**-5%**	**Vrosc(V)*1000/Rosc(KΩ)**	**+5%**	µA
2048-4096 Count Threshold	Adjust ROSC value to find threshold		16		kΩ
1024-2048 Count Threshold	Adjust ROSC value to find threshold		20		kΩ
Error Amplifiers					
System Set-Point Accuracy (Deviation from Table 1, 2, and 3 per test circuit in Figures 2A & 2B)	VID ≥ 1V	**-0.5**		**0.5**	%
	0.8V ≤ VID < 1V	-5		+5	mV
	0.5V ≤ VID < 0.8V	-8		+8	mV
Input Offset Voltage	Measure V(FBx) – V(VDACx)). Note 2	-1	0	1	mV
FB1 Bias Current		**-5%**	**Vrosc(V)*1000/Rosc(KΩ)**	**+5%**	µA
FB2 Bias Current		-1	0	1	µA
DC Gain	Note 1	**100**	**110**	**135**	dB
Bandwidth	Note 1	**20**	30	40	MHz
Slew Rate	Note 1	**5.5**	12	20	V/µs
Sink Current		0.4	0.85	1	mA
Source Current		5.0	8.5	12.0	mA
Maximum Voltage	Measure V(VCCL) – V(EAOUTx)	500	780	950	mV
Minimum Voltage			120	250	mV
Open Voltage Loop Detection Threshold	Measure V(VCCL) - V(EAOUT), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Voltage Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUTx) = V(VCCL) to PGOOD = low.		8		Pulses
Enable Input					
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
VDAC References					
Source Currents	Includes I(OCSETx)	**-8%**	**3050*Vrosc(V) / ROSC(kΩ)**	**+8%**	µA
Sink Currents	Includes I(OCSETx)	**-8%**	**2650*Vrosc(V) / ROSC(kΩ)**	**+8%**	µA
PGOOD Output					
Under Voltage Threshold - Voutx Decreasing	Reference to VDACx	-365	-315	-265	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Under Voltage Threshold - Voutx Increasing	Reference to VDACx	-325	-275	-225	mV
Under Voltage Threshold Hysteresis		5	53	110	mV
Output Voltage	I(PGOOD) = 4mA		150	300	mV
Leakage Current	V(PGOOD) = 5.5V		0	10	μA
VCCL Activation Threshold	I(PGOOD) = 4mA, V(PGOOD) = 300mV		1.73	3.5	V
Over Voltage Protection (OVP) Comparators					
Threshold at Power-up		1.60	1.73	1.83	V
Voutx Threshold Voltage	Compare to V(VDACx)	**220**	**260**	**285**	mV
OVP Release Voltage during Normal Operation	Compare to V(VDACx)	-20	3	25	mV
Threshold during Dynamic VID down		1.8	1.85	1.9	V
Dynamic VID Detect Comparator Threshold	Note 1	25	50	75	mV
Propagation Delay to IIN	Measure time from V(Voutx) > V(VDACx) (250mV overdrive) to V(IINx) transition to > 0.9 * V(VCCL).		90	180	ns
OVP High Voltage	Measure V(VCCL)-V(ROSC/OVP)	0		1.2	V
OVP Power-up High Voltage	V(VCCLDRV)=1.8V. Measure V(VCCL)-V(ROSC/OVP)	0		0.2	V
Propagation Delay to OVP	Measure time from V(Voutx) > V(VDACx) (250mV overdrive) to V(ROSC/OVP) transition to >1V.		150	300	nS
IIN Pull-up Resistance			5	15	Ω
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(Voutx) < [V(VOSENx+) – V(LGND)] / 2	29	62.5	90	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	86.5	89.0	91.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(Voutx) = 100mV	200	500	700	uA
VCCL Regulator Amplifier					
Reference Feedback Voltage		1.15	1.2	1.25	V
VCCLFB Bias Current		-1	0	1	uA
VCCLDRV Sink Current		10	40		mA
UVLO Start Threshold	Compare to V(VCCL)	89.0	93.5	97.0	%
UVLO Stop Threshold	Compare to V(VCCL)	81.0	85.0	89.0	%
Hysteresis	Compare to V(VCCL)	7.0	8.25	9.5	%
ENABLE, PWROK Inputs					
Threshold Increasing		1.3	1.65	**1.9**	V
Threshold Decreasing		**0.8**	0.99	1.2	V
Threshold Hysteresis		470	620	770	mV
Bias Current	0V ≤ V(x) ≤ 3.5V, SVC not asserted	-5	0	5	uA
PWROK VFIX Mode Threshold		3.3 V	(VCCL +3.3)(V) / 2	VCCL	V
General					
VCCL Supply Current		**3.5**	**10**	**15**	mA

Note 1: Guaranteed by design, but not tested in production **Note 2:** VDACx Outputs are trimmed to compensate for Error & Amp Remote Sense Amp input offset.

PHSOUT FREQUENCY VS RROSC CHART

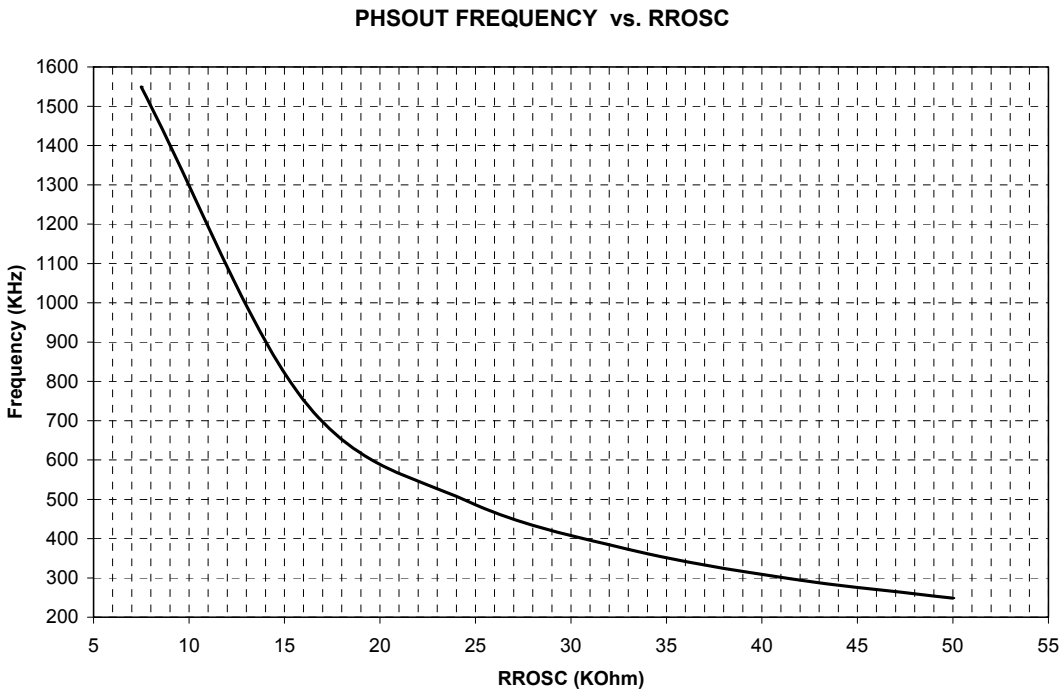


Figure 2 - Phout Frequency vs. RROSC chart

System Fault Table

Response	Open Daisy	Open Sense	Open Voltage	UVLO (VCCL)	Over Voltage	Disable	VID_OFF SVID	OC Before	OC After	UVLO (Vout)
Latch	UV & EN Latch			EN Fault Latch		SS Latch				No
Reset	Recycle VCCL then Enable			Recycle Enable		SS discharge below 0.2V				No
Outputs Affected	Both	Single		Both	Both	Both	Single	Single		Single
Disables EA	Yes									No
SS/DELx Discharge	Yes									No
Flags PGood	Yes									
Delays	32 Clock Pulses	No	8 PHSOUT Pulses	No	No	250ns Blanking Time	No	PHSOUT Pulses*	SS/DELx Discharge Threshold	No
Additional Flagged Response	No				Yes, IINx and Rosc pins pulled-up to VCCL	No				

* Pulse number range depends on Rosc value selected (See Specifications Table)

SYSTEM SET POINT TEST

The converter output voltage is determined by the system set point voltage which is the voltage that appears at the FBx pins when the converter is in regulation. The set point voltage includes error terms for the VDAC digital-to-analog converters, Error Amp input offsets, and Remote Sense input offsets. The voltage appearing at the VDACx pins is not the system set point voltage. System set point voltage test circuits for Outputs 1 and 2 are shown in Figures 3A and 3B.

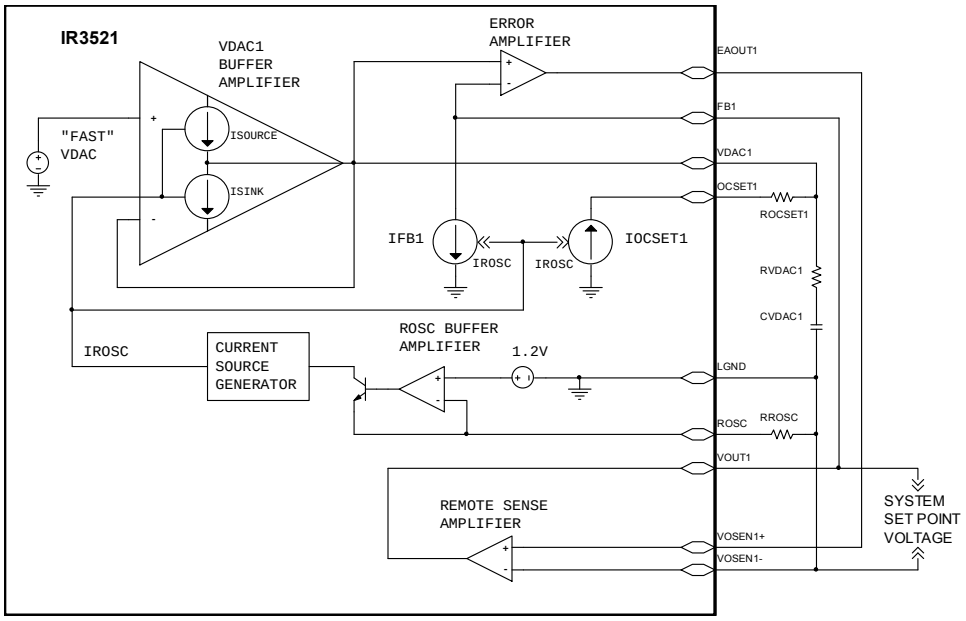


Figure 3A - Output 1 System Set Point Test Circuit

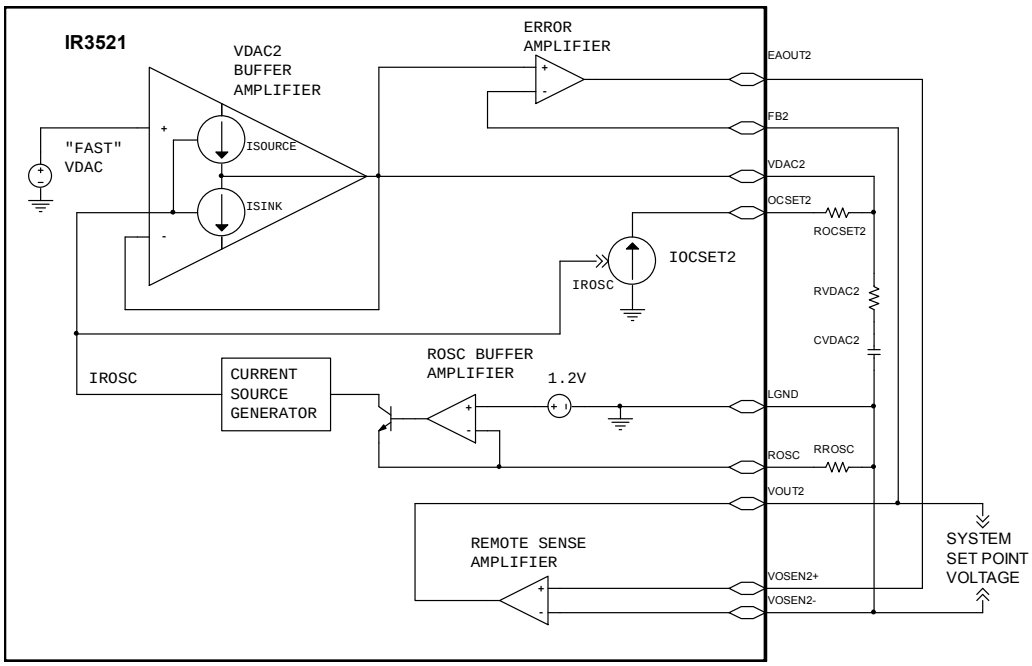


Figure 3B - Output 2 System Set Point Test Circuit

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *xPHASE3*™ architecture is shown in Figure 4. Feed-forward voltage mode control with trailing edge modulation is used to provide system control. A voltage type error amplifier with high-gain and wide-bandwidth, located in the Control IC, is used for the voltage control loop. The feed-forward control is performed by the phase ICs as a result of sensing the input voltage (FET's drain voltage). The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

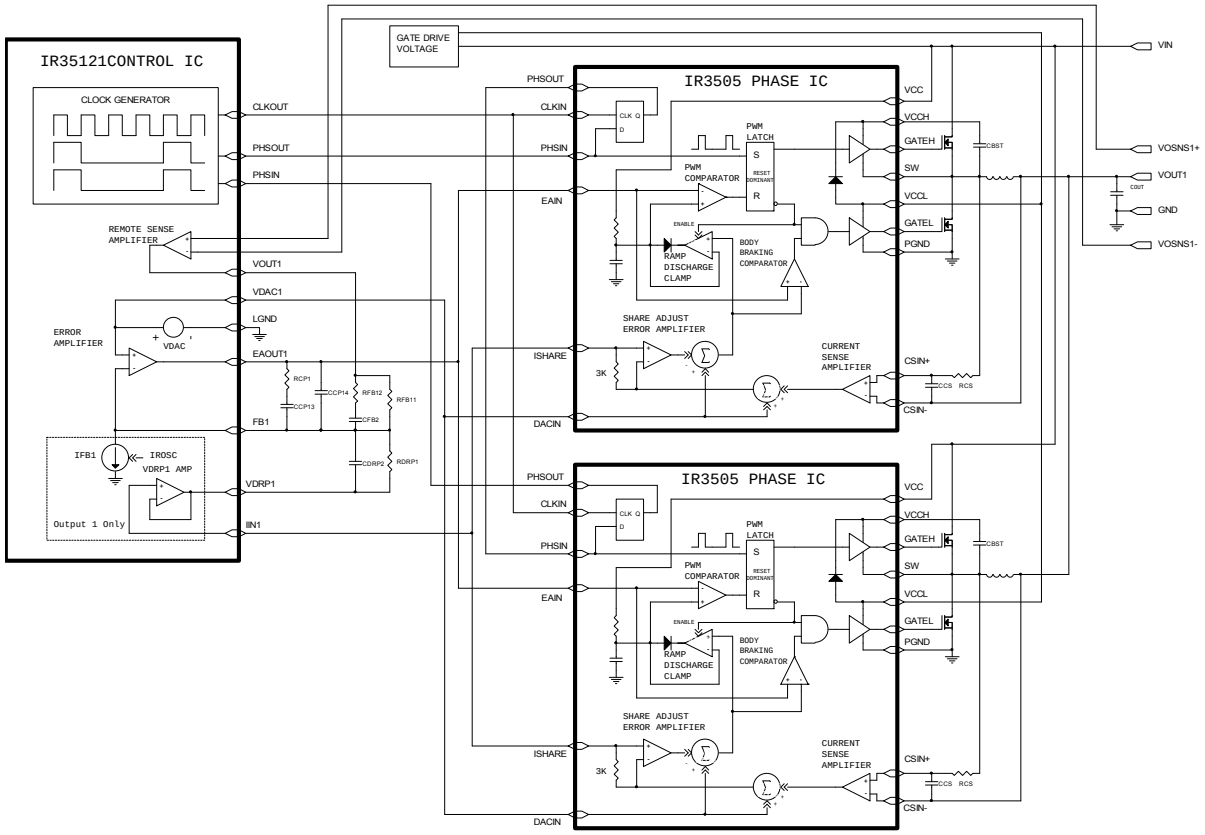


Figure 4 - PWM Block Diagram

Frequency and Phase Timing Control

The oscillator (system clock) is located in the Control IC and is programmable from 250 kHz to 9 MHZ by an external resistor. The control IC clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop. The control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. The last phase IC (PHSOUT) is connected back to PHSIN of the control IC to complete the loop. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 5 shows the phase timing for a four phase converter.

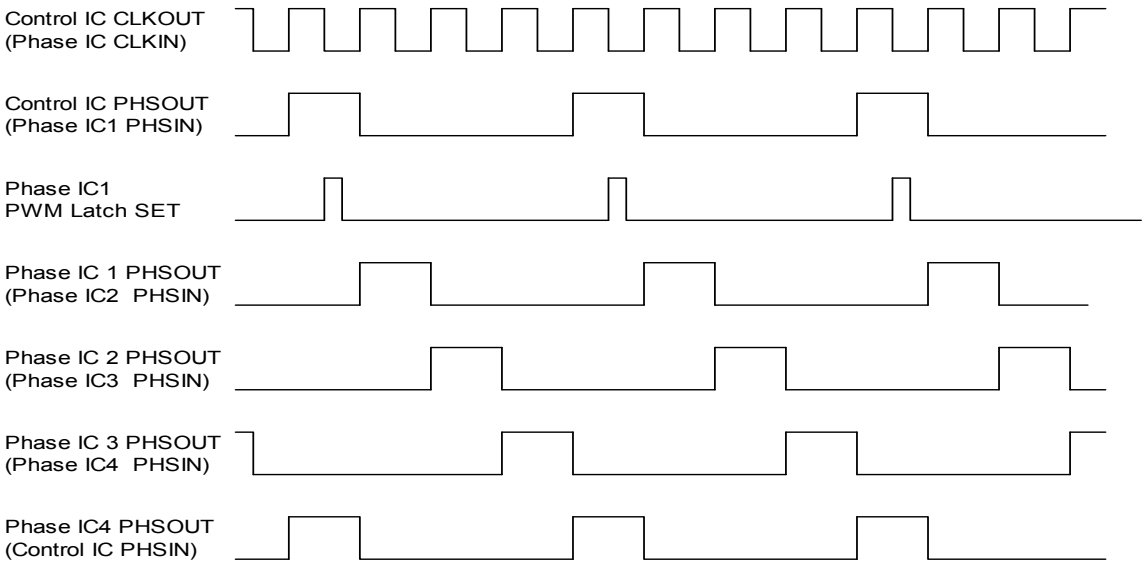


Figure 5 Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock, the PWM latch is set and the PWM ramp amplitude begins to increase prompting the low side driver is turned off. After the non-overlap time (GATEL < 1.0V), the high side driver is turned on. When the PWM ramp voltage exceeds the error amplifier's output voltage, the PWM latch is reset. This also turns off the high side driver, turns on the low side driver after the non-overlap time and the PWM ramp discharged current is clamped which quickly discharges the internal capacitor to the output voltage of share adjust amplifier, in phase IC, until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 6 depicts PWM operating waveforms under various conditions.

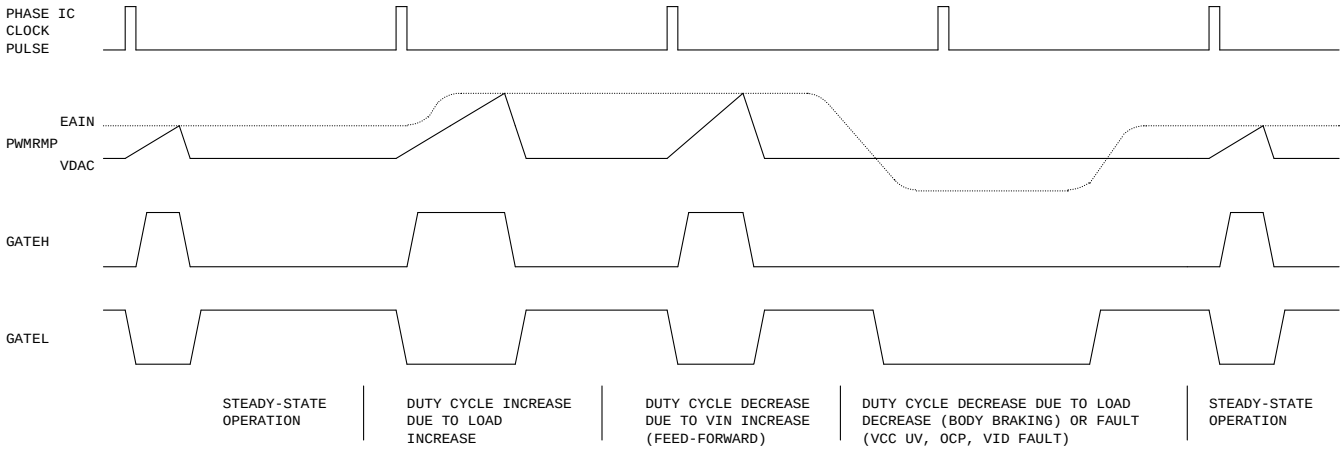


Figure 6 PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the VDAC voltage or a programmable voltage, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 7. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

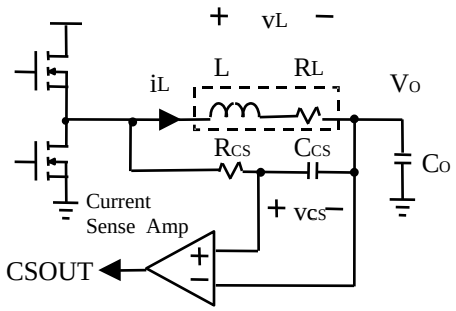


Figure 7 Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 7. Its gain is nominally 34 at 25ºC, and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

IR3521 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3521 is shown in Figure 8. The following discussions are applicable to either output plane unless otherwise specified.

Serial VID Control

The two Serial VID Interface (SVID) pins SVC and SVD are used to program the Boot VID voltage upon assertion of ENABLE while PWROK is de-asserted. See Table 1 for the 2-bit Boot VID codes. Both VDAC1 and VDAC2 voltages will be programmed to the Boot VID code until PWROK is asserted. The Boot VID code is stored by the IR3521 to be utilized again if PWROK is de-asserted.

Serial VID communication from the processor is enabled after the PWROK is asserted. Addresses and data are serially transmitted in 8-bit words. The IR3521 has three fixed addresses to control VDAC1, VDAC2, or both VDAC1 and VDAC2 (See Table 6 for addresses). The first data bit of the SVID data word represents the PSI_L bit and if pulled low will force all phase ICs, connected to the PSI_L pin, in to a power-saving mode. The remaining data bits SVID[6:0] select the desired VDACx regulation voltage as defined in Table 3. SVID[6:0] are the inputs to the Digital-to-Analog Converter (DAC) which then provides an analog reference voltage to the transconductance type buffer amplifier. This VDACx buffer provides a system reference on the VDACx pin. The VDACx voltage along with error amplifier and remote sense differential amplifier input offsets are post-package trimmed to provide a 0.5% system set-point accuracy, as measured in Figures 3A and 3B. VDACx slew rates are programmable by properly selecting external series RC compensation networks located between the VDACx and the LGND pins. The VDACx source and sink currents are derived off the external oscillator frequency setting resistor, R_{ROSC}. The programmable slew rate enables the IR3521 to smoothly transition the regulated output voltage throughout VID transitions. This results in power supply input and output capacitor inrush currents along with output voltage overshoot to be well controlled.

The two Serial VID Interface (SVID) pins SVC and SVD can also program the VFIX VID voltage upon assertion of ENABLE while PWROK is equal to VCCL. See Table 2 for the 2-bit VFIX VID codes. Both VDAC1 and VDAC2 voltages will be programmed to the VFIX code.

The SVC and SVD pins require external pull-up biasing and should not be floated.

Output 1 (VDD) Adaptive Voltage Positioning

The IR3521 provides Adaptive Voltage Positioning (AVP) on the output1 plane only. AVP helps reduces the peak to peak output voltage excursions during load transients and reduces load power dissipation at heavy load. The circuitry related to the voltage positioning is shown in Figure 9. Resistor R_{FB1} is connected between the error amplifiers inverting input pin FB1 and the remote sense differential amplifier output, VOUT1. An internal current sink on the FB1 pin along with R_{FB1} provides programmability of a fixed offset voltage above the VDAC1 voltage. The offset voltage generated across R_{FB1} forces the converter's output voltage higher to maintain a balance at the error amplifiers inputs. The FB1 sink current is derived by the external resistor R_{ROSC} that programs the oscillator frequency.

The VDRP1 pin voltage is a buffered reproduction of the IIN1 pin which is connected to the current share bus ISHARE. The voltage on ISHARE represents the system average inductor current information. At each phase IC, an RC network across the inductor provides current information which is gained up 32.5X and then added to the $VDAC_X$ voltage. This phase current information is provided on the ISHARE bus via a 3K resistor in the phase ICs.

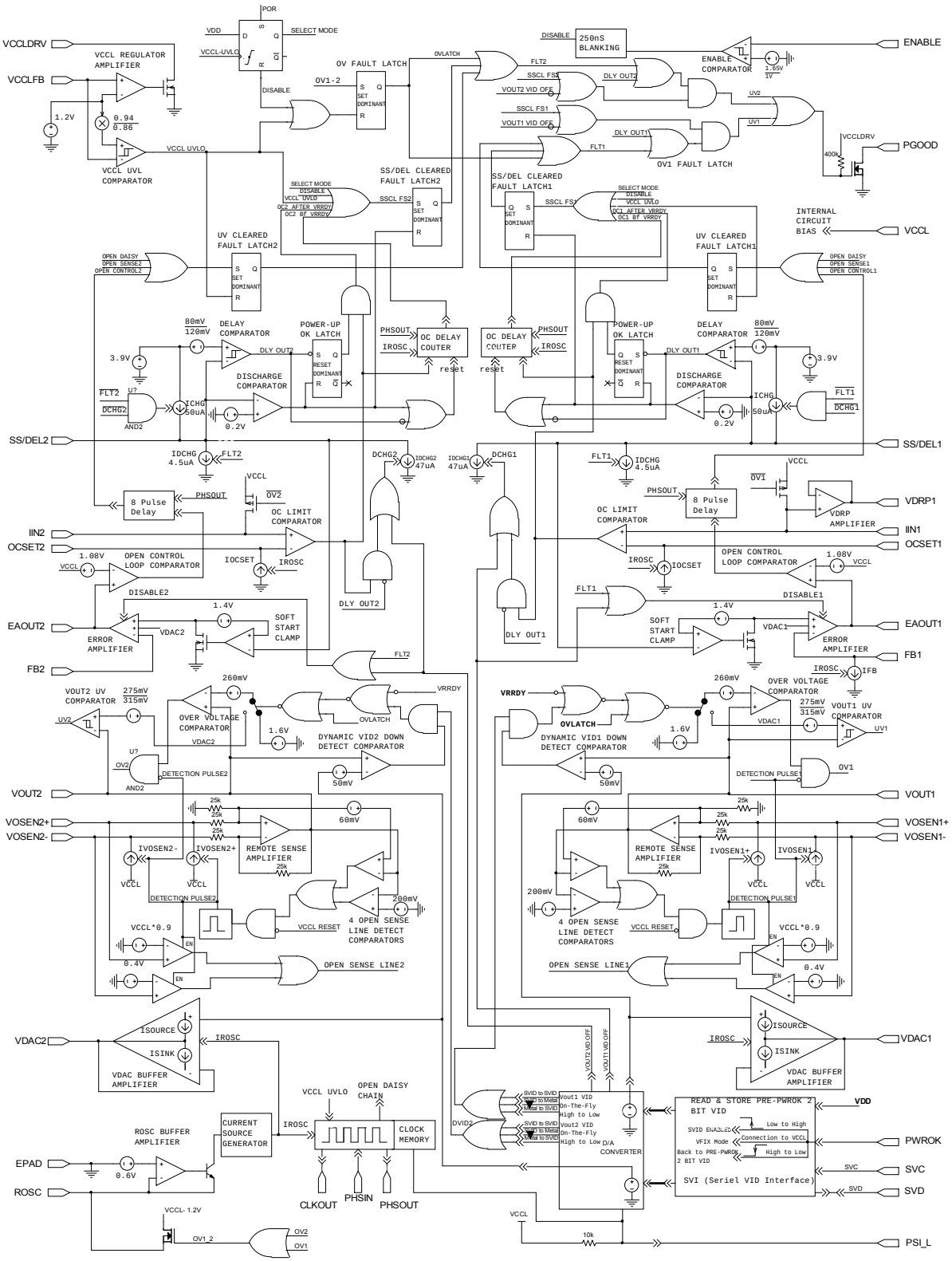


Figure 8 Block Diagram

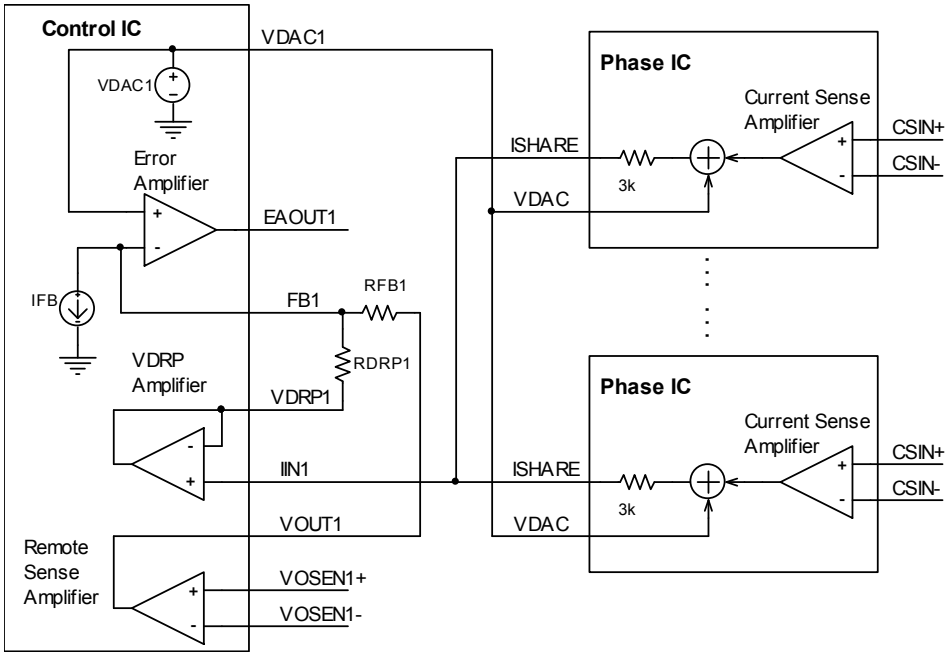


Figure 9 Adaptive voltage positioning

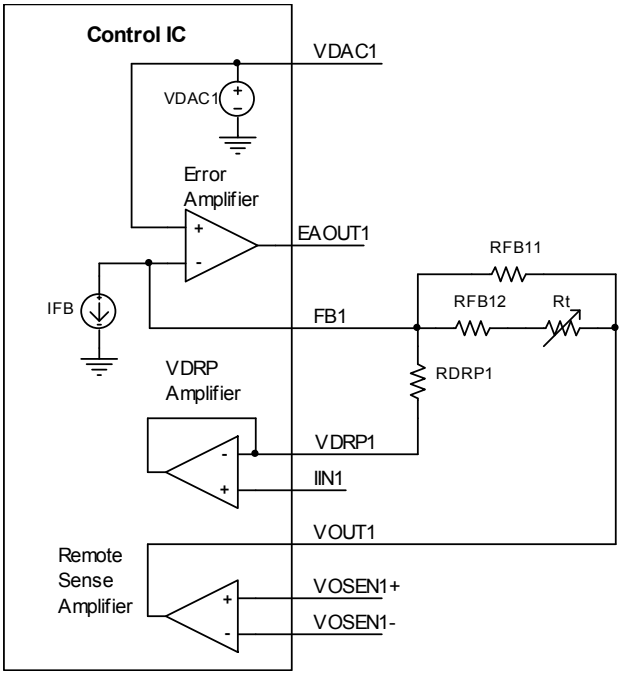


Figure 10 Temperature compensation of Output1 inductor DCR

Output 1 (VDD) Adaptive Voltage Positioning (continued)

The voltage difference between VDRP1 and FB1 represents the gained up average current information. Placing a resistor R_{DRP1} between VDRP1 and FB1 converts the gained up current information (in the form of a voltage) into a current forced onto the FB1 pin. This current, which can be calculated using (VDRP1-VDAC1) / R_{DRP1}, will vary the offset voltage produced across R_{FB1}. Since the error amplifier will force the loop to maintain FB1 to equal the VDAC1 reference voltage, the output regulation voltage will be varied. When the load current increases, the adaptive positioning voltage V(VDRP1) increases accordingly. (VDRP1-VDAC1) / R_{DRP1} increases the voltage drop across the feedback resistor R_{FB1}, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor R_{DRP1} so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to VDAC1 and are not affected by changes in the VDAC1 voltage.

Output1 Inductor DCR Temperature Compensation

A negative temperature coefficient (NTC) thermistor can be used for output1 inductor DCR temperature compensation. The thermistor should be placed close to the output1 inductors and connected in parallel with the feedback resistor, as shown in Figure 10. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

Remote Voltage Sensing

$VOSEN_X$+ and $VOSEN_X$- are used for remote sensing and connected directly to the load. The remote sense differential amplifiers are high speed, have low input offset and low input bias currents to ensure accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3521 has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL_X and LGND pins controls soft start timing, over-current protection delay and hiccup mode timing. Constant current sources and sinks control the charge and discharge rates of the SS/DEL_X.

Figure 11 depicts the SVID start-up sequence. If the ENABLE input is asserted and there are no faults, the SS/DEL_X pin will begin charging, the pre-PWROK 2 bit Boot VID codes are read and stored, and both VDAC pins transition to the pre-PWROK Boot VID code. The error amplifier output $EAOUT_X$ is clamped low until SS/DEL_X reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the $V(SS/DEL_X)$-1.4V offset until the converter output reaches the 2-bit Boot VID code. The SS/DEL_X voltage continues to increase until it rises above the threshold of Delay Comparator where the PGOOD output is allowed to go high. The SVID interface is activated upon PWROK assertion and the $VDAC_X$ along with the converter output voltage will change in response to any SVID commands.

VCCL under voltage, over current, or a low signal on the ENABLE input immediately sets the fault latch, which causes the EAOUT pin to drive low, thereby turning off the phase IC drivers. The PGOOD pin also drives low and SS/DEL_X discharges to 0.2V. If the fault has cleared, the fault latch will be reset by the SS/DEL_X discharge comparator allowing another soft start charge cycle to occur.

Other fault conditions, such as output over voltage, open VOSNS sense lines, or an open phase timing daisy chain set a different group of fault latches that can only be reset by cycling VCCL power. These faults discharge SS/DEL_X, pull down $EAOUT_X$ and drive PGOOD low.

SVID OFF codes turn off the converter by discharging SS/DEL_X and pulling down EAOUTx but do not drive PGOOD low. Upon receipt of a non-off SVID code the converter will re-soft start and transition to the voltage represented by the SVID code as shown in Figure 11.
The converter can be disabled by pulling the SS/DELx pins below 0.6V.

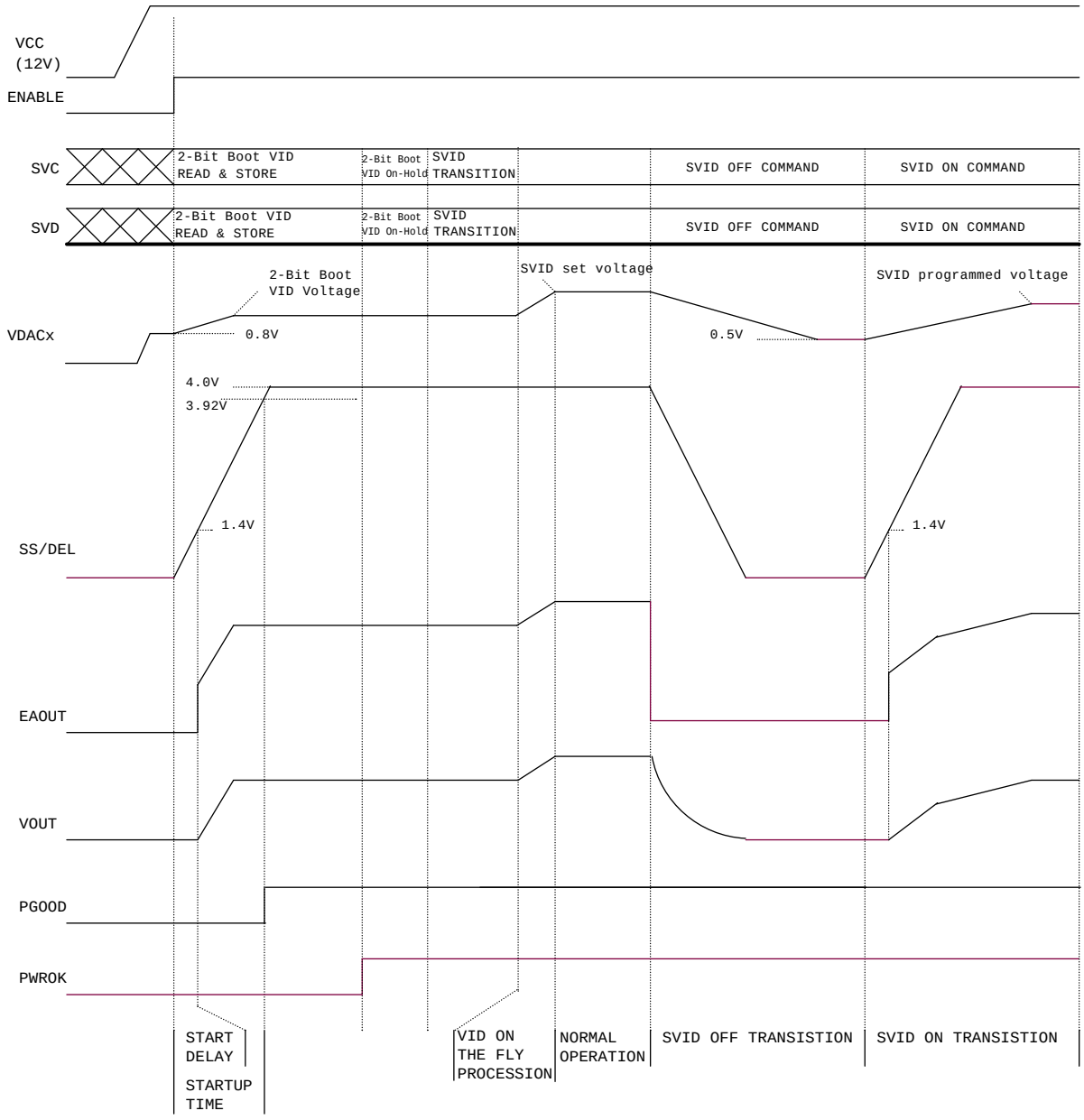


Figure 11 SVID Start-up Sequence Transitions

Serial VID Interface Protocol and VID-on-the-fly Transition

The IR3521 supports the AMD SVI bus protocol and the AMD Server and desktop SVI wire protocol which are based on High-Speed I^2C. SVID commands from an AMD processor are communicated through SVID bus pins SVC and SVD. The SVC pin of the IR3521 does not have an open drain output since AMD SVID protocol does not support slave clock stretching.

The IR3521 transitions from a 2-bit Boot VID mode to SVI mode upon assertion of PWROK. The SMBus *send byte* protocol is used by the IR3521 VID-on-the-fly transactions. The IR3521 will wait until it detects a start bit which is defined as an SVD falling edge while SVC is high. A 7bit address code plus one write bit (low) should then follow the start bit. This address code will be compared against an internal address table and the IR3521 will reply with an acknowledge ACK bit if the address is one of the three stored addresses otherwise the ACK bit will not be sent out. The SVD pin is pulled low by the IR3521 to generate the ACK bit. Table 4 has the list of addresses recognized by the IR3521.

The processor should then transmit the 8-bit data word immediately following the ACK bit. The first data bit (bit 7), of the SVID data word, represents the **Power State Indicator (PSI)** bit which is passed on to the phase ICs via the IR3521 PSI_L pin. PSI_L is pulled high by an internal 10K resistor to VCCL when data bit 7 of an SVID command is high. A low, on this bit (bit 7), will pull the PSL_pin low and trigger all connected, predetermine, phase ICs to turn off. If transitioning from one phase to multiple phases, the last phase IC, or returning phase IC, should be left on to ensure the fastest possible clock frequency calibration. A shorter calibration time will help minimize droop at the VDD output when leaving PSI_L mode. The remaining data bits SVID[6:0] select the desired VDACx regulation voltage as defined in Table 3. The IR3521 replies again with an ACK bit once the data is received. If the received data is not a VID-OFF command, the IR3521 immediately changes the DAC analog outputs to the new target. VDAC1 and VDAC2 then slew to the new VID voltages. See Figure 12 for a send byte example.

Table 1 – 2-bit Boot VID codes

SVC	SVD	Output Voltage(V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Table 2 – VFIX mode 2 bit VID Codes

SVC	SVD	Output Voltage(V)
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

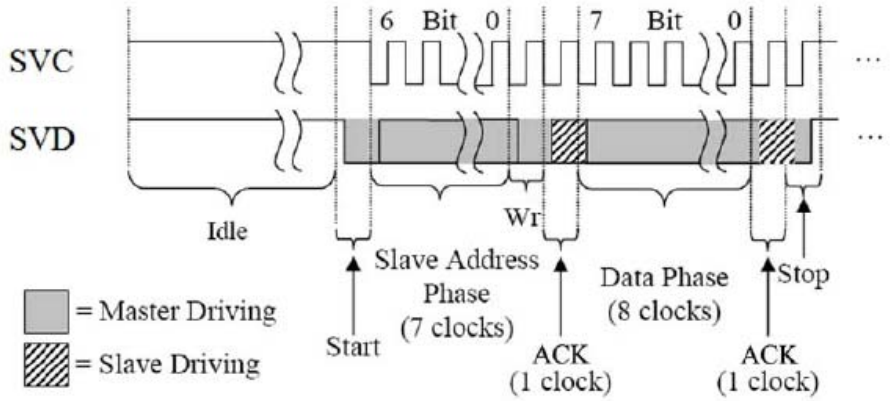


Figure 12 Send Byte Example

Table 3 - AMD 7 BIT SVID CODES

SVID [6:0]	Voltage (V)		SVID [6:0]	Voltage (V)		SVID [6:0]	Voltage (V)		SVID [6:0]	Voltage (V)
000_0000	1.5500		010_0000	1.1500		100_0000	0.7500		110_0000	0.5000
000_0001	1.5375		010_0001	1.1375		100_0001	0.7375		110_0001	0.5000
000_0010	1.5250		010_0010	1.1250		100_0010	0.7250		110_0010	0.5000
000_0011	1.5125		010_0011	1.1125		100_0011	0.7125		110_0011	0.5000
000_0100	1.5000		010_0100	1.1000		100_0100	0.7000		110_0100	0.5000
000_0101	1.4875		010_0101	1.0875		100_0101	0.6875		110_0101	0.5000
000_0110	1.4750		010_0110	1.0750		100_0110	0.6750		110_0110	0.5000
000_0111	1.4625		010_0111	1.0625		100_0111	0.6625		110_0110	0.5000
000_1000	1.4500		010_1000	1.0500		100_1000	0.6500		110_1000	0.5000
000_1001	1.4375		010_1001	1.0375		100_1001	0.6375		110_1001	0.5000
000_1010	1.4250		010_1010	1.0250		100_1010	0.6250		110_1010	0.5000
000_1011	1.4125		010_1011	1.0125		100_1011	0.6125		110_1011	0.5000
000_1100	1.4000		010_1100	1.0000		100_1100	0.6000		110_1100	0.5000
000_1101	1.3875		010_1101	0.9875		100_1101	0.5875		110_1101	0.5000
000_1110	1.3750		010_1110	0.9750		100_1110	0.5750		110_1110	0.5000
000_1111	1.3625		010_1111	0.9625		100_1111	0.5625		110_1111	0.5000
001_0000	1.3500		011_0000	0.9500		101_0000	0.5500		111_0000	0.5000
001_0001	1.3375		011_0001	0.9375		101_0001	0.5375		111_0001	0.5000
001_0010	1.3250		011_0010	0.9250		101_0010	0.5250		111_0010	0.5000
001_0011	1.3125		011_0011	0.9125		101_0011	0.5125		111_0011	0.5000
001_0100	1.3000		011_0100	0.9000		101_0100	0.5000		111_0100	0.5000
001_0101	1.2875		011_0101	0.8875		101_0101	0.5000		111_0101	0.5000
001_0110	1.2750		011_0110	0.8750		101_0110	0.5000		111_0110	0.5000
001_0111	1.2625		011_0111	0.8625		101_0111	0.5000		111_0111	0.5000
001_1000	1.2500		011_1000	0.8500		101_1000	0.5000		111_1000	0.5000
001_1001	1.2375		011_1001	0.8375		101_1001	0.5000		111_1001	0.5000
001_1010	1.2250		011_1010	0.8250		101_1010	0.5000		111_1010	0.5000
001_1011	1.2125		011_1011	0.8125		101_1011	0.5000		111_1011	0.5000
001_1100	1.2000		011_1100	0.8000		101_1100	0.5000		111_1100	OFF
001_1101	1.1875		011_1101	0.7875		101_1101	0.5000		111_1101	OFF
001_1110	1.1750		011_1110	0.7750		101_1110	0.5000		111_1110	OFF
001_1111	1.1625		011_1111	0.7625		101_1111	0.5000		111_1111	OFF

Table 4 - SVI Send Byte Address Table

SVI Address [6:0] + Wr	Description
110xx100b	Set VID only on Output 1
110xx010b	Set VID only on Output 2
110xx110b	Set VID on both Output 1 and Output 2

Note: 'x' in the above Table 4 means the bit could be either '1' or '0'.

Over-Current Hiccup Protection after Soft Start

The over current limit threshold is set by a resistor connected between $OCSET_X$ and $VDAC_X$ pins. Figure 13 shows the hiccup over-current protection with delay after PGOOD is asserted. The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IIN_X pin voltage, which is proportional to the average current plus $VDAC_X$ voltage, exceeds the OCSETx voltage after PGOOD is asserted, it will initiate the discharge of the capacitor at SS/DEL_X through the discharge current 47uA. If the over-current condition persists long enough for the SS/DEL_X capacitor to discharge below the 120mV offset of the delay comparator, the fault latch will be set which will then pull the error amplifier's output low to stop phase IC switching and will also de-asserting the PGOOD signal. The SS/DEL capacitor will then continue to be discharged by a 4.5 uA current until it reaches 200 mV where the fault latch will reset to allow another soft start cycle to occur. The output current is not controlled during the delay time. If an over-current condition is again encountered during the soft start cycle, the over-current action will repeat and the converter will be in hiccup mode.

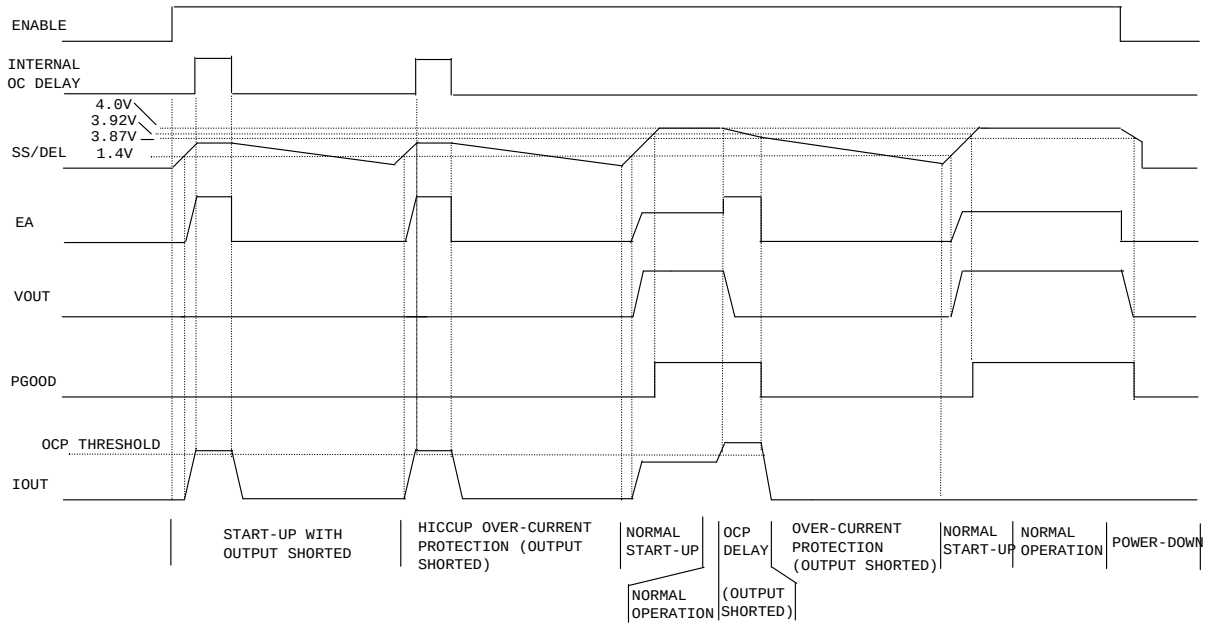


Figure 13 Hiccup over-current waveforms

Linear Regulator Output (VCCL)

The IR3521 has a built-in linear regulator controller, and only an external NPN transistor is needed to create a linear regulator. The output voltage of the linear regulator can be programmed between 4.75V and 7.5V [?] by the resistor divider at VCCLFB pin. The regulator output powers the gate drivers and other circuits of the phase ICs along with circuits in the control IC, and the voltage is usually programmed to optimize the converter efficiency. The linear regulator can be compensated by a 4.7uF capacitor at the VCCL pin. As with any linear regulator, due to stability reasons, there is an upper limit to the maximum value of capacitor that can be used at this pin and it's a function of the number of phases used in the multiphase architecture and their switching frequency. Figure 14 shows the stability plots for the linear regulator with 5 phases switching at 750 kHz.

For powering the IR3521 and up to two phase ICs an NPN transistor in a SOT-23 package could be used. For a larger number of phase ICs an NPN transistor in DPAK package is recommended. .

VCCL voltage must be regulated by a closed control loop based on the IR3521's VCCL regulator controller in order to keep both VCCLDRV and VCCLFB voltages in the operating points that would support correct UVLO operation. No external power rail can be connected to VCCL pin."

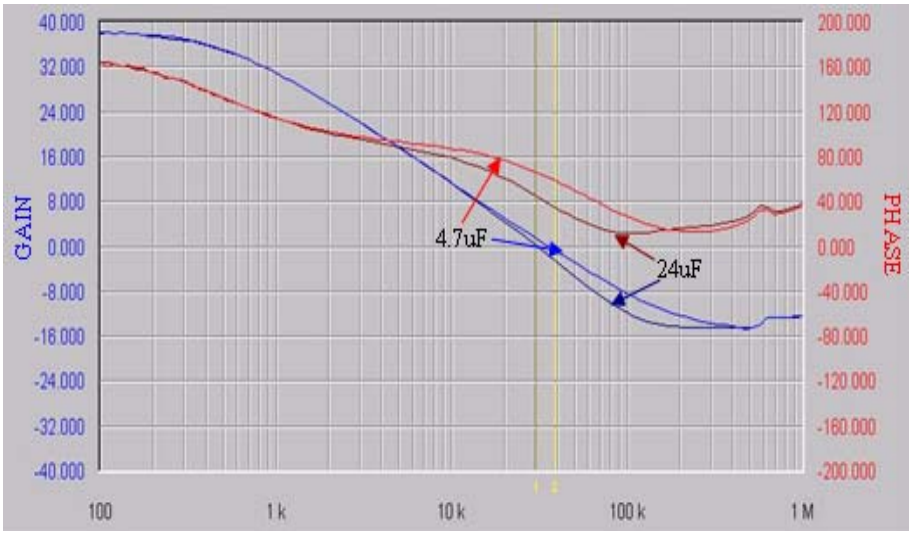


Figure 14 VCCL regulator stability with 5 phases and PHSOUT equals 750 kHz

VCCL Under Voltage Lockout (UVLO)

The IR3521 does not directly monitor VCC for under voltage lockout but instead monitors the system VCCL supply voltage since this voltage is used for the gate drive. As VCC begins to rise during power up, the VCCLDRV pin will be high impedance therefore allowing VCCL to roughly follow VCC-NPN_{VBE} until VCCL is above 94% of the voltage set by resistor divider at VCCLFB pin. At this point, the OV_X and UV CLEARED fault latches will be released. If VCCL voltage drops below 86% of the set value, the SS/DEL CLEARED fault latch will be set.

VID OFF Codes

SVID OFF codes of 111_1100, 111_1101, 111_1110, and 111_1111 turn off the converter by pulling down $EAOUT_X$ voltage and discharging SS/DEL_X through the 50uA discharge current, but do not drive PGOOD low. Upon receipt of a non-off SVID code the converter will turn on and transition to the voltage represented by the SVID as shown in Figure 10.

Power Good (PGOOD)

The PGOOD pin is an open-collector output and should have an external pull-up resistor. During soft start, PGOOD remains low until the output voltage is in regulation and SS/DEL_X is above 3.9V. The PGOOD pin becomes low if ENABLE is low, VCCL is below 86% of target, an over current condition occurs for at least 1024 PHSOUT clocks prior to PGOOD, an over current condition occurs after PGOOD and SS/DEL_X discharges to the delay threshold, an open phase timing daisy chain condition occurs, VOSNS lines are detected open, $VOUT_X$ is 315mV below $VDAC_X$, or if the error amp is sensed as operating open loop for 8 PHSOUT cycles. A high level at the PGOOD pin indicates that the converter is in operation with no fault and ensures the output voltage is within the regulation.

PGOOD monitors the output voltage. If any of the voltage planes fall out of regulation, PGOOD will become low, but the VR continues to regulate its output voltages. The PWROK input may or may not de-assert prior to the voltage planes falling out of specification. Output voltage out of spec is defined as 315mV to 275mV below nominal voltage. VID on-the-fly transition which is a voltage plane transitioning between one voltage associated with one VID code and a voltage associated with another VID code is not considered to be out of specification.

A PWROK de-assert while ENABLE is high results in all planes regulating to the previously stored 2-bit Boot VID. If the 2-bit Boot VID is higher than the VID prior to PWROK de-assertion, this transition will NOT be treated as VID on-the-fly and if either of the two outputs is out of spec high, PGOOD will be pulled down.

Open Voltage Loop Detection

The output voltage range of error amplifier is continuously monitored to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08V for 8 PHSOUT switching cycles, the fault latch is set. The fault latch can only be cleared by cycling the power to VCCL.

Load Current Indicator Output

The VDRP pin voltage represents the average current of the converter plus the DAC voltage. The load current information can be retrieved by using a differential amplifier to subtract VDAC1 voltage from the VDRP1 voltage.

Enable Input

Pulling the ENABLE pin below 0.8V sets the Fault Latch. Forcing ENABLE to a voltage above 1.94V results in the pre-PWROK 2 bit VID codes off the SVD and SVC pins to be read and stored. SS/DEL_X pins are also allowed to begin their power-up cycles.

Over Voltage Protection (OVP)

Output over-voltage might occur due to a high side MOSFET short or if the output voltage sense path is compromised. If the over-voltage protection comparators sense that either $VOUT_X$ pin voltage exceeds $VDAC_X$ by 260mV, the over voltage fault latch is set which pulls the error amplifier output low to turn off the converter power stage. The IR3521 communicates an OVP condition to the system by raising the ROSC/OVP pin voltage to within V(VCCL) – 1.2 V. An OVP condition is also communicated to the phase ICs by forcing the IIN pin (which is tied to the ISHARE bus and ISHARE pins of the phase ICs) to VCCL as shown in Figure 15. In each phase IC, the OVP circuit overrides the normal PWM operation to ensure the low side MOSFET turn-on within approximately 150ns. The low side MOSFET will remain on until the ISHARE pins fall below V(VCCL) - 800mV. An over voltage fault condition is latched in the IR3521 and can only be cleared by cycling the power to VCCL.

During dynamic VID down at light to no load, false OVP triggering is prevented by increasing the OVP threshold to a fixed 1.85V whenever a dynamic VID is detected and the difference between output voltage and the fast internal VDAC is more than 50mV, as shown in Figure 16. The over-voltage threshold is changed back to VDAC+125mV if the difference between output voltage and the fast internal VDAC is less than 50mV.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered thus providing effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

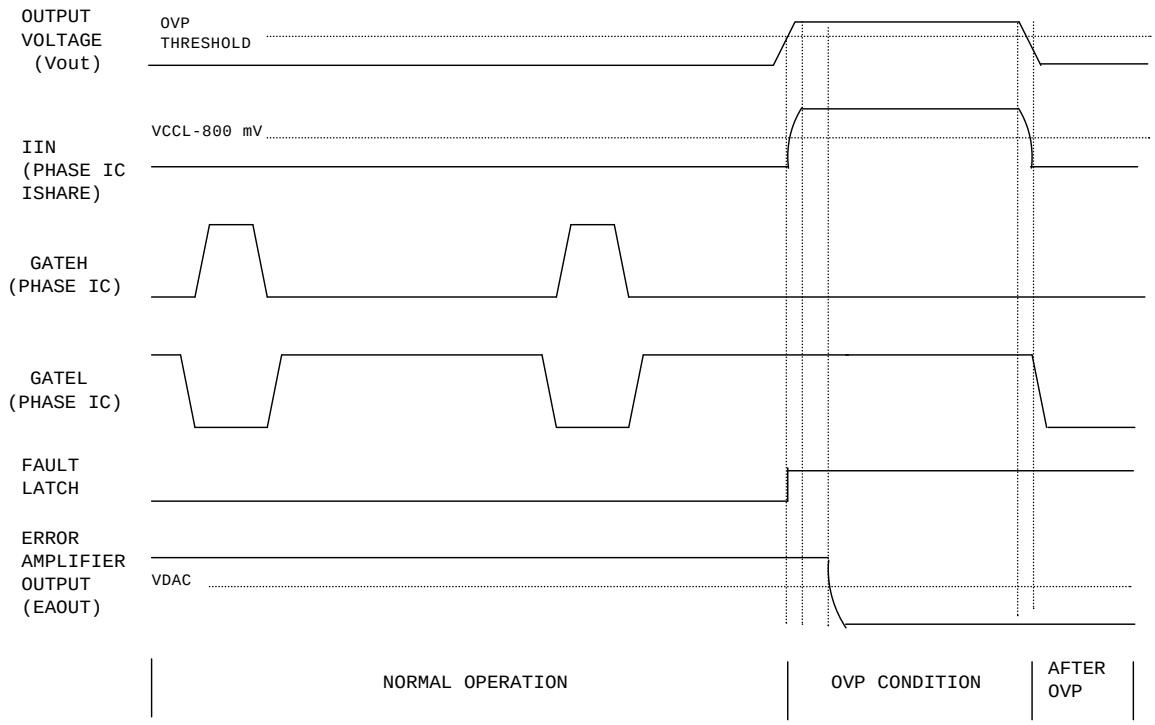


Figure 15 - Over-voltage protection during normal operation

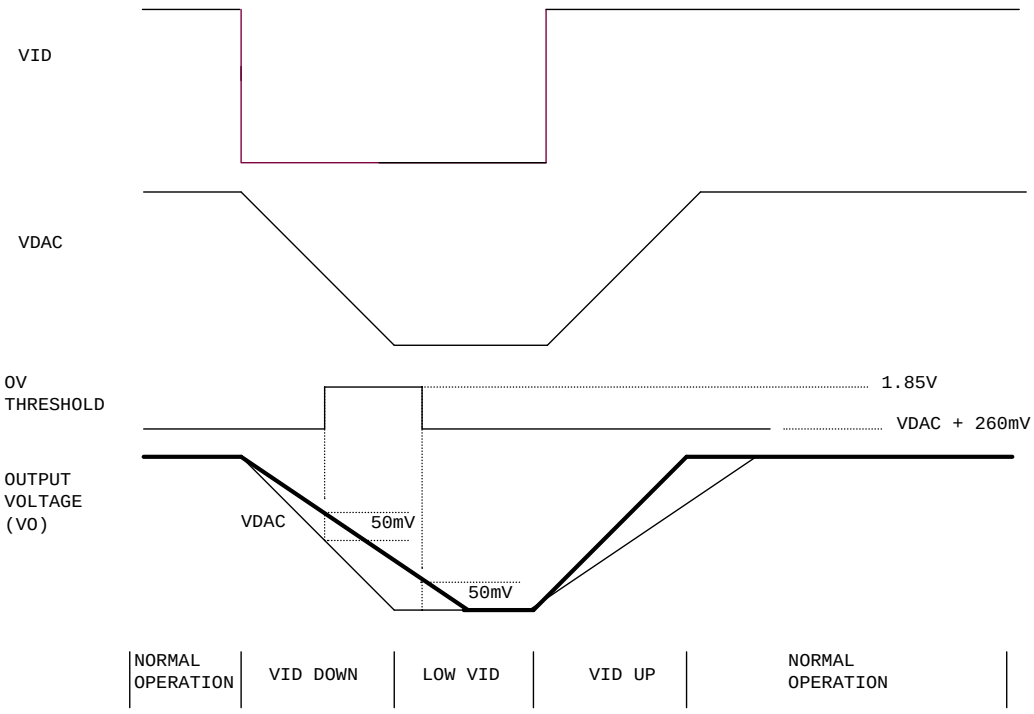


Figure 16 Over-voltage protection during dynamic VID

Open Remote Sense Line Protection

If either remote sense line $VOSEN_X$+ or $VOSEN_X$- is open, the output of Remote Sense Amplifier ($VOUT_X$) drops. The IR3521 continuously monitors the $VOUT_X$ pin and if $VOUT_X$ is lower than 200 mV, two separate pulse currents are applied to the $VOSEN_X$+ and $VOSEN_X$- pins to check if the sense lines are open. If $VOSEN_X$+ is open, a voltage higher than 90% of V(VCCL) will be present at $VOSEN_X$+ pin and the output of Open Line Detect Comparator will be high. If $VOSEN_X$- is open, a voltage higher than 400mV will be present at $VOSEN_X$- pin and the Open Line Detect Comparator output will be high. With either sense line open, the Open Sense Line Fault Latch will be set to force the error amplifier output low and immediately shut down the converter. SS/DEL_X will be discharged and the Open Sense Fault Latch can only be reset by cycling the power to VCCL.

Open Daisy Chain Protection

The IR3521 checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 32 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the Open Daisy Chain fault is registered, and SS/DEL_X is not allowed to charge. The fault latch can only be reset by cycling the power to VCCL.

After powering up, the IR3521 monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an Open Daisy Chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3521 checks the timing of the input pulse at PHSIN pin to determine the phase number.

APPLICATIONS INFORMATION

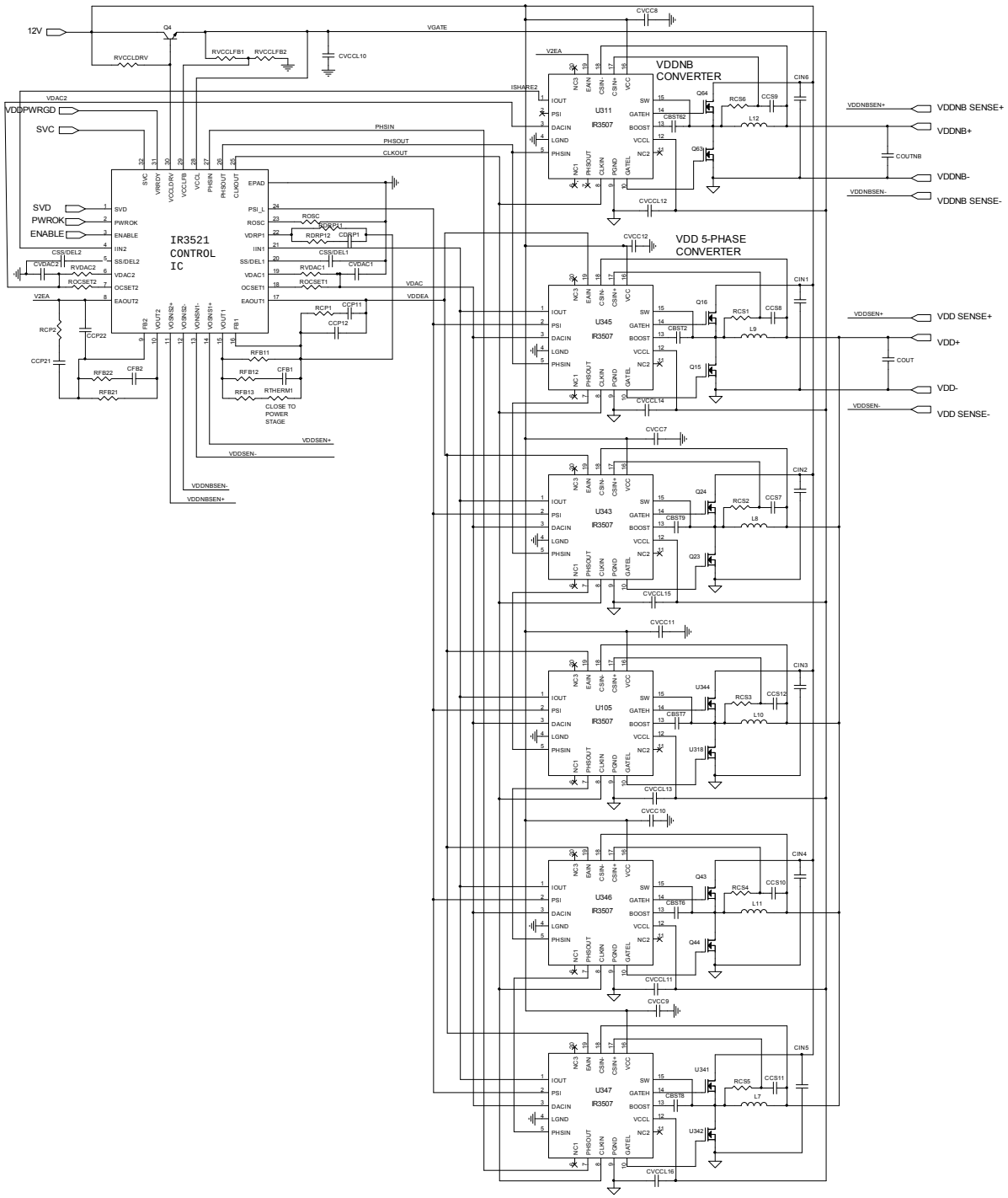


Figure 17 IR3521 \ IR3507 Five Phases – One Phase Dual Outputs AMD SVID Converter

DESIGN PROCEDURES - IR3521 AND IR3508 CHIPSET

IR3521 EXTERNAL COMPONENTS

All the output components are selected using one output but suitable for both unless otherwise specified.

Oscillator Resistor *RROSC*

The IR3521 generates square wave pulses to synchronize the phase ICs. The switching frequency of the each phase converter equals the PHSOUT frequency, which is set by the external resistor RROSC (use Figure 2 to determine the RROSC value). The CLKOUT frequency equals the switching frequency multiplied by the phase number.

Soft Start Capacitor *CSS/DEL*

The Soft Start capacitor CSS/DEL programs four different time parameters: soft start delay time, soft start time, PGOOD delay time and over-current fault latch delay time after PGOOD.

SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 11. Once the ENABLE pin rises above 1.65V, there is a soft-start delay time TD1 during which SS/DEL pin is charged from zero to 1.4V. Once SS/DEL reaches 1.4V the error amplifier output is released to allow the soft start. The soft start time, TD2, represents the time during which converter voltage rises from zero to pre-PWROK VID voltage and the SS/DEL pin voltage rises from 1.4V to pre-PWROK VID voltage plus 1.4V. PGOOD delay time TD3 is the time period from VR reaching the pre-PWROK VID voltage to the PGOOD signal assertion.

Calculate CSS/DEL based on the required soft start time TD2.

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{V_{pre-PWROK}} = \frac{TD2 * 50 * 10^{-6}}{V_{pre-PWROK}} \quad (1)$$

The soft start delay time TD1 and PGOOD delay time TD3 are determined by equation (2) and (3) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{50 * 10^{-6}} \quad (2)$$

$$TD3 = \frac{C_{SS/DEL} * (3.92 - V_{pre-PWROK} - 1.4)}{I_{CHG}} = \frac{C_{SS/DEL} * (3.92 - V_{pre-PWROK} - 1.4)}{50 * 10^{-6}} \quad (3)$$

Once CSS/DEL is chosen, use equation (4) to calculate the maximum over-current fault latch delay time tOCDEL.

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{C_{SS/DEL} * 0.12}{47 * 10^{-6}} \quad (4)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope SRDOWN can be programmed by the external capacitor CVDAC as defined in (5), where ISINK is the VDAC buffer sink current. The resistor RVDAC is used to compensate VDAC circuit and is determined by (6). The up and down slow are equal due to symmetrical sink and source capabilities of the VDAC buffer.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (5)$$

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}{}^2} \quad (6)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/°C, and therefore the maximum inductor DCR can be calculated from (7), where R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature, T_{L_MAX}, and room temperature, T_{L_ROOM}, respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{L\_ROOM})] \quad (7)$$

The total input offset voltage (V_{CS_TOFST}), of the phase IC's current sense amplifier, is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor R_{CS}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS} \quad (8)$$

The over-current limit is set by the external resistor R_{OCSET} as defined in (9). I_{LIMIT} is the required over-current limit. I_{OCSET} is the bias current of OCSET pin and can be calculated with the equation located in the ELECTRICAL CHARACTERISTICS Table. G_{CS} is the gain of the current sense amplifier. K_P is the ratio of inductor peak current over the average current in each phase and can be calculated using equation (10).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET} \quad (9)$$

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_O / n} \quad (10)$$

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Since VCCL voltage is proportional to the MOSFET gate driver loss and inversely proportional to the MOSFET conduction loss, the optimum voltage should be chosen to maximize the converter efficiency. VCCL linear regulator consists of an external NPN transistor, a ceramic capacitor and a programmable resistor divider. Pre-select $R_{VCCLFB1}$, and calculate $R_{VCCLFB2}$ from (11).

$$R_{VCCLFB2} = \frac{R_{VCCLFB1} * 1.23}{VCCL - 1.23} \quad (11)$$

No Load Offset Setting Resistor *RFB11, RFB13, RTHERM1* and Adaptive Voltage Positioning Resistor *RDRP11* for Output1

Define R_{FB_R} as the effective offset resistor at room temperature equals to $R_{FB11}//(R_{FB13}+R_{THERM1})$. Given the offset voltage V_{O_NLOFST} (offset above the DAC voltage) and calculating the sink current from the FB1 pin I_{FB1}, using the equation in the ELECTRICAL CHARACTERISTICS Table, the effective offset resistor value, R_{FB1}, can be determined from equation (12).

$$R_{FB\_R} = \frac{V_{O\_NLOFST}}{I_{FB1}} \quad (12)$$

Adaptive voltage positioning lowers the converter voltage by $R_O * I_O$, where R_O is the required output impedance of the converter. Pre-select feedback resistor R_{FB}, and calculate the droop resistor RDRP,

$$R_{DRP11} = \frac{R_{FB\_R} * R_{L\_ROOM} * G_{CS}}{n * R_O} \quad (13)$$

Calculate the desired effective feedback resistor at the maximum temperature R_{FB_M} using (14)

$$R_{FB\_M} = \frac{R_{DRP11} * R_O * n}{G_{CS} * R_{L\_MAX}} \quad (14)$$

A negative temperature constant (NTC) thermistor R_{THERM1} is required to sense the temperature of the power stage for the inductor DCR thermal compensation. Pre-select the value of R_{THERM}. R_{THERM} must be bigger than R_{FB_R} at room temperature but also bigger than R_{FB_M} at the maximum allowed temperature. R_{TMAX1} is defined as the NTC thermistor resistance at maximum allowed temperature, T_{MAX}. R_{TMAX1} is calculated from (15).

$$R_{TMAX1} = R_{THERM1} * EXP[B_{THERM1} * (\frac{1}{T_{L\_MAX}} - \frac{1}{T_{\_ROOM}})] \quad (15)$$

Select the series resistor R_{FB13} by using equation (16). R_{FB13} is incorporated to linearize the NTC thermistor which has non-linear characteristics in the operational temperature range.

$$R_{FB13} = \frac{\sqrt{(R_{THERM\,1} + R_{TMAX\,1})^2 - 4 * (R_{THERM\,1} * R_{TMAX\,1} - (R_{THERM\,1} - R_{TMAX\,1}) * R_{FB\_R} * R_{FB\_M} / (R_{FB\_R} - R_{FB\_M}))} - (R_{THERM\,1} + R_{TMAX\,1})}{2} \quad (16)$$

Use equation (17) to determine RFB11.

$$\frac{1}{R_{FB11}} = \frac{1}{R_{FB\_R}} - \frac{1}{R_{FB13} + R_{THERM1}} \quad (17)$$

IDD Dynamic OC Limit Capacitor

The latest AMD processors require two over current limits: one for normal thermal design current (TDC) operation and the other for system IDD_Spike. TDC over-current is set by following instructions outlined in the Over Current Setting Resistor Rocset section. IDD_Spike occur when the load current exceeds the TDC for a very short duration (10 ms). Figure 18 shows the boundaries of an event. The current over a moving average of 10 ms does not exceed the TDC limit. Higher IDD-Spike will last for a shorter duration.

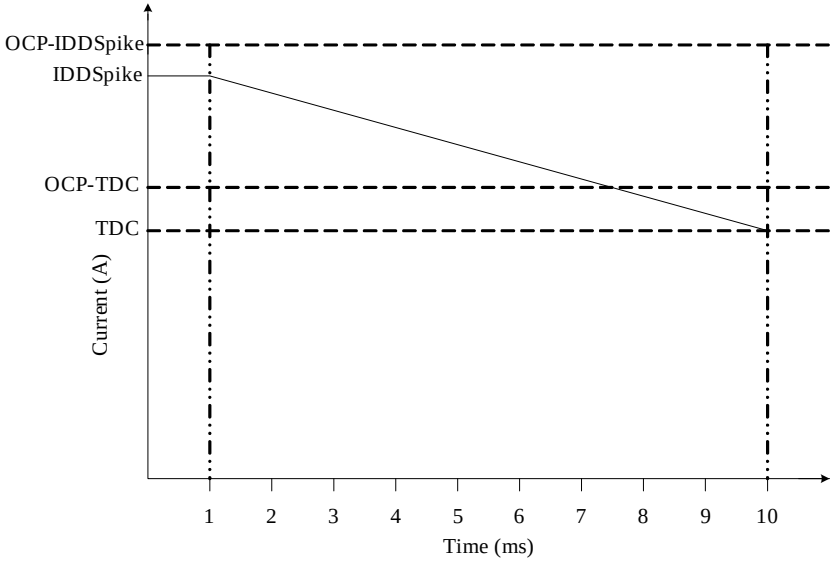


Figure 18 Showing IDD_Spike Boundaries

The IDD_Spike over current threshold can be implemented by incorporation a properly sized capacitor between the OCSET (18) and the IN1 (21) pins (see Figure 19).

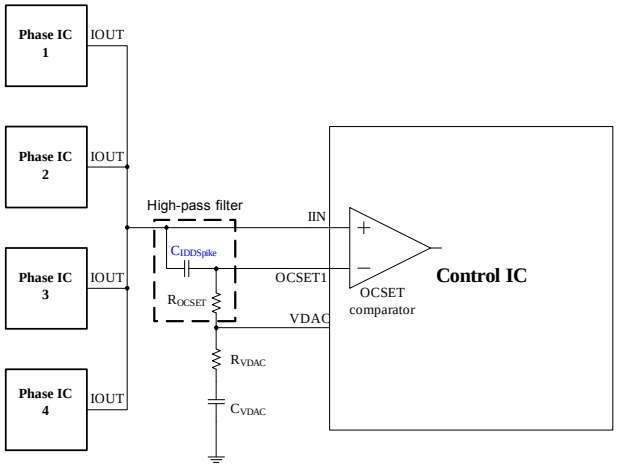


Figure 19 $C_{IDDSpike}$ and R_{OCSET} form a High Pass Filter

When a step load is applied, the capacitor acts as a short-circuit, at that instant, and pushes the OCSET signal up by ΔV (i.e. change in IIN) instantaneously. After an increase in its level, the OCP signal starts decaying exponentially towards its original value. The rate of decay is determined by the RC time constant. The VR will enter hiccup mode when the OCSET signal falls below the IIN value. The following equation (18) is use to calculate the ideal capacitor value:

$$C_{IDD\_Spike} = \frac{t_{spike\_oc}}{-R_{OC} \times In\left|\frac{I_{spike} - I_{OC}}{I_{spike} - I_{TDC}}\right|}, \quad (18)$$

where,

t_{spike_oc} = IDD_Spike OC time (choose >1.5ms),
R_{oc} = OC resistor (TDC),
I_{spike} = IDD_Spike Max,
I_{OC} = TDC OC Threshold,
I_{TDC} = Thermal Design Current.

The following graph shows a dynamic OC response with t_{spike} set for 1.5ms.

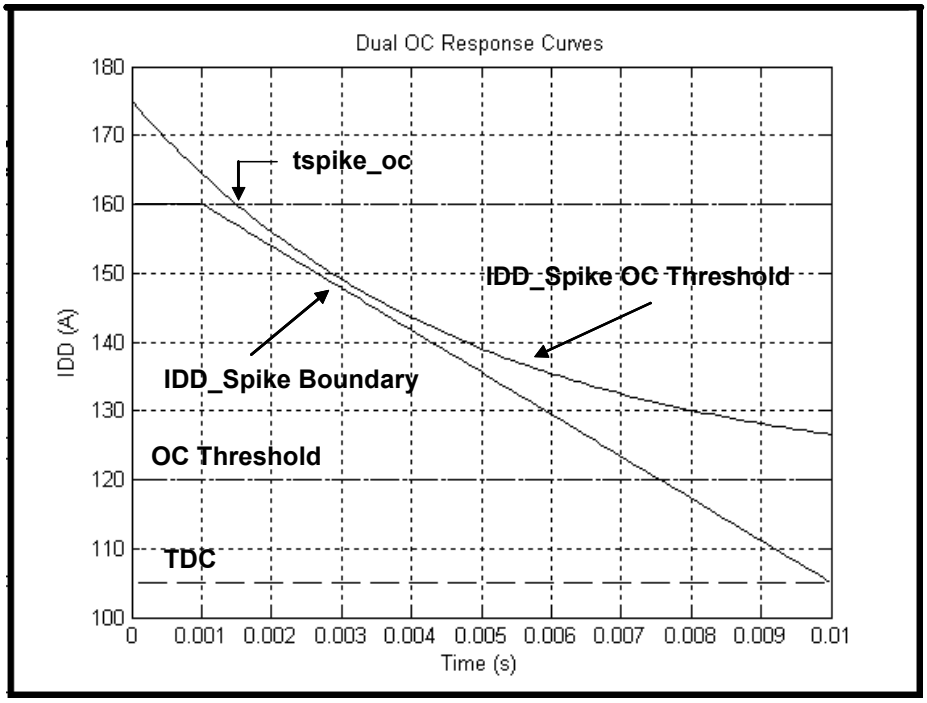


Figure 20 Showing Dynamic OC Response

IR3508 EXTERNAL COMPONENTS

Inductor Current Sensing Capacitor *CCS* and Resistor *RCS*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS and capacitor CCS in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS and calculate RCS as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \tag{19}$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a capacitor in the range of 0.1uF to 1uF is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

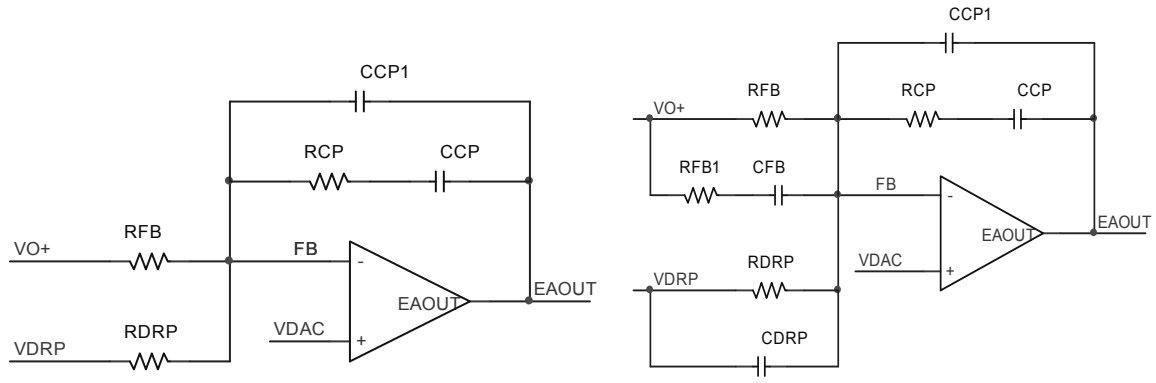
VOLTAGE LOOP COMPENSATION

The adaptive voltage positioning (AVP) is usually adopted in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Adaptive voltage positioning lowers the converter voltage by $R_O * I_O$, where R_O is the required output impedance of the converter.

The selection of compensation types depends on the output capacitors used in the converter. For the applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 21(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 21(b) is preferred.

For applications where AVP is not required, the compensation is the same as for the regular voltage mode control. For converter using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 18(b) with R_{DRP} and C_{DRP} removed.



(a) Type II compensation (b) Type III compensation

Figure 21 Voltage loop compensation network

Type II Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine R_{CP} and C_{CP} from (20) and (21), where L_E and C_E are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (20)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (21)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Assume the RC, resistor and capacitor across the output inductors, and L/DCR time constant matches, the crossover frequency and phase margin of the voltage loop can be estimated by (22) and (23), where R_{LE} is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (22)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (23)$$

Choose the desired crossover frequency fc around fc1, estimated by (22), or choose fc between 1/10 and 1/5 of the switching frequency per phase. The components should be selected to ensure the close loop gain slope is -20dB /Dec around the crossover frequency. Choose resistor R_{FB1} according to (24), and determine C_{FB} and C_{DRP} from (25) and (26).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (24)$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \quad (25)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (26)$$

R_{CP} and C_{CP} have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine R_{CP} and C_{CP} from (27) and (28).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I} \quad (27)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (28)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for Non-AVP Applications

Resistor R_{DRP} and capacitor C_{DRP} are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from (29), and determine the component values based on (30) to (34),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \quad (29)$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * 5}{V_I * K} \quad (30)$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \quad (31)$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \quad (32)$$

$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \quad (33)$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \quad (34)$$

CURRENT SHARE LOOP COMPENSATION

The internal compensation of current share loop ensures that crossover frequency of the current share loop is at least one decade lower than that of the voltage loop so that the interaction between the two loops is eliminated.

DESIGN EXAMPLE – AMD FIVE + ONE PHASE DUAL OUTPUT CONVERTER (FIGURE 17)

SPECIFICATIONS

Input Voltage: V_I=12 V
DAC Voltage: V_{DAC}=1.2 V
No Load Output Voltage Offset for output1: V_{O_NLOFST}=15 mV
Output1 Current: I_{O1}=95 ADC
Output2 Current: I_{O1}=20 ADC
Output1 Over Current Limit: I_{limit1}=115 ADC
Output2 Over Current Limit: I_{limit2}= 25 ADC
Output Impedance: R_{O1}=0.3 mΩ
Dynamic VID Slew Rate: SR=3.25mV/uS
Over Temperature Threshold: T_{MAX}=110 ºC

POWER STAGE

Phase Number: n1=5, n2=1
Switching Frequency: f_{SW}=520 kHz
Output Inductors: L1=120 nH, L2=220 nH, R_{L1}= 0.52mΩ, R_{L2}= 0.47mΩ
Output Capacitors: POSCAPs, C=470uF, R_C= 8mΩ, Number Cn1=9, Cn2=5

IR3500 EXTERNAL COMPONENTS

Oscillator Resistor *R_{ROSC}*

Once the switching frequency is chosen, R_{ROSC} can be determined from Figure 2. For switching frequency of 520kHz per phase, choose R_{OSC}=23.2kΩ.

Soft Start Capacitor *$C_{SS/DEL}$*

Determine the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{Vboot} = \frac{2*10^{-3} * 50*10^{-6}}{1.0} = 0.1uF$$

The soft start delay time is

$$TD1 = \frac{C_{SS/DEL} * 1.1}{I_{CHG}} = \frac{0.1*10^{-6} * 1.1}{50*10^{-6}} = 2.2mS$$

The PGOOD delay time is

$$TD3 = \frac{C_{SS/DEL} * (3.92 - V_{boot} - 1.1)}{I_{CHG}} = \frac{0.1*10^{-6} * (3.92 - 1 - 1.1)}{50*10^{-6}} = 3.6mS$$

The maximum over current fault latch delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.12}{I_{DISCHG}} = \frac{0.1*10^{-6} * 0.12}{47*10^{-6}} = 0.638mS$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{45.2*10^{-6}}{3.2*10^{3}} = 14.1nF$$, Choose CVDAC=22nF

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^{2}} = 7.1Ohm$$

Over Current Setting Resistor *ROCSET*

The output1 over current limit is 115A and the output2 over current limit is 25A. From the electrical characteristics table can get the bias current of OCSET pin (I_{OCSET}) is 26uA with R_{OSC}=23.2 kΩ. The total current sense amplifier input offset voltage is around 0mV, Calculate constant K_P, the ratio of inductor peak current over average current in each phase,

$$K_P1 = \frac{(V_I - V_O)*V_O/(L*V_I*f_{SW}*2)}{I_{LIMIT}/n} = \frac{(12-1.2)*1.2/(120*10^{-9}*12*520*10^{3}*2)}{115/5} = 0.38$$

$$K_P2 = \frac{(12-1.2)*1.2/(220*10^{-9}*12*520*10^{3}*2)}{25} = 0.19$$

$$R_{OCSET}1 = [\frac{I_{LIMIT}}{n}*R_L*(1+K_P)+V_{CS\_TOFST}]*G_{CS}/I_{OCSET}$$

$$= (\frac{115}{5}*0.52*10^{-3}*1.38)*34/(26*10^{-6}) = 21.6k\Omega$$

$$R_{OCSET}2 = [\frac{I_{LIMIT}}{n}*R_L*(1+K_P)+V_{CS\_TOFST}]*G_{CS}/I_{OCSET}$$

$$= (\frac{25}{1}*0.47*10^{-3}*1.19)*34/(26*10^{-6}) = 18.4k\Omega$$

VCCL Programming Resistor *RVCCLFB1* and *RVCCLFB2*

Choose VCCL=7V to maximize the converter efficiency. Pre-select $R_{VCCLFB1}$=20kΩ, and calculate $R_{VCCLFB2}$.

$$R_{VCCLFB2} = \frac{R_{VCCLFB1}*1.23}{VCCL-1.23} = \frac{20*10^{3}*1.23}{7-1.23} = 4.26k\Omega$$

No Load Offset Setting Resistor *RFB11, RFB13, RTHERM1* and Adaptive Voltage Positioning Resistor *RDRP11* for Output1

Define R_{FB_R} is the effective offset resistor at room temperature equals to R_{FB11}//(R_{FB13}+R_{THERM1}). Given the offset voltage V_{O_NLOFST} above the DAC voltage, calculate the sink current from the FB1 pin I_{FB1}= 26uA using the equation in the ELECTRICAL CHARACTERISTICS Table, then the effective offset resistor value $R_{FB\_R}1$ can be determined by:

$$R_{FB\_R}1 = \frac{V_{O\_NLOFST}}{I_{FB1}} = \frac{15*10^{-3}}{26*10^{-6}} = 577Ohm$$

Adaptive voltage positioning lowers the converter voltage by R_O*I_O, where R_O is the required output impedance of the converter. Pre-select feedback resistor R_{FB}, and calculate the droop resistor RDRP,

$$R_{DRP}1 = \frac{R_{FB\_R} * R_{L\_ROOM} * G_{CS}}{n * R_O} = \frac{577 * 0.52 * 10^{-3} * 34}{5 * 0.3 * 10^{-3}} = 6.7KOhm$$

In the case of thermal compensation is required, use equation (14) to (17) to select the RFB network resistors.

IR3508 EXTERNAL COMPONENTS

Inductor Current Sensing Capacitor *Ccs* and Resistor *Rcs*

Choose CCS1=Ccs2=0.1uF, and calculate RCS,

$$R_{CS}1 = \frac{L/R_L}{C_{CS}} = \frac{120 * 10^{-9} / (0.52 * 10^{-3})}{0.1 * 10^{-6}} = 2.3k\Omega$$

$$R_{CS}2 = \frac{L/R_L}{C_{CS}} = \frac{220 * 10^{-9} / (0.47 * 10^{-3})}{0.1 * 10^{-6}} = 4.7k\Omega$$

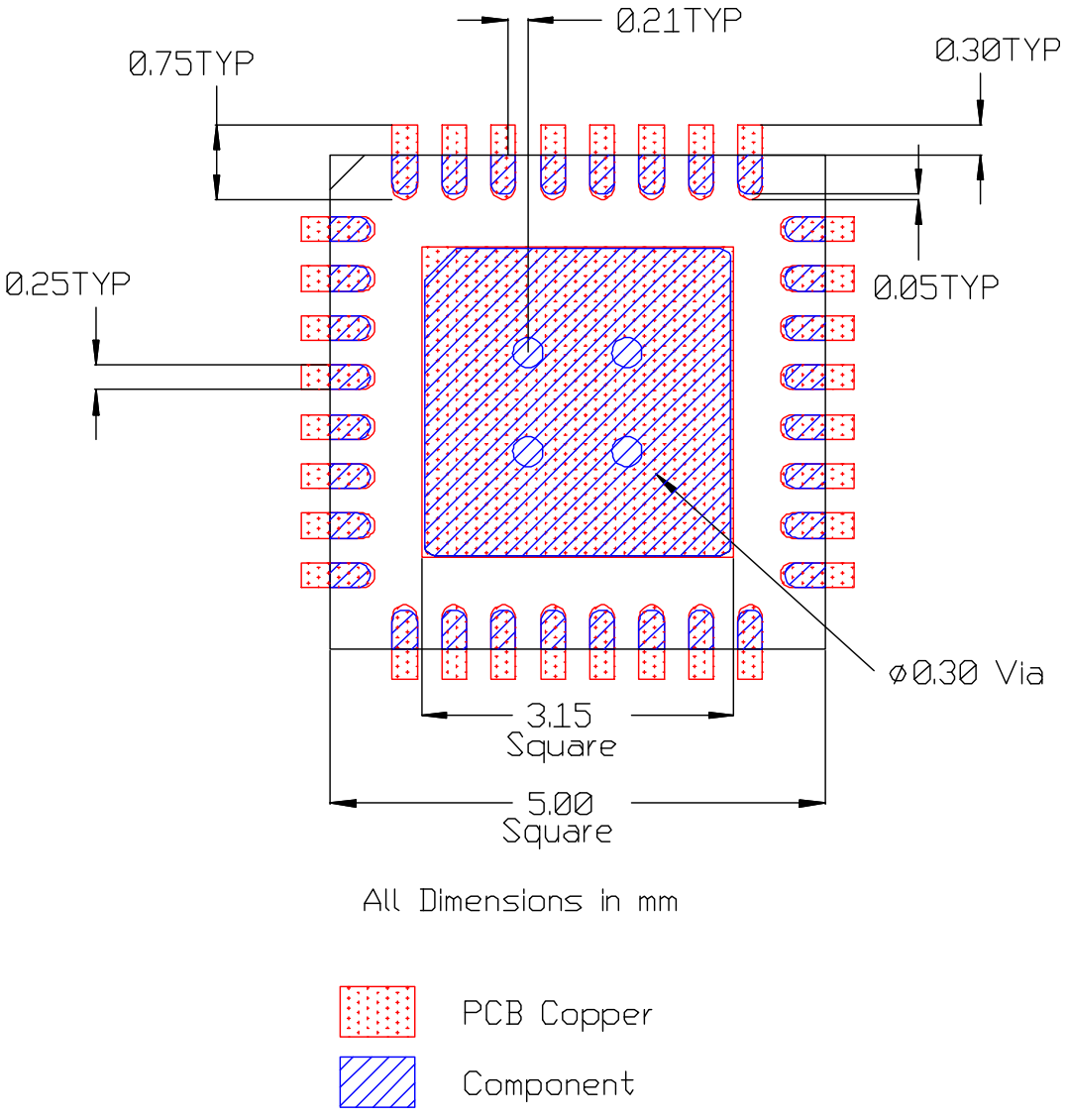
LAYOUT GUIDELINES

The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Separate analog bus (EAIN, DACIN and ISHARE) from digital bus (CLKIN, PHSIN, and PHSOUT) to reduce the noise coupling.
- Place VCCL decoupling capacitor VCCL as close as possible to VCCL and LGND pins.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, and CSS/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB, VO and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Avoid analog control bus signals, VDAC, IIN, and especially EAOUT, crossing over the fast transition nodes.
- Separate digital bus, CLKOUT, PHSOUT and PHSIN from the analog control bus and other compensation components.

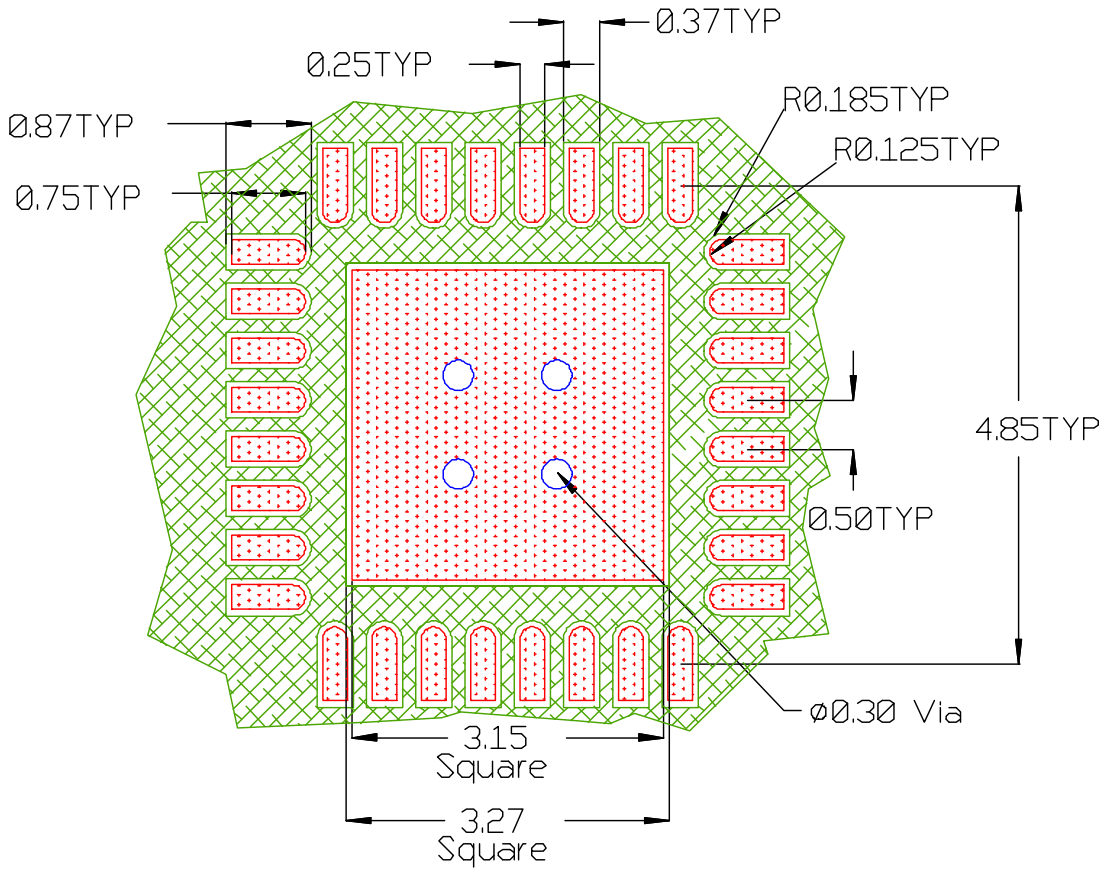
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.30mm diameter vias shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.
- No pcb traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the pcb resulting in poor solder joints to the IC leads.



SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- Four vias in the land pad should be tented or plugged from bottom boardside with solder resist.



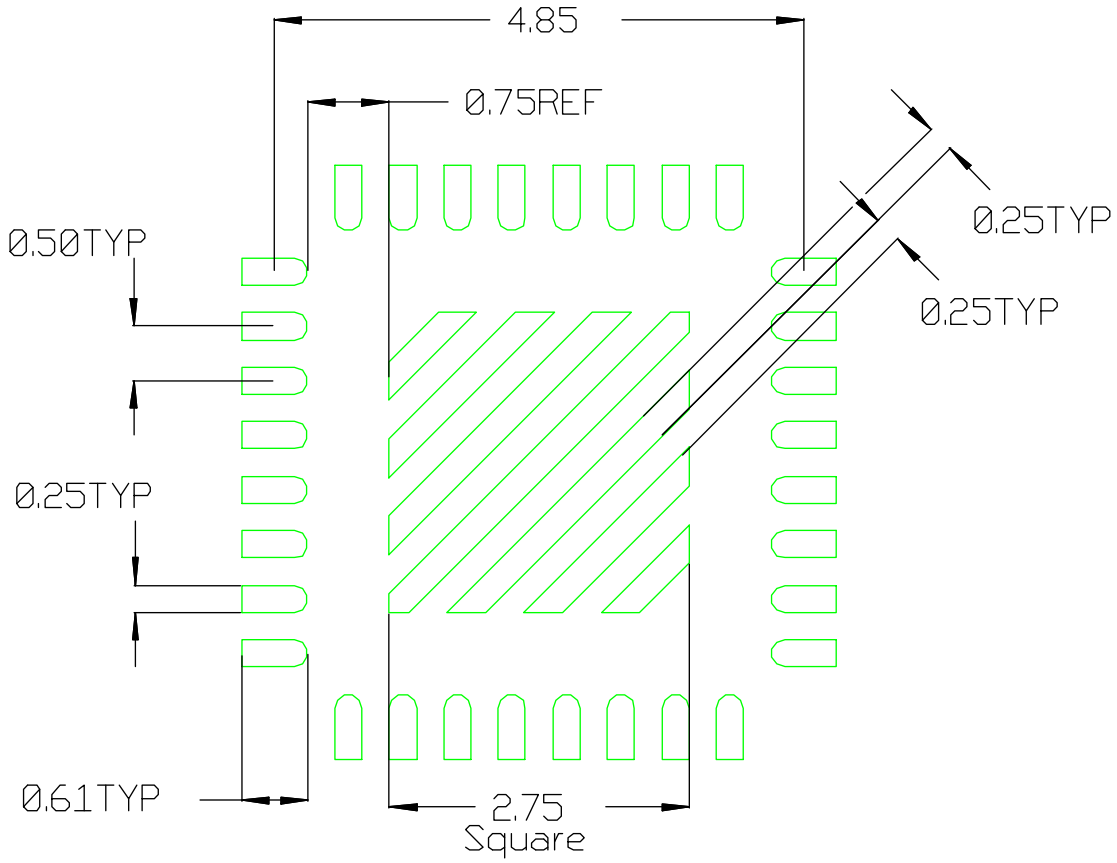
All Dimensions in mm

PCB Copper

PCB Solder Resist

STENCIL DESIGN

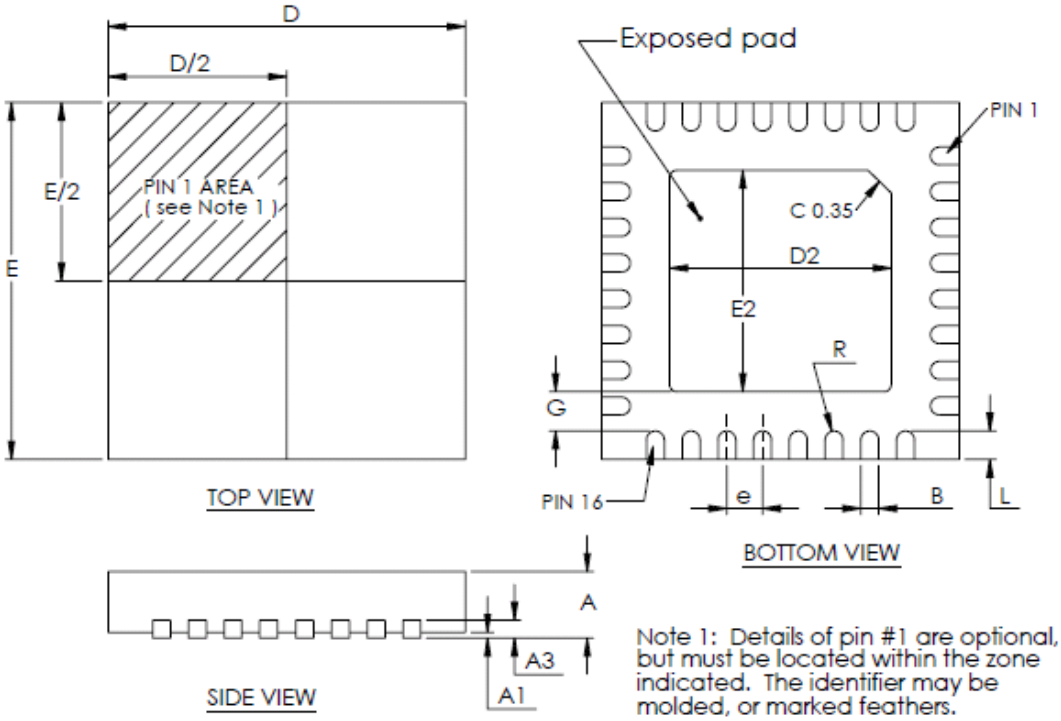
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) θ_{JA} =24.4 °C/W, θ_{JC} =0.86 °C/W



32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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