FAIRCHILD SEMICONDUCTOR®

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RV4141A
Low-Power, Ground-Fault Interrupter

Features

- Powered from the AC Line
- Built-In Rectifier
- Direct Interface to SCR
- 500µA Quiescent Current
- Precision Sense Amplifier
- Adjustable Time Delay
- Minimum External Components
- Meets UL 943 Requirements
- Compatible with 110V or 220V Systems
- Available in an 8-Pin SOIC Package

Description

The RV4141A is a low-power controller for AC-receptacle, ground-fault circuit interrupters. These devices detect hazardous current paths to ground and ground to neutral faults. The circuit interrupter then disconnects the load from the line before a harmful or lethal shock occurs.

Internally, the RV4141A contains a diode rectifier, shunt regulator, precision sense amplifier, current reference, time delay circuit, and SCR driver.

Two sense transformers, SCR, solenoid, three resistors, and four capacitors complete the design of the basic circuit interrupter. The simple layout and minimum component count ensure ease of application and long-term reliability. Features not found in other GFCI controllers include a low offset voltage sense amplifier, eliminating the need for a coupling capacitor between the sense transformer and sense amplifier, and an internal rectifier to eliminate high-voltage rectifying diodes.

The RV4141A is powered only during the positive half period of the line voltage, but can sense current faults independent of its phase relative to the line voltage. The gate of the SCR is driven only during the positive half cycle of the line voltage.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
RV4141AN	-30 to +85°C	Green	8-Lead, Plastic Dual-Inline Package (DIP)	Rails
RV4141AMT	-30 to +85°C	Green	8-Lead, Plastic Small-Outline Integrated Circuit (SOIC)	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

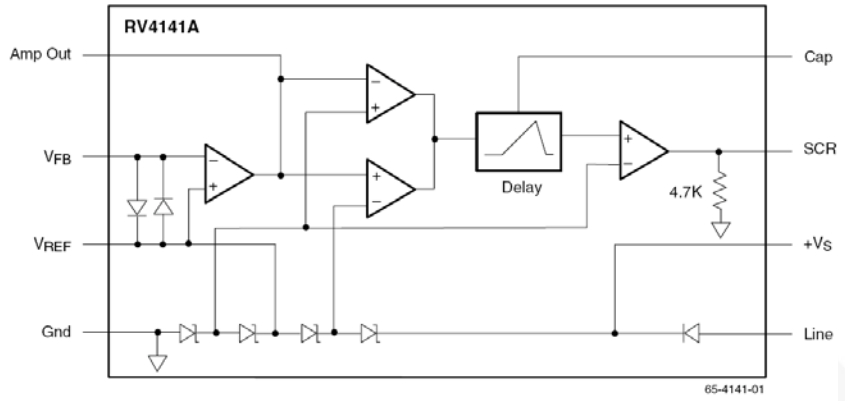


Figure 1. Block Diagram

Pin Configuration

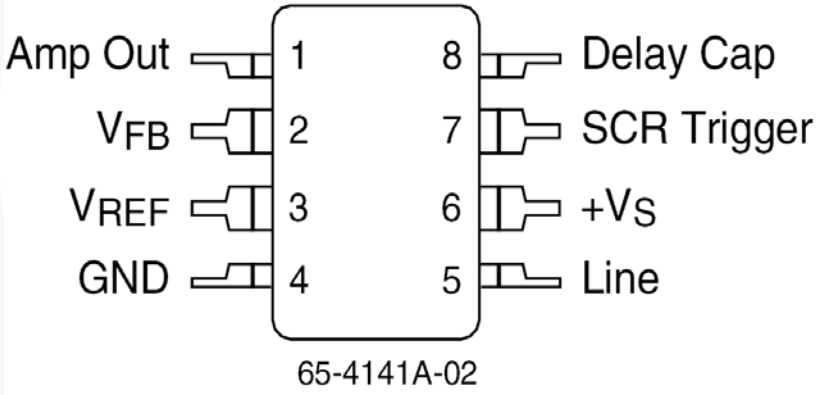


Figure 2. Pin Assignment

Pin Definitions

Pin #	Name	Description
1	Amp Out	Sense Amplifier Output – an external resistor to V_{FB} sets the I_{FAULT} threshold
2	V_{FB}	Sense amplifier negative input
3	V_{REF}	Sense amplifier positive input – biased internally at $+V_S/2$
4	GND	Substrate ground for all circuitry
5	Line	Anode of internal diode connected to supply voltage
6	$+V_S$	Supply input for RV4141A circuitry
7	SCR Trigger	Output for triggering external SCR when a fault is detected
8	Delay Cap	An external capacitor to ground sets the delay time for a ground fault to be present before triggering the SCR

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply			10	mA
P_D	Internal Power Dissipation			500	mW
T_{STG}	Storage Temperature Range		-65	+150	°C
T_A	Operating Temperature Range		-35	+80	°C
T_J	Junction Temperature			+125	°C
T_L	Lead Soldering Temperature	10 Seconds, SOIC		+260	°C
		60 Seconds, DIP		+300	

Thermal Characteristics

Symbol	Parameter		Typ.	Max.	Unit
Θ_{JA}	Thermal Resistance	SOIC	240		°C/W
		DIP	160		

Electrical Characteristics

I_{LINE} = 1.5mA and T_A = +25°C, R_{SET}= 650kΩ.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Shunt Regulator (Pins 5 to 4)						
V_{REG}	Regulated Voltage	I_{2-3} = 11µA	25	27	29	V
		I_{LINE} = 750µA, I_{2-3} = 9µA	25	27	29	
I_Q	Quiescent Current	V_{5-4} = 24V		500		µA
Sense Amplifier (Pins 2 to 3)						
V_{OFF}	Offset Voltage		-200	0	200	µV
GBW	Gain Bandwidth	Design Value		3		MHz
t_{SK}	Slew Rate	Design Value		1		V/µS
I_{BIAS}	Input Bias Current	Design Value		30	100	nA
SCR Trigger (Pins 7 to 4)						
R_{OUT}	Output Resistance	V_{7-4} = Open, I_{2-3} = µA	3.8	4.7	5.6	kΩ
V_{OUT}	Output Voltage	I_{2-3} = 9µA	0	0.1	10.0	mV
		I_{2-3} = 11µA	3.0	3.8	4.5	V
I_{OUT}	Output Current	V_{7-4} = 0V, I_{2-3} = 11µA	400	600		µA
Reference Voltage (Pins 3 to 4)						
V_{REF}	Reference Voltage	I_{LINE} = 750µA	12	13	14	V
Delay Timer (Pins 8 to 4)						
	Discharge / Charge Ratio	I_{2-3} = 0/11µA	1.8	2.5	3.0	µA/µA
t_{DLY}	Delay Time[(1)]	C_{8-4} = 12nF		2		ms
I_{DLY}	Delay Current	I_{2-3} = 11µA	30	40	50	µA

Notes:

1. Delay time is defined as starting when the instantaneous sense current (I_{2-3}) exceeds 6.5V/R_{SET} and ending when the SCR trigger voltage V_{7-6} goes HIGH.

Circuit Operation

(*Refer to Figure 1 and Figure 3.*)

The precision op amp connected to pins 1 through 3 senses the fault current flowing in the secondary of the sense transformer, converting it to a voltage at pin 1. The ratio of secondary current to output voltage is directly proportional to feedback resistor, R_{SET}.

R_{SET} converts the sense transformer secondary current to a voltage at pin 1. Due to the virtual ground created at the sense amplifier input by its negative feedback loop, the sense transformer's burden is equal to the value of R_{IN}. From the transformer's point of view, the ideal value for R_{IN} is 0Ω. This causes it to operate as a true current transformer with minimal error. However, making R_{IN} equal to zero creates a large offset voltage at pin 1 due to the sense amplifier's very high DC gain. R_{IN} should be selected as high as possible, consistent with preserving the transformer's operation as a true current mode transformer. A typical value for R_{IN} is between 200 and 1000Ω.

As seen in Equation (1), maximizing R_{IN} minimizes the DC offset error at the sense amplifier output. The DC offset voltage at pin 1 contributes directly to the trip current error. The offset voltage at pin 1 is:

$$V_{OS} \times R_{SET} / (R_{IN} + RS_{EC}) \quad (1)$$

where:
V_{OS} = Input offset voltage of sense amplifier;
R_{SET} = Feedback resistor;
R_{IN} = Input resistor;
R_{SEC} = Transformer secondary winding resistance.

The sense amplifier has a specified maximum offset voltage of 200µV to minimize trip current errors. Two comparators connected to the sense amplifier output are configured as a window detector, whose references are -6.5V and +6.5V, referred to pin 3. When the sense transformer secondary RMS current exceeds $4.6/R_{SET}$, the output of the window detector starts the delay circuit. If the secondary current exceeds the predetermined trip current for longer than the delay time, a current pulse appears at pin 7, triggering the SCR.

The SCR anode is directly connected to a solenoid or relay coil. The SCR can be tripped only when its anode is more positive than its cathode.

Supply Current Requirements

The RV4141A is powered directly from the line through a series-limiting resistor called R_{LINE}; its value is between 24kΩ and 91kΩ.

The controller IC has a built-in diode rectifier, eliminating the need for external power diodes. The recommended value for R_{LINE} is 24kΩ to 47kΩ for 110V systems and 47kΩ to 91kΩ for 220V systems. When R_{LINE} is 47kΩ, the shunt regulator current is limited to 3.6mA. The recommended maximum peak line current through R_{LINE} is 10mA.

GFCI Application

(Refer to Figure 3)

The GFCI detects a ground fault by sensing a difference in current in the line and neutral wires. The difference in current is assumed to be a fault current creating a potentially hazardous path from line to ground. Since the line and neutral wires pass through the center of the sense transformer, only the differential primary current is transferred to the secondary. Assuming the turns ratio is 1:1000, the secondary current is 1/1000th the fault current. The RV4141A's sense amplifier converts the secondary current to a voltage compared with either of the two window detector reference voltages. If the fault current exceeds the design value for the duration of the programmed time delay, the RV4141A sends a current pulse to the gate of the SCR.

Detecting ground-to-neutral faults is more difficult. R_B represents a normal ground fault resistance. R_N is the wire resistance of the electrical circuit between load/neutral and earth ground. R_G represents the ground-to-neutral fault condition. According to UL 943, the GFCI must trip when R_N = 0.4Ω, R_G = 1.6Ω, and the normal ground fault is 6mA.

Assuming the ground fault to be 5mA, 1mA, and 4mA goes through R_G and R_N, respectively, causing an effective 1mA fault current. This current is detected by the sense transformer and amplified by the sense amplifier. The ground / neutral and sense transformers are mutually coupled by R_G, R_N, and the neutral wire ground loop, producing a positive feedback loop around the sense amplifier. The newly created feedback loop causes the sense amplifier to oscillate at a frequency determined by ground/neutral transformer secondary inductance and C4, which occurs at 8KHz.

C2 is used to program the time required for the fault to be present before the SCR is triggered. Refer to Equation (2) for calculating the value of C2. Its typical value is 12nF for a 2ms delay. R_{SET} is used to set the fault current at which the GFCI trips. When used with a 1:1000 sense transformer, its typical value is 1MΩ for a GFCI designed to trip at 5mA.

R_{IN} should be the highest value possible that ensures a predictable secondary current from the sense transformer. If R_{IN} is set too high, normal production variations in the transformer permeability causes unit-to-unit variations in the secondary current. If it is too low, a large offset voltage error at pin 1 is present. This error voltage in turn creates a trip current error proportional to the input offset voltage of the sense amplifier. As an example, if R_{IN} is 500Ω, R_{SET} is 1MΩ, R_{SEC} is 45Ω, and the V_{OS} of the sense amplifier is its maximum of 200µV; the trip current error is ±5.6%.

The SCR anode is directly connected to a solenoid or relay coil. It can be tripped only when its anode is more positive than its cathode. It must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger it. Also the SCR must have a gate drive requirement less than 200µA. C3 is a noise filter that prevents high-frequency line pulses from triggering the SCR. The relay solenoid should have a response time of 3ms or less to meet the UL 943 timing requirement.

Sense Transformers and Cores

The sense and ground/neutral transformer cores are usually fabricated using high-permeability laminated steel rings. Their single-turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns. Transformers may be obtained from Magnetic Metals, Inc. *(www.magmet.com).*

Calculating the Values of R_{SET} and C2

Determine the nominal ground-fault trip-current requirement. This is typically 5mA in North America ($117V_{AC}$) and 22mA in the UK and Europe ($220V_{AC}$). Determine the minimum delay time required to prevent nuisance tripping, typically 1 to 2ms. The value of C2 required to provide the desired delay time is:

$$C2 = 6 \times t \quad (2)$$

where:
C2 is in Nf and t is the desired delay time in ms.

The value of R_{SET} to meet the nominal ground fault trip current specification is:

$$R_{SET} = \frac{4.6 \times N}{I_{FAULT} \times COS\,180(t/P)} \quad (3)$$

where:
R_{SET} is in kΩ;
t is the time delay in ms;
P is the period of the line frequency in ms;
I_{FAULT} is the desired ground fault trip current in mA RMS;
N is the number of sense transformer secondary turns.

Note:
2. This formula assumes an ideal sense transformer is used. The calculated value of R_{SET} may have to be changed up to 30% when using a non-ideal transformer.

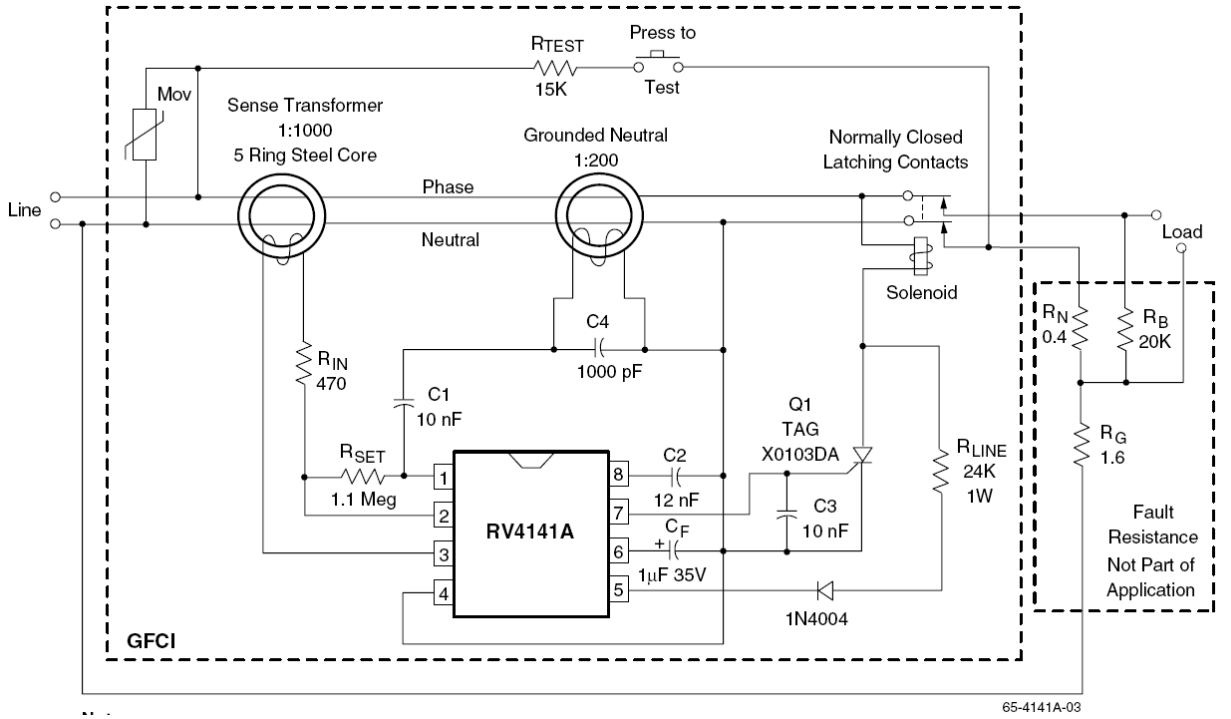
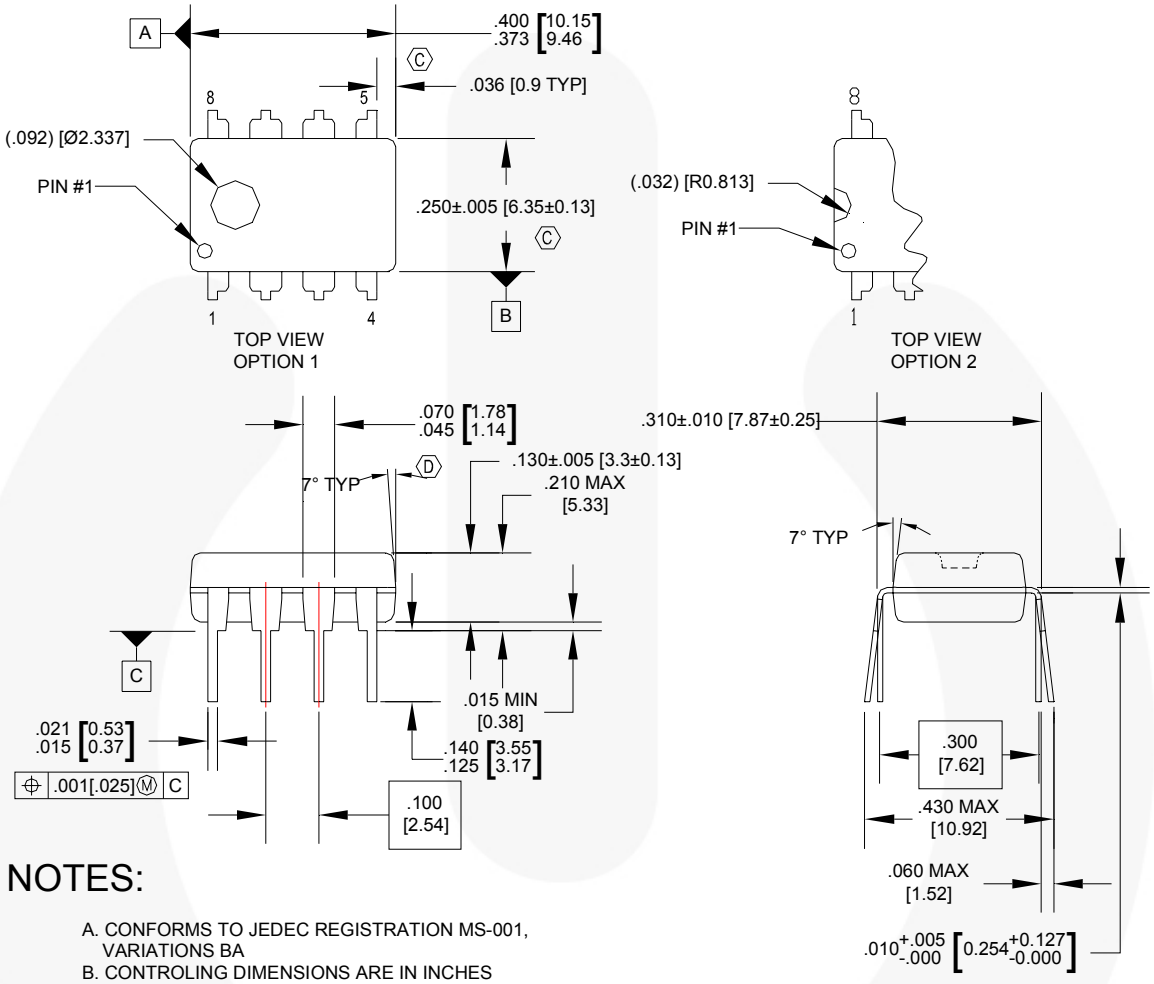


Figure 3. GFI Application Circuit

Physical Dimensions



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B. CONTROLING DIMENSIONS ARE IN INCHES REFERENCE DIMENSIONS ARE IN MILLIMETERS
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D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

Figure 4. 8-Lead, Plastic Dual-Inline Package (DIP)

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Physical Dimensions

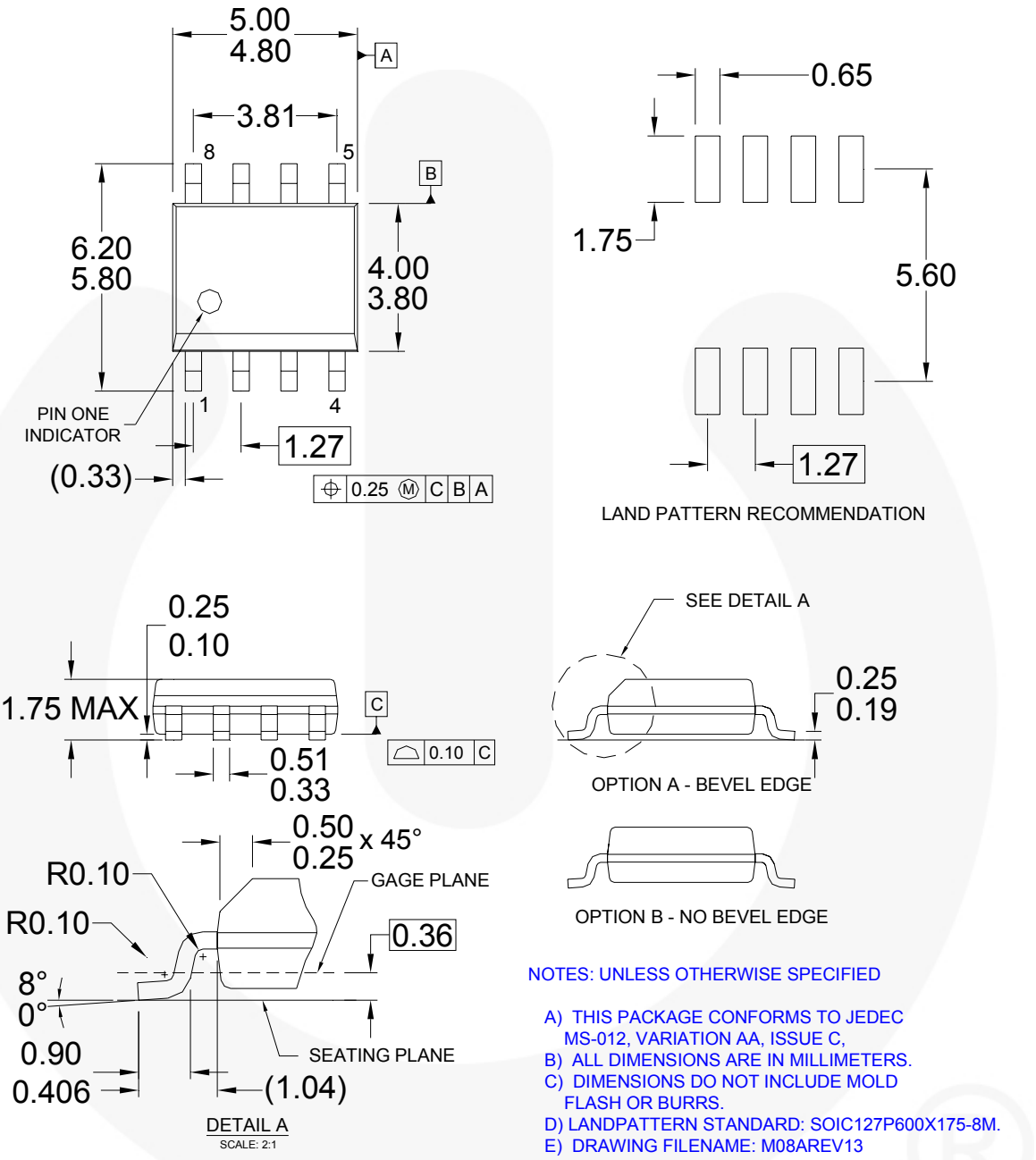

Figure 5. 8-Lead, Plastic Small-Outline Integrated Circuit (SOIC)

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