Thermoelectric Cooler (TEC) Controller

ADN8831

FEATURES

On-chip temperature measurement amplifiers
TEC current voltage monitoring
Programmable maximum TEC voltage
Programmable maximum TEC current
Separate heating and cooling current limits
High efficiency: >90%
Temperature lock indication
Programmable switching frequency up to 1 MHz
Oscillator synchronization with an external signal
Clock phase adjustment for multiple operation
Compact 5 mm x 5 mm LFCSP

APPLICATIONS

Thermoelectric cooler (TEC) control
Optical transceiver modules
Optical fibre amplifiers
Optical networking systems

GENERAL DESCRIPTION

The ADN8831 is a monolithic controller that drives a thermoelectric cooler (TEC) to stabilize the temperature of a laser diode or a passive component used in communications equipment.

This device relies on a negative temperature coefficient (NTC) thermistor or a positive temperature coefficient RTD device to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage either from a DAC or with an external resistor divider.

The loop is stabilized by a PID compensation amplifier with high stability and low noise. The compensation network can be adjusted by the user to optimize temperature settling time.

The ADN8831 measures and limits a TEC current for both heating and cooling, independently. A 2.5 V voltage reference is provided for the thermistor temperature sensing bridge.

FUNCTIONAL BLOCK DIAGRAM

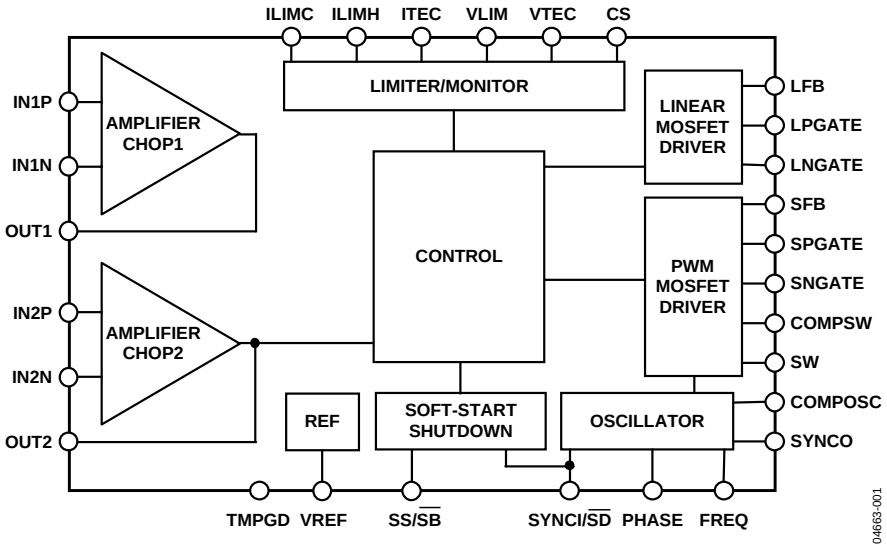

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/05 –Revision 0: Initial Version

SPECIFICATIONS

Electrical characteristics V_{DD} = 3.0 V to 5.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Conditions	Min	Typ	Max	Unit
PWM OUTPUT DRIVER						
Output Transition Time	t_R, t_F	C_L = 3,300 pF		20		ns
Nonoverlapping Clock Delay			40	80		ns
Output Resistance	$R_{O\ (SNGATE,\ SPGATE)}$	I_L = 10 mA, V_{DD} = 3.0 V		6		Ω
Output Voltage Swing[2]	SFB	V_{LIM} = VREF	0		V_{DD}	V
LINEAR OUTPUT AMPLIFIER						
Output Resistance	$R_{O,\ LNGATE}$	I_{OUT} = 2 mA, V_{DD} =3.0 V		200		Ω
	$R_{O,\ LPGATE}$	I_{OUT} = 2 mA, V_{DD} = 3.0 V		100		Ω
Output Voltage Swing[2]	LFB		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.0		5.5	V
Supply Current	I_{SY}	PWM not switching		8	12	mA
		−40°C ≤ T_A ≤ +85°C			15	mA
Shutdown Current	I_{SD}	SYNCI/$\overline{SD}$ = 0 V		8		µA
Soft Start Charging Current	I_{SS}	V_{SS} = 0 V		8		µA
Undervoltage Lockout	UVLO	Low to high threshold		2.2	2.6	V
Standby Current	I_{SB}	SYNCI/$\overline{SD}$ = V_{DD}, SS/$\overline{SB}$ = 0 V		2		mA
Standby Threshold	V_{SB}	SYNCI/$\overline{SD}$ = V_{DD}		150	200	mV
ERROR/COMPENSATION AMPLIFIERS						
Input Offset Voltage	V_{OS1}	V_{CM1} = 1.5 V, V_{IN1P} − V_{IN1M}		10	100	µV
	V_{OS2}	V_{CM2} = 1.5 V, V_{IN2P} − V_{IN2M}		10	100	µV
Input Voltage Range	$V_{CM1,\ 2}$		0		V_{DD}	V
Common-Mode Rejection Ratio	$CMRR_{1,\ 2}$	$V_{CM1,\ 2}$ = 0.2 V to V_{DD} − 0.2 V		120		dB
Output Voltage High	$V_{OH1,\ 2}$		V_{DD} − 0.03			V
Output Voltage Low	$V_{OL1,\ 2}$				25	mV
Power Supply Rejection Ratio	$PSRR_{1,\ 2}$	3.0 V ≤ V_{DD} ≤ 5.0 V		110		dB
Output Current	$I_{OUT1,\ 2}$	Sourcing and sinking	5			mA
Gain Bandwidth Product	$GBW_{1,\ 2}$	V_{OUT} = 0.5 V to (V_{DD} − 1 V)		2		MHz
OSCILLATOR						
Sync Range	f_{CLK}	SYNCI/$\overline{SD}$ connected to external clock	300		1,000	kHz
Oscillator Frequency	f_{CLK}	COMPOSC = V_{DD}, R_{FREQ} = 118 kΩ, SYNCI/$\overline{SD}$ = V_{DD}, V_{DD} = 5.0 V	800	1,000	1,250	kHz
Nominal Free-Run Oscillation Frequency	$f_{CLK-NOMINAL}$	COMPOSC = V_{DD}, SYNCI/$\overline{SD}$ = V_{DD}	200		1,000	kHz
Phase Adjustment Range[2]	Φ_{CLK}	V_{PHASE} = 0.13 V, $f_{SYNCI/\overline{SD}}$ = 1 MHz			50	degree
		V_{PHASE} = 2.3 V, $f_{SYNCI/\overline{SD}}$ = 1 MHz	330			degree
Phase Adjustment Default	Φ_{CLK}	PHASE = open		180		degree
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	I_{REF} = 2 mA		2.35		V
		I_{REF} = 0 mA	2.37	2.47	2.57	V
LOGIC OUTPUTS						
Logic Low Output Voltage	V_{OL}	TMPGD, SYNCO, I_O = 0 A			0.2	V
Logic High Output Voltage	V_{OH}	TMPGD, SYNCO, I_O = 0 A	V_{DD} − 0.2			V
Output High Impedance		V_{DD} = 5.0 V		35		Ω
Output Low Impedance		V_{DD} = 5.0 V		20		Ω
Output High Impedance		V_{DD} = 3.0 V		50		Ω
Output Low Impedance		V_{DD} = 3.0 V		25		Ω

Parameter[1]	Symbol	Conditions	Min	Typ	Max	Unit
TEC CURRENT MEASUREMENT						
ITEC Gain	$A_{V, ITEC}$	$V_{ITEC}/(V_{LFB} - V_{CS})$		25		V/V
ITEC Output Range High	$V_{ITEC, HIGH}$	No load	$V_{DD} - 0.05$			V
ITEC Output Range Low	$V_{ITEC, LOW}$				0.05	V
ITEC Input Range[2]	$V_{CS, VLFB}$		0		V_{DD}	V
ITEC Bias Voltage	$V_{ITEC, B}$	$V_{LFB} = V_{CS} = 0$	1.10	1.20	1.30	V
ITEC Output Current	$I_{OUT, TEC}$			1.5		mA
TEC VOLTAGE MEASUREMENT						
VTEC Gain	$A_{V, VTEC}$	$V_{VTEC}/(V_{LFB} - V_{SFB})$	0.23	0.25	0.28	V/V
VTEC Output Range[2]	V_{VTEC}	$V_{DD} = 5.0$ V	0.05		2.5	V
VTEC Bias Voltage[2]	$V_{VTEC, B}$	$V_{LFB} = V_{SFB} = 0$ V	1.20	1.25	1.35	V
VTEC Output Load Resistance	R_{VTEC}	$I_{VTEC} = 300$ µA		35		Ω
VOLTAGE LIMIT						
VLIM Gain	$A_{V, LIM}$	$(V_{LFB} - V_{SFB})/V_{VLIM}$		5		V/V
VLIM Input Range[2]	V_{VLIM}		0		V_{DD}	V
VLIM Input Current, Cooling	$I_{VLIM, COOL}$	$V_{OUT2} < V_{DD}/2$			100	nA
VLIM Input Current, Heating	$I_{VLIM, HEAT}$	$V_{OUT2} > V_{DD}/2$		I_{FREQ}		mA
VLIM Input Current Accuracy, Heating	$I_{VLIM, HEAT}$	I_{VLIM}/I_{FREQ}	0.8	1.0	1.18	A/A
CURRENT LIMIT						
ILIMC Input Voltage Range	V_{ILIMC}		1.1		$V_{DD} - 1$	V
ILIMH Input Voltage Range	V_{ILIMH}		0.1		1.3	V
ILIMC Limit Threshold	$V_{TH, ILIMC}$	$V_{ITEC} = 2.0$ V	1.98	2.0	2.02	V
ILIMH Limit Threshold	$V_{TH, ILIMH}$	$V_{ITEC} = 0.5$ V	0.48	0.5	0.52	V
TEMPERATURE GOOD						
High Threshold	$V_{OUT1, TH1}$	IN2M tied to OUT2, $V_{IN2P} = 1.5$ V		1.55	1.60	V
Low Threshold	$V_{OUT1, TH2}$	IN2M tied to OUT2, $V_{IN2P} = 1.5$ V	1.40	1.45		V

[1] Logic inputs meet typical CMOS I/O conditions for source/sink current (~1 µA).
[2] Guaranteed by design or indirect test methods.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to Vs + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Operating Junction Temperature	125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-lead LFCSP (ACP)	35	10	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

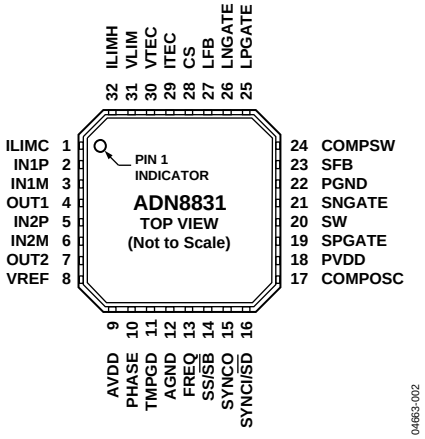

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	ILIMC	Analog Input	Sets TEC Cooling Current Limit.
2	IN1P	Analog Input	Noninverting Input to Error Amplifier.
3	IN1M	Analog Input	Inverting Input to Error Amplifier.
4	OUT1	Analog Output	Output of Error Amplifier.
5	IN2P	Analog Input	Noninverting Input to Compensation Amplifier.
6	IN2M	Analog Input	Inverting Input to Compensation Amplifier.
7	OUT2	Analog Output	Output of Compensation Amplifier.
8	VREF	Analog Output	2.5 V Voltage Reference Output.
9	AVDD	Power	Power for Nondriver Sections. 3.0 V minimum; 5.5 V maximum.
10	PHASE	Analog Input	Sets SYNCO Clock Phase Relative to SYNCI/$\overline{SD}$ Clock.
11	TMPGD	Digital Output	Logic Output. Active high. Indicates when OUT1 voltage is within ±100 mV of IN2P voltage.
12	AGND	Ground	Analog Ground. Connect to low noise ground.
13	FREQ	Analog Input	Sets Switching Frequency with an External Resistor.
14	SS/$\overline{SB}$	Analog Input	Sets Soft Start Time for Output Voltage. Pull low (VTEC = 0 V) to put ADN8831 into standby mode.
15	SYNCO	Digital Output	Phase Adjustment Clock Output. Phase set from PHASE pin. Used to drive SYNCI/$\overline{SD}$ of other ADN8831 devices.
16	SYNCI/$\overline{SD}$	Digital Input	Optional Clock Input. If not connected, clock frequency is set by FREQ pin. Pull low to put ADN8831 into shutdown mode. Pull high to negate shutdown mode.
17	COMPOSC	Analog Output	Compensation for Oscillator. Connect to PVDD when in free-run mode, connect to R-C network when in external clock mode.
18	PVDD	Power	Power for Output Driver Sections. 3.0 V minimum; 5.5 V maximum.
19	SPGATE	Analog Output	PWM Output Drives External PMOS Gate.
20	SW	Analog Input	Connects to PWM FET Drains.
21	SNGATE	Analog Output	PWM Output Drives External NMOS Gate.
22	PGND	Ground	Power Ground. External NMOS devices connect to PGND. Connect to digital ground.
23	SFB	Analog Input	PWM Feedback. Connect to the negative (–) TEC pin of TEC.
24	COMPSW	Analog Input	Compensation for Switching Amplifier.
25	LPGATE	Analog Output	Linear Output Drives External PMOS Gate.
26	LNGATE	Analog Output	Linear Output Drives External NMOS Gate.
27	LFB	Analog Input	Linear Feedback. Connect to the positive (+) TEC pin of TEC.
28	CS	Analog Input	Connect to Output Current Sense Resistor.

Pin No.	Mnemonic	Type	Description
29	ITEC	Analog Output	Indicates TEC Current.
30	VTEC	Analog Output	Indicates TEC Voltage.
31	VLIM	Analog Input	Sets Maximum TEC Voltage.
32	ILIMH	Analog Input	Sets TEC Heating Current Limit.

DETAILED BLOCK DIAGRAM

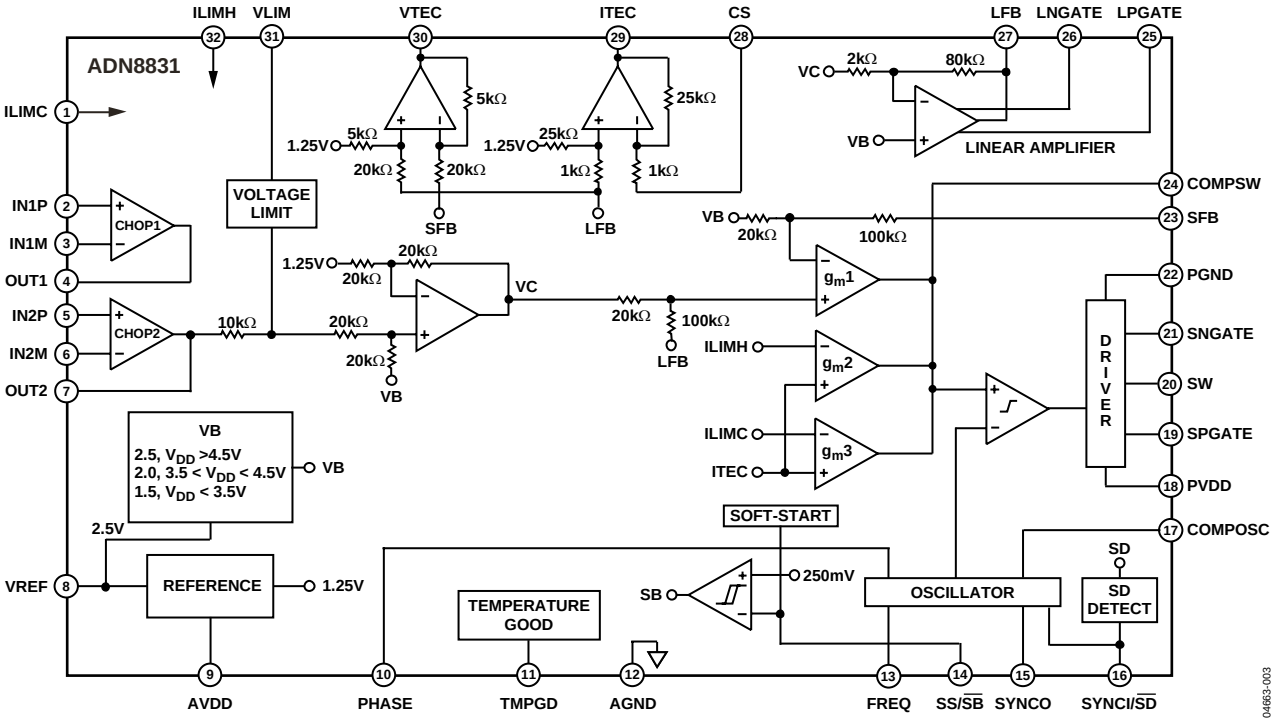

Figure 3. Detailed Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

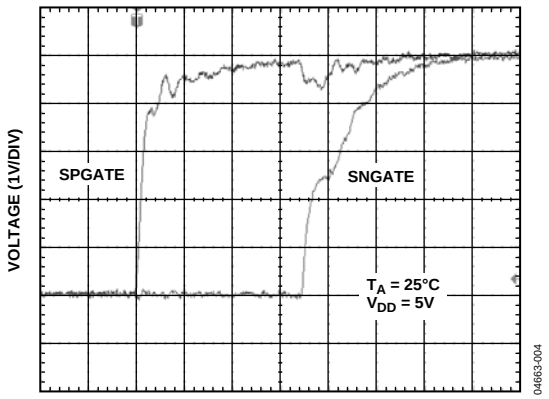

Figure 4. SPGATE and SNGATE Rise Time Using Circuit Shown in Figure 12

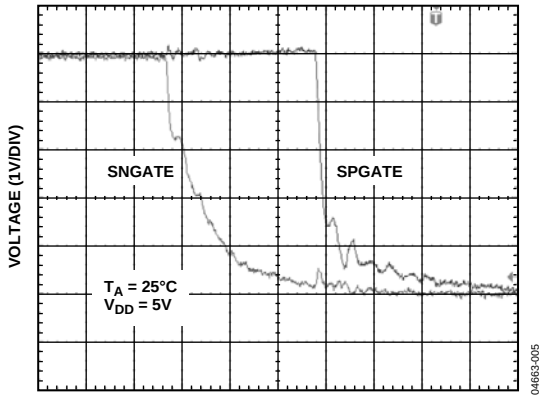

Figure 5. SNGATE and SPGATE Fall Time Using Circuit Shown in Figure 12

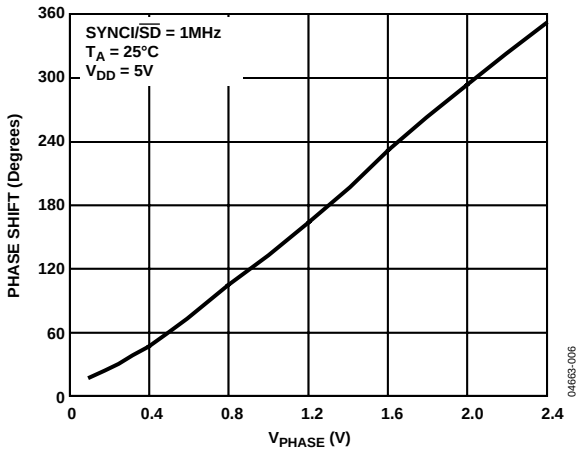

Figure 6. Clock Phase Shift vs. Phase Voltage

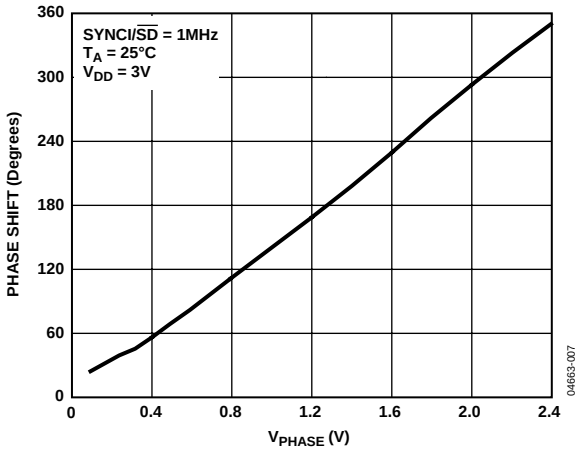

Figure 7. Clock Phase Shift vs. Phase Voltage

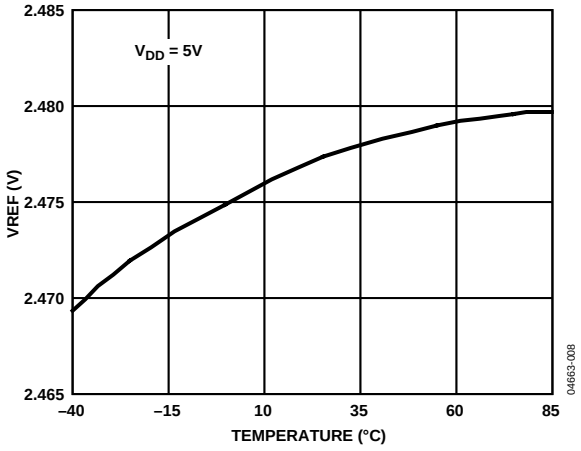

Figure 8. V_{REF} vs. Temperature

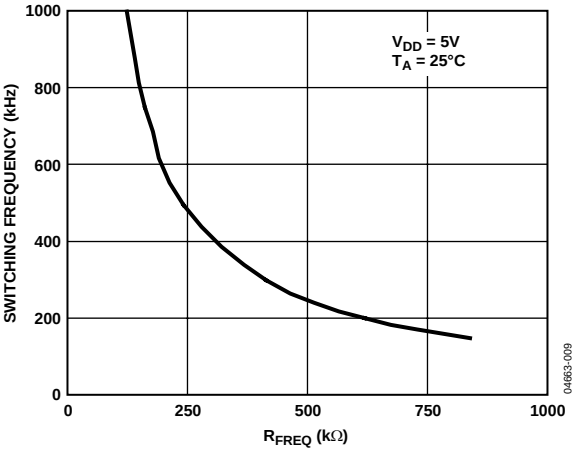

Figure 9. Switching Frequency vs. R_{FREQ}

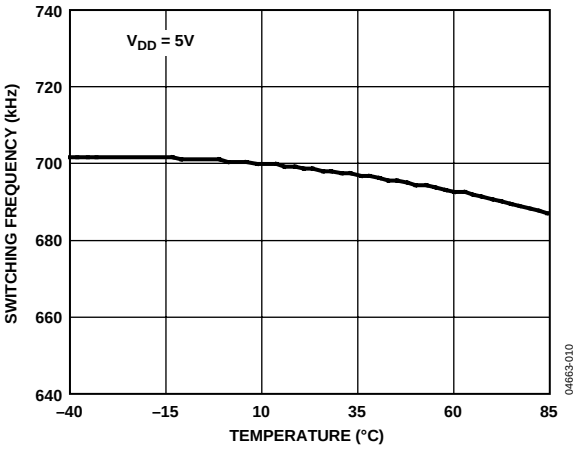

Figure 10. Switching Frequency vs. Temperature

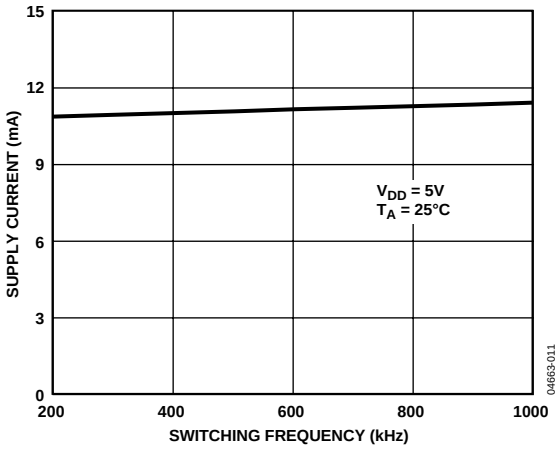

Figure 11. Supply Current vs. Switching Frequency

THEORY OF OPERATION

The ADN8831 is a controller for a thermoelectric cooler (TEC). The voltage applied to the input of the ADN8831 corresponds to the target temperature set point. The appropriate current is then applied to the TEC to pump heat either to, or away from, the object whose temperature is being regulated. The temperature of the object is measured by a thermistor and is fed back to the ADN8831 to correct the loop and settle the TEC to the appropriate final temperature. For best stability, the thermistor should be mounted in close proximity to the object. In most laser diode modules, the TEC and thermistor are already mounted in the unit and are used to regulate the temperature of the laser diode.

The ADN8831 integrates self-correcting auto-zero amplifiers (Chop1 and Chop2). The Chop1 amplifier can be used as a temperature measurement amplifier to create a voltage that is proportional to the object temperature. The output of the temperature measurement amplifier (Chop1) is then fed into the compensation amplifier (Chop2). In a compensation stage, the temperature measurement voltage is compared against the temperature set input voltage, creating an error voltage that is proportional to the difference. Also, an external network consisting of several resistors and capacitors is connected around the compensation amplifier. The user can adjust this network to optimize the step response of the TEC temperature, either in terms of settling time or maximum current change. Details of how to adjust the compensation network are in the PID Compensation Amplifier (Chop2) section. The TEC is differentially driven using an H-bridge configuration. The ADN8831 drives external transistors that are used to provide the current to the TEC. To further improve the power efficiency of the system, one side of the H-bridge uses a switched output. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H-bridge uses linear output without requiring any additional circuitry. This proprietary configuration allows the ADN8831 to provide efficiency of >90%. For most applications, a 4.7 µH inductor, a 22 µF capacitor, and a switching frequency of 1 MHz maintain less than 0.5% worst-case output voltage ripple across the TEC.

The maximum voltage across the TEC and current flowing through the TEC can be set using the VLIM and ILIM pins. Additional details are in the Maximum TEC Voltage Limit and Maximum TEC Current Limit sections.

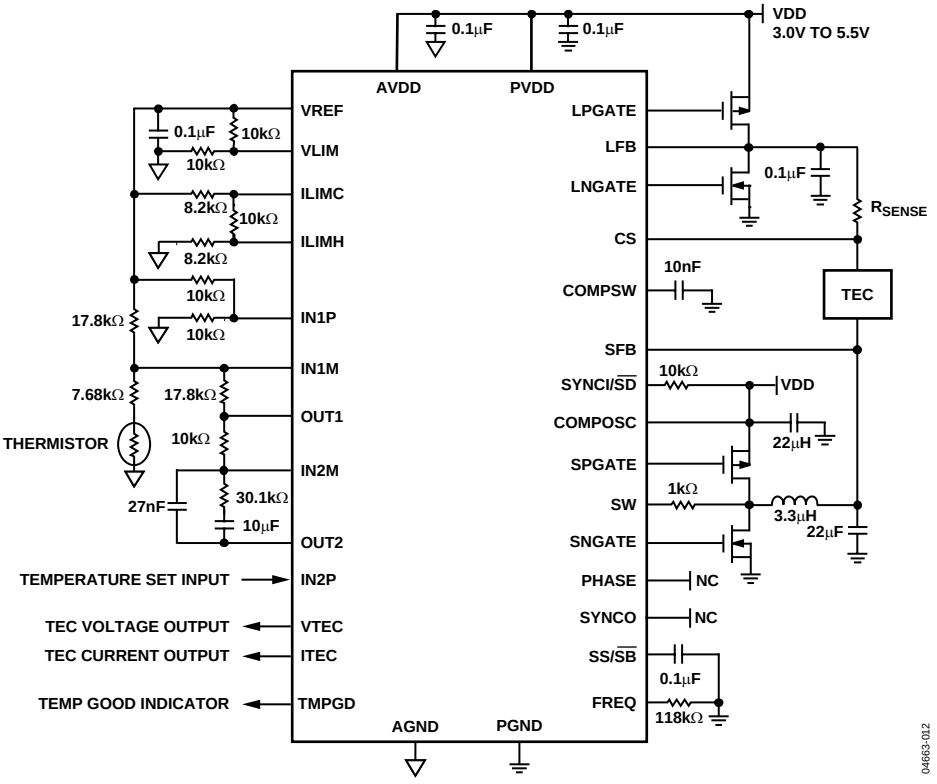

Figure 12. Typical Application Circuit 1

OSCILLATOR CLOCK FREQUENCY

The ADN8831 has an internal oscillator to generate the switching frequency for the output stage. This oscillator can be set in either free-run mode or synchronized to an external clock signal.

Free-Run Operation

The switching frequency is set by a single resistor connected from FREQ (Pin 13) to ground. Table 5 shows R_{FREQ} for some common switching frequencies. For free-run operation, connect SYNCI/$\overline{SD}$ (Pin 16) and COMPOSC (Pin 17) to PVDD.

Table 5. Switching Frequencies vs. R_{FREQ}

f_{SWITCH}	R_{FREQ}
250 kHz	484 kΩ
500 kHz	249 kΩ
750 kHz	168 kΩ
1 MHz	118 kΩ

Higher switching frequencies reduce the voltage ripple across the TEC. However, high switching frequencies will create more power dissipation in the external transistors due to the more frequent charging and discharging of the transistor gate capacitances.

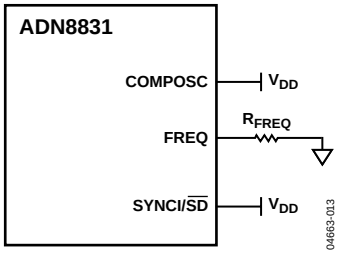

Figure 13. Free-Run Mode

External Clock Operation

The switching frequency of the ADN8831 can be synchronized with an external clock. Connect the clock signal to SYNCI/$\overline{SD}$ (Pin 16) and connect the COMPOSC (Pin 17) to an R-C network. This network compensates a PLL to lock on to the external clock.

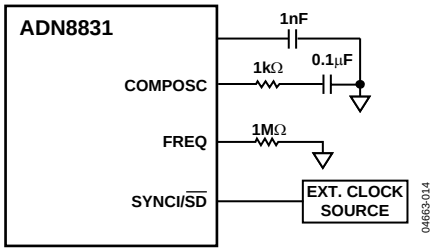

Figure 14. Synchronize to an External Clock

Connecting Multiple ADN8831 Devices

Connecting the SYNCO to the SYNCI/$\overline{SD}$ pin of another ADN8831 allows multiple ADN8831 devices to be driven using a single clock. Multiple ADN8831 devices can be driven from either a single master ADN8831 device by connecting its SYNCO pin to each slave SYNCI/$\overline{SD}$ pin, or daisy-chained by connecting each device's SYNCO to the next device's SYNCI/$\overline{SD}$ pin. When multiple ADN8831 devices are clocked at the same frequency, adjust its phase to reduce power supply ripple.

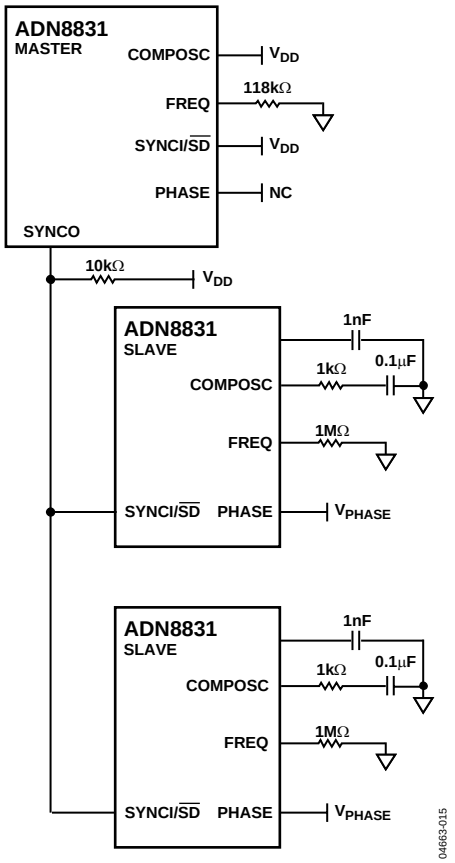

Figure 15. Multiple ADN8831 Devices Driven from a Master Clock

OSCILLATOR CLOCK PHASE

Adjust the oscillator clock phase using a simple resistor divider at the PHASE pin. Phase adjustment allows two or more ADN8831 devices to operate from the same clock frequency and not have all outputs simultaneously switch, potentially creating an excessive power supply ripple.

To ensure the correct operation of the oscillator, V_{PHASE} should remain between 100 mV and 2.4 V. The PHASE pin is internally biased at 1.2 V. If the PHASE pin is left open, clock phase is set at 180° as the default.

TEMPERATURE LOCK INDICATOR

The TMPGD pin (Pin 11) outputs a logic high when the OUT1 voltage reaches the IN2P voltage. The TMPGD has a detection range of ±25 mV and a 10 mV typical hysteresis. This allows direct interfacing to the microcontrollers or supervisory circuitry.

SOFT START ON POWER-UP

The ADN8831 can be programmed to ramp up for a specified time after the power supply is applied or after shutdown is de-asserted. This feature, known as soft start, is useful for gradually increasing the duty cycle of the PWM amplifier. The soft start time is set with a single capacitor connected from SS (Pin 14) to ground. Calculate the capacitor value by

$$\tau_{SS} = 150 \times C_{SS}$$

Where C_{SS} is the value of the capacitor in microfarads, and τ_{SS} is the soft start time in milliseconds. To set a soft start time of 15 ms, C_{SS} should equal 0.1 µF.

SHUTDOWN MODE

The shutdown mode sets the ADN8831 into an ultralow current state. The current draw for the ADN8831 in shutdown is typically 5 µA. The shutdown input $\overline{SD}$ pin (Pin 16) is active low. To shut down the device, drive $\overline{SD}$ to logic low. Once a logic high is applied, the ADN8331 will reactivate after the delay set by the soft start circuitry. Refer to the Soft Start on Power-Up section for more details on this feature.

STANDBY MODE

The ADN8831 has a standby mode that deactivates a MOSFET driver stage. The current draw for the ADN8831 in the standby mode is less than 1 mA. The standby input $\overline{SB}$ pin (Pin 14) is active low. After applying a logic high, the ADN8331 reactivates following the delay.

TEC VOLTAGE/CURRENT MONITOR

TEC voltage and current are monitored at the VTEC and ITEC pins, respectively.

Voltage Monitor

VTEC is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center VTEC voltage of 1.25 V corresponds to 0 V across TEC. The output voltage is calculated as

$$V_{VTEC} = 1.25 + 0.25 \times (V_{LFB} - V_{SFB})$$

Current Monitor

ITEC is an analog voltage output pin with a voltage proportional to the actual current through the TEC. A center ITEC voltage of 1.25 V corresponds to 0 A through the TEC. The output voltage is calculated as

$$V_{ITEC} = 1.25 + 25 \times (V_{LFB} - V_{CS})$$

The TEC current is obtained from this voltage by the following equation:

$$I_{TEC} = \frac{V_{ITEC} - 1.25}{25 \times R_{SENSE}}$$

MAXIMUM TEC VOLTAGE LIMIT

Set the maximum TEC voltage by applying a voltage at the VLIM pin to protect the TEC. This voltage can be set with a resistor divider or a DAC. The voltage limiter operates in bidirectional TEC voltage, and cooling and heating voltage.

Using a DAC

Both the cooling and heating voltage limits are set at the same levels when a voltage source directly drives the VLIM pin. The maximum TEC voltage is

$$V_{TEC(MAX)} = 5 \times V_{VLIM}$$

Where $V_{TEC\,(MAX)}$ is the maximum TEC voltage and V_{VLIM} is the voltage applied at the VLIM pin.

Using a Resistor Divider

Separate voltage limits can be set using a resistor divider. The internal current sink circuitry connected to the VLIM pin draws a current when the ADN8831 drives the TEC in a heating direction, thus lowering the voltage at the VLIM. The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

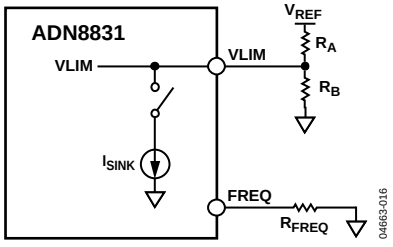

Figure 16. Using a Resistor Divider

The sink current is set by the resistor connected from the FREQ pin to ground. Calculate the sink current as

$$I_{SINK} = \frac{1.25}{R_{FREQ}}$$

Where I_{SINC} is the sink current at the VLIM pin, and R_{FREQ} is the resistor connected at FREQ. Then, calculate the cooling and heating limits as

$$V_{VLIM,COOL} = \frac{V_{REF} \times R_B}{R_A + R_B}$$

$$V_{VLIM,HEAT} = V_{VLIM,COOL} - I_{SINK} \times R_A \| R_B$$

MAXIMUM TEC CURRENT LIMIT

Set separate maximum TEC current limits in cooling and heating directions by applying a voltage at the ILIMC and ILIMH pins to protect the TEC. Maximum TEC currents are given as

$$I_{TEC,MAX,COOL} = \frac{V_{ILIMC} - 1.25}{25 \times R_{SENSE}}$$

$$I_{TEC,MAX,HEAT} = \frac{1.25 - V_{ILIMH}}{25 \times R_{SENSE}}$$

APPLICATIONS

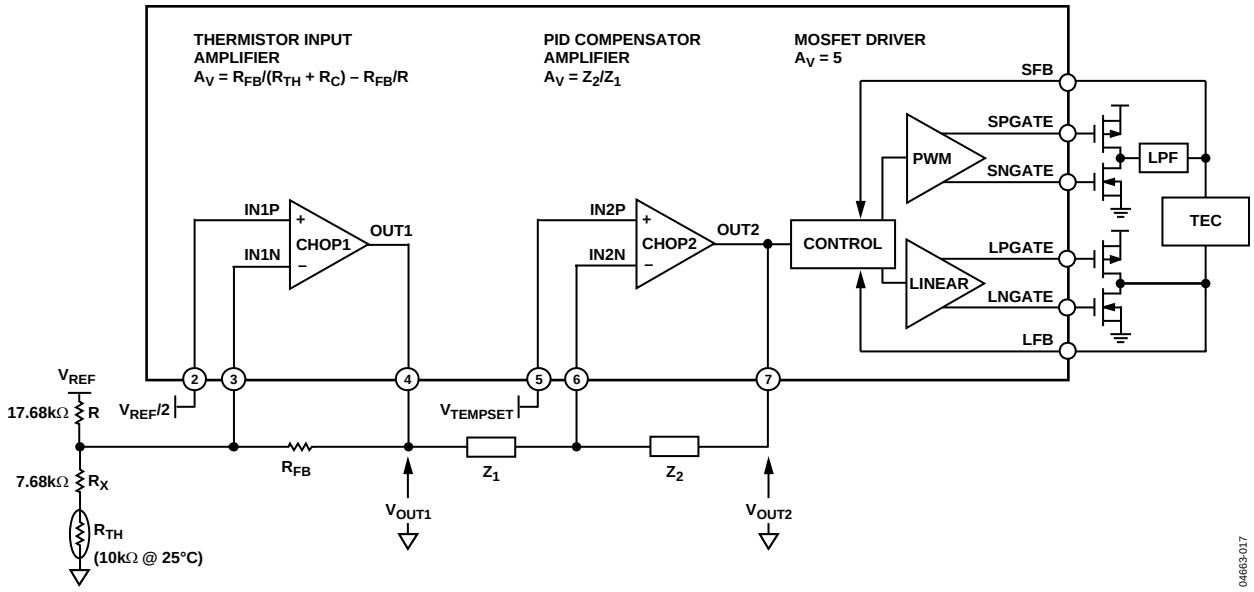

Figure 17. Signal Flow Block Diagram

SIGNAL FLOW

The ADN8831 integrates two auto-zero amplifiers defined as the Chop1 amplifier and Chop2 amplifier. Both of the amplifiers can be used as standalone amplifiers, thus, the implementation of temperature control can vary. Figure 17 shows the signal flow through the ADN8831, and a typical implementation of the temperature control loop using the Chop1 and Chop2 amplifiers.

In Figure 17, the Chop1 and Chop2 amplifiers are configured as the thermistor input amplifier and the PID compensation amplifier, respectively. The thermistor input amplifier gains the thermistor voltage then outputs to the PID compensation amplifier. The PID compensation amplifier then compensates a loop response over the frequency domain.

The output from the compensation loop at OUT2 is fed to the linear MOSFET gate driver. The voltage at LFB is fed with OUT2 into the PWM MOSFET gate driver. Including the external transistors, the gain of the differential output section is fixed at 5. For details on the output drivers, see the MOSFET Driver Amplifier section.

THERMISTOR SETUP

The thermistor has a nonlinear relationship to temperature; near optimal linearity over a specified temperature range can be achieved with the proper value of R_X placed in series with the thermistor. First, the resistance of the thermistor must be known, where

$$R_{LOW} = R_{TH} @ T_{LOW}$$
$$R_{MID} = R_{TH} @ T_{MID}$$
$$R_{HIGH} = R_{TH} @ T_{HIGH}$$

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. These resistances can be found in most thermistor data sheets. In some cases, only the B constant is given, R_{TH} is calculated as

$$R_{TH} = R_R \exp\left\{B\left(\frac{1}{T} - \frac{1}{T_R}\right)\right\}$$

Where, R_{TH} is a resistance at T[K], R_R is a resistance at T_R[K].

R_X is then found as

$$R_X = \left(\frac{R_{LOW}R_{MID} + R_{MID}R_{HIGH} - 2R_{LOW}R_{HIGH}}{R_{LOW} + R_{HIGH} - 2R_{MID}}\right)$$

THERMISTOR AMPLIFIER (CHOP1)

The Chop1 amplifier can be used as a thermistor input amplifier. In Figure 17, the output voltage is a function of the thermistor temperature. The voltage at OUT1 is expressed as

$$V_{OUT1} = \left(\frac{R_{FB}}{R_{TH} + R_X} - \frac{R_{FB}}{R} + 1\right) \times \frac{V_{REF}}{2}$$

Where, R_{TH} is a thermistor, R_X is a compensation resistor. R is calculated as

$$R = R_X + R_{TH\,@\,25°C}$$

The V_{OUT1} is centered around $V_{REF}/2$ at 25°C. With the typical values shown in Figure 17, an averaged temperature-to-voltage coefficient is −25mV/°C at a range of +5°C to +45°C.

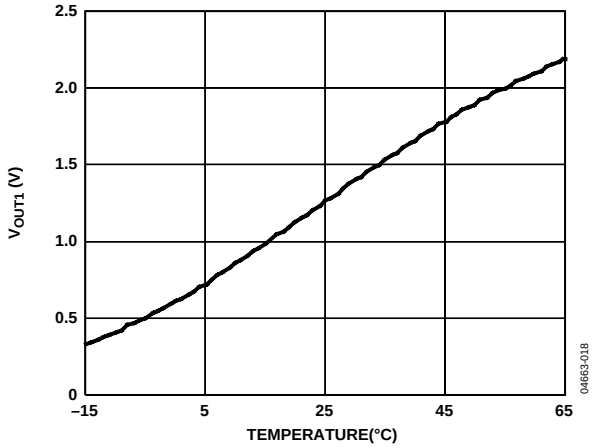

Figure 18. V_{OUT1} vs. Temperature

PID COMPENSATION AMPLIFIER (CHOP2)

Use the Chop2 amplifier as the PID compensation amplifier. The voltage at OUT1 feeds into the PID compensation amplifier. The frequency response of the PID compensation amplifier is dictated by the compensation network. Apply the temperature set voltage at IN2P. In Figure 17, the voltage at OUT2 is expressed as

$$V_{OUT2} = V_{TEMPSET} - \frac{Z2}{Z1}(V_{OUT1} - V_{TEMPSET})$$

The user sets the exact compensation network. This network can vary from a simple integrator to PI, PID, or any other type of network. The user also determines the type of compensation and component values because they are dependent on the thermal response of the object and the TEC. One method for empirically determining these values is to input a step function to IN2P, thus changing the target temperature, and adjusting the compensation network to minimize the settling time of the object's temperature.

A typical compensation network used for temperature control of a laser module is a PID loop consisting of a very low frequency pole and two separate zeros at higher frequencies. Figure 19 shows a simple network for implementing PID compensation. To reduce the noise sensitivity of the control loop, an additional pole is added at a higher frequency than the zeros. The bode plot of the magnitude is shown in Figure 20. The unity-gain crossover frequency of the feed-forward amplifier is

$$f_{0\,dB} = \frac{1}{2\pi R3C1} \times 80 \times TECGAIN$$

To ensure stability, the unity-gain crossover frequency should be lower than the thermal time constant of the TEC and thermistor. However, this thermal time constant is sometimes unspecified making it difficult to characterize. There are many texts written on loop stabilization, and it is beyond the scope of this data sheet to discuss all methods and trade offs in optimizing compensation networks.

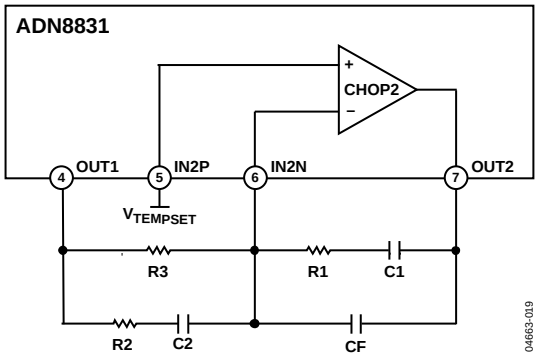

Figure 19. Implementing a PID Compensation Loop

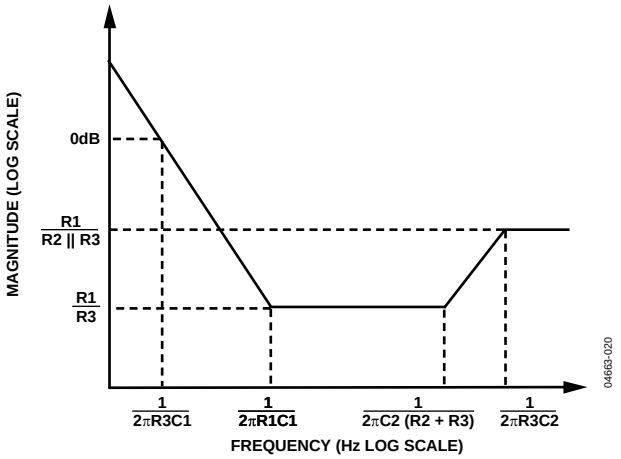

Figure 20. Bode Plot for PID Compensation

MOSFET DRIVER AMPLIFIER

The ADN8831 has two separate MOSFET drivers: a switched output or pulse-width modulated (PWM) amplifier, and a high gain linear amplifier. Each amplifier has a pair of outputs that drive the gates of external MOSFETs which, in turn, drive the TEC as in Figure 17. A voltage across the TEC is monitored via SFB and LFB. Although both MOSFET drivers achieve the same result, to provide constant voltage and high current, their operation is different. The exact equations for the two outputs are

$$V_{LFB} = V_B - 40(V_{OUT2} - 1.5)$$

$$V_{SFB} = V_{OUT2} + 5(V_{OUT2} - 1.5)$$

Where V_{OUT2} is the voltage at OUT2 pin. V_B is determined by V_{DD} as

$$V_B = 1.5[V_{DD} < 3.5]$$

$$V_B = 2.0[3.5 < V_{DD} < 4.5]$$

$$V_B = 2.5[4.5 < V_{DD}]$$

The voltage at OUT2 is determined by the compensation network that receives temperature set voltage and thermistor voltage fed by the input amplifier. V_{LFB} has a low limit of 0 V and an upper limit of V_{DD}. Figure 21 shows the graphs of these equations.

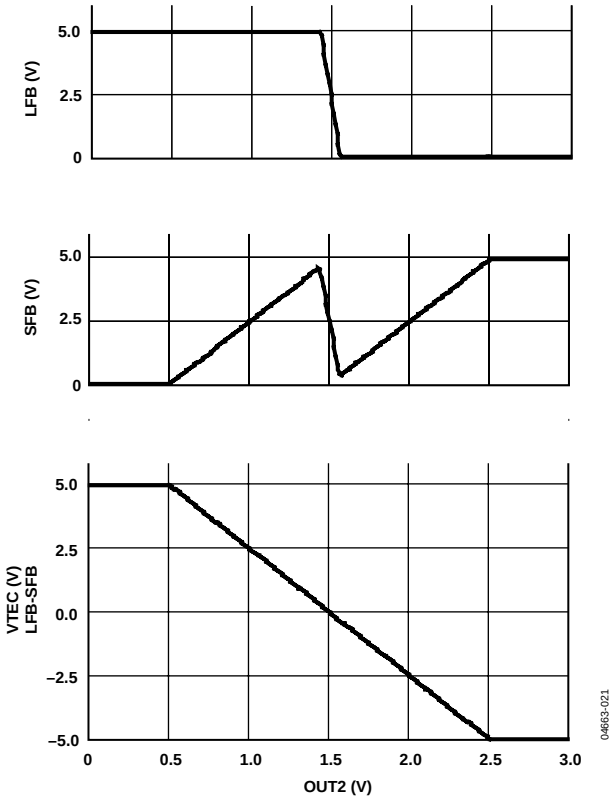

Figure 21. OUT2 Voltage vs. TEC Voltage

OUTLINE DIMENSIONS

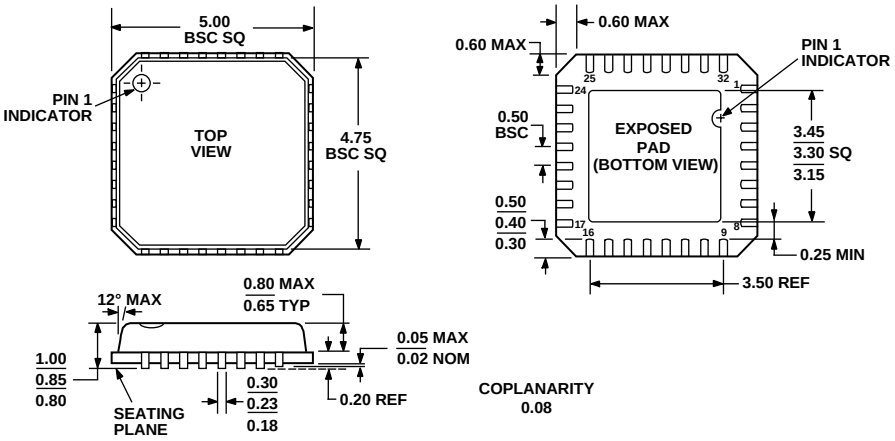

Figure 22. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
(CP-32-3)
Dimensions Shown in Millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN8831ACPZ-REEL7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
EVAL-ADN8831	−40°C to +85°C	Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

NOTES