PM6670AS

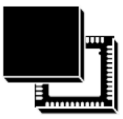
Complete DDR2/3 memory power supply controller

Features

- Switching section (VDDQ)
  - 4.5 V to 36 V input voltage range
  - 0.9 V, ±1% voltage reference
  - 1.8 V (DDR2) or 1.5 V (DDR3) fixed output voltages
  - 0.9 V to 2.6 V adjustable output voltage
  - 1.237 V ±1% reference voltage available
  - Very fast load transient response using constant-on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft-start internally fixed at 3 ms
  - Selectable pulse skipping at light load
  - selectable no-audible (33 kHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
- VTT LDO and VTTREF
  - 2 Apk LDO with foldback for VTT
  - Remote VTT sensing
  - High-Z VTT output in S3
  - Ceramic output capacitors supported
  - ±15 mA Low noise buffered reference

Applications

- DDR2/3 memory supply
- Digital TV system
- SSTL18, SSTL15 and HSTL bus termination



VFQFPN-24 4 mm x 4 mm

Description

The device PM6670AS is a complete DDR2/3 power supply regulator designed to meet JEDEC specifications.

It integrates a constant on-time (COT) buck controller, a 2 Apk sink/source low drop out regulator and a 15 mA low noise buffered reference.

The COT architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

The 2 Apk sink/source linear regulator provides the memory termination voltage with fast load transient response.

The device is full compliant with system sleep states S3 and S4/S5, providing LDO output high impedance in Suspend-To-RAM and Tracking Discharge of all outputs in Suspend-To-Disk.

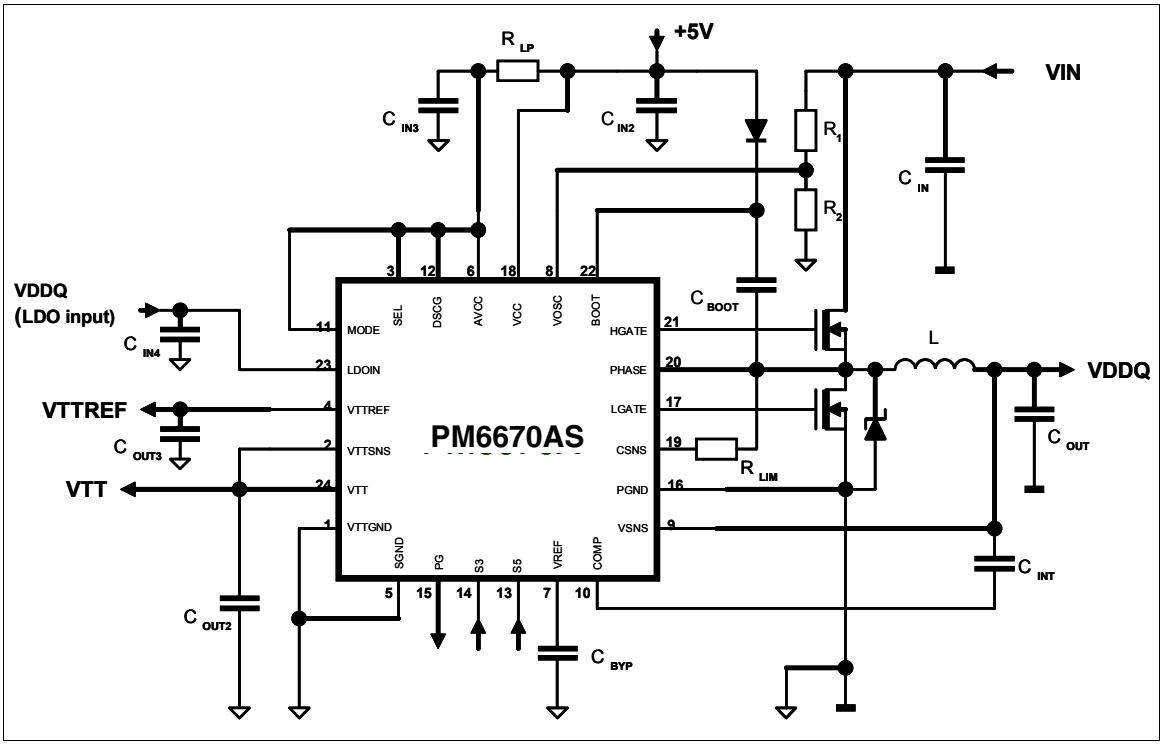
Table 1. Device summary

Order codes	Package	Packaging
PM6670AS	VFQFPN-24 4x4 (Exposed pad)	Tube
PM6670ASTR		Tape and reel

Contents

1 Typical application circuit

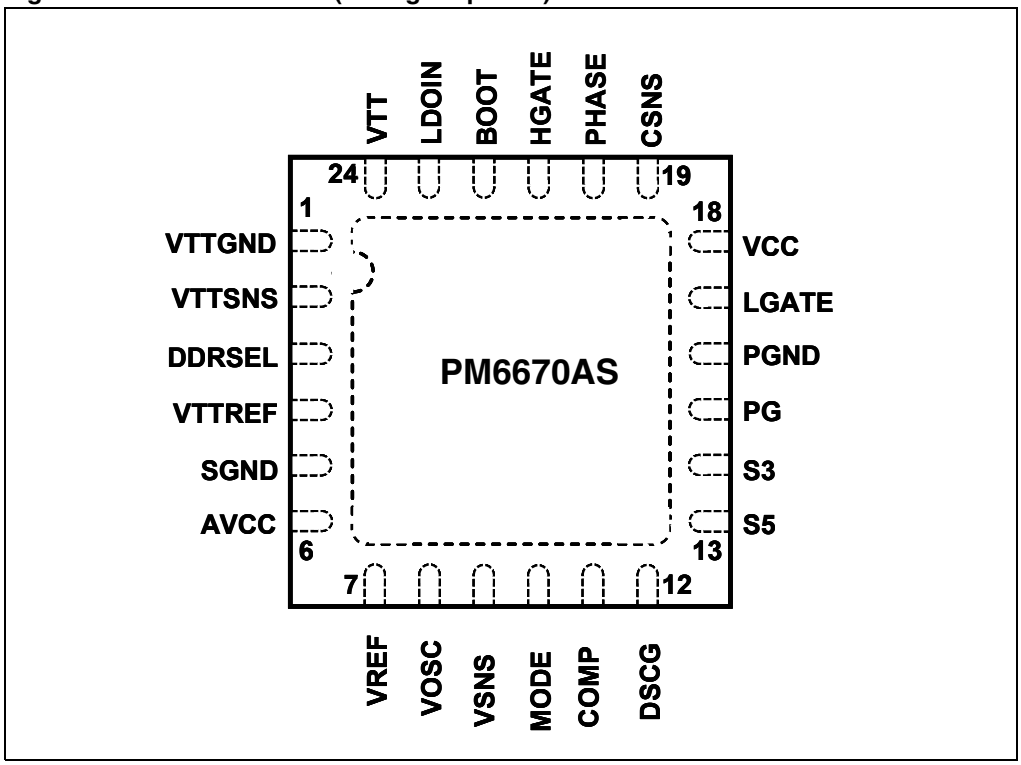
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	VTTGND	LDO power ground. Connect to negative terminal of VTT output capacitor.
2	VTTSNS	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	DDRSEL	DDR voltage selector (if MODE is tied to VCC) or pulse-skip/no-audible pulse-skip selector in adjustable mode (MODE voltage lower than 3 V). See *Mode of Operation Selection* section for details.
4	VTTREF	Low noise buffered DDR Reference Voltage. A 22 nF (minimum) ceramic bypass capacitor is required in order to achieve stability.
5	SGND	Ground reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5 V supply for internal logic. Connect to +5 V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237 V) for multilevel pins setting. It can deliver up to 50 µA. Connect a 100 nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Device Description* section for details.
9	VSNS	VDDQ output remote sensing. Discharge path for VDDQ in non-tracking discharge. Input for internal resistor divider that provides VDDQ/2 to VTTREF and VTT. Connect as close as possible to the load via a low noise PCB trace.
10	MODE	Mode of operation selector. If MODE pin voltage is higher than 4 V, the fixed output mode is selected. If MODE pin voltage is lower than 4 V, it is used as negative input of the error amplifier. See *Mode of Operation Selection* section for details.
11	COMP	DC voltage error compensation input for the switching section. Refer to *Mode of Operation Selection* section for more details.
12	DSCG	Discharge mode selection. Refer to *output discharge selection* section for tracking/non-tracking discharge or no-discharge options.
13	S5	Switching controller enable. Connect to S5 system status signal to meet S0-S5 power management states compliance. See *Power Management Pins* section for details. S5 pin can't be left floating.
14	S3	Linear regulator enable. Connect to S3 system status signal to meet S0-S5 power management states compliance. See *Power Management Pins* section for details. S3 pin can't be left floating.
15	PG	Power-Good signal (open drain output). High when VDDQ output voltage is within ±10% of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.

Table 2. Pin functions (continued)

N°	Pin	Function
18	VCC	+5 V low-side gate driver supply. Bypass with a 100 nF capacitor to PGND.
19	CSNS	Current Sense Input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDSon sensing)
20	PHASE	Switch node connection and return path for the high-side gate driver.
21	HGATE	High-side gate driver output
22	BOOT	Bootstrap capacitor connection. Positive supply input of the high-side gate driver.
23	LDOIN	Linear regulator input. Connect to VDDQ in normal configuration or to a lower supply to reduce the power dissipation. A 10 µF bypass ceramic capacitor is suggested for noise rejection enhancement. See Device Description section for more details.
24	VTT	LDO linear regulator output. Bypass with a 20 µF (2x10 µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, VTTGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{VCC} +0.3	
	CSNS, PG, S3, S5, DSCG, COMP, VSNS, VOSC, VREF, MODE, DDRSEL to GND	-0.3 to V_{AVCC} + 0.3	
	VTTREF, VREF, VTT, VTTSNS to SGND	-0.3 to V_{AVCC} + 0.3	
	LDOIN, VTT, VTTREF, LDOIN to VTTGND	-0.3 to V_{AVCC} + 0.3	
P_{TOT}	Power dissipation @T_A = 25 °C	2.3	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	- 50 to 150	°C
T_A	Operating ambient temperature range	- 40 to 125	°C
T_J	Junction operating temperature range	- 40 to 125	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	4.5	-	36	V
V_{AVCC}	IC supply voltage	4.5	-	5.5	
V_{VCC}	IC supply voltage	4.5	-	5.5	

4 Electrical characteristics

T_A = -25 °C to 85 °C, VCC = AVCC = +5 V and LDOIN connected to VDDQ output if not otherwise specified [(a)]

Table 6. Electrical characteristics

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Supply section							
I_{IN}	Operating current	S3, S5, MODE and DDRSEL connected to AVCC, No Load on VTT and VTTREF outputs. VCC connected to AVCC			0.8	2	mA
I_{STR}	Operating current in STR	S5, MODE and DDRSEL connected to AVCC, S3 tied to SGND, No Load on VTTREF. VCC connected to AVCC			0.6	1	
I_{SH}	Operating current in shutdown	S3 and S5 tied to SGND. Discharge mode active. VCC connected to AVCC			1	10	µA
UVLO	AVCC under voltage lockout upper threshold			4.1	4.25	4.4	V
	AVCC under voltage lockout lower threshold			3.85	4.0	4.1	
	UVLO hysteresis			70			mV
ON-time (SMPS)							
t_{ON}	On-time duration	MODE and DDRSEL high, V_{VSNS} = 2 V	VOSC = 300 mV	650	750	850	ns
			VOSC = 500 mV	390	450	510	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum off time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5 V < V_{IN} < 36 V		1.224	1.237	1.249	V
	Load regulation	-50 µA< I_{VREF} < 50 µA		-4		4	mV
	Undervoltage lockout fault threshold				800		
VDDQ output							

a. Specifications referred to $T_J = T_A$. All the parameters at operating temperatures extremes are guaranteed by design and statistical correlation (not production tested)

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{VDDQ}	DDR3 VDDQ output voltage	MODE connected to AVCC, DDRSEL tied to SGND, no load		1.5		V
	DDR2 VDDQ output voltage	MODE and DDRSEL connected to AVCC, no load		1.8		
	Feedback accuracy	MODE and DDRSEL connected to AVCC, no load	-1.5		1.5	%
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		110	120	130	µA
	Comparator offset		-6		6	mV
	Positive current limit threshold	Rsense = 1 kΩ V_{PGND} - V_{CSNS}		120		mV
	Fixed negative current limit threshold			110		mV
$V_{ZC,OFFS}$	Zero crossing comparator offset		-11	-5	1	mV
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pull-up)		1.4	2.1	
		LGATE low state (pull-down)		0.6	0.9	
UVP/OVP protections and PGOOD SIGNAL (SMPS only)						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	Power-good upper threshold		107	110	113	
	Power-good lower threshold		86	90	93	
$I_{PG,LEAK}$	PG leakeage current	PG forced to 5 V			1	µA
$V_{PG,LOW}$	PG low-level voltage	$I_{PG,SINK}$ = 4 mA		150	250	mV
Soft-start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		1.5	3	4	ms
	Soft-start current limit step			30		µA
Soft-end section						
	VDDQ discharge resistance in non-tracking discharge mode		15	25	35	Ω
	VTT discharge resistance in non-tracking discharge mode		15	25	35	

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	VTTREF discharge resistance in non-tracking discharge mode		1	1.5	2	kΩ
	VDDQ Output threshold synchronous for final tracking to non-tracking discharge transition		0.2	0.4	0.6	V
V_{TT} LDO section						
$I_{LDOIN,ON}$	LDO input bias current in full-on state	S3 = S5 = +5 V, No Load on VTT		1	10	µA
$I_{LDOIN,STR}$	LDO input bias current in suspend-to-RAM state	S3 = 0 V, S5 = +5 V, No Load on VTT			10	
$I_{LDOIN,STD}$	LDO input bias current in suspend-to-disk state	S3 = S5 = 0 V, No Load on VTT			1	
$I_{VTTSNS,BIAS}$	VTTSNS bias current	S3 = +5 V, S5 = +5 V, $V_{VTTSNS} = V_{VSNS}/2$			1	µA
$I_{VTTSNS,LEAK}$	VTTSNS leakage current	S3 = 0V, S5 = +5 V, $V_{VTTSNS} = V_{VSNS}/2$			1	
$I_{VTT,LEAK}$	VTT leakage current	S3 = 0V, S5 = +5 V, $V_{VTT} = V_{VSNS}/2$	-10		10	
V_{VTT}	LDO linear regulator output voltage (DDR2)	S3 = S5= +5 V, I_{VTT} = 0 A, MODE = DDRSEL = +5 V		0.9		V
	LDO linear regulator output voltage (DDR3)	S3 = S5= +5 V, I_{VTT} = 0 A, MODE = +5 V, DDRSEL = 0 V		0.75		
	LDO output accuracy respect to VTTREF	S3 = S5 = MODE = + 5 V, -1 mA < I_{VTT} < 1 mA	-20		20	mV
		S3 = S5 = MODE = +5 V, -1 A < I_{VTT} < 1 A	-25		25	
		S3 = S5 = MODE = +5 V, -2 A < I_{VTT} < 2 A	-35		35	
$I_{VTT,CL}$	LDO source current limit	$V_{VTT} < 1.10*(V_{VSNS}/2)$	2	2.3	3	A
		$V_{VTT} > 1.10*(V_{VSNS}/2)$	1	1.15	1.4	
	LDO sink current limit	$V_{VTT} > 0.90*(V_{VSNS}/2)$	-3	-2.3	-2	
		$V_{VTT} < 0.90*(V_{VSNS}/2)$	-1.4	-1.15	-1	
VTTREF section						
V_{VTTREF}	VTTREF output voltage	I_{VTTREF} = 0 A, V_{VSNS} = 1.8 V		0.9		V
	VTTREF output voltage accuracy respect to VSNS/2	-15 mA < I_{VTTREF} < 15 mA, V_{VSNS} = 1.8 V	-2		2	%
I_{VTTREF}	VTTREF current limit	VTTREF = 0 or VSNS		±40		mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Power management section						
S3,S5	Turn OFF level		0.4			V
	Turn ON level				1.6	
V_{MODE}	MODE pin high level threshold		V_{AVCC} - 0.7			
	MODE pin low level threshold				V_{AVCC} - 1.3	
V_{DDRSEL}	DDRSEL pin high level threshold		V_{AVCC} - 0.8			
	DDRSEL pin middle level window		1.0		V_{AVCC} - 1.5	
	DDRSEL pin low level threshold				0.5	
V_{DSCG}	DSCG pin high level threshold		V_{AVCC} - 0.8			
	DSCG pin middle level window		1.0		2.0	
	DSCG pin low level threshold				0.5	
$I_{IN,LEAK}$	Logic inputs leakage current	S3, S5 = 5 V			10	µA
$I_{IN3,LEAK}$	Multilevel inputs leakage current	MODE, DDRSEL and DSCG = 5 V			10	µA
$I_{OSC,LEAK}$	VOSC input leakage current	VOSC = 500 mV			1	µA
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)			150		°C

1. Guaranteed by design. Not production tested

5 Typical operating characteristics

Figure 3. Efficiency vs load - 1.5 V and 1.8 V, Vin = 12 V

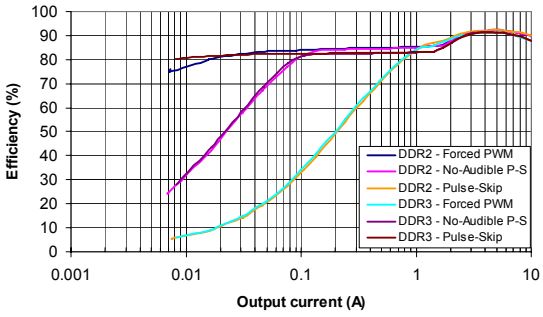


Figure 4. Switching frequency vs load - 1.8 V, Vin = 12 V

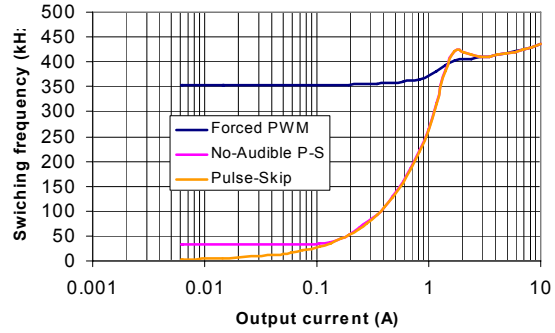


Figure 5. Switching frequency vs input voltage, 1.8 V

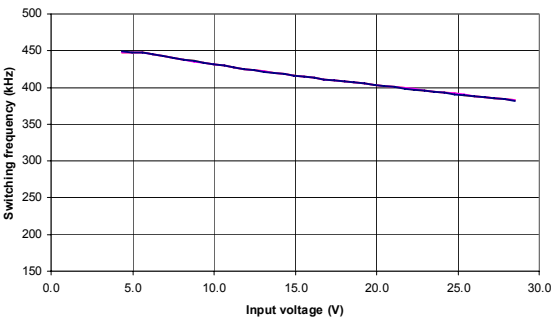


Figure 6. Switching frequency vs input voltage, 1.5 V

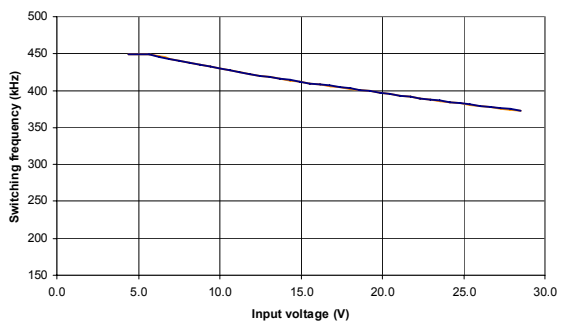


Figure 7. VDDQ line regulation, 1.8 V, 7 A

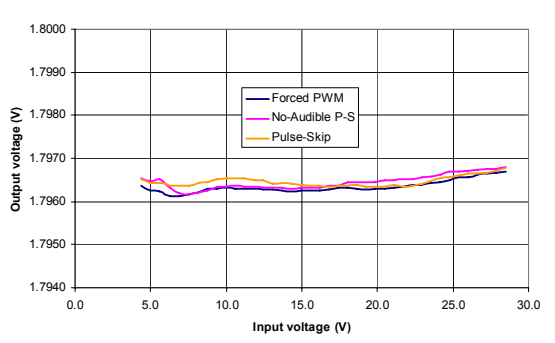


Figure 8. VDDQ line regulation, 1.5 V, 7 A

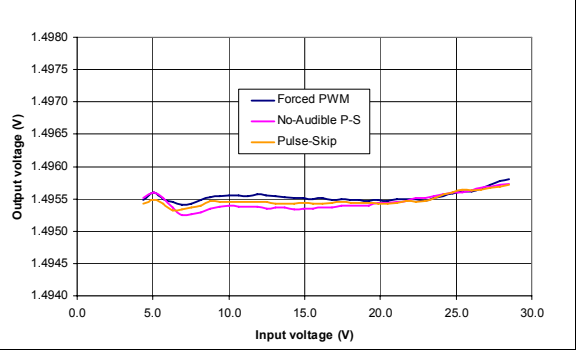


Figure 9. VDDQ load regulation, 1.8 V, Vin = 12 V

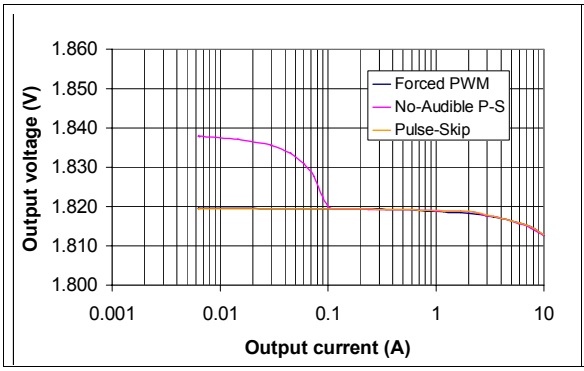


Figure 10. VDDQ load regulation, 1.5 V, Vin = 12 V

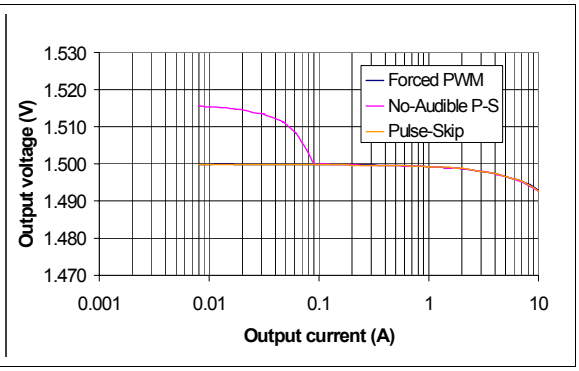


Figure 11. VTT load regulation, 0.9 V, LDOIN = 1.8 V

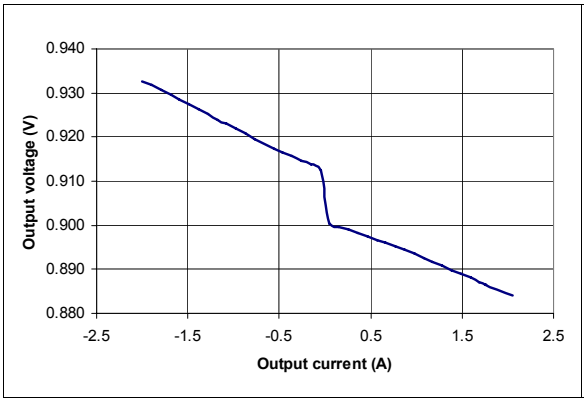


Figure 12. VTT load regulation, 0.75 V, LDOIN = 1.5 V

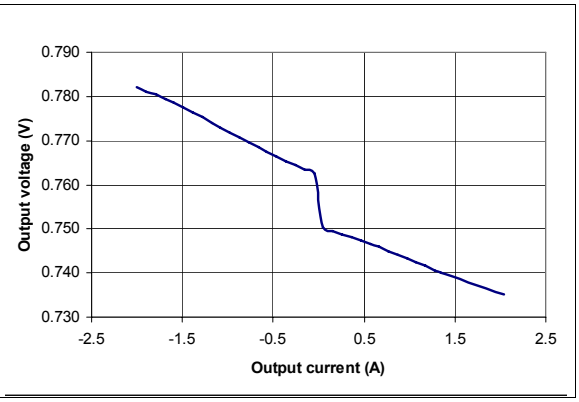


Figure 13. VTTREF load regulation, 0.9 V, VSNS = 1.8 V

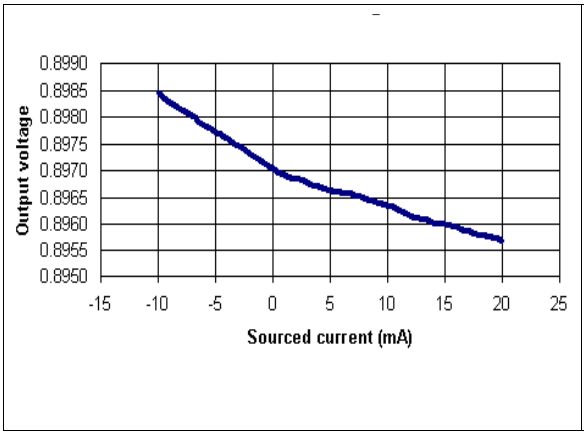


Figure 14. No-audible pulse-skip waveforms

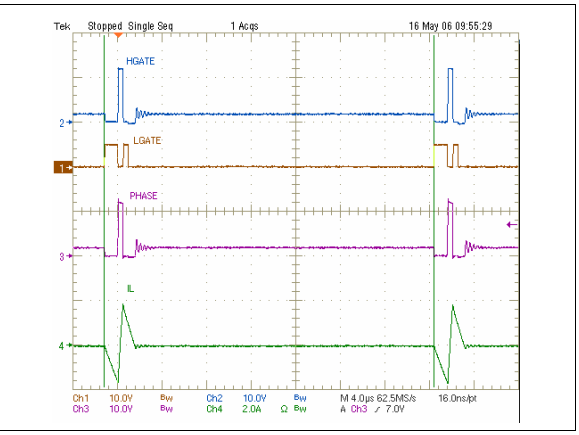


Figure 15. Power-up sequence - AVCC above UVLO

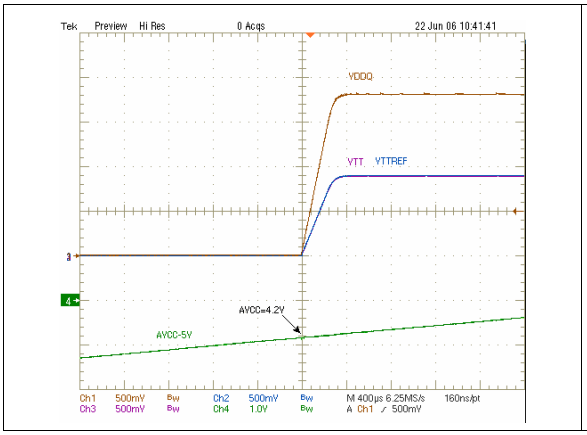


Figure 16. VDDQ soft-start, 1.8 V, heavy load

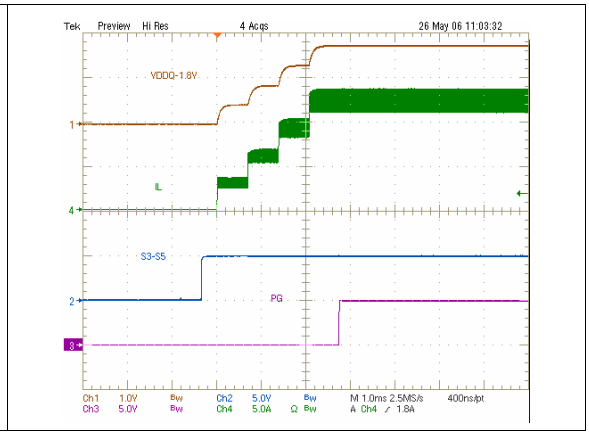


Figure 17. - 1.8 A to 1.8 A VTT load transient, 0.9 V

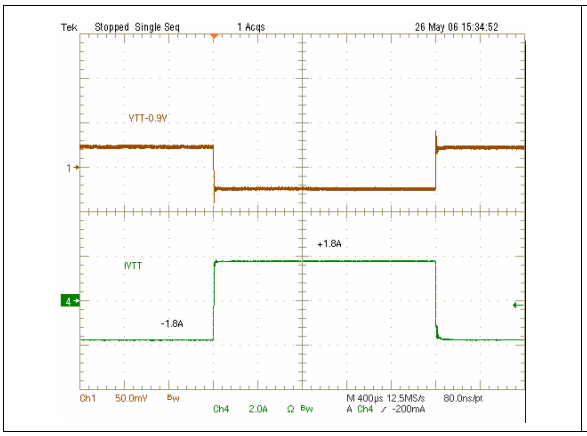


Figure 18. 0 mA to 9 mA VTTREF load transient, 0.9 V

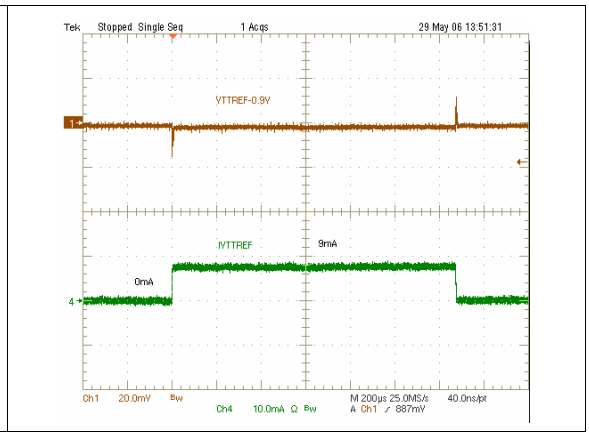


Figure 19. Non-tracking (soft) discharge

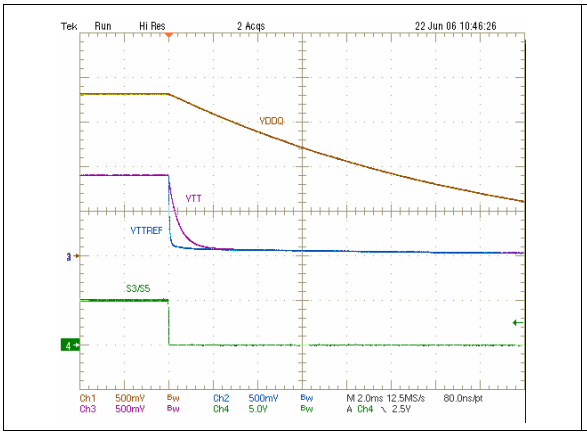


Figure 20. Tracking (fast) discharge, LDOIN = VDDQ

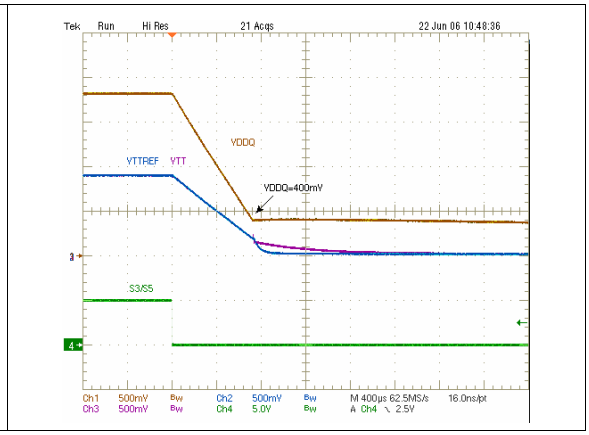


Figure 21. 0 A to 10 A VDDQ load transient, PWM

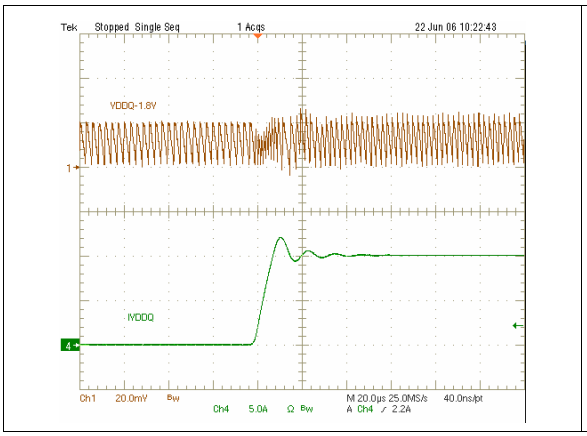


Figure 22. 10 A to 0 A VDDQ load transient, PWM

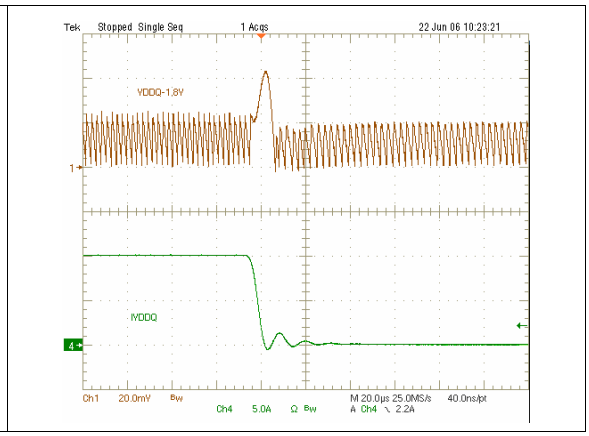


Figure 23. Over-voltage protection, VDDQ = 1.8 V

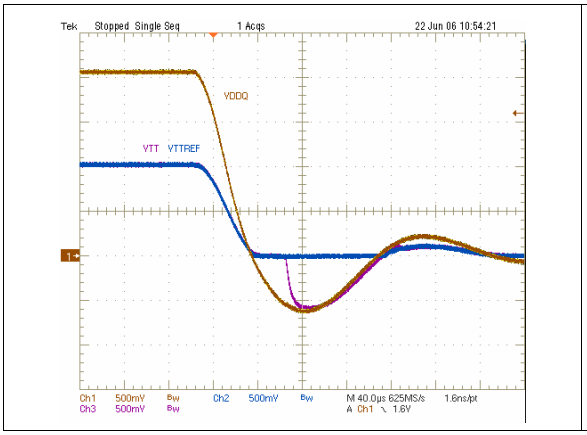
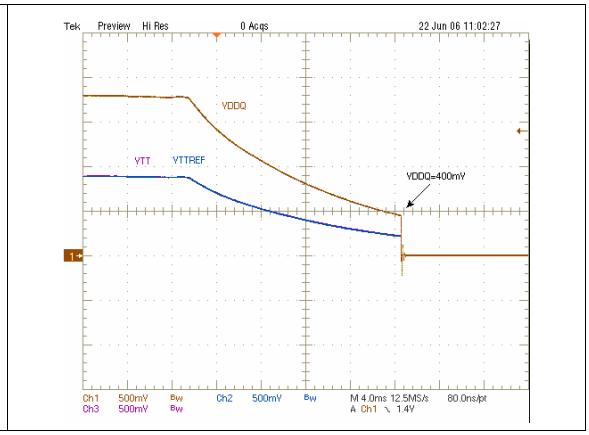


Figure 24. Under-voltage protection, VDDQ = 1.8 V



6 Block diagram

Figure 25. Functional and block diagram

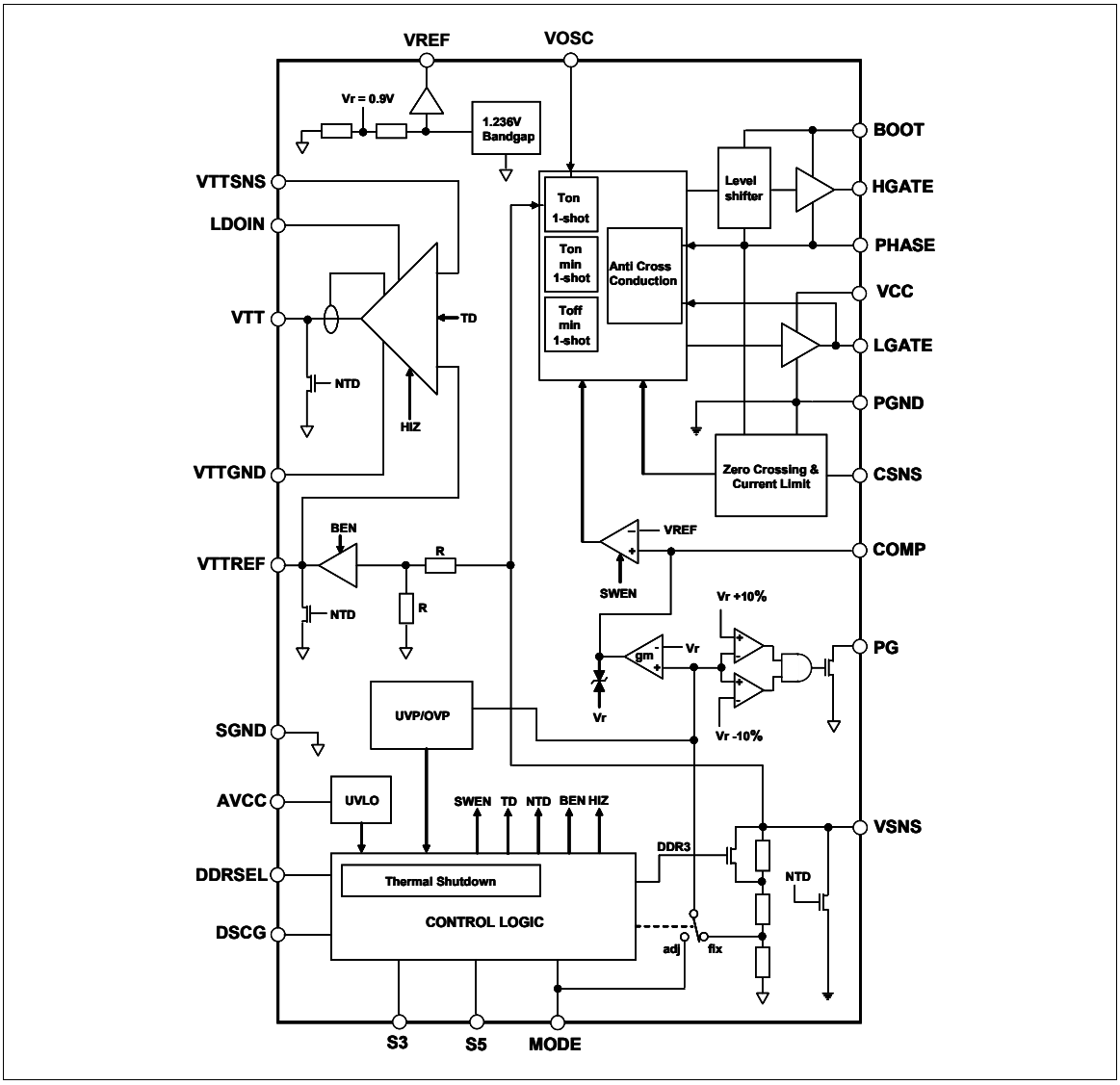


Table 7. Legend

SWEN	Switching controller enable
TD	Tracking discharge enable
NTD	Non-tracking discharge enable
BEN	VTTREF buffer enable
HIZ	LDO high impedance mode enable

7 Device description

The PM6670AS is designed to satisfy DDR2-3 power supply requirements combining a synchronous buck controller, a 15 mA buffered reference and a high-current low-drop out (LDO) linear regulator capable of sourcing and sinking up to 2 Apk. The switching controller section is a high-performance, pseudo-fixed frequency, constant-on-time (COT) based regulator specifically designed for handling fast load transient over a wide range of input voltages.

The DDR2-3 supply voltage VDDQ can be easily set to 1.8 V (DDR2) or 1.5 V (DDR3) without additional components. The output voltage can also be adjusted in the 0.9 V to 2.6 V range using an external resistor divider. The switching mode power supply (SMPS) can handle different modes of operation in order to minimize noise or power consumption, depending on the application needs.

A lossless current sensing scheme, based on the low-side MOSFET's on resistance avoids the need for an external current sense resistor.

The output of the linear regulator (VTT) tracks the memory's reference voltage VTTREF within ±30 mV over the full operating load conditions. The input of the LDO can be either VDDQ or a lower voltage rail in order to reduce the total power dissipation. Linear regulator stability is achieved by filtering its output with a ceramic capacitor (20 µF or greater).

The reference voltage (VTTREF) section provides a voltage equal to one half of VSNS with an accuracy of 1%. This regulator can source and sink up to ±15 mA. A 10 nF to 100 nF bypass capacitor is required between VTTREF and SGND for stability.

According to DDR2/3 JEDEC specifications, when the system enters the Suspend-To-RAM state the LDO output is left in high impedance while VTTREF and VDDQ are still alive. When the suspend-to-disk state (S3 and S5 tied to ground) is entered, all outputs are actively discharged when either tracking or non-tracking discharge is selected.

7.1 VDDQ section - constant on-time PWM controller

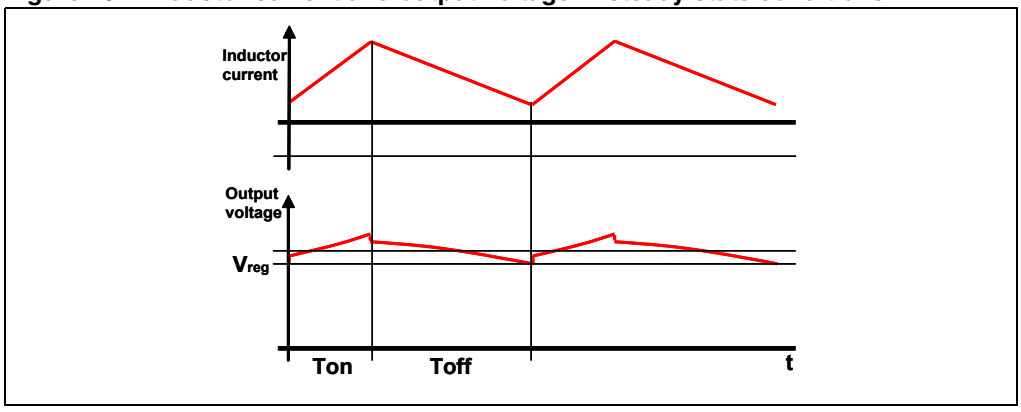
The PM6670AS uses a pseudo-fixed frequency, constant on-time (COT) controller as the core of the switching section. It is well known that the COT controller uses a relatively simple algorithm and uses the ripple voltage derived across the output capacitor's ESR to trigger the on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. Nearly constant switching frequency is achieved by the system's loop in steady-state operating conditions by varying the on-time duration, avoiding thus the need for a clock generator. The on-time one shot duration is directly proportional to the output voltage, sensed at VSNS pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows:

Equation 1

$$T_{ON} = K_{OSC} \frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130ns typ.) and τ is the internal propagation delay (40 ns typ.). The one-shot generator directly drives the high-side MOSFET at the beginning of each switching cycle allowing the inductor current to increase; after the on-time has expired, an off-time phase, in which the low-side MOSFET is turned on, follows. The off-time duration is solely determined by the output voltage: when lower than the set value (i.e. the voltage at VSNS pin is lower than the internal reference V_R = 0.9 V), the synchronous rectifier is turned off and a new cycle begins (*Figure 26*).

Figure 26. Inductor current and output voltage in steady state conditions



The duty-cycle of the buck converter is, in steady-state conditions, given by

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC}\frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 4a

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 4b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

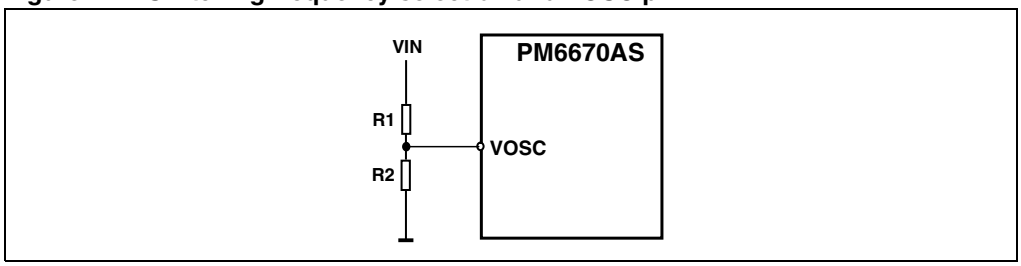
Referring to the typical application schematic (figures on cover page and *Figure 27*), the final expression is then:

Equation 5

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

Even if the switching frequency is theoretically independent from battery and output voltages, parasitic parameters involved in power path (like MOSFETs' on-resistance and inductor's DCR) introduce voltage drops responsible for slight dependence on load current. In addition, the internal delay is due to a small dependence on input voltage. The PM6670AS switching frequency can be set by an external divider connected to the VOSC pin.

Figure 27. Switching frequency selection and VOSC pin



The suggested voltage range for VOSC pin is 0.3V to 2V, for better switching frequency programmability.

7.1.1 Constant-on-time architecture

Figure 28 shows the simplified block diagram of the constant-on-time controller.

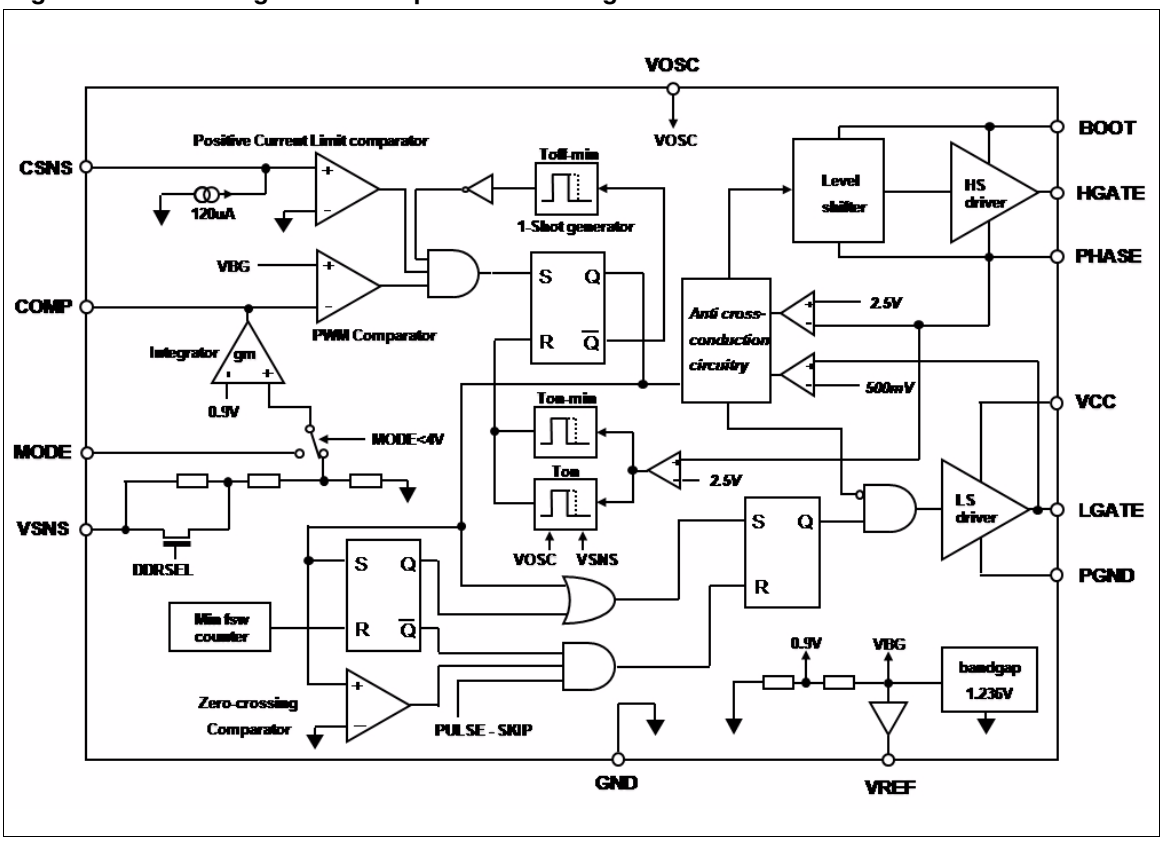
The switching regulator of the PM6670AS owns a one-shot generator that ignites the high-side MOSFET when the following conditions are simultaneously satisfied: the PWM comparator is high (i.e. output voltage is lower than Vr = 0.9 V), the synchronous rectifier current is below the current limit threshold and the minimum off-time has expired.

A minimum off-time constraint (300 ns typ.) is introduced to assure the boot capacitor charge and allow inductor valley current sensing on low-side MOSFET. A minimum on-time is also introduced to assure the start-up switching sequence.

Once the on-time has timed out, the high side switch is turned off, while the synchronous rectifier is ignited according to the anti-cross conduction management circuitry.

When the output voltage reaches the valley limit (determined by internal reference Vr = 0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 28. Switching section simplified block diagram

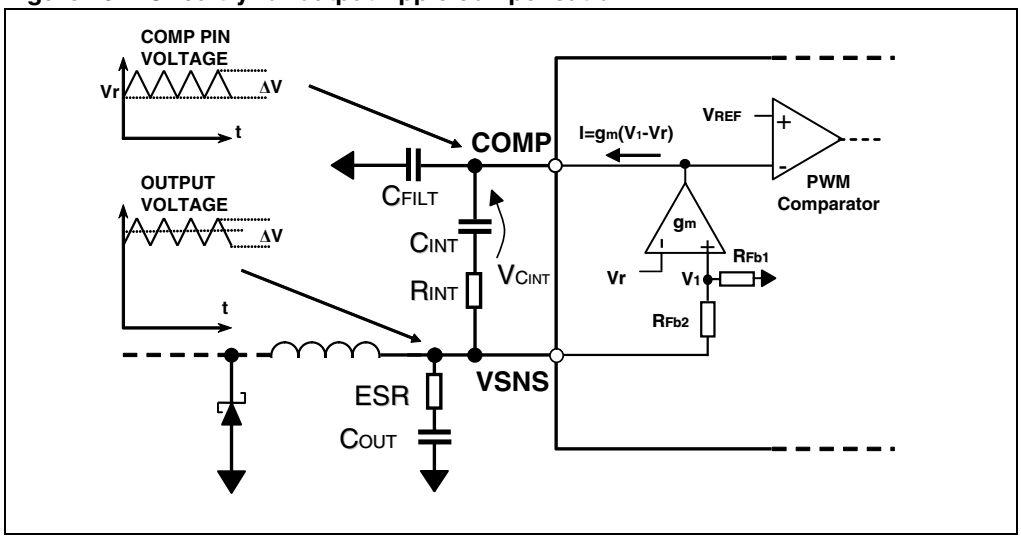


7.1.2 Output ripple compensation and loop stability

The loop is closed connecting the center tap of the output divider (internally, when the fixed output voltage is chosen, or externally, using the MODE pin in the adjustable output voltage mode). The feedback node is the negative input of the error comparator, while the positive input is internally connected to the reference voltage (Vr = 0.9 V). When the feedback voltage becomes lower than the reference voltage, the PWM comparator goes to high and sets the control logic, turning on the high-side MOSFET. After the On-Time (calculated as previously described) the system releases the high-side MOSFET and turns on the synchronous rectifier.

The voltage drop along ground and supply PCB paths, used to connect the output capacitor to the load, is a source of DC error. Furthermore the system regulates the output voltage valley, not the average, as shown in *Figure 26*. Thus, the voltage ripple on the output capacitor is an additional source of DC error. To compensate this error, an integrative network is introduced in the control loop, by connecting the output voltage to the COMP pin through a capacitor (C_{INT}) as shown in *Figure 29*.

Figure 29. Circuitry for output ripple compensation



The additional capacitor is used to reduce the voltage on the COMP pin when higher than 300 mVpp and is unnecessary for most of applications. The trans conductance amplifier (gm) generates a current, proportional to the DC error, used to charge the CINT capacitor. The voltage across the CINT capacitor feeds the negative input of the PWM comparator, forcing the loop to compensate the total static error. An internal voltage clamp forces the COMP pin voltage range to ±150 mV with respect to VREF. This is useful to avoid or smooth output voltage overshoot during a load transient. When the pulse-skip mode is entered, the clamping range is automatically reduced to 60mV in order to enhance the recovering capability. In the ripple amplitude is larger than 150 mV, an additional capacitor CFILT can be connected between the COMP pin and ground to reduce ripple amplitude, otherwise the integrator will operate out of its linearity range. This capacitor is unnecessary for most of applications and can be omitted.

The design of the external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 20mV, the correct CINT capacitor is usually enough to keep the loop stable. The stability of the system depends firstly on the output capacitor zero frequency.

The following condition must be satisfied:

Equation 6

$$f_{SW} > k \cdot f_{Zout} = \frac{k}{2\pi \cdot C_{out} \cdot ESR}$$

where k is a fixed design parameter (k > 3). It determines the minimum integrator capacitor value:

Equation 7

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout}\right)} \cdot \frac{Vr}{Vout}$$

where gm = 50 µs is the integrator trans conductance.

In order to ensure stability it must be also verified that:

Equation 8

$$C_{INT} > \frac{g_m}{2\pi \cdot f_{Zout}} \cdot \frac{Vr}{V_{OUT}}$$

If the ripple on the COMP pin is greater than the integrator 150 mV, the auxiliary capacitor C_{FILT} can be added. If q is the desired attenuation factor of the output ripple, C_{FILT} is given by:

Equation 9

$$C_{FILT} = \frac{C_{INT} \cdot (1-q)}{q}$$

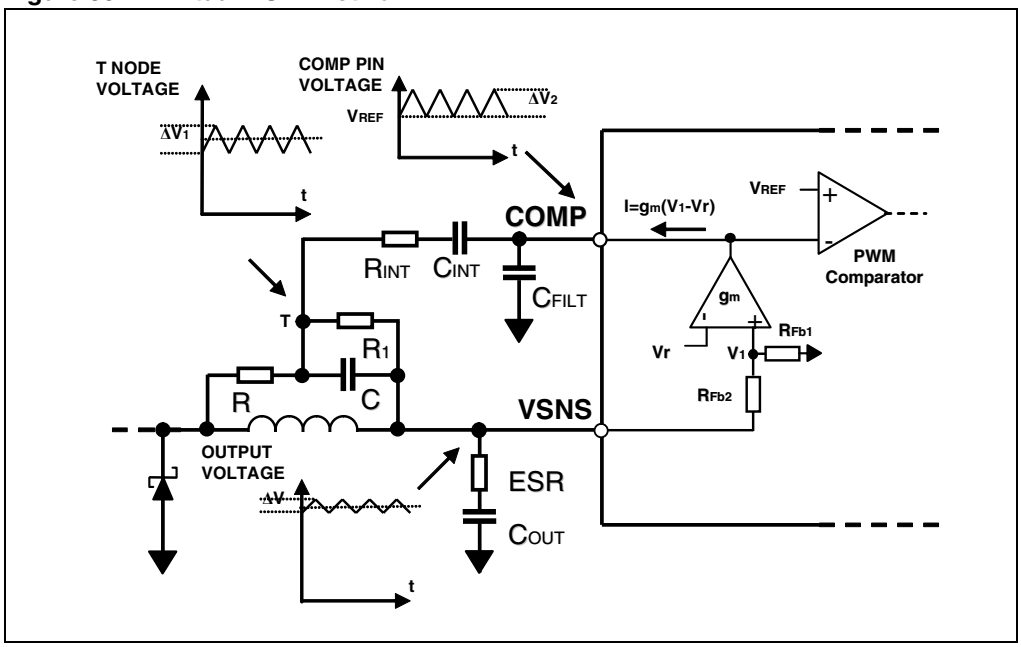
In order to reduce the noise on the COMP pin, it is possible to add a resistor R_{INT} that, together with CINT and C_{FILT}, becomes a low pass filter. The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency:

Equation 10

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \cdot \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

If the ripple is very small (lower than approximately 20 mV), a different compensation network, called “Virtual-ESR” Network, is needed. This additional circuit generates a triangular ripple that is added to the output voltage ripple at the input of the integrator. The complete control scheme is shown in *Figure 30*.

Figure 30. "Virtual-ESR" Network



The ripple on the COMP pin is the sum of the output voltage ripple and the triangular ripple generated by the Virtual-ESR Network. In fact the Virtual-ESR Network behaves like a another equivalent series resistor R_{VESR}.

A good trade-off is to design the network in order to achieve an RVESR given by:

Equation 11

$$R_{VESR} = \frac{V_{RIPPLE}}{\Delta I_L} - ESR$$

where ΔI_L is the inductor current ripple and V_{RIPPLE} is the total ripple at the T node, chosen greater than approximately 20 mV.

The new closed-loop gain depends on C_{INT}. In order to ensure stability it must be verified that:

Equation 12

$$C_{INT} > \frac{g_m}{2\pi \cdot f_Z} \cdot \frac{Vr}{Vout}$$

where:

Equation 13

$$f_Z = \frac{1}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

and:

Equation 14

$$R_{TOT} = ESR + R_{VESR}$$

Moreover, the C_{INT} capacitor must meet the following condition:

Equation 15

$$f_{SW} > k \cdot f_Z = \frac{k}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

where R_{TOT} is the sum of the ESR of the output capacitor and the equivalent ESR given by the Virtual-ESR Network (R_{VESR}). The k parameter must be greater than unity (k > 3) and determines the minimum integrator capacitor value C_{INT}:

Equation 16

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_Z\right)} \cdot \frac{Vr}{Vout}$$

The capacitor of the Virtual-ESR Network, C, is chosen as follows:

Equation 17

$$C > 5 \cdot C_{INT}$$

and R is calculated to provide the desired triangular ripple voltage:

Equation 18

$$R = \frac{L}{R_{VESR} \cdot C}$$

Finally the R1 resistor is calculated according to expression 19:

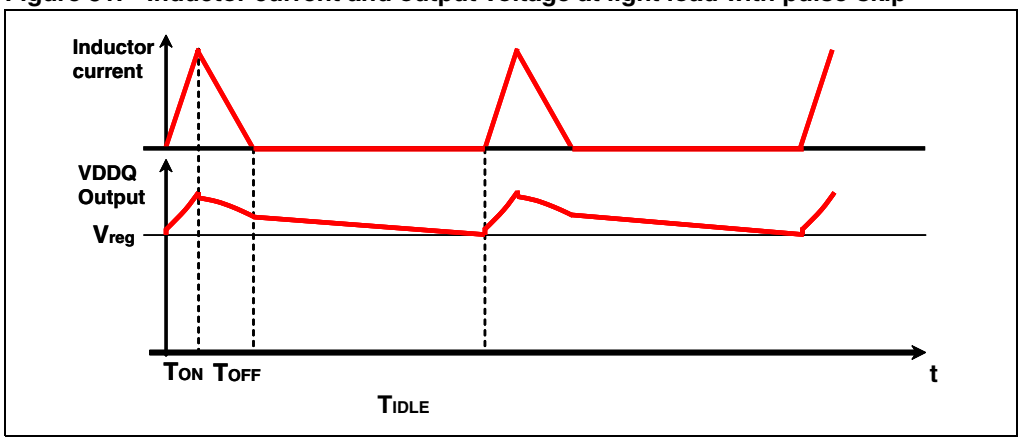
Equation 19

$$R1 = \frac{R \cdot \left(\frac{1}{C \cdot \pi \cdot f_Z}\right)}{R - \frac{1}{C \cdot \pi \cdot f_Z}}$$

7.1.3 Pulse-skip and no-audible pulse-skip modes

High efficiency at light load conditions is achieved by PM6670AS entering the pulse-skip mode (if enabled). When one of the two fixed output voltages is set, pulse-skip power saving is a default feature. At light load conditions the zero-crossing comparator truncates the low-side switch on-time as soon as the inductor current becomes negative; in this way the comparator determines the on-time duration instead of the output ripple (see *Figure 31*).

Figure 31. Inductor current and output voltage at light load with pulse-skip



As a consequence, the output capacitor is left floating and its discharge depends solely on the current drained from the load. When the output ripple on the pin COMP falls under the reference, a new shot is triggered and the next cycle begins. The pulse-skip mode is naturally obtained enabling the zero-crossing comparator and automatically takes part in the COT algorithm when the inductor current is about half the ripple current amount, i.e. migrating from continuous conduction mode (C.C.M.) to discontinuous conduction mode (D.C.M.).

The output current threshold related to the transition between PWM mode and pulse-skip mode can be approximately calculated as:

Equation 20

$$I_{LOAD}(PWM2Skip) = \frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}$$

At higher loads, the inductor current never crosses zero and the device works in pure PWM mode with a switching frequency around the nominal value.

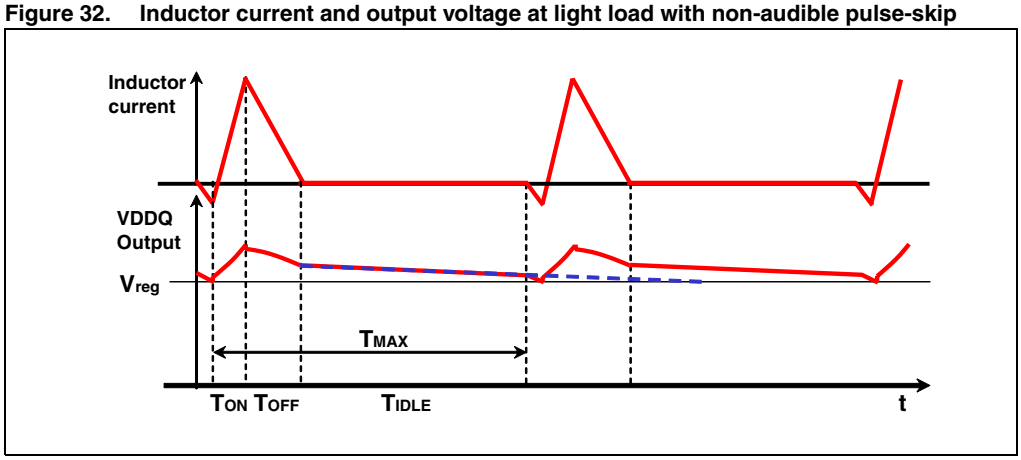
A physiological consequence of pulse-skip mode is a more noisy and asynchronous (than normal conditions) output, mainly due to very low load. If the pulse-skip is not compatible with the application, the PM6670AS, when set in adjustable mode-of-operation, allows the user to choose between forced-PWM and no-audible pulse-skip alternative modes (see 4.1.4 for details).

No-audible pulse-skip mode

Some audio-noise sensitive applications cannot accept the switching frequency to enter the audible range as is possible in pulse-skip mode with very light loads. For this reason, the PM6670AS implements an additional feature to maintain a minimum switching frequency of 33 kHz despite a slight efficiency loss. At very light load conditions, if any switching cycle

has taken place within 30 µs (typ.) since the last one (because the output voltage is still higher than the reference), a no-audible pulse-skip cycle begins. The low-side MOSFET is turned on and the output is driven to fall until the reference has been crossed. Then, the high-side switch is turned on for a T_{ON} period and, once it has expired, the synchronous rectifier is enabled until the inductor current reaches the zero-crossing threshold (see *Figure 32*).

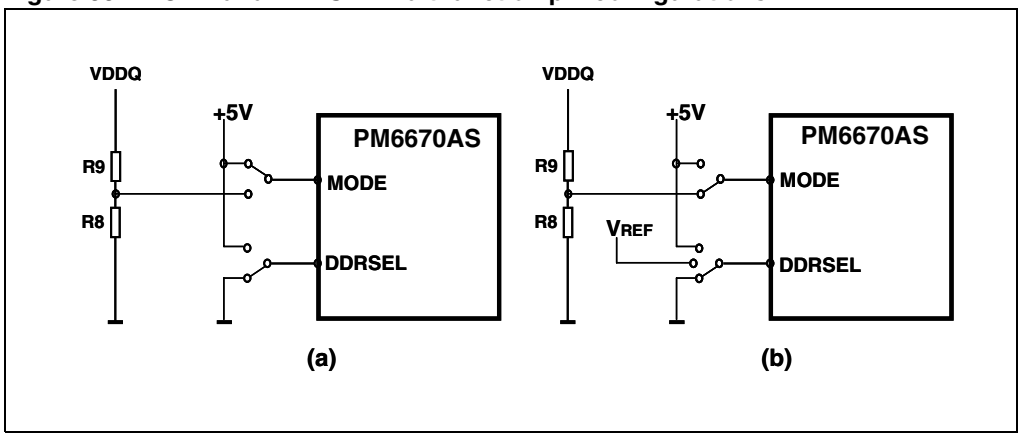
Figure 32. Inductor current and output voltage at light load with non-audible pulse-skip



For frequencies higher than 33 kHz (due to heavier loads) the device works in the same way as in Pulse-Skip mode. It is important to notice that in both Pulse-Skip and No-Audible Pulse-Skip modes the switching frequency changes not only with the load but also with the input voltage.

7.1.4 Mode-of-operation selection

Figure 33. MODE and DDRSEL multifunction pin configurations



The PM6670AS has been designed to satisfy the widest range of applications involving DDR2/3 memories, SSTL15-18 buses termination and I/O supplies for CPU/Chipset. The device is provided with multilevel pins which allow the user to choose the appropriate configuration. The MODE pin is used to firstly decide between fixed preset or adjustable (user defined) output voltages.

When the MODE pin is connected to +5 V, the PM6670AS allows setting the VDDQ voltage to 1.8 V or 1.5 V just forcing the DDRSEL multilevel pin to +5 V or to ground respectively (see *Figure 33*a).

In this condition the pulse-skip feature is enabled. This device configuration is suitable for standard DDR2/3 memory supply applications avoiding the need for an external, high accuracy, divider for output voltage setting.

Applications requiring different output voltages can be managed by PM6670AS simply setting the adjustable mode. If MODE pin voltage is higher than 4 V, the fixed output mode is selected. Connecting an external divider to the MODE pin (*Figure 33*b), it is used as negative input of the error amplifier and the output voltage is given by expression (21).

Equation 21

$$VDDQ_{ADJ} = 0.9 \cdot \frac{R8 + R9}{R8}$$

VDDQ output voltage can be set in the range from 0.9 V to 2.6 V. Adjustable mode automatically switches DDRSEL pin to become the power saving algorithm selector: if tied to +5 V, the forced-PWM (fixed frequency) control is performed. If grounded or connected to VREF pin (1.237 V reference voltage), the pulse-skip or non-audible pulse-skip modes are respectively selected.

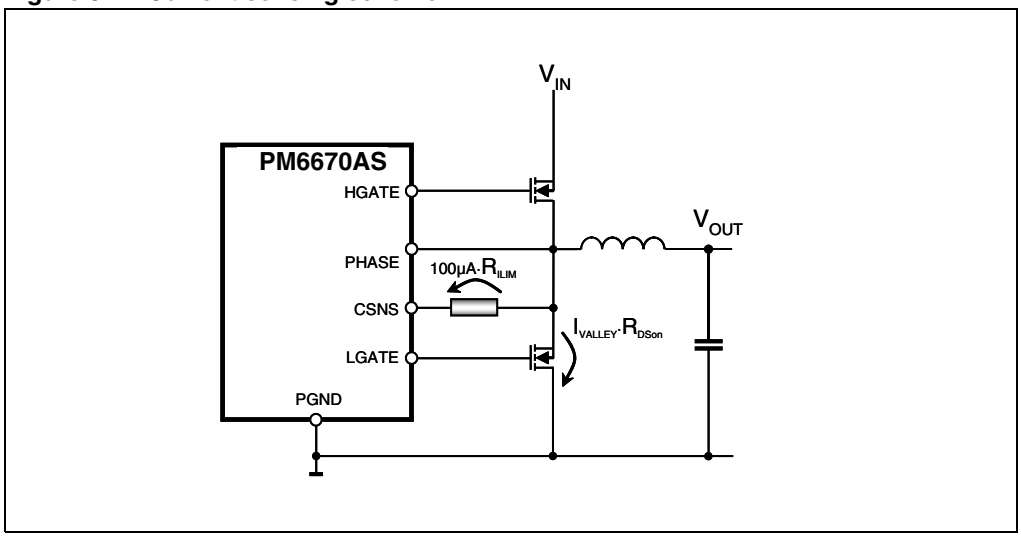
Table 8. Mode-of-operation settings summary

Mode	DDRSEL	VDDQ	Operating mode
V_{MODE} > 4.3 V	V_{DDRSEL} > 4.2 V	1.8 V	Pulse-Skip
	1 V < V_{DDRSEL} < 3.5 V	1.5 V	
	<0.5 V		
V_{MODE} < 3.7 V	V_{DDRSEL} > 4.2 V	ADJ	Forced-PWM
	1V < V_{DDRSEL} < 3.5 V		Non-Audible Pulse-skip
	V_{DDRSEL} < 0.5 V		Pulse-Skip

7.1.5 Current sensing and current limit

The PM6670AS switching controller uses a valley current sensing algorithm to properly handle the current limit protection and the inductor current zero-crossing information. The current is sensed during the conduction time of the low-side MOSFET. The current sensing element is the on-resistance of the low-side switch. The sensing scheme is visible in *Figure 34*.

Figure 34. Current sensing scheme



An internal 120 µA current source is connected to C_{SNS} pin that is also the non-inverting input of the positive current limit comparator. When the voltage drop developed across the sensing parameter equals the voltage drop across the programming resistor R_{ILIM}, the controller skips subsequent cycles until the overcurrent condition is detected or the output UV protection latches off the device (see *Section 7.1.11: Over voltage and under voltage protections on page 35*).

Referring to *Figure 34*, the RDSon sensing technique allows high efficiency performance without the need for an external sensing resistor. The on-resistance of the MOSFET is affected by temperature drift and nominal value spread of the parameter itself; this must be considered during the R_{ILIM} setting resistor design.

It must be taken into account that the current limit circuit actually regulates the inductor valley current. This means that R_{ILIM} must be calculated to set a limit threshold given by the maximum DC output current plus half of the inductor ripple current:

Equation 22

$$I_{CL} = 120\mu A \cdot \frac{R_{ILIM}}{R_{DSon}}$$

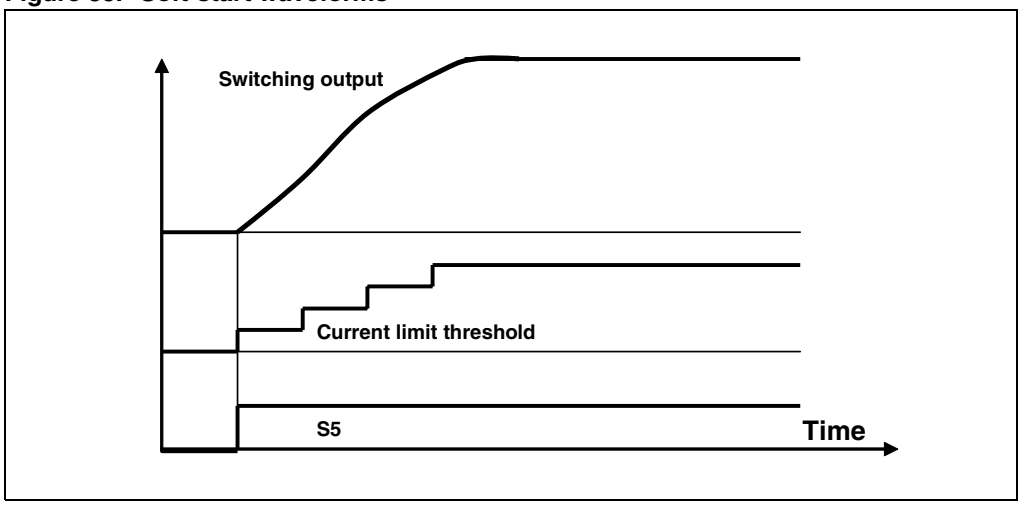
The PM6670AS provides also a fixed negative current limit to prevent excessive reverse inductor current when the switching section sinks current from the load in forced-PWM (3rd quadrant working conditions). This negative current limit threshold is measured between PHASE and PGND pins, comparing the drop magnitude on PHASE pin with an internal 120 mV fixed threshold.

7.1.6 POR, UVLO and soft-start

The PM6670AS automatically performs an internal startup sequence during the rising phase of the analog supply of the device (AVCC). The switching controller remains in a stand-by state until AVCC crosses the upper UVLO threshold (4.2 V typ.), keeping active the internal discharge MOSFETs (only if AVCC > 1 V).

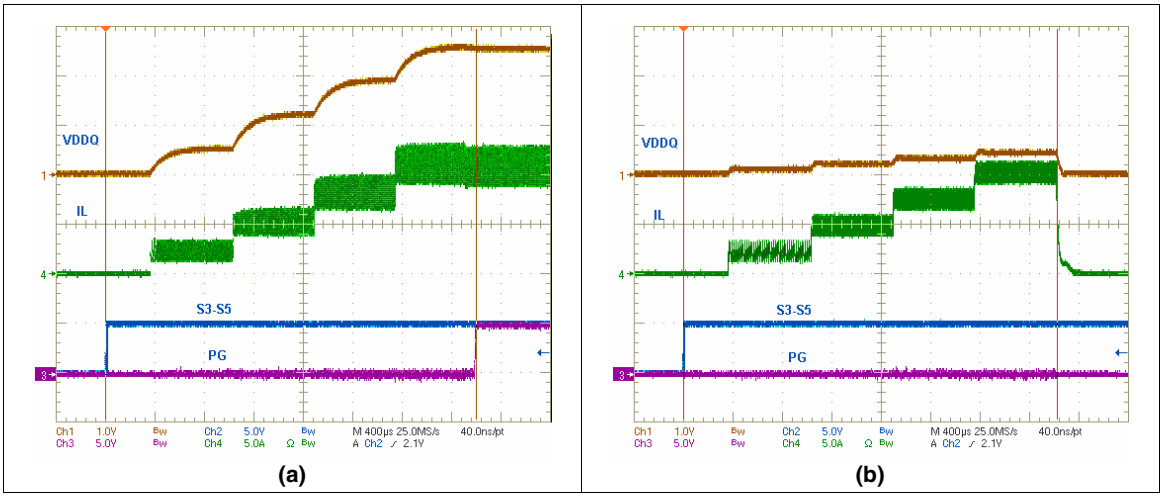
The soft-start allows a gradual increase of the internal current limit threshold during start-up reducing the input/output surge currents. At the beginning of start-up, the PM6670AS current limit is set to 25% of nominal value and the under voltage protection is disabled. Then, the current limit threshold is sequentially brought to 100% in four steps of approximately 750 µs (*Figure 35*).

Figure 35. Soft-start waveforms



After a fixed 3 ms total time, the soft-start finishes and UVP is released: if the output voltage doesn't reach the Power-Good lower threshold within soft-start duration, the UVP condition is detected and the device performs a soft end and latches off. Depending on the load conditions, the inductor current may or may not reach the nominal value of the current limit during the soft-start (*Figure 36* shows two examples).

Figure 36. Soft-start at heavy load (a) and short-circuit (b) conditions, pulse-skip enabled



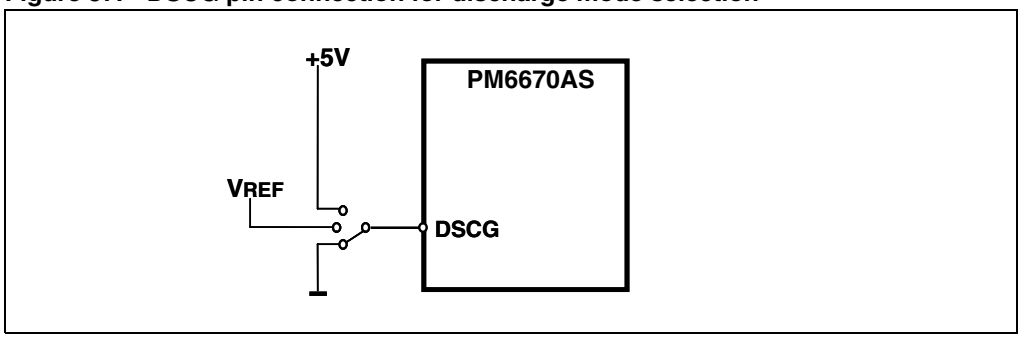
7.1.7 Power-Good signal

The PG pin is an open drain output used to monitor output voltage through VSNS (in fixed output voltage mode) or MODE (in adjustable output voltage mode) pins and is enabled after the soft-start timer has expired. PG signal is held low if the VDDQ output voltage drops 10% below or rises 10% above the nominal regulated value. The PG output can sink current up to 4 mA.

7.1.8 VDDQ output discharge

Active discharge of VDDQ output occurs when PM6670AS enters the suspend-to-disk system state (S3 and S5 tied to GND) and DSCG pin has been properly set.

Figure 37. DSCG pin connection for discharge mode selection



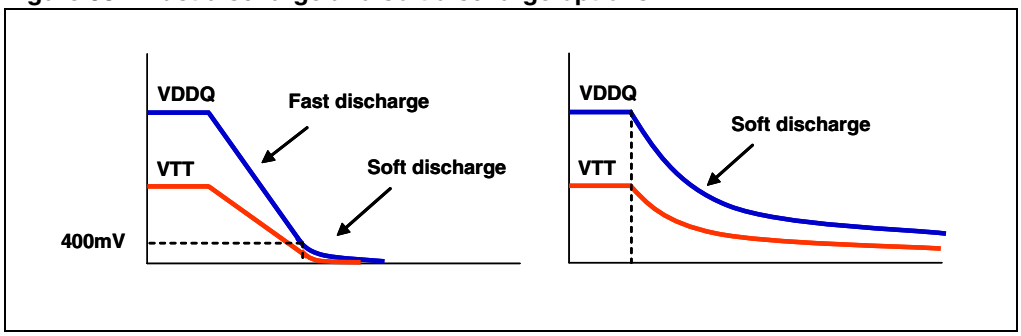
The PM6670AS allows the user to choose between fast discharge (tracking discharge), soft discharge (non-tracking discharge) or no discharge modes. Voltage on DSCG multilevel pin determines discharge mode as shown in *Table 2 on page 6*.

Table 9. Discharge mode selection

DSCG voltage	Soft-end type	Description
VDSCG >4.2V	No discharge	All outputs left floating.
1V< VDSCG <3.5V	Fast (tracking)	VDDQ and VTT actively discharged by LDO trough LDOIN and VTT pins;
VDSCG <0.5V	Soft (non-tracking)	All outputs discharged by dedicated internal MOS.

Tracking discharge allows the fastest discharge of all outputs but requires the LDOIN to be self-supplied from VDDQ output voltage. When an external supply rail is connected to LDOIN, it must be taken into account to avoid damage to the device. Discharge current (1 A) flows through the LDOIN pin until the output has reached approximately 400 mV and then a soft discharge completes the process by discharging the output with an internal 22 Ω switch.

Figure 38. Fast discharge and soft discharge options



7.1.9 Gate drivers

The integrated high-current gate drivers allow using different power MOSFETs. The high-side driver uses a bootstrap circuit which is supplied by the +5 V rail. The BOOT and PHASE pins work respectively as supply and return path for the high-side driver, while the low-side driver is directly fed through VCC and PGND pins.

An important feature of the PM6670AS gate drivers is the adaptive anti-cross-conduction circuitry, which prevents high-side and low-side MOSFETs from being turned on at the same time. When the high-side MOSFET is turned off, the voltage at the PHASE node begins to fall. The low-side MOSFET is turned on only when the voltage at the PHASE node reaches an internal threshold (2.5 V typ.). Similarly, when the low-side MOSFET is turned off, the high-side one remains off until the LGATE pin voltage is above 1 V.

The power dissipation of the drivers is a function of the total gate charge of the external power MOSFETs and the switching frequency, as shown in the following equation:

Equation 23

$$P_D(\text{driver}) = V_{DRV} \cdot Q_g \cdot f_{SW}$$

The low-side driver has been designed to have a low-resistance pull-down transistor (0.6 Ω typ.) in order to prevent undesired ignition of the low-side MOSFET due to the Miller effect.

7.1.10 Reference voltage and bandgap

The 1.237 V internal bandgap reference has a granted accuracy of ±1% over the 0 °C to 85 °C temperature range. The VREF pin is a buffered replica of the bandgap voltage. It can supply up to ±100 µA and is suitable to set the intermediate level of MODE, DDRSEL and DSCG multifunction pins. A 100 nF (min.) bypass capacitor toward SGND is required to enhance noise rejection. If VREF falls below 0.87 V (typ.), the system detects a fault condition and all the circuitry is turned OFF.

An internal divider derives a 0.9 V±1% voltage (Vr) from the bandgap. This voltage is used as a reference by the switching regulator output. The over-voltage protection, the under-voltage protection and the Power-Good signal are also referred to Vr.

7.1.11 Over voltage and under voltage protections

When the switching output voltage is about 115% of its nominal value, a latched over-voltage protection (OVP) occurs. In this case the synchronous rectifier immediately turns on while the high-side MOSFET turns OFF. The output capacitor is rapidly discharged and the load is preserved from being damaged. The OVP is also active during the soft-start. Once an OVP has occurred, a toggle on S5 pin or a power-on-reset is necessary to exit from the latched state.

When the switching output voltage is below 70% of its nominal value, a latched under-voltage protection occurs. This event causes the switching section to be immediately disabled and both switches to be opened. The controller enters in soft-end mode and the output is eventually kept to ground, turning the low side MOSFET on when the voltage is lower than 400 mV. If S3 and S5 are forced low, the low-side MOSFET is released and only the 22 Ω switch is active.

The under-voltage protection circuit is enabled only at the end of the soft-start. Once an UVP has occurred, a toggle on S5 pin or a power-on-reset is necessary to clear the fault state and restart the device.

7.1.12 Device thermal protection

The internal control circuitry of the PM6670AS self-monitors the junction temperature and turns all outputs off when the 150 °C limit has been overrun. This event causes the switching section to be immediately disabled and both switches to be opened. The controller enters in soft-end Mode and the output is eventually kept to ground, turning the low side MOSFET on when the voltage is lower than 400 mV. If S3 and S5 are forced low, the low-side switch is released and only the 22 Ω discharge MOSFET is active.

The thermal fault is a latched protection and normal operating condition is restored by a power-on reset or toggling S5.

Table 10. OV, UV and OT faults management

Fault	Conditions	Action
VDDQ over voltage	VDDQ > 115% of the nominal value	LGATE pin is forced high and the device latches off. Exit by a power-on reset or toggling S5
VDDQ under voltage	VDDQ < 70% of the nominal value	LGATE pin is forced high after the soft-end, then the device latches off. Exit by a power-on reset or toggling S5.
Junction over temperature	T_J > +150 °C	LGATE pin is forced high after the soft-end, then the device latches off. Exit by a power-on reset or toggling S5 after 15°C temperature drop.

7.2 VTTREF buffered reference and VTT LDO section

The PM6670AS provides the required DDR2/3 reference voltage on the VTTREF pin. The internal buffer tracks half the voltage on the VSNS pin and has a sink and source capability up to 15 mA.

Higher currents rapidly deteriorate the output accuracy. A 10 nF to 100 nF (33 nF typ.) bypass capacitor to SGND is required for stability.

The VTT low-drop-out linear regulator has been designed to sink and source up to 2 A peak current and 1 A continuously. The VTT voltage tracks VTTREF within ±35 mV.

A remote voltage sensing pin (VTTSNS) is provided to recovery voltage drops due to parasitic resistance. In DDR2/3 applications, the linear regulator input LDOIN is typically connected to VDDQ output; connecting LDOIN pin to a lower voltage, if available in the system, reduces the power dissipation of the LDO.

A minimum output capacitance of 20 µF (2x10 µF MLCC capacitors) is enough to assure stability and fast load transient response.

7.2.1 VTT and VTTREF soft-start

Soft-start on VTT and VTTREF outputs is achieved by current clamping.

The LDO linear regulator is provided with a current foldback protection: when the output voltage exits the internal ±10% VTT-Good window, the output current is clamped at ±1 A. Re-entering VTT-Good window releases the current limit clamping.

The foldback mechanism naturally implements a two steps soft-start charging the output capacitors with a 1 A constant current.

Something similar occurs at VTTREF pin, where the output capacitor is smoothly charged at a fixed 40 mA current limit.

7.2.2 VTTREF and VTT outputs discharge

The tracking discharge mechanism involves the VTT linear regulator. When the suspend-to-disk state is entered, the switching regulator is turned OFF.

At the same time the LDO drains a 1A constant current from LDOIN and keeps VTT in track with VTTREF that, in turn, is half the voltage at the VSNS pin. When the VDDQ output reaches 400mV, the PM6670AS switches on the internal discharge MOSFETs to complete the process (see *Section 7.1.8: VDDQ output discharge on page 33*).

In Soft Discharge (i.e. non-tracking discharge) the PM6670AS disables the internal regulators and suddenly turns on the discharge MOSFETs on each output.

7.3 S3 and S5 power management pins

According to DDR2/3 memories supply requirements, the PM6670AS can manage all S0 to S5 system states by connecting S3-S5 pins to their respective sleep-mode signals in the notebook's motherboard.

Keeping S3 and S5 high, the S0 (Full-On) state is decoded and the outputs are alive.

In S3 state (S5 = 1, S3 = 0), the PM6670AS maintains VDDQ and VTTREF outputs active and VTT output in high-impedance as needed.

In S4/S5 states (S5 = S3 = 0) all outputs are turned off and, according to DSCG pin voltage, the proper soft-end is performed.

Table 11. S3 and S5 Sleep-states decoding

S3	S5	System State	VDDQ	VTTREF	VTT
1	1	S0 (Full-On)	On	On	On
0	1	S3 (Suspend-To-RAM)	On	On	Off (Hi-Z)
0	0	S4/S5 (Suspend-To-Disk)	Off (Discharge)	Off (Discharge)	Off (Discharge)

8 Application information

The purpose of this chapter is to show the design procedure of the switching section.

The design starts from three main specifications:

- The input voltage range, provided by the battery or the AC adapter. The two extreme values (V_{INMAX} and V_{INmin}) are important for the design.
- The maximum load current, indicated by $I_{LOAD,MAX}$.
- The maximum allowed output voltage ripple $V_{RIPPLE,MAX}$.

It's also possible that specific designs should involve other specifications.

The following paragraphs will guide the user into a step-by-step design.

8.1 External components selection

The PM6670AS uses a pseudo-fixed frequency, constant on-time (COT) controller as the core of the switching section. The switching frequency can be set by connecting an external divider to the VOSC pin. The voltage seen at this pin must be greater than 0.8 V and lower than 2 V in order to ensure system's linearity.

Nearly constant switching frequency is achieved by the system's loop in steady-state operating conditions by varying the on-time duration, avoiding thus the need for a clock generator. The on-time one shot duration is directly proportional to the output voltage, sensed at VSNS pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows:

Equation 24

$$T_{ON} = K_{OSC} \frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130 ns typ.) and τ is the internal propagation delay (40 ns typ.).

The duty cycle of the buck converter is, under steady state conditions, given by

Equation 25

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 26

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC} \cdot \frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 27a

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 27b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

Referring to the typical application schematic (figure in cover page and *Figure 27*), the final expression is then:

Equation 28

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

The switching frequency directly affects two parameters:

- Inductor size: greater frequencies mean smaller inductances. In most of the applications, real estate solutions (i.e. low-profile power inductors) are mandatory also with high saturation and r.m.s. currents.
- Efficiency: switching losses are proportional to the frequency. Generally, higher frequencies imply lower efficiency.

Even if the switching frequency is theoretically independent from input and output voltages, parasitic parameters involved in power path (like MOSFETs' on-resistance and inductor's DCR) introduce voltage drops responsible for a slight dependence on load current.

In addition, the internal delay is due to a light dependence on input voltage.

Table 12. Typical values for switching frequency selection

R1 (kΩ)	R2 (kΩ)	Approx switching frequency (kHz)
330	11	250
330	13	300
330	15	350
330	18	400
330	20	450
330	22	500

8.1.1 Inductor selection

Once the switching frequency has been defined, the inductance value depends on the desired inductor ripple current. Low inductance value means great ripple current that brings poor efficiency and great output noise. On the other hand a great current ripple is desirable for fast transient response when a load step is applied.

High inductance brings higher efficiency, but the transient response is critical, especially if V_{INmin} - V_{OUT} is small. Moreover a minimum output ripple voltage is necessary to assure system stability and jitter-free operations (see Output capacitor selection paragraph). The product of the output capacitor's ESR multiplied by the inductor ripple current must be taken into consideration. A good trade-off between the transient response time, the efficiency, the cost and the size is choosing the inductance value in order to maintain the inductor ripple current between 20% and 50% (usually 40%) of the maximum output current.

The maximum inductor ripple current, $\Delta I_{L,MAX}$, occurs at the maximum input voltage.

Given these considerations, the inductance value can be calculated with the following expression:

Equation 29

$$L = \frac{V_{IN} - V_{OUT}}{fsw \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where f_{SW} is the switching frequency, V_{IN} is the input voltage, V_{OUT} is the output voltage and ΔI_L is the inductor ripple current.

Once the inductor value is determined, the inductor ripple current is then recalculated:

Equation 30

$$\Delta I_{L,MAX} = \frac{V_{IN,MAX} - V_{OUT}}{fsw \cdot L} \cdot \frac{V_{OUT}}{V_{IN,MAX}}$$

The next step is the calculation of the maximum r.m.s. inductor current:

Equation 31

$$I_{L,RMS} = \sqrt{(I_{LOAD,MAX})^2 + \frac{(\Delta I_{L,MAX})^2}{12}}$$

The inductor must have an r.m.s. current greater than $I_{L,RMS}$ in order to assure thermal stability.

Then the calculation of the maximum inductor peak current follows:

Equation 32

$$I_{L,PEAK} = I_{LOAD,MAX} + \frac{\Delta I_{L,MAX}}{2}$$

$I_{L,PEAK}$ is important in inductor selection in term of its saturation current.

The saturation current of the inductor should be greater than $I_{L,PEAK}$ not only in case of hard saturation core inductors. Using soft-ferrite cores it is possible (but not advisable) to push the inductor working near its saturation current.

In *Table 13* some inductors are listed.

Table 13. Evaluated inductors (@fsw = 400 kHz)

Manufacturer	Series	Inductance (µH)	+40 °C rms current (A)	-30% saturation current (A)
COILCRAFT	MLC1538-102	1	13.4	21.0
COILCRAFT	MLC1240-901	0.9	12.4	24.5
COILCRAFT	MVR1261C-112	1.1	20	20
WURTH	7443552100	1	16	20
COILTRONICS	HC8-1R2	1.2	16.0	25.4

In pulse-skip mode, low inductance values produce a better efficiency versus load curve, while higher values result in higher full-load efficiency because of the smaller current ripple.

8.1.2 Input capacitor selection

In a buck topology converter the current that flows through the input capacitor is pulsed and with zero average value. The RMS input current can be calculated as follows:

Equation 33

$$I_{CinRMS} = \sqrt{I_{LOAD}{}^2 \cdot D \cdot (1-D) + \frac{1}{12} D \cdot (\Delta I_L)^2}$$

Neglecting the second term, the equation 10 is reduced to:

Equation 34

$$I_{CinRMS} = I_{LOAD} \sqrt{D \cdot (1-D)}$$

The losses due to the input capacitor are thus maximized when the duty-cycle is 0.5:

Equation 35

$$P_{loss} = ESR_{Cin} \cdot I_{CinRMS}(max)^2 = ESR_{Cin} \cdot (0.5 \cdot I_{LOAD}(max))^2$$

The input capacitor should be selected with a RMS rated current higher than I_{CINRMS}(max). Tantalum capacitors are good in terms of low ESR and small size, but they occasionally can burn out if subjected to very high current during operation. Multi-layers-ceramic-capacitors (MLCC) have usually a higher RMS current rating with smaller size and they remain the best choice. The drawback is their quite high cost.

It must be taken into account that in some MLCC the capacitance decreases when the operating voltage is near the rated voltage. In *Table 14* some MLCC suitable for most of applications are listed.

Table 14. Evaluated MLCC for input filtering

Manufacturer	Series	Capacitance (µF)	Rated voltage (V)	Maximum Irms @100 kHz (A)
TAIYO YUDEN	UMK325BJ106KM-T	10	50	2
TAIYO YUDEN	GMK316F106ZL-T	10	35	2.2
TAIYO YUDEN	GMK325F106ZH-T	10	35	2.2
TAIYO YUDEN	GMK325BJ106KN	10	35	2.5
TDK	C3225X5R1E106M	10	25	

8.1.3 Output capacitor selection

Using tantalum or electrolytic capacitors, the selection is made referring to ESR and voltage rating rather than by a specific capacitance value.

The output capacitor has to satisfy the output voltage ripple requirements. At a given switching frequency, small inductor values are useful to reduce the size of the choke but increase the inductor current ripple. Thus, to reduce the output voltage ripple a low ESR capacitor is required.

To reduce jitter noise between different switching regulators in the system, it is preferable to work with an output voltage ripple greater than 25 mV.

As far as it concerning the load transient requirements, the Equivalent Series Resistance (ESR) of the output capacitor must satisfy the following relationship:

Equation 36

$$ESR \leq \frac{V_{RIPPLE,MAX}}{\Delta I_{L,MAX}}$$

where V_{RIPPLE} is the maximum tolerable ripple voltage.

In addition, the ESR must be high enough high to meet stability requirements. The output capacitor zero must be lower than the switching frequency:

Equation 37

$$f_{SW} > f_Z = \frac{1}{2\pi \cdot ESR \cdot C_{out}}$$

If ceramic capacitors are used, the output voltage ripple due to inductor current ripple is negligible. Then the inductance could be smaller, reducing the size of the choke. In this case it is important that output capacitor can adsorb the inductor energy without generating an over-voltage condition when the system changes from a full load to a no load condition.

The minimum output capacitance can be chosen by the following equation:

Equation 38

$$C_{OUT,min} = \frac{L \cdot I_{LOAD,MAX}^2}{Vf^2 - Vi^2}$$

where Vf is the output capacitor voltage after the load transient, while V_I is the output capacitor voltage before the load transient.

In *Table 15* are listed some tested polymer capacitors are listed.

Table 15. Evaluated output capacitors

Manufacturer	Series	Capacitance (µF)	Rated voltage (V)	ESR max @100 kHz (mΩ)
SANYO	4TPE220MF	220	4 V	15 to 25
	4TPE150MI	220	4 V	18
	4TPC220M	220	4 V	40
HITACHI	TNCB OE227MTRYF	220	2.5 V	25

8.1.4 MOSFETs selection

In most of the applications, power management efficiency is a high level requirement. Power dissipation on the power switches becomes an important factor in the selection of switches. Losses of high-side and low-side MOSFETs depend on their working condition.

Considering the high-side MOSFET, the power dissipation is calculated as:

Equation 39

$$P_{DHighSide} = P_{conduction} + P_{switching}$$

Maximum conduction losses are approximately given by:

Equation 40

$$P_{conduction} = R_{DSon} \cdot \frac{V_{OUT}}{V_{IN.min}} \cdot I_{LOAD,MAX}^2$$

where R_{DSon} is the drain-source on-resistance of the control MOSFET.

Switching losses are approximately given by:

Equation 41

$$P_{switching} = \frac{V_{IN} \cdot (I_{LOAD}(max) - \frac{\Delta I_L}{2}) \cdot t_{on} \cdot f_{sw}}{2} + \frac{V_{IN} \cdot (I_{LOAD}(max) + \frac{\Delta I_L}{2}) \cdot t_{off} \cdot f_{sw}}{2}$$

where t_{ON} and t_{OFF} are the turn-on and turn-off times of the MOSFET and depend on the gate-driver current capability and the gate charge Q_{gate}. A greater efficiency is achieved with low R_{DSon}. Unfortunately low R_{DSon} MOSFETs have a great gate charge.

As general rule, the R_{DSon} x Q_{gate} product should be minimized to find out the suitable MOSFET.

Logic-level MOSFETs are recommended, as long as low-side and high-side gate drivers are powered by V_{VCC} = +5 V. The breakdown voltage of the MOSFETs (V_{BRDSS}) must be greater than the maximum input voltage.V_{INmax}.

Table 16 lists tested high-side MOSFETs.

Table 16. Evaluated high-side MOSFETs

Manufacturer	Type	R_{DSon} (mΩ)	Gate charge (nC)	Rated reverse voltage (V)
ST	STS12NH3LL	10.5	12	30
IR	IRF7811	9	18	30

In buck converters the power dissipation of the synchronous MOSFET is mainly due to conduction losses:

Equation 42

$$P_{DLowSide} \cong P_{conduction}$$

Maximum conduction losses occur at the maximum input voltage:

Equation 43

$$P_{conduction} = R_{DSon} \cdot \left(1 - \frac{V_{OUT}}{V_{IN,MAX}}\right) \cdot I_{LOAD,MAX}^{2}$$

The synchronous rectifier should have the lowest R_{DSon} as possible. When the high-side MOSFET turns on, high d_V/d_t of the phase node can bring up even the low-side gate through its gate-drain capacitance C_{RRS}, causing a cross-conduction problem. Once again, the choice of the low-side MOSFET is a trade-off between on resistance and gate charge; a good selection should minimize the ratio C_{RSS} / C_{GS} where

Equation 44

$$C_{GS} = C_{ISS} - C_{RSS}$$

Tested low-side MOSFETs are listed in *Table 17*.

Table 17. Evaluated low-side MOSFETs

Manufacturer	Type	R_{DSon} (mΩ)	$C_{GD} \setminus C_{GS}$	Rated reverse voltage (V)
ST	STS12NH3LL	13.5	0.069	30
ST	STS25NH3LL	4.0	0.011	30
IR	IRF7811	24	0.054	30

Dual N-MOS can be used in applications with lower output current.

Table 18 shows some suitable dual MOSFETs for applications requiring about 3 A.

Table 18. Suitable dual MOSFETs

Manufacturer	Type	R_{DSon} (mΩ)	Gate charge (nC)	Rated reverse voltage (V)
ST	STS8DNH3LL	25	10	30
IR	IRF7313	46	33	30

8.1.5 Diode selection

A rectifier across the synchronous switch is recommended. The rectifier works as a voltage clamp across the synchronous rectifier and reduces the negative inductor swing during the dead time between turning the high-side MOSFET off and the synchronous rectifier on. Moreover it increases the efficiency of the system.

Choose a schottky diode as long as its forward voltage drop is very little (0.3 V). The reverse voltage should be greater than the maximum input voltage V_{INmax} and a minimum recovery reverse charge is preferable. *Table 19* shows some evaluated diodes.

Table 19. Evaluated recirculation rectifiers

Manufacturer	Type	Forward voltage (V)	Rated reverse voltage (V)	Reverse current (μA)
ST	STPS1L30M	0.34	30	0.00039
ST	STPS1L30A	0.34	30	0.00039

8.1.6 VDDQ current limit setting

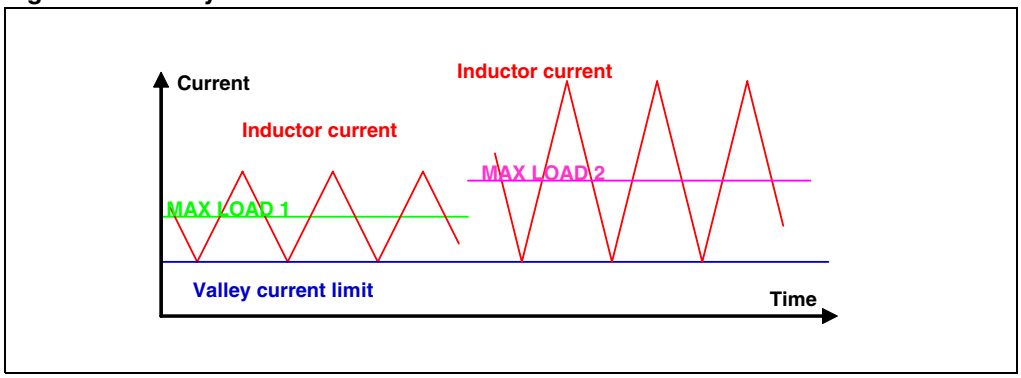
The valley current limit is set by R_{CSNS} and must be chosen to support the maximum load current. The valley of the inductor current $I_{Lvalley}$ is:

Equation 45

$$I_{Lvalley} = I_{LOAD}(max) - \frac{\Delta I_L}{2}$$

The output current limit depends on the current ripple as shown I *Figure 39*:

Figure 39. Valley current limit waveforms



As the valley threshold is fixed, the greater the current ripple, the greater the DC output current will be. If an output current limit greater than $I_{LOAD}(max)$ over all the input voltage range is required, the minimum current ripple must be considered in the previous formula.

Then the resistor R_{CSNS} is:

Equation 46

$$R_{CSNS} = \frac{R_{DSon} \cdot I_{Lvalley}}{100uA}$$

where R_{DSon} is the drain-source on-resistance of the low-side switch. Consider the temperature effect and the worst case value in R_{DSon} calculation (typically +0.4%/°C).

The accuracy of the valley current also depends on the offset of the internal comparator (±5 mV).

The negative valley-current limit (if the device works in forced-PWM mode) is given by:

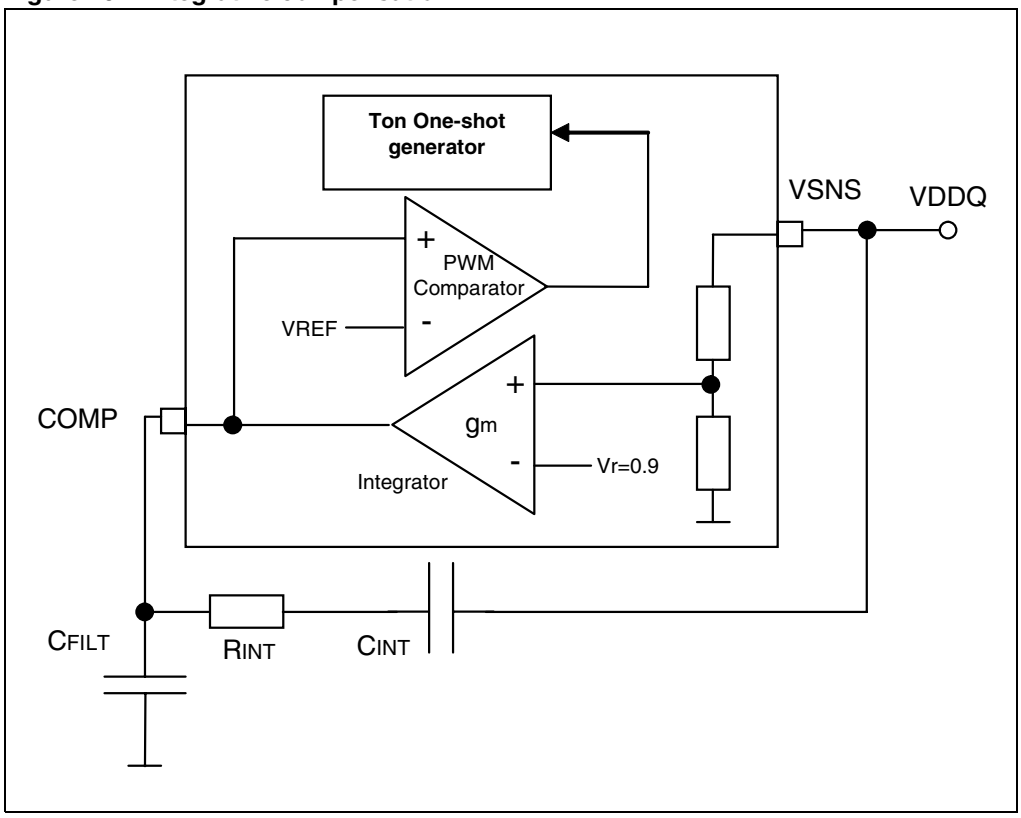
Equation 47

$$I_{NEG} = \frac{120mV}{R_{DSon}}$$

8.1.7 All ceramic capacitors application

Design of external feedback network depends on the output voltage ripple across the output capacitors' ESR. If the ripple is great enough (at least 20 mV), the compensation network simply consists of a C_{INT} capacitor.

Figure 40. Integrative compensation



The stability of the system depends firstly on the output capacitor zero frequency. It must be verified that:

Equation 48

$$f_{SW} > k \cdot f_{Zout} = \frac{k}{2\pi \cdot R_{out} C_{out}}$$

where k is a free design parameter greater than unity (k > 3). It determines the minimum integrator capacitor value C_{INT}:

Equation 49

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout} \right)} \cdot \frac{Vref}{Vo}$$

If the ripple on pin COMP is greater than the integrator output dynamic (150 mV), an additional capacitor C_{filt} could be added in order to reduce its amplitude. If q is the desired attenuation factor of the output ripple, select:

Equation 50

$$C_{filt} = \frac{C_{INT} \cdot (1-q)}{q}$$

In order to reduce noise on pin COMP, it's possible to introduce a resistor R_{INT} that, together with C_{INT} and C_{filt}, becomes a low psas filter. The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency of the section:

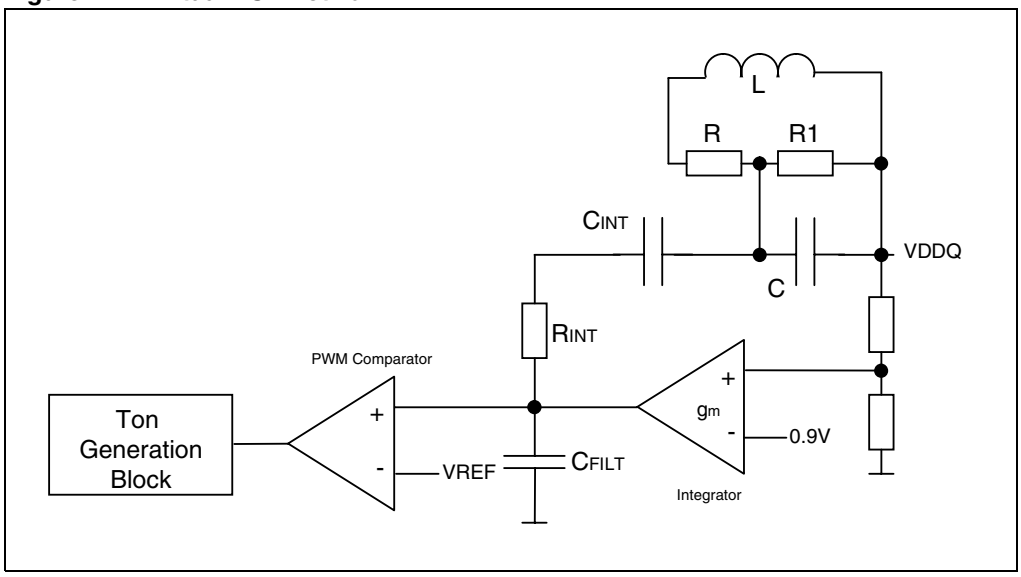
Equation 51

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

For most of applications both R_{INT} and C_{filt} are unnecessary.

If the ripple is very small (e.g. such as with ceramic capacitors), an additional compensation network, called “Virtual ESR” network, is needed. This additional part generates a triangular ripple that substitutes the ESR output voltage ripple. The complete compensation scheme is represented in *Figure 41*.

Figure 41. Virtual ESR network



Select C as shown:

Equation 52

$$C > 5 \cdot C_{INT}$$

Then calculate R in order to have enough ripple voltage on the integrator input:

Equation 53

$$R = \frac{L}{R_{VESR} \cdot C}$$

Where R_{VESR} is the new virtual output capacitor ESR. A good trade-off is to consider an equivalent ESR of 30-50 mΩ, even though the choice depends on inductor current ripple.

Then choose R1 as follows:

Equation 54

$$R1 = \frac{R \cdot \left(\frac{1}{C \pi f_Z} \right)}{R - \frac{1}{C \pi f_Z}}$$

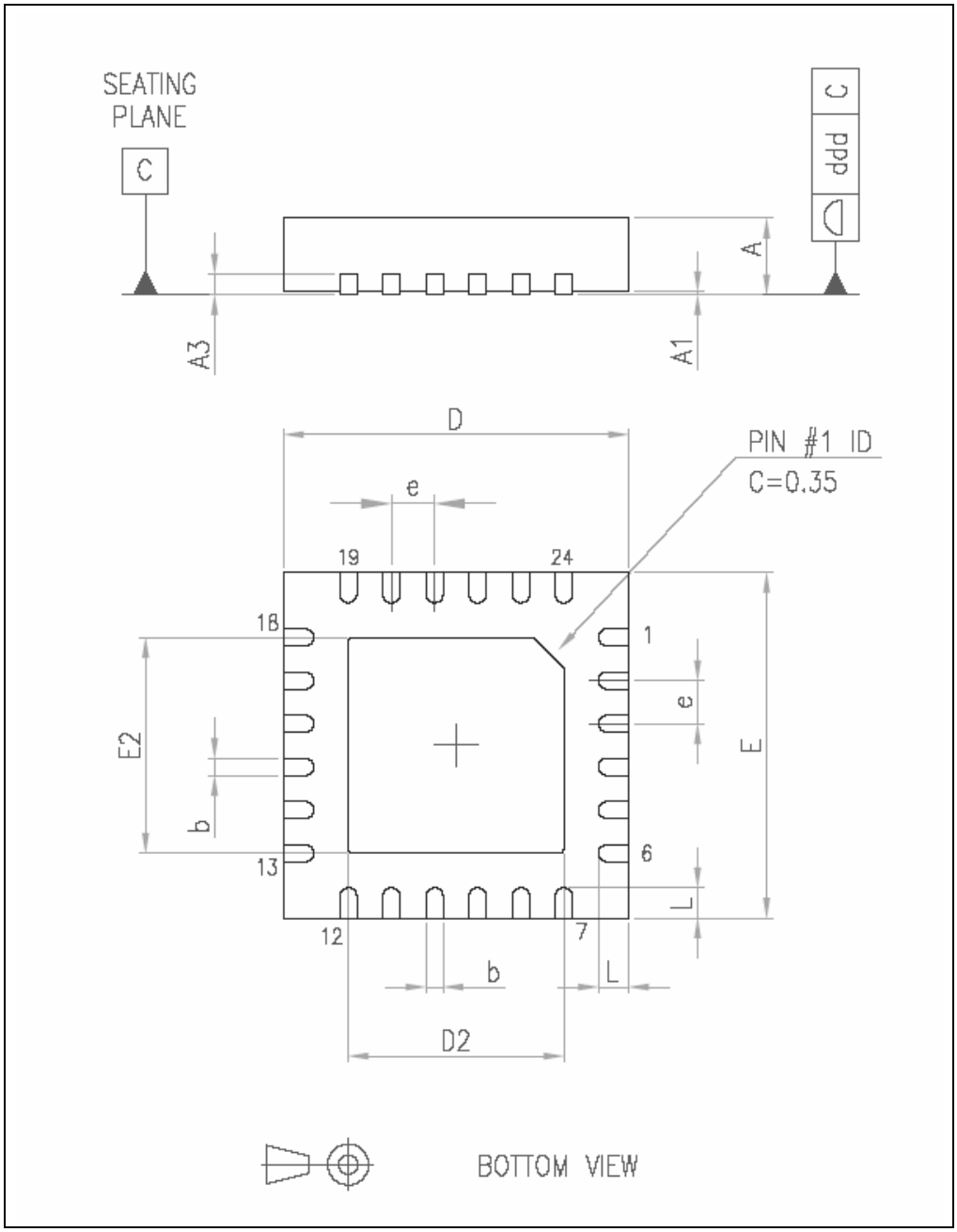
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 20. VFQFPN-24 4mm x 4mm mechanical data

Dim.	mm.		
	Min	Typ	Max
A	0.80	0.90	1.00
A1		0.0	0.05
A2		0.65	0.80
D		4.00	
D1		3.75	
E		4.00	
E1		3.75	
θ			12°
P	0.24	0.42	0.60
e		0.50	
N		24.00	
Nd		6.00	
Ne		6.00	
L	0.30	0.40	0.50
b	0.18		0.30
D2	2.40		2.70
E2	2.40		2.70

Figure 42. Package dimensions



10 Revision history

Table 21. Document revision history

Date	Revision	Changes
14-Feb-2008	1	Initial release.
17-Feb-2010	2	Updated: Coverpage, *Table 2*, *Table 6*, *Section 7.1*, *Figure 28* and *Table 8*

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