Linear SuperCap Charger with Current-Limited Ideal Diode and V/I Monitor

FEATURES

- **50mΩ Ideal Diode from V_{IN} to V_{OUT}**
- **Smart Charge Current Profile Limits Inrush Current**
- **Internal Cell Balancer (No External Resistors)**
- **Programmable Output Voltage (LDO Mode)**
- **Programmable V_{IN} to V_{OUT} Current Limit**
- **Continuous Monitoring of V_{IN} to V_{OUT} Current via PROG Pin**
- **Low Quiescent Current: 20µA**
- V_{IN} Power Fail, PGOOD Indicator
- 2.45V/2.7V Cell Protection Shunts (4.9V/5.4V SuperCap Max Top-Off Voltage)
- 3A Peak Current Limit, Thermal Limiting
- Tiny Application Circuit, 3mm × 3mm × 0.75mm DFN and 12-Lead MSOP Packages

APPLICATIONS

- High Peak Power Battery/USB Powered Equipment
- Industrial PDAs
- Portable Instruments/Monitoring Equipment
- Power Meters, SuperCap Backup Circuits
- PC Card/USB Modems

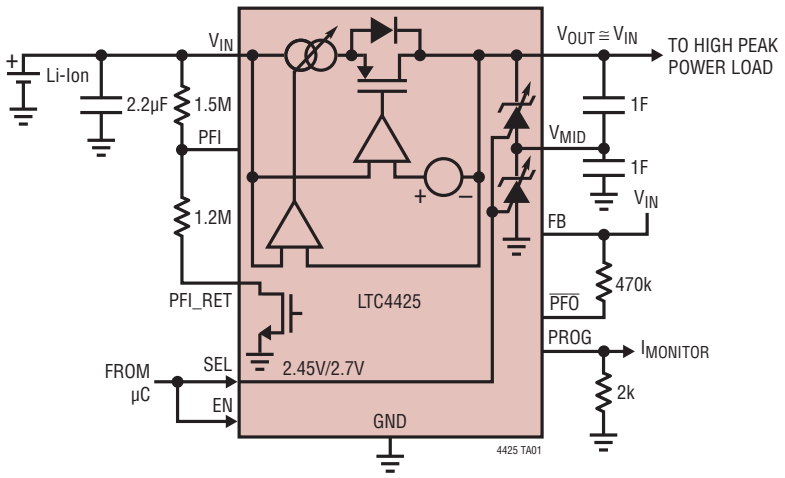
DESCRIPTION

The LTC®4425 is a constant-current/constant-voltage linear charger designed to charge a 2-cell supercap stack from either a Li-Ion/Polymer battery, a USB port, or a 2.7V to 5.5V current-limited supply. The part operates as an ideal diode with an extremely low 50mΩ on-resistance making it suitable for high peak-power/low average power applications. The LTC4425 charges the output capacitors to an externally programmed output voltage in LDO mode at a constant charge current, or to V_{IN} in normal mode with a smart charge current profile to limit the inrush current until the V_{IN} to V_{OUT} differential is less than 250mV. In addition the LTC4425 can be set to clamp the output voltage to 4.9V or 5.4V.

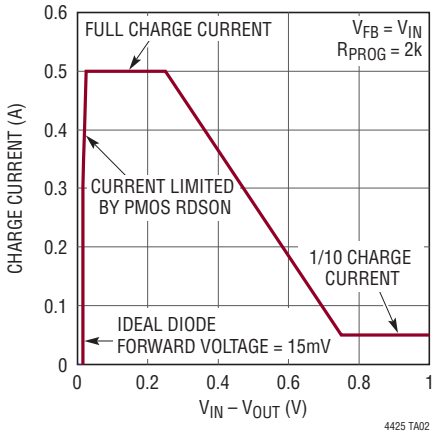
Charge current (V_{OUT} current limit) is programmed by connecting a resistor between PROG and GND. The voltage on the PROG pin represents the current flowing from V_{IN} to V_{OUT} for current monitoring. An internal active balancing circuit maintains equal voltages across each supercapacitor and clamps the peak voltage across each cell to a pin-selectable maximum value. The LTC4425 operates at a very low 20µA quiescent current (shutdown current <3µA) and is available in a low profile 12-pin 3mm × 3mm DFN or a 12-lead MSOP package.

TYPICAL APPLICATION

Charging 2-Cell Series Supercapacitor from Li-Ion Source



Charge Current vs V_{IN} to V_{OUT} Differential

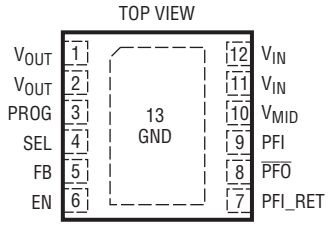


ABSOLUTE MAXIMUM RATINGS

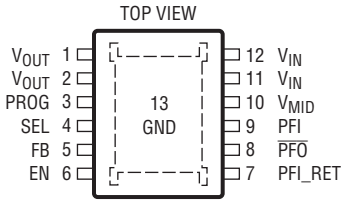
(Notes 1, 2)

V_{IN}, V_{OUT}, V_{MID}, FB, PFI_RET, $\overline{PFO}$ Voltage . . . –0.3V to 6V
EN, SEL, PFI Voltage . . . . –0.3V to MAX(V_{IN}, V_{OUT}) + 0.3V
Operating Junction Temperature . . . . . –40°C to 125°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature, MSOP Only
(Soldering, 10 sec) . . . . . 300°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W (Note 3)
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 35°C/W (Note 3)
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4425EDD#PBF	LTC4425EDD#TRPBF	LFMQ	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4425IDD#PBF	LTC4425IDD#TRPBF	LFMQ	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4425EMSE#PBF	LTC4425EMSE#TRPBF	4425	12-Lead Plastic MSOP	–40°C to 125°C
LTC4425IMSE#PBF	LTC4425IMSE#TRPBF	4425	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Supply Range		●	2.7		5.5	V
$I_{Q(IN)}$	Quiescent Current from V_{IN}	$V_{IN} = V_{OUT}$			20		µA
$I_{Q(OUT)}$	Quiescent Current from V_{OUT}	$V_{IN} = V_{OUT}$			3		µA
I_{SD}	Quiescent Current in Shutdown	EN = 0				3	µA
Ideal Diode							
V_{FWD}	Forward Voltage				15		mV
R_{FWD}	Open Loop Forward On-Resistance				50		mΩ
Supercap Charger							
V_{FB}	Feedback Voltage		●	1.18	1.2	1.22	V
I_{FB}	Feedback Pin Input Leakage					100	nA
I_{CHG}	Charge Current in LDO Mode (FB = 0V)	R_{PROG} = 0.5k R_{PROG} = 5k			2 0.2		A A
	Charge Current in Normal Mode (FB = V_{IN})	R_{PROG} = 0.5k, $V_{IN} - V_{OUT}$ < 250mV R_{PROG} = 0.5k, $V_{IN} - V_{OUT}$ > 750mV			2 0.2		A A
		R_{PROG} = 5k, $V_{IN} - V_{OUT}$ < 250mV R_{PROG} = 5k, $V_{IN} - V_{OUT}$ > 750mV			200 20		mA mA
V_{PROG}	PROG Pin Servo Voltage in LDO Mode	FB < 1.2V			1.00		V
h_{PROG}	Ratio of Charge Current to PROG Pin Current				1000		mA/mA
V_{PROG}	PROG Pin Servo Voltage in Normal Mode (FB = V_{IN})	$V_{IN} - V_{OUT}$ < 250mV $V_{IN} - V_{OUT}$ > 750mV			1.00 0.1		V V
I_{SC}	Charger Short-Circuit Current Limit	PROG Pin Shorted to GND, FB = 0		2	3	4	A
t_{SS}	Charger Soft Start Time	FB = 0			1.5		ms
T_{LIM}	Junction Temperature in Constant Temperature Mode (Note 5)	V_{OUT} = 0, FB = 0, R_{PROG} = 0.5k			105		°C
Voltage Clamps							
V_{CLAMP}	Maximum Voltage Across the Top Capacitor	V_{SEL} = Lo V_{SEL} = Hi	● ●		2.45 2.7	2.5 2.75	V V
	Maximum Voltage Across the Bottom Capacitor	V_{SEL} = Lo V_{SEL} = Hi	● ●		2.45 2.7	2.5 2.75	V V
V_{RIP}	V_{OUT} Clamp Hysteresis	If Either Capacitor Reaches Clamp Voltage i.e. $V_{OUT} < V_{IN}$			50		mV
$I_{SH(TOP)}$	Top Shunt Current	R_{PROG} = 1k, ($V_{OUT} - V_{MID}$) > V_{CLAMP}			160		mA
$I_{SH(BOT)}$	Bottom Shunt Current	R_{PROG} = 1k, $V_{MID} > V_{CLAMP}$			140		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Leakage Balancer							
V_{MID}	V_{MID} Output Voltage	V_{OUT} = 3.6V		1.76	1.8	1.84	V
	V_{MID} Maximum Current Sourcing Capability	$V_{MID} < V_{OUT/2}$, $V_{MID} < V_{CLAMP}$			0.7		mA
	V_{MID} Maximum Current Sinking Capability	$V_{MID} > V_{OUT/2}$, $V_{MID} < V_{CLAMP}$			1.2		mA
$\overline{PFO}$, PFI_RET, PFI							
	Output Low Voltage ($\overline{PFO}$, PFI_RET)	I_{PIN} = 5mA			65		mV
	Pin Leakage Current ($\overline{PFO}$, PFI_RET)	V_{PIN} = 5V, EN = 0				1	µA
	FB Threshold Voltage for Power Good (Rising)	LDO Mode	●	1.09	1.11	1.13	V
	Input-to-Output Differential for Power Good (Rising)	Normal Mode			265		mV
V_{PFI}	PFI Threshold (Falling)		●	1.18	1.2	1.22	V
	PFI Hysteresis				10		mV
I_{PFI}	PFI Pin Input Leakage					100	nA
	Power Good Timer Delay				200		ms
Logic Inputs (EN, SEL)							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.2			V
I_{IH}	Input Current High	EN, SEL Pins at 5.5V		–1		1	µA
I_{IL}	Input Current Low	EN, SEL Pins at GND		–1		1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

Note 3: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much greater than 43°C/W on the DD package and greater than 35°C/W on MSE package.

Note 4: The LTC4425E (E grade) is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4425I (I grade) is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature, T_J, is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}\ °C/W).$$

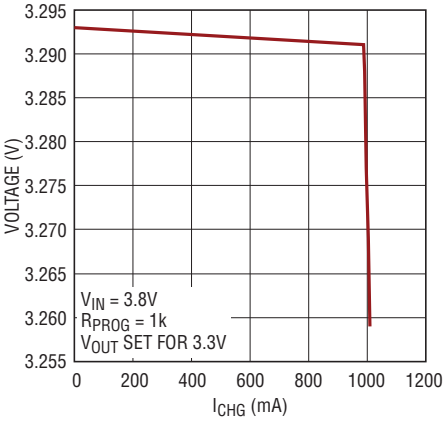
Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors.

Note 5: V_{IN} to V_{OUT} charge current is reduced by thermal foldback as junction temperature approaches 105°C.

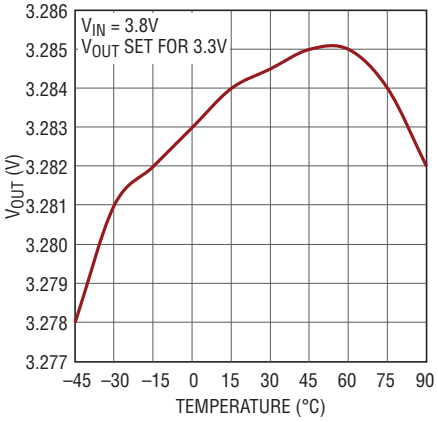
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

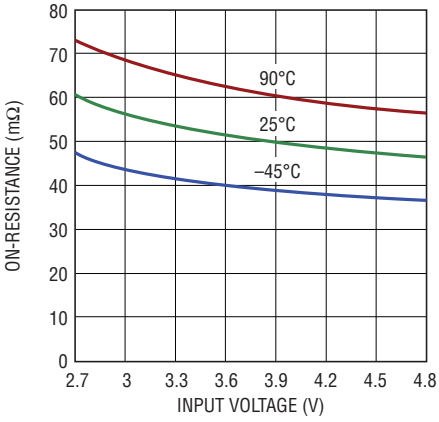
LDO Regulation Voltage vs Charge Current



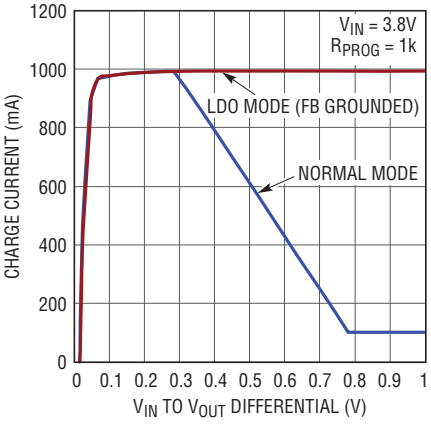
LDO Regulation Voltage vs Temperature



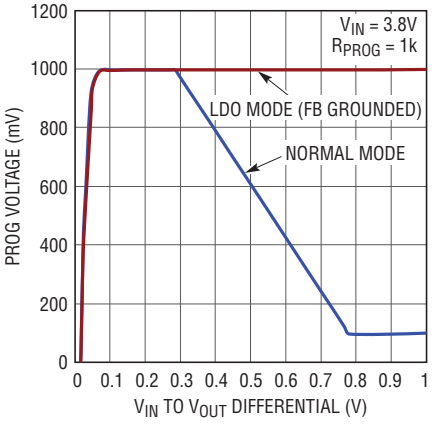
Charger FET On-Resistance vs Supply Voltage



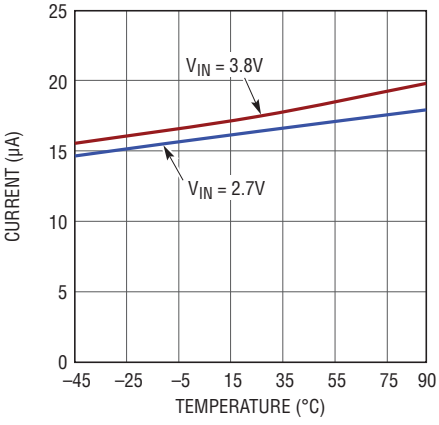
Charge Current vs (V_{IN}–V_{OUT}) Differential



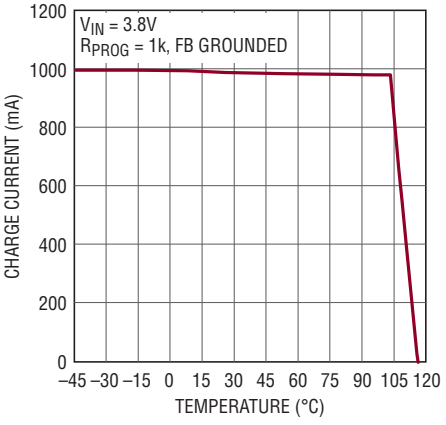
PROG Pin Voltage vs (V_{IN} – V_{OUT}) Differential



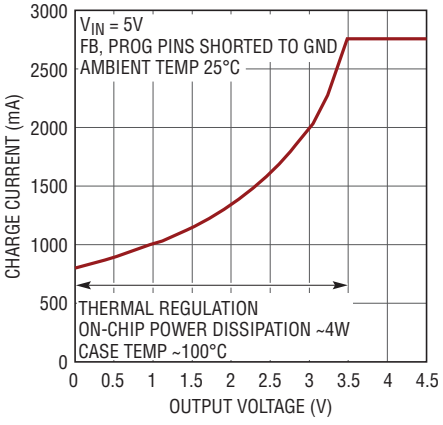
V_{IN} Quiescent Current vs Temperature (V_{IN} ≥ V_{OUT})



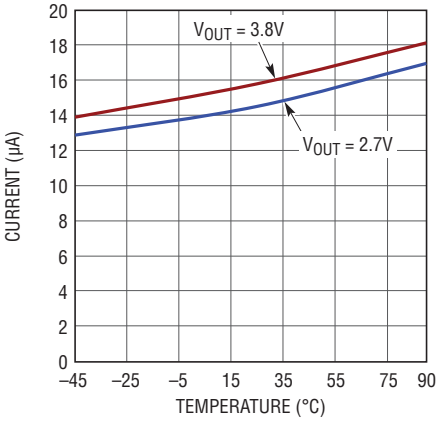
Charge Current vs Junction Temperature



Charge Current vs V_{OUT} in Thermal Regulation



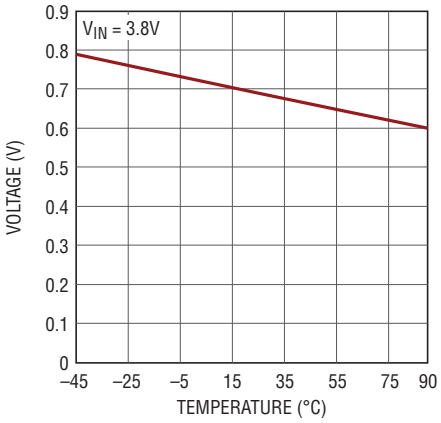
V_{OUT} Quiescent Current vs Temperature (V_{IN} < V_{OUT})



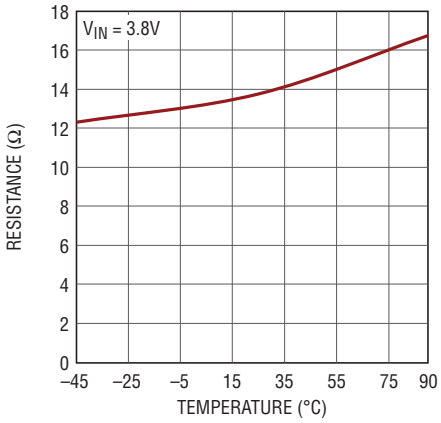
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

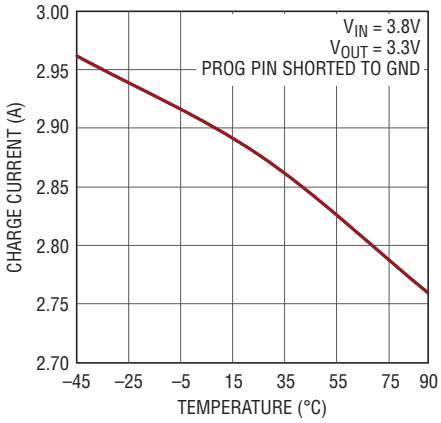
Logic Inputs (EN and SEL) Threshold Voltage vs Temperature



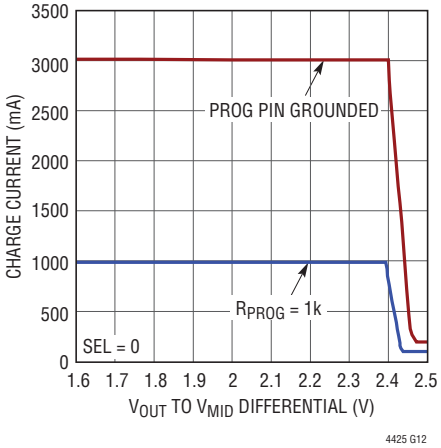
Open Drain Outputs (PFI_RET and PFO) FET On-Resistance vs Temperature



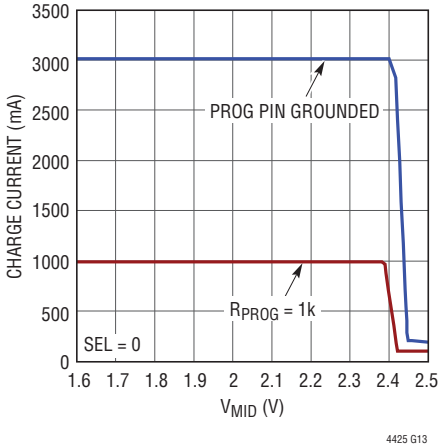
PROG Pin Short Circuit Charge Current vs Temperature



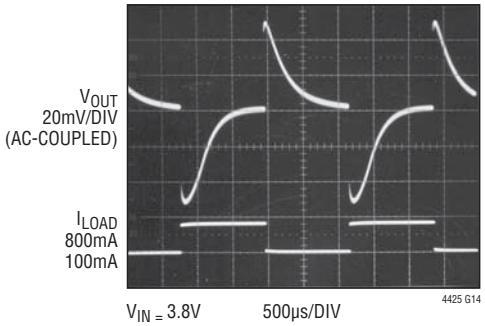
Charge Current vs Voltage Across Top Capacitor (V_{OUT} – V_{MID})



Charge Current vs Voltage Across Bottom Capacitor (V_{MID})

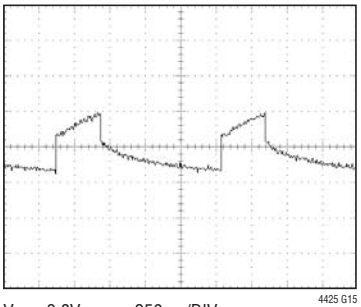


Output Voltage Transient Step Response Waveform (LDO Mode)



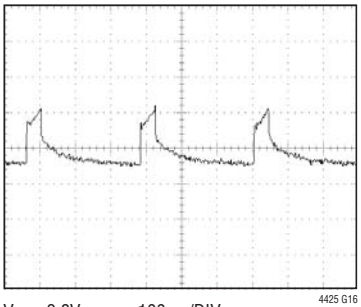
V_{IN} = 3.8V 500µs/DIV
R_{PROG} = 500Ω
SUPERCAP VALUE = 0.55F
V_{OUT} (DC) = 3.3V

Output Voltage Waveform When V_{MID} is Shorted to GND



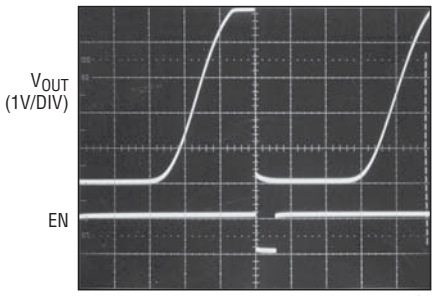
V_{IN} = 3.8V 250ms/DIV
R_{PROG} = 1k SUPERCAP VALUE = 0.55F
SEL = 0 V_{OUT} (DC) = 2.45V

Output Voltage Waveform When V_{MID} is Shorted to V_{OUT}



V_{IN} = 3.8V 100ms/DIV
R_{PROG} = 1k SUPERCAP VALUE = 0.55F
SEL = 0 V_{OUT} (DC) = 2.45V

PROG Pin Soft-Start Waveform (Normal Mode)



V_{IN} = 5V 500µs/DIV
R_{PROG} = 1k

PIN FUNCTIONS

V_{OUT} (Pin 1, 2): Output Pin of the Charger. Typically connects to the top of the 2-cell supercap stack.

PROG (Pin 3): Charge Current Program and Charge Current Monitor Pin. A resistor connected from PROG to ground programs the charge current. In LDO mode, this pin always servos to 1V. However, if the charge current profile is turned on, this pin servos to a voltage between 1V and 0.1V depending on the input-to-output differential. In all cases, the voltage on this pin always represents the actual charge current.

SEL (Pin 4): Logic Input to Select One of the Two Possible Clamp Voltages (V_{CLAMP}). If the pin is a logic low, the maximum voltage across any supercap of the stack is 2.45V. If the pin is a logic high, it is 2.7V. Do not float this pin.

FB (Pin 5): In LDO mode, output voltage is programmed by a resistor divider from V_{OUT} via the FB pin. In this mode, the voltage on this pin always servos to the internal reference voltage of 1.2V. If the FB pin is pulled up to V_{IN}, the LDO mode is disabled and the charge current profile mode is turned on. Shorting the FB pin to GND turns off charge current profile mode. Do not float this pin.

EN (Pin 6): Digital Input to Enable the Charger. If this pin is a logic high, the part is enabled and it draws only 20µA of quiescent current from the input or output when idle. If this pin is a logic low, the part is in shutdown mode and draws less than 3µA. Do not float this pin.

PFI_RET (Pin 7): This pin connects to the bottom of the external resistor divider for the input power-fail comparator. In shutdown mode, an internal switch opens up this path to reduce the current drawn by the resistor divider.

$\overline{PFO}$ (Pin 8): Open Drain Output of the Power-Fail Comparator. This pin is driven to logic low if at least one of the following conditions is true: (1) V_{IN} is less than a value programmed by an external divider via PFI, (2) V_{OUT} has not reached within 7.5% of its final programmed value in LDO mode, or (3) V_{OUT} is not within 250mV of V_{IN} in charge current profile mode. When all these conditions are false for at least 200ms, this pin goes high impedance indicating that power is good.

PFI (Pin 9): Input to the Power-Fail Comparator. The input voltage below which $\overline{PFO}$ pin indicates a power-fail condition can be programmed by connecting this pin to an external resistor divider between V_{IN} and PFI_RET pin.

V_{MID} (Pin 10): Connects to the Midpoint of the 2-Cell supercap stack. An internal leakage balancing amplifier drives this pin to a voltage which is exactly half of V_{OUT}.

V_{IN} (Pin 11, 12): Input Power Pin. Typically connected to a DC source like a Li-Ion/Polymer battery or a USB port. This pin should be bypassed with a low-ESR ceramic capacitor.

GND (Exposed Pad Pin 13): GND. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the part to achieve optimum thermal conduction.

BLOCK DIAGRAM

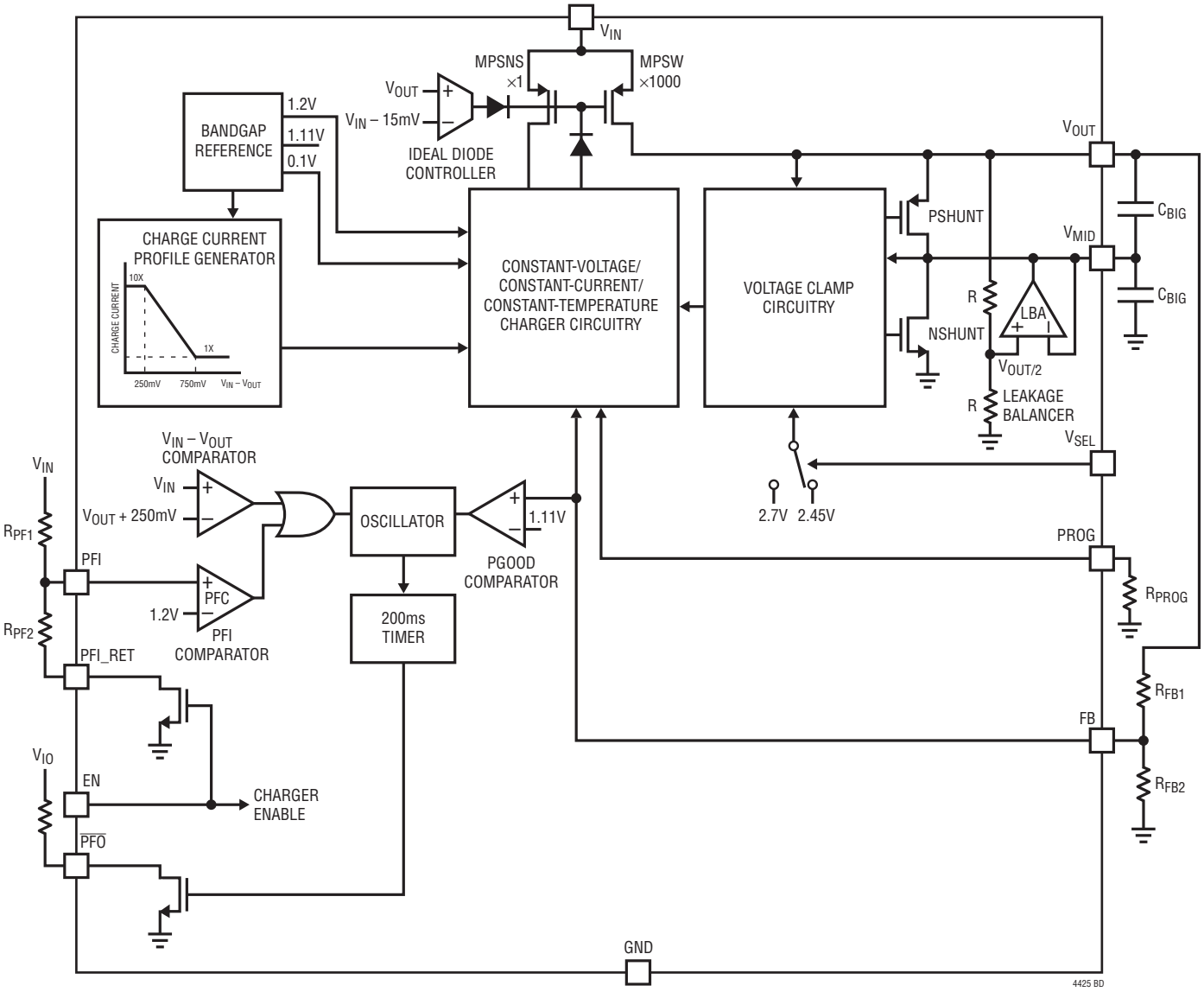


Figure 1. LTC4425 Block Diagram

OPERATION

The LTC4425 is a linear charger designed to charge a two-cell series supercap stack by employing a constant-current, constant-voltage, and constant-temperature architecture. It has two modes of operation: charge current profile mode (also referred to as normal mode) and LDO mode. In LDO mode, the LTC4425 charges the top of the stack to an externally programmed output voltage with a fixed charge current that is also externally programmable. In charge current profile mode, the LTC4425 charges the top of the stack to the input voltage V_{IN} with a charge current that varies based on the input-to-output differential voltage.

LDO Mode

In LDO mode, the output voltage V_{OUT} is programmed by an external resistor divider network consisting of R_{FB1} and R_{FB2} via the FB pin and the charge current is programmed by an external resistor R_{PROG} via the PROG pin. Please refer to the Block Diagram shown in Figure 1. The charger control circuitry consists of a constant-current amplifier and a constant-voltage amplifier. When the part is enabled to charge a discharged supercap stack, initially the constant-current amplifier is in control and servos the PROG pin voltage to 1V. The current through the PROG resistor gets multiplied by approximately 1000, the ratio of the sense MOSFET (MPSNS) and the power MOSFET (MPSW), to charge the supercap stack. As the output voltage V_{OUT} gets close to the programmed value, the constant-voltage amplifier takes over and backs off the charge current as necessary to maintain the FB pin voltage equal to an internal reference voltage of 1.2V. Since the PROG pin current is always about 1/1000 of the charge current, the PROG pin voltage continues to give an indication of the actual charge current even when the constant-voltage amplifier is in control.

Charge Current Profile or Normal Mode

The LTC4425 is in charge current profile mode when the FB pin is shorted to the input voltage V_{IN}. In this mode of operation, the constant-voltage amplifier is internally disabled but the charge current is still programmed by the external R_{PROG} resistor. The charger provides 1/10 of the programmed charge current if the input-to-output voltage differential (V_{IN}–V_{OUT}) is more than 750mV to limit the power dissipation within the chip. As this differential voltage decreases from 750mV, the charge current increases linearly to its full programmed value when V_{OUT} is within 250mV or closer to V_{IN}. As V_{OUT} rises further, the voltage across the charger FET gets too small to support the full charge current. So the charge current gradually falls off and the charger FET enters into its triode (ohmic) region of operation (see Figure 2). Since the charger FET $R_{DS(ON)}$ is approximately 50mΩ, with a programmed charge current of 2A, the FET will enter the ohmic (triode) region and the charge current will start to fall off when V_{OUT} is within about 100mV of V_{IN}.

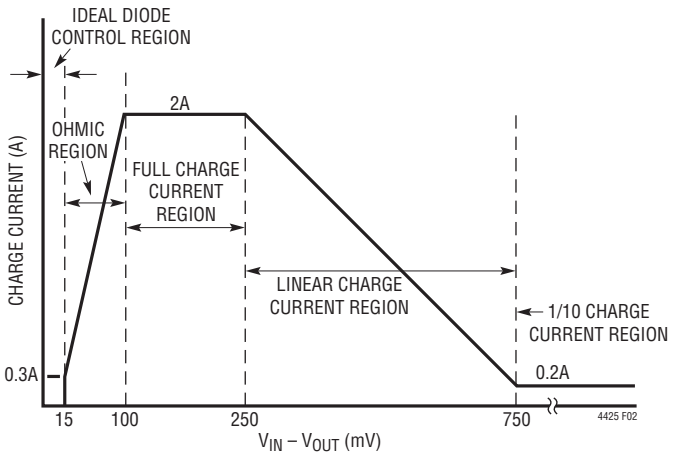


Figure 2. Different Regions of Charge Current Profile

The Ideal Diode Controller

When the input-to-output differential approaches 15mV, the ideal diode controller takes over the control from the constant-current amplifier and backs off the charge current by pulling up the gate of the charger FET as much as necessary to maintain a 15mV delta across the FET (see Figure 2). As a result, V_{OUT} can only be charged to 15mV below V_{IN}. In the event V_{IN} suddenly drops below V_{OUT}, the controller will quickly turn the FET completely off to prevent any loss of charge due to the reverse flow of charge from the supercap back to the supply.

OPERATION

Thermal Regulation

In either mode, if the die temperature starts to approach 105°C due to internal power dissipation, a thermal regulator limits the die temperature to approximately 105°C by reducing the charge current. Even in thermal regulation, the PROG pin continues to give an indication of the charge current. The thermal regulation protects the LTC4425 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without the risk of damaging the LTC4425 or the external components. Another benefit of this feature is that the charge current can be set according to typical, rather than worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the charge current in worst-case conditions.

Voltage Clamp Circuitry

The LTC4425 is equipped with circuitry to limit the voltage across any supercap of the stack to a maximum allowable voltage V_{CLAMP}. There are two preset voltages, 2.45V or 2.7V, for V_{CLAMP} selectable by the SEL pin. The SEL pin should be set to logic low for lower V_{CLAMP} voltage of 2.45V and to logic high for the higher V_{CLAMP} voltage of 2.7V. If the voltage across the bottom capacitor, i.e., the V_{MID} pin voltage reaches V_{CLAMP} first, an NMOS shunt transistor turns on and starts to bleed charge off of the bottom capacitor to GND. Similarly, if the voltage across the top capacitor, V_{TOP}, reaches the V_{CLAMP} voltage first, a PMOS shunt transistor turns on and starts to bleed charge off of the top capacitor to the bottom one.

When the voltage across any of the supercaps reaches within 50mV of V_{CLAMP}, a transconductance amplifier starts to cut back the charge current linearly. By the time any of the shunt devices are on, the charge current gets reduced to 1/10 of the programmed value and stays at this reduced level as long as the shunt device is on. This is to prevent the shunt devices from getting damaged by excessive heat. The comparators that control the shunt devices have a 50mV hysteresis meaning that when the voltage across either capacitor is reduced by 50mV, the shunt devices turn off and normal charging resumes with full charge current unless limited by any of the other amplifiers controlling the gate of the charger FET. In the event both capacitors exceed their maximum allowable voltage, V_{CLAMP}, the main charger FET completely shuts off and both shunt devices turn on. Both shunt devices are actually current mirrors guaranteed to shunt more current away than that coming through the charger FET.

Leakage Balancing Circuitry

The LTC4425 is equipped with an internal leakage balancing amplifier, LBA, which servos the midpoint, i.e., V_{MID} pin voltage, to exactly half of the output voltage, V_{OUT}. However it has a very limited source and sink capability of approximately 1mA. It is designed to handle slight mismatch of the supercaps due to leakage currents; not to correct any gross mismatch due to defects. The balancer is only active as long as there is an input present. The internal balancer eliminates the need for external balancing resistors.

Short-Circuit Current Limit

In the event the PROG pin gets shorted to GND, the LTC4425 limits the PROG pin current to approximately 3mA which, in turn, limits the maximum charge current to about 3A. While in short-circuit, if one of the supercaps approaches within 50mV of its maximum allowable voltage, V_{CLAMP}, a current-limit foldback circuit cuts back the short-circuit current limit to approximately 1/10 of its full value or to about 300mA.

Supply Status Monitor

The LTC4425 includes an input power-fail comparator, PFC, which monitors the input voltage V_{IN} via the PFI pin. At anytime, if V_{IN} falls below a certain externally program-mable threshold, it reports the undervoltage situation by pulling down the open-drain output $\overline{PFO}$ low. This under-voltage threshold is programmed by connecting an external resistor divider network (consisting of R_{PF1} andR_{PF2}) between V_{IN} and the PFI_RET pins. When the part is enabled, a low $R_{DS(ON)}$ (approx. 13Ω) internal pull-down transistor pulls the bottom end of R_{PF2}, i.e., the PFI_RET pin to GND to complete the divider network. When the part is disabled, this transistor opens R_{PF2} from GND, thereby saving the current drawn by the divider network. The power-fail comparator has a built-in filter to reject any transient supply glitch that is less than 10µS long.

OPERATION

Output Status Monitor

The LTC4425 has an internal comparator to always monitor the output voltage V_{OUT}. At any time, if V_{OUT} falls below 7.5% of its final programmed value in LDO mode or more than 250mV below the input voltage V_{IN} in charge current profile mode, the comparator reports the power-fail condition by pulling the same open-drain output $\overline{PFO}$ low. When both input and output voltages are good for at least 200ms, the $\overline{PFO}$ pin goes high impedance and can be pulled up to any external supply by a resistor to indicate a power good situation. In normal mode, the load should not exceed 1/10th of the programmed charge current until $\overline{PFO}$ is high.

$V_{OUT} > V_{IN}$ Operation

If the EN pin is pulled high and V_{IN} is below V_{OUT} or floating, most of the circuitry including the voltage clamp circuitry is kept alive and the part draws about 20µA from the output capacitors. However, the internal leakage balancer is turned off under this condition.

Shutdown Mode

The LTC4425 can be shut down by pulling the EN pin low. In shutdown mode, very minimal circuitry is alive and the part draws less than 3µA from the supply or from the output capacitors if the supply is not present.

Charge Current Soft-Start

The LTC4425 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to full-scale over a period of approximately 1ms and this soft-start can be monitored by observing the PROG pin voltage. This has the effect of minimizing the transient current load on the power supply during start-up.

Thermal Shutdown

The LTC4425 includes a thermal shutdown circuit in addition to the thermal regulator. If for any reason, the die temperature exceeds 160°C, the entire part shuts down. It resumes normal operation once the temperature drops by about 14°C, to approximately 146°C.

APPLICATIONS INFORMATION

Programming the Output Voltage

In LDO mode, the LTC4425 output voltage can be programmed for any voltage between 2.7V and V_{IN} by using a resistor divider from V_{OUT} pin to GND via the FB pin such that:

$$V_{OUT} = V_{FB} \bullet (1 + R_{FB1}/R_{FB2})$$

where V_{FB} is 1.2V. See Figure 3.

Typical values for R_{FB} are in the range of 40k to 1M. Too small a resistor will result in a large quiescent current whereas too large a resistor coupled with FB pin capacitance will create an additional pole and may cause loop instability.

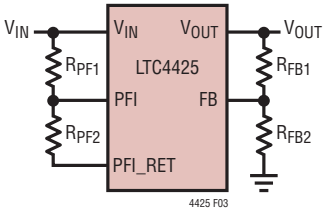


Figure 3. Programming Output Voltage and Input Threshold for Power Fail Comparator.

Programming the Input Voltage Threshold for Power Fail Status Indicator

The input voltage below which the power fail status pin $\overline{PFO}$ indicates a power-fail condition is programmed by using a resistor divider from the V_{IN} pin to the PFI_RET pin via the PFI pin such that:

$$V_{IN,\,\overline{PFO}} = V_{PFI} \bullet (1 + R_{PF1}/R_{PF2})$$

where V_{PFI} is 1.2V. See Figure 3.

Typical values for R_{PF} are in the range of 40k to 1M. In shutdown mode, this divider network is disconnected from ground via the PFI_RET pin to save the quiescent current drawn by the network.

Programming the Charge Current

The LTC4425 charge current is programmed using a single resistor from the PROG pin to ground. The charge current out of the V_{OUT} pin is 1000 times the current out of the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = 1000 \bullet (1V/I_{CHRG}),\ I_{CHRG} = 1000 \bullet (1V/R_{PROG})$$

where I_{CHRG} is the charge current out of the V_{OUT} pin. The charge current out of the V_{OUT} pin can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{CHRG} = 1000 \bullet (V_{PROG}/R_{PROG})$$

Stability Considerations

In LDO mode, the LTC4425 supercapacitor charger has two principal control loops: constant-voltage and constant-current. The constant-voltage loop is stable when connected to a supercap of at least 0.2F. However, when disconnected from the supercap, the voltage loop requires at least 10µF capacitance in series with 500Ω resistance for stability.

In constant-current mode, the PROG pin voltage is in the feedback loop, not the V_{OUT} pin voltage. Because of the additional pole created by the PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with a program resistor as high as 100k. However, any additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq 1/(2\pi \bullet 100kHz \bullet C_{PROG})$$

Board Layout Considerations

To be able to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the LTC4425's two packages have a good thermal contact to the PC board ground. Correctly soldered to a 2500mm^2 double-sided 1 oz. copper board, the DFN package has a thermal resistance of approximately 43°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in a thermal resistance far greater than 43°C/W.

APPLICATIONS INFORMATION

Charge Current Reduction by the Thermal Regulator

To protect the part against excessive heat generated by internal power dissipation, the LTC4425 is equipped with a thermal regulator which automatically reduces the charge current to maintain a maximum die temperature of 105°C. Ignoring the quiescent current, the power dissipation can be approximated by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{CHRG}$$

If θ_{JA} is the thermal resistance and T_A is the ambient temperature, then the die temperature can be calculated as:

$$T_{DIE} = T_A + P_D \bullet \theta_{JA}$$

When the part is in thermal regulation, the die temperature is 105°C and for a given V_{IN} and V_{OUT}, the charge current can be determined by the following equation:

$$I_{CHRG} = \frac{105 - T_A}{(V_{IN} - V_{OUT}) \bullet \theta_{JA}}$$

For example, if the LTC4425 in the DFN package is used in LDO mode to charge a completely discharged supercap stack (V_{OUT} = 0V) at a room temperature of 25°C from a 5V source, the charge current, at first, will be limited to approximately:

$$I_{CHRG} = \frac{105°C - 25°C}{(5-0)V \bullet 43°C/W} = \frac{80°C}{215°C/A} = 372mA$$

As the output voltage rises, the charge current will gradually rise to the full charge current programmed by the PROG pin resistor as long as the constant-current loop is in control. If the LTC4425 is programmed for a charge current of 2A, the output voltage at which the part will deliver full charge current can be determined by the following equation:

$$V_{OUT} = V_{IN} - \frac{105 - T_A}{I_{CHRG} \bullet \theta_{JA}}$$

Using the previous example, for full charge current, the output voltage has to rise to at least:

$$V_{OUT} = 5V - \frac{(105-25)°C}{2A \bullet 43°C/W} = 5V - \frac{80°C}{86°C/V} = 4.07V$$

Figure 4 shows the graph of charge current vs output voltage when the charge current profile is turned off by shorting the FB pin to GND and the charge current is limited by thermal regulation.

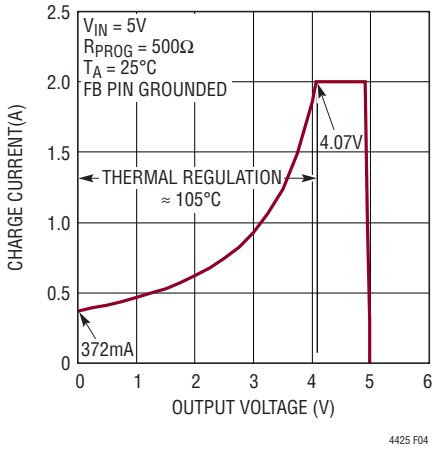


Figure 4. Charge Current vs Output Voltage under Thermal Regulation (LDO Mode)

Charging a Single Supercapacitor

The LTC4425 can also be used to charge a single supercapacitor by connecting two series-connected matched ceramic capacitors with a minimum capacitance of 100µF in parallel with the supercapacitor as shown in Figure 5. Refer to Table 1 for supercapacitor manufacturers.

Table 1. Supercapacitor Manufacturers

CAP-XX	www.cap-xx.com
NESS CAP	www.nesscap.com
Maxwell	www.maxwell.com
Bussmann	www.cooperbussmann.com
AVX	www.avx.com
Illinois Capacitor	www.illcap.com
Tecate Group	www.tecategroup.com

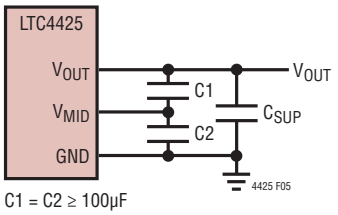
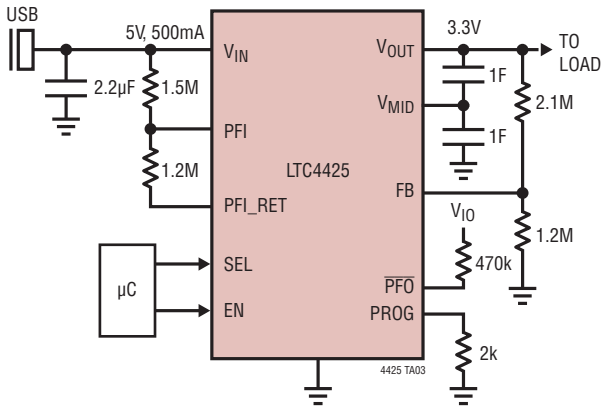


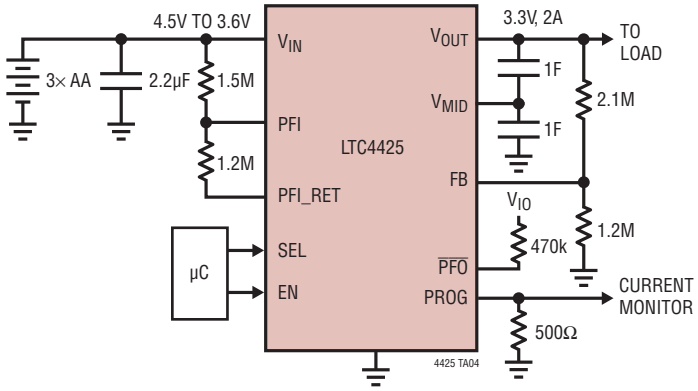
Figure 5. Charging a Single Supercapacitor

TYPICAL APPLICATIONS

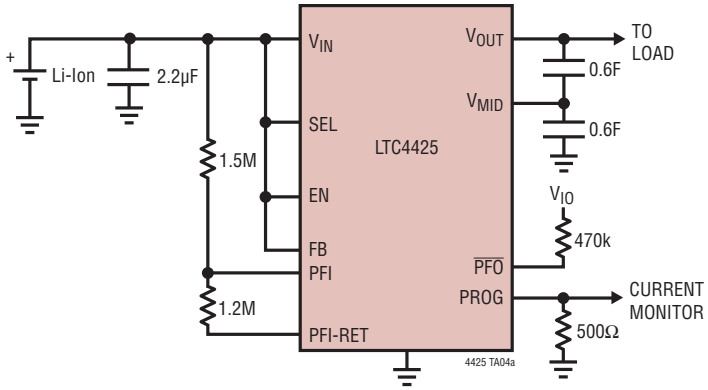
USB to High Peak Power 3.3V Charging



3 × AA Alkaline to High Peak Power 3.3V Charging

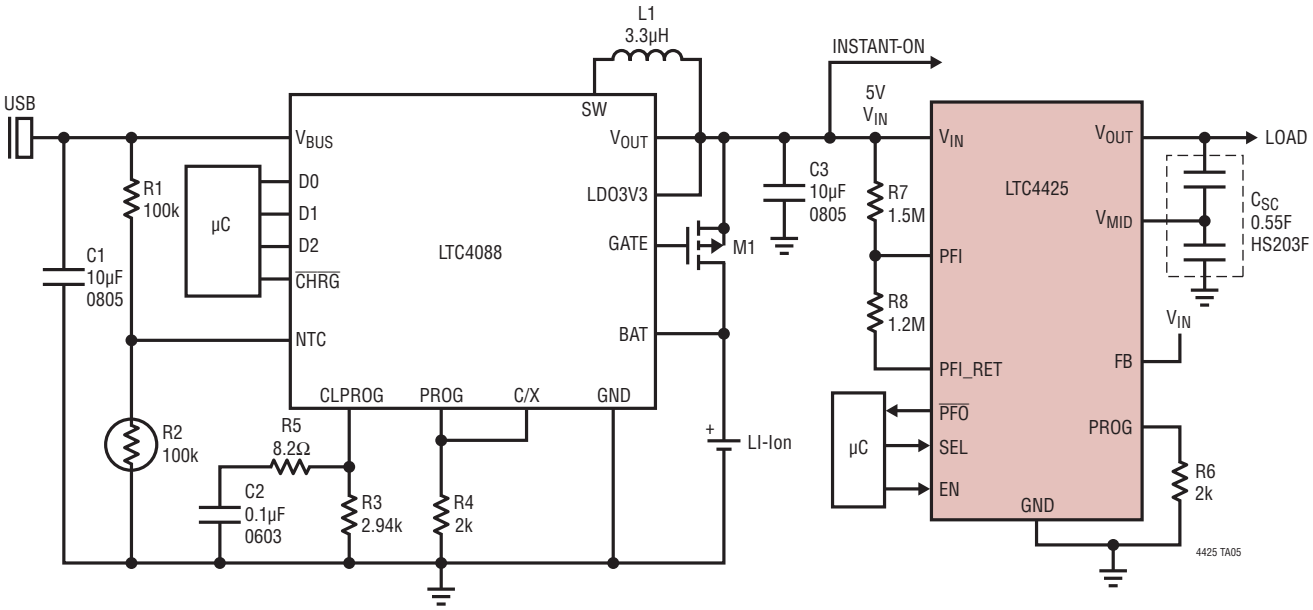


Li-Ion High Peak Power Battery Buffer



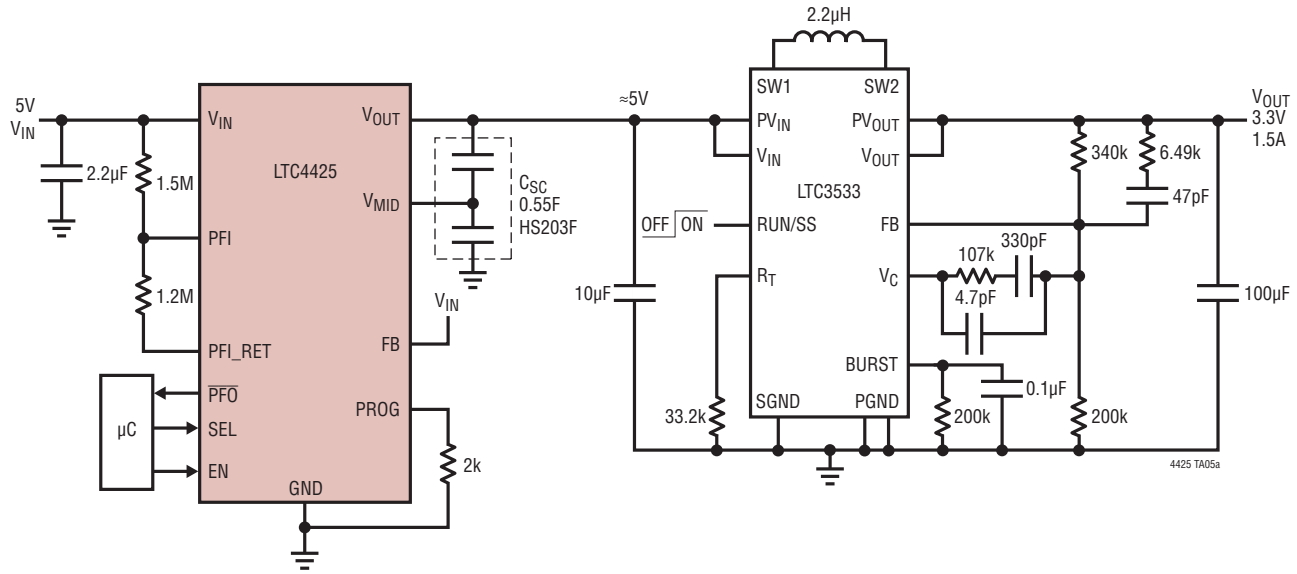
TYPICAL APPLICATIONS

High Current USB Charging with Power Path Control



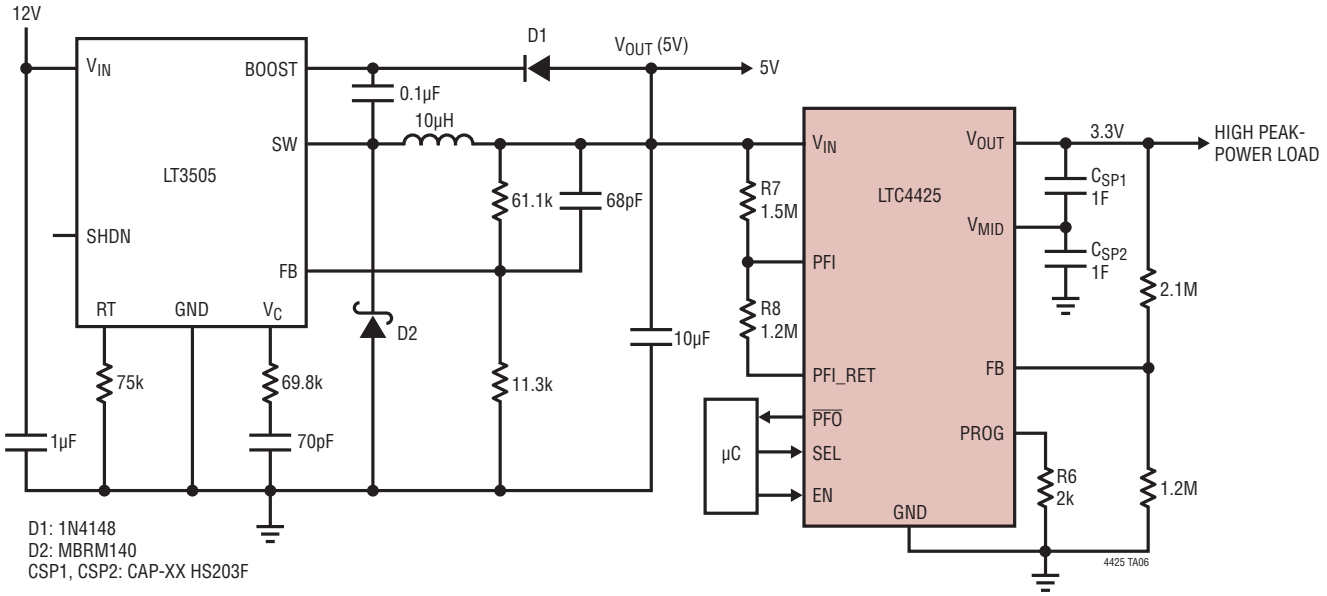
L1: COILCRAFT LPS4018-332MLC
M1: SILICONIX Si2333
R2: VISHAY-DALE NTHS0603N011-N1003F
C1, C3: MURATA GRM21BR61A106KE19
C2: MURATA GRM188R71C104KA01
CSC: CAP-XX HS203F

3.3V Peak-Power/Back-up Supply

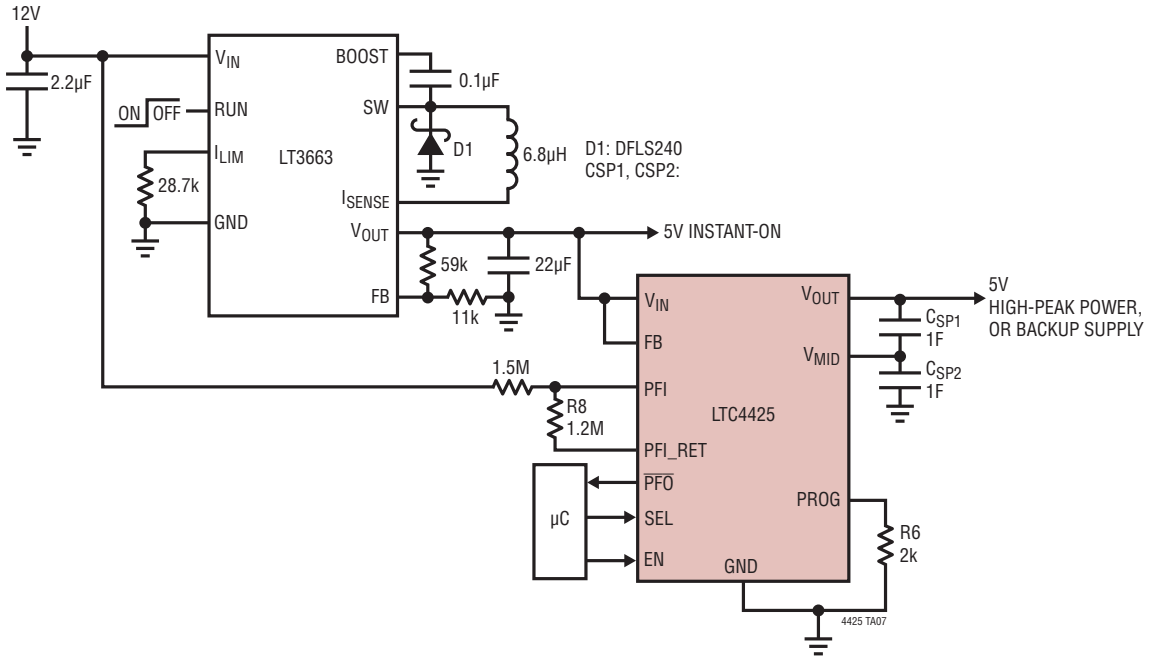


TYPICAL APPLICATIONS

12V to 5V/3.3V High Peak Power Supply

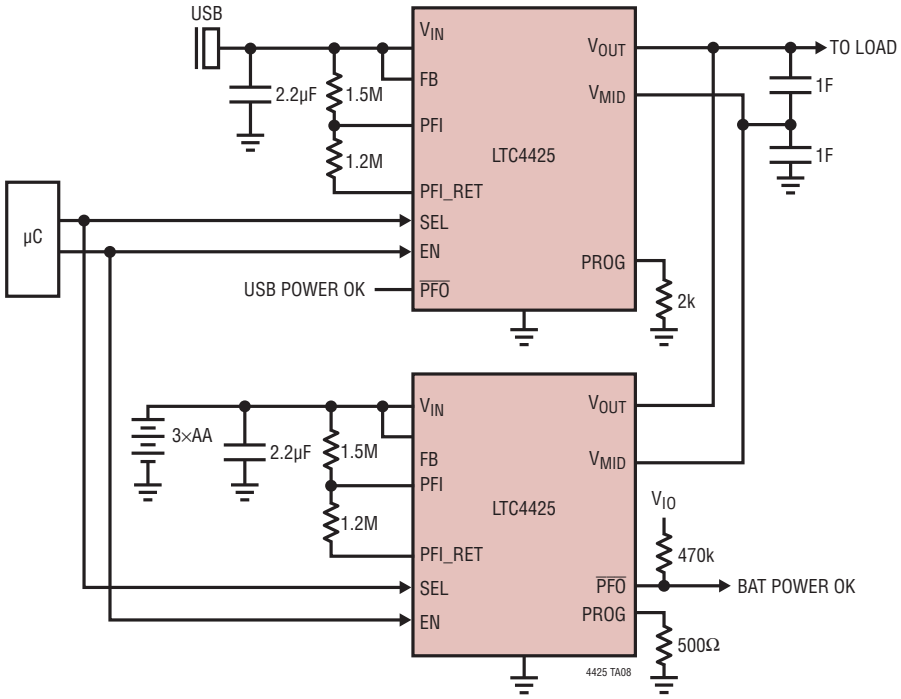


12V Input to 5V Outputs with Input Voltage Monitoring



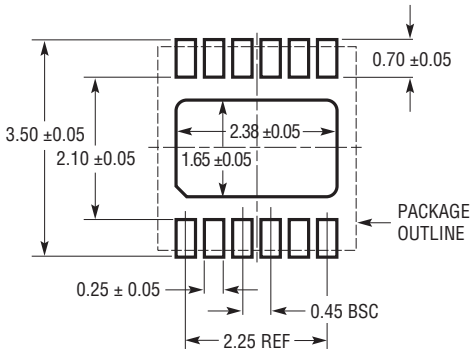
TYPICAL APPLICATIONS

Redundant High Peak Power Battery Supplies

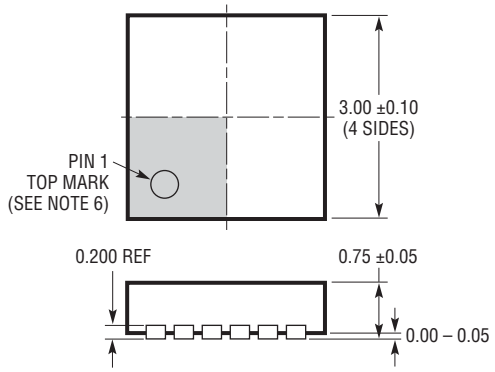


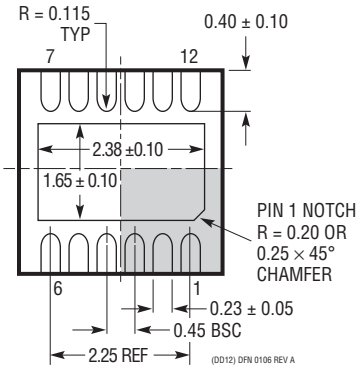
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



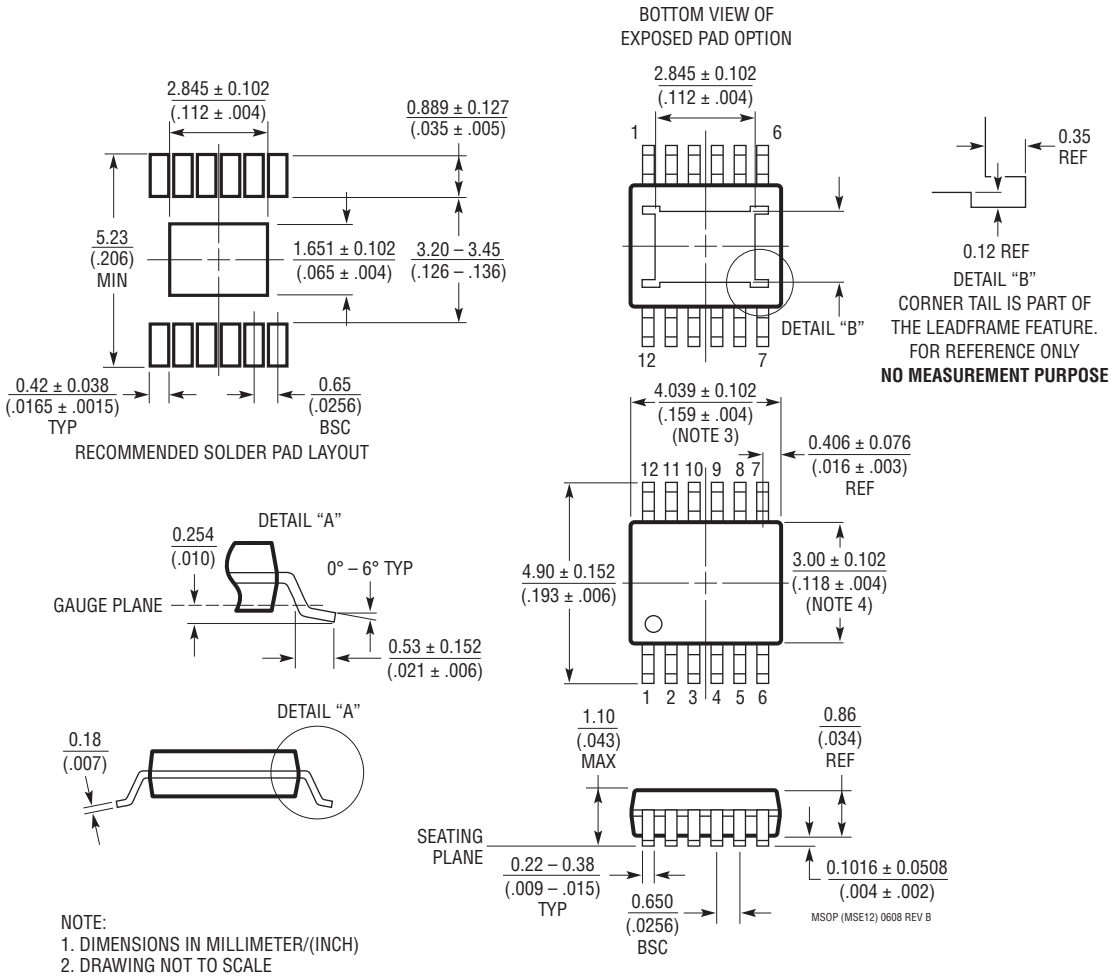


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

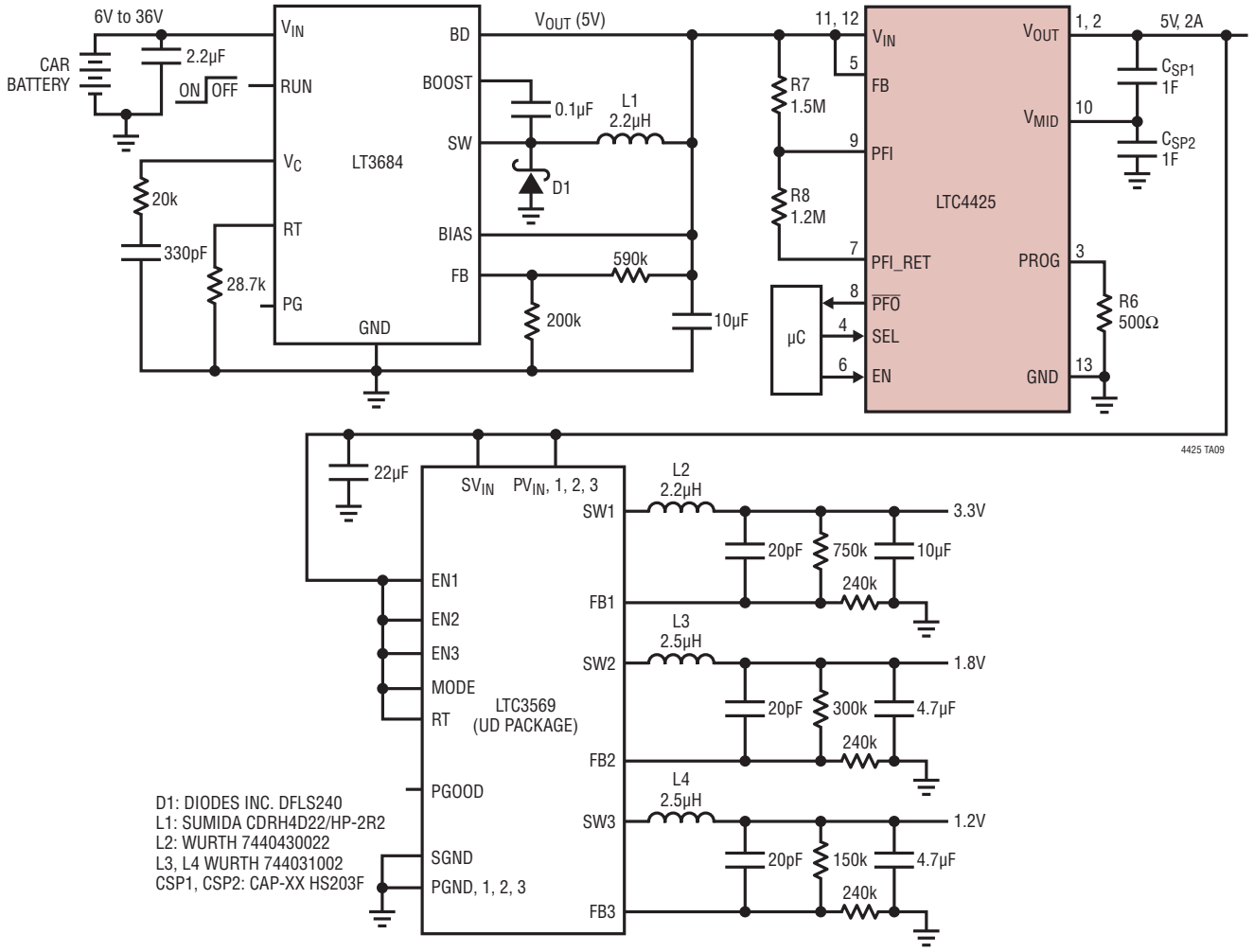
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Embedded Automotive Backup Controller



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3225-1 LTC3225	150mA Supercapacitor Charger	Programmable Supercapacitor Charger Designed to Charge Two Supercapacitors in Series to a Fixed Output Voltage (4.8V/5/3V Selectable)
LT3485-0/LT3485-1/ LT3485-2/LT3485-3	1.4A/0.7A/1A/2A Photoflash Capacitor Charger with Output Voltage Monitor and IGBT	V_{IN}; 1.8V to 10V, Charge Time = 3.7 Seconds for the LT3485-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 3mm × 3mm 10-Lead DFN
LT3750	Capacitor Charger Controller	Charges Any Size Capacitor, 10-Lead MS Package
LT3751	Capacitor Controller with Regulation	Charges Any Size Capacitor, 4mm × 5mm QFN-20 Package

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