

FPF1003A IntelliMAX™ Advanced Load Management Products

Features

- 1.2 to 5.5V Input Voltage Range
- $R_{DS(ON)} = 30\text{ m}\Omega$ @ $V_{IN} = 5.5\text{V}$
- $R_{DS(ON)} = 35\text{ m}\Omega$ @ $V_{IN} = 3.3\text{V}$
- ESD Protected, above 5500V HBM
- RoHS Compliant

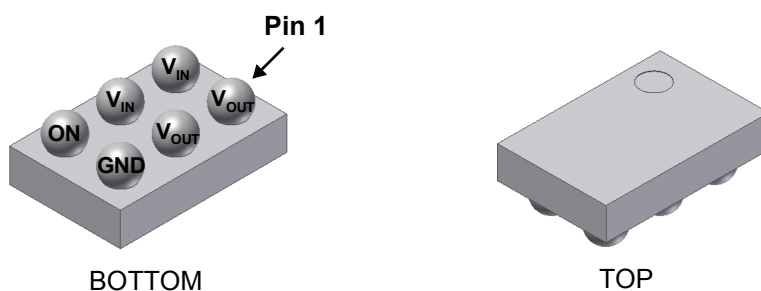
Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Hot Swap Supplies

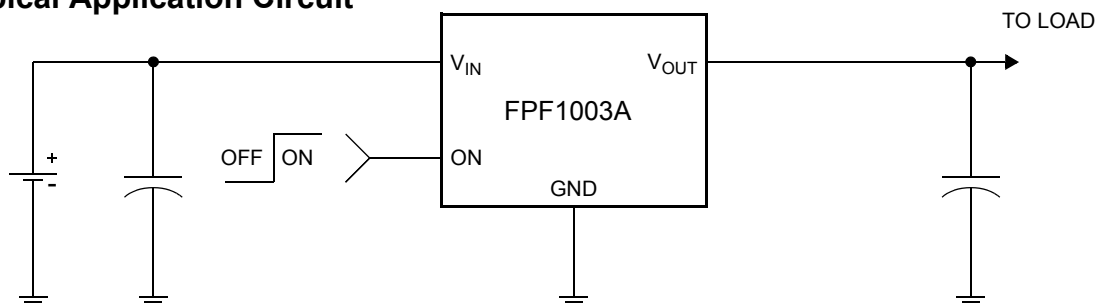
General Description

The FPF1003A is low RDS P-Channel MOSFET load switches with controlled turn-on. The input voltage range operates from 1.2V to 5.5V to fulfill today's Ultra Portable Device's supply requirement. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signal.

FPF1003A is available in a space-saving 1.0x1.5 mm² chip scale package, 1.0X1.5CSP-6.



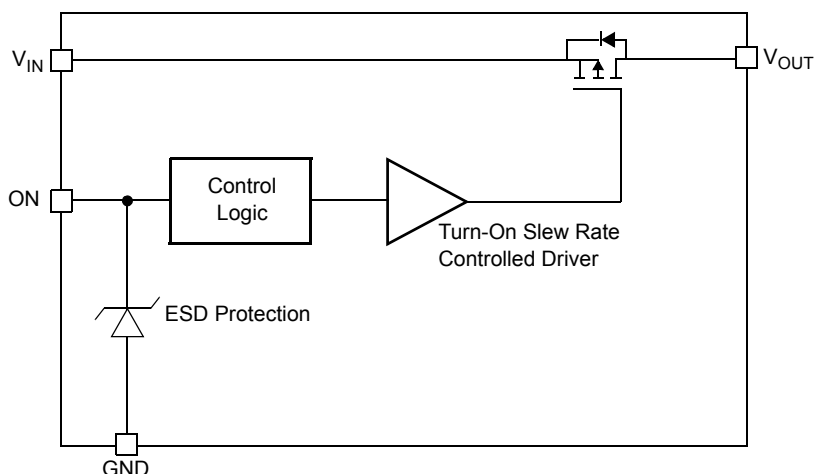
Typical Application Circuit



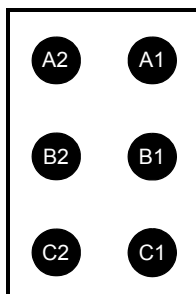
Ordering Information

Part	Switch	Input buffer	Output Discharge	ON Pin Activity
FPF1003A	30mΩ, PMOS	Schmitt	NA	Active HI

Functional Block Diagram



Pin Configuration



1.0 x 1.5 CSP Bottom View

Pin Description

Pin	Name	Function
A2, B2	V_{IN}	Supply Input: Input to the power switch and the supply voltage for the IC
C2	ON	ON Control Input
A1, B1	V_{OUT}	Switch Output: Output of the power switch
C1	GND	Ground

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{IN} , V_{OUT} , ON to GND		-0.3	6	V
Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)			1.2	W
Maximum Continuous Switch Current			2.0	A
Operating Temperature Range		-40	125	$^\circ\text{C}$
Storage Temperature		-65	150	$^\circ\text{C}$
Thermal Resistance, Junction to Ambient			85	$^\circ\text{C/W}$
Electrostatic Discharge Protection	HBM	5500		V
	CDM	1500		V

Recommended Operating Range

Parameter	Min	Max	Unit
V_{IN}	1.2	5.5	V
Ambient Operating Temperature, T_A	-40	85	°C

Electrical Characteristics

V_{IN} = 1.2 to 5.5V, T_A = -40 to +85°C unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Basic Operation						
Operating Voltage	V_{IN}		1.2		5.5	V
Quiescent Current	I_Q	$I_{OUT} = 0\text{mA}$, $V_{IN} = V_{ON}$			1	μA
Off Supply Current	$I_{Q(off)}$	$V_{ON} = \text{GND}$, $OUT = \text{open}$			1	μA
Off Switch Current	$I_{SD(off)}$	$V_{ON} = \text{GND}$, $V_{OUT} = 0$ @ $V_{IN} = 5.5\text{V}$, $T_A = 85^\circ\text{C}$			1	μA
		$V_{ON} = \text{GND}$, $V_{OUT} = 0$ @ $V_{IN} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$		10	100	nA
On-Resistance	R_{ON}	$V_{IN} = 5.5\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^\circ\text{C}$		20	30	mΩ
		$V_{IN} = 3.3\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^\circ\text{C}$		25	35	
		$V_{IN} = 1.5\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^\circ\text{C}$		50	75	
		$V_{IN} = 1.2\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^\circ\text{C}$		95	150	
		$V_{IN} = 3.3\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 85^\circ\text{C}$		30	42	
		$V_{IN} = 3.3\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	12		42	
ON Input Logic High Voltage	V_{IH}	$V_{IN} = 2.7\text{V}$ to 5.5V	2			V
		$V_{IN} = 1.2\text{V}$	0.8			
ON Input Logic Low Voltage	V_{IL}	$V_{IN} = 2.7\text{V}$ to 5.5V			0.8	V
		$V_{IN} = 1.2\text{V}$			0.35	
ON Input Leakage		$V_{ON} = V_{IN}$ or GND			1	μA
Dynamic						
Turn On Delay	t_{ON}	$V_{IN} = 3.3\text{V}$, $R_L = 500\Omega$, $C_L = 0.1\mu\text{F}$, $T_A = 25^\circ\text{C}$		13		μs
Turn Off Delay	t_{OFF}	$V_{IN} = 3.3\text{V}$, $R_L = 500\Omega$, $C_L = 0.1\mu\text{F}$, $T_A = 25^\circ\text{C}$		45		μs
V_{OUT} Rise Time	t_R	$V_{IN} = 3.3\text{V}$, $R_L = 500\Omega$, $C_L = 0.1\mu\text{F}$, $T_A = 25^\circ\text{C}$		13		μs
V_{OUT} Fall Time	t_F	$V_{IN} = 3.3\text{V}$, $R_L = 500\Omega$, $C_L = 0.1\mu\text{F}$, $T_A = 25^\circ\text{C}$		113		μs

Note 1: Package power dissipation on 1square inch pad, 2 oz. copper board.

Typical Characteristics

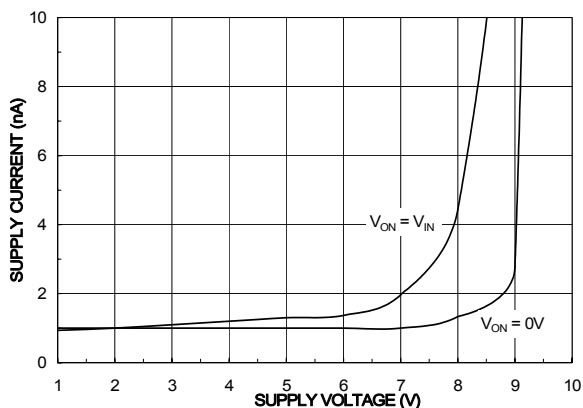


Figure 1. Quiescent Current vs. V_{IN}

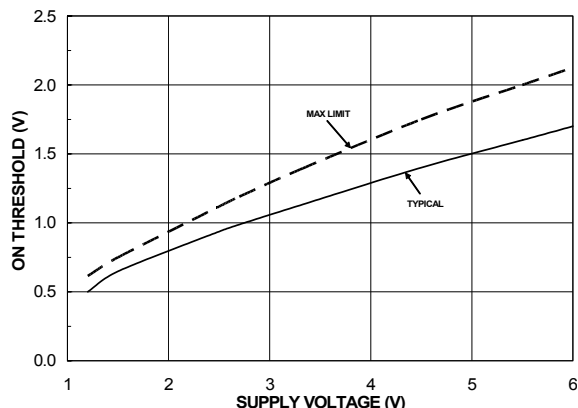


Figure 2. ON Threshold vs. V_{IN}

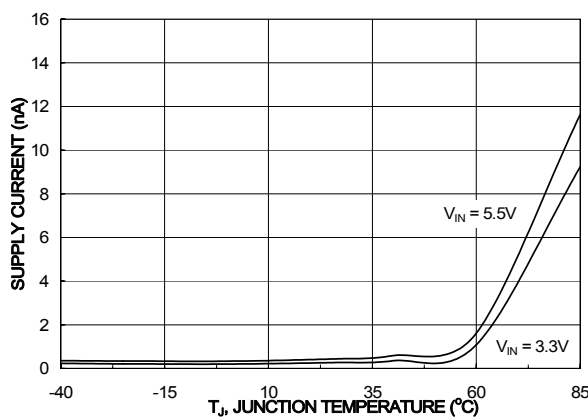


Figure 3. Quiescent Current vs. Temperature

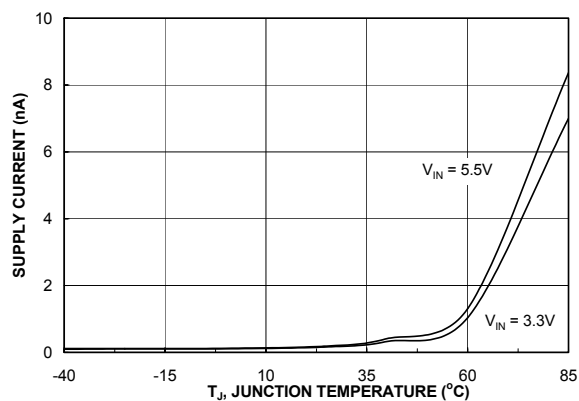


Figure 4. Quiescent Current (off) vs. Temperature

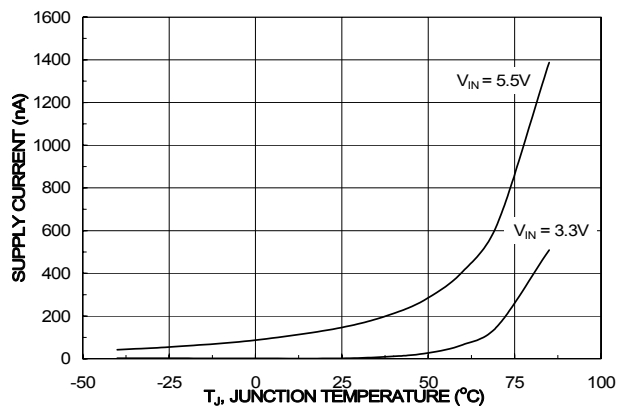


Figure 5. $I_{\text{SWITCH-OFF}}$ Current vs. Temperature

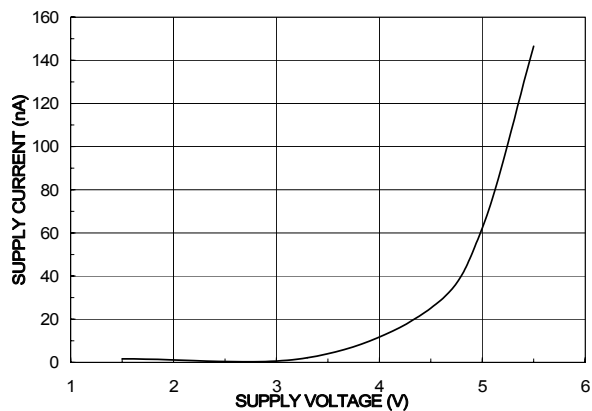


Figure 6. $I_{\text{SWITCH-OFF}}$ Current vs. V_{IN}

Typical Characteristics

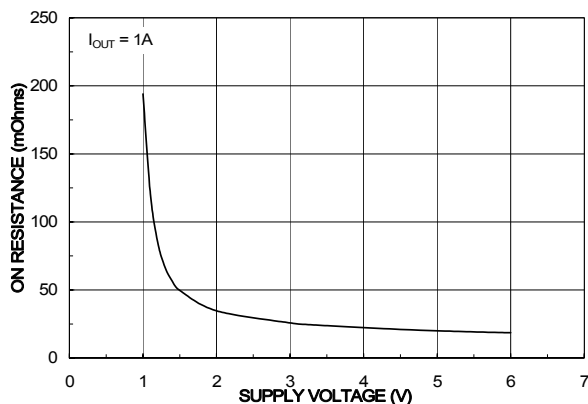


Figure 7. R_{ON} vs. V_{IN}

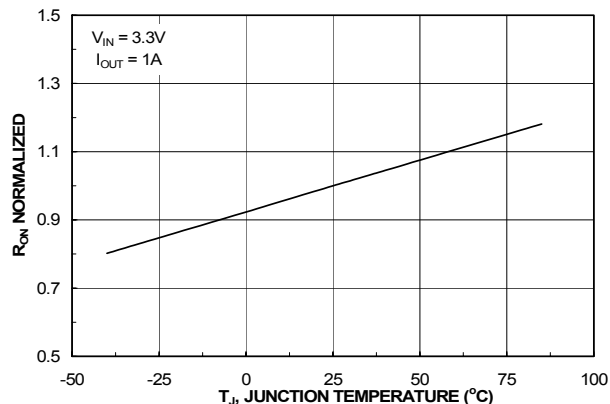


Figure 8. R_{ON} vs. Temperature

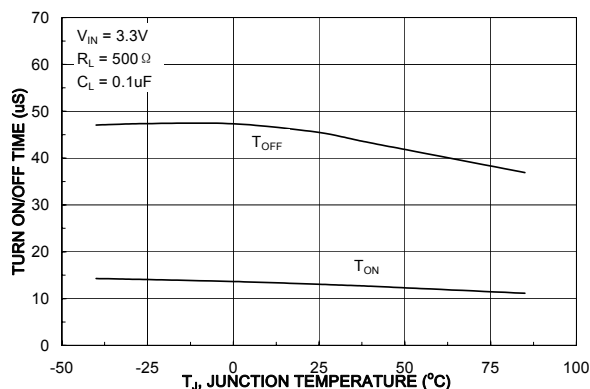


Figure 9. T_{ON}/T_{OFF} vs. Temperature

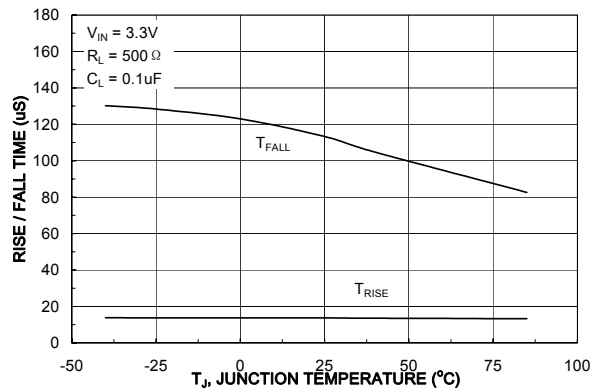


Figure 10. T_{RISE}/T_{FALL} vs. Temperature

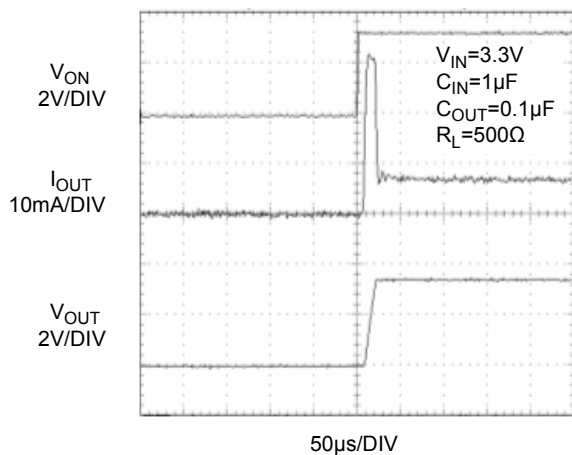


Figure 11. T_{ON} Response

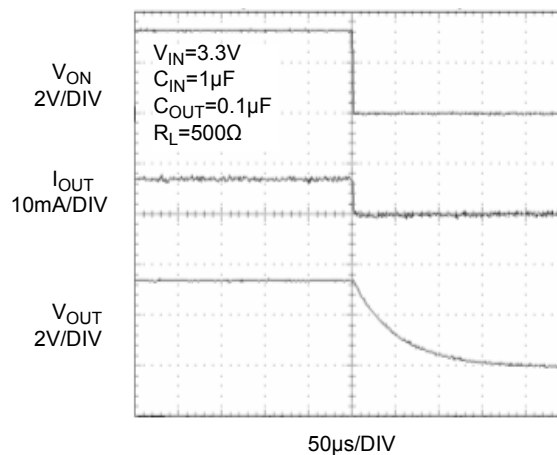


Figure 12. T_{OFF} Response

Typical Characteristics

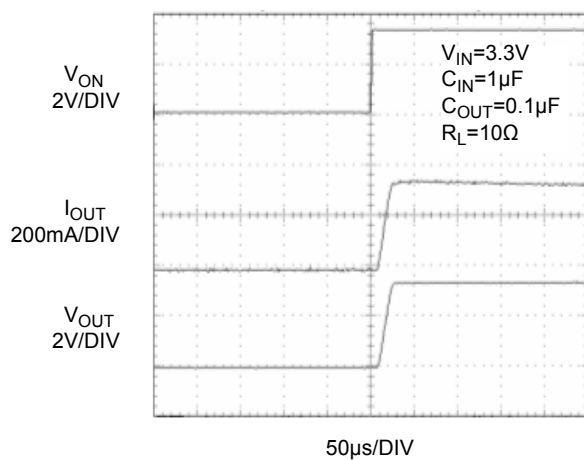


Figure 13. T_{ON} Response

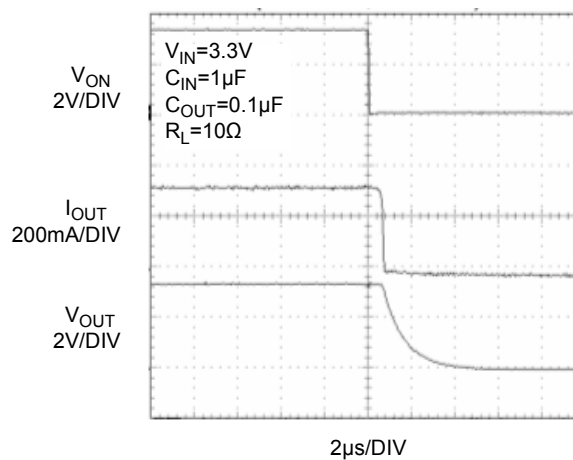


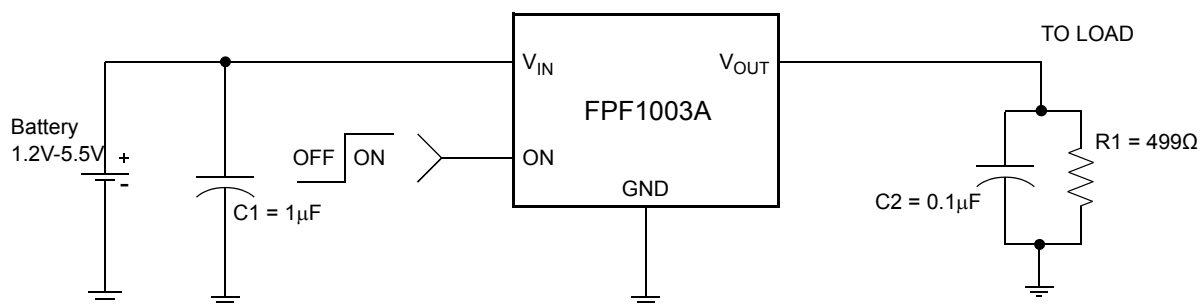
Figure 14. T_{OFF} Response

Description of Operation

The FPF1003A is low $R_{DS(ON)}$ P-Channel load switches with controlled turn-on. The core of each device is a 30mΩ P-Channel MOSFET and a controller capable of functioning over a wide input operating range of 1.2-5.5V. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signal.

Application Information

Typical Application



Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns-on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 0.1μF ceramic capacitor, C_{IN} , must be placed close to the V_{IN} pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

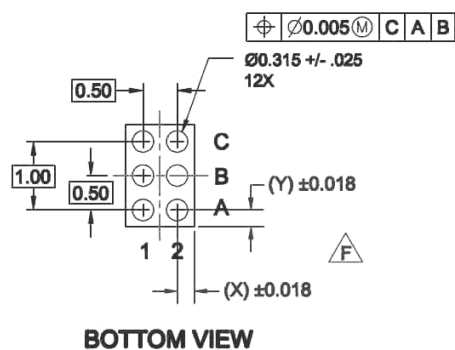
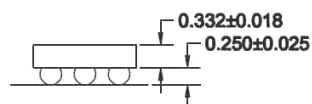
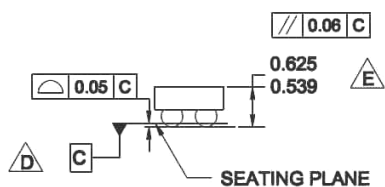
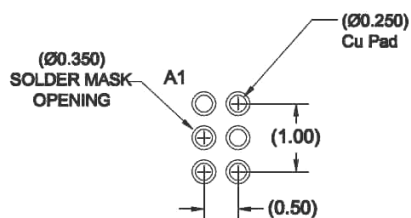
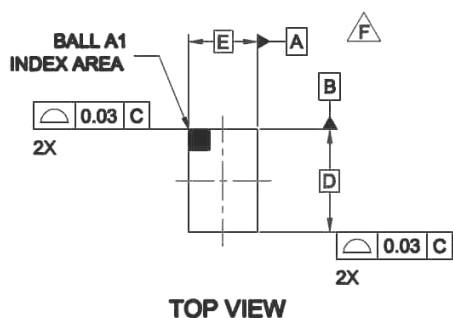
Output Capacitor

A 0.1μF capacitor, C_{OUT} , should be placed between V_{OUT} and GND. This capacitor will prevent parasitic board inductance from forcing V_{OUT} below GND when the switch turns-off. Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_{OUT} is highly recommended. A C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Dimensional Outline and Pad Layout



NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. BALL COMPOSITION: Sn95.5Ag3.9Cu0.6
- H. DRAWING FILNAME: MKT-UC006ARev1.

Product	D	E	X	Y
FPF1003A	1.500+/-0.030	1.000+/- 0.030	0.240	0.240

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