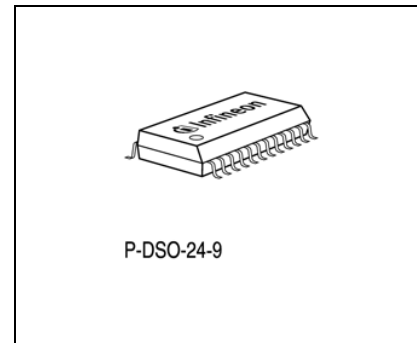


2-Phase Stepper-Motor Driver Bipolar-IC

TLE 4729 G

Features

- 2×0.7 amp. full bridge outputs
- Integrated driver, control logic and current control (chopper)
- Very low current consumption in inhibit mode
- Fast free-wheeling diodes
- Max. supply voltage 45 V
- Output stages are free of crossover current
- Offset-phase turn-ON of output stages
- All outputs short-circuit proof
- Error-flag for overload, open load, over-temperature
- SMD package P-DSO-24-9



| Type | Ordering Code | Package |
|------------|---------------|------------------|
| TLE 4729 G | on request | P-DSO-24-9 (SMD) |

Functional Description

TLE 4729 G is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate by constant current. It is fully pin and function compatible except the current programming is inverse to the TLE 4728 G with an additional inhibit feature. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.7 A per phase at operating voltages up to 16 V.

The direction and value of current are programmable for each phase via separate control inputs. In the case of low at all four current program inputs the device is switched to inhibit mode automatically. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in full-bridge configuration include fast integrated freewheeling diodes and are free of crossover current. The device can be driven directly by a microprocessor in several modes by programming phase direction and current control of each bridge independently.

With the two error outputs the TLE 4729 G signals malfunction of the device. Setting the control inputs low resets the error flag and by reactivating the bridges one by one the location of the error can be found.

Pin Configuration

(top view)

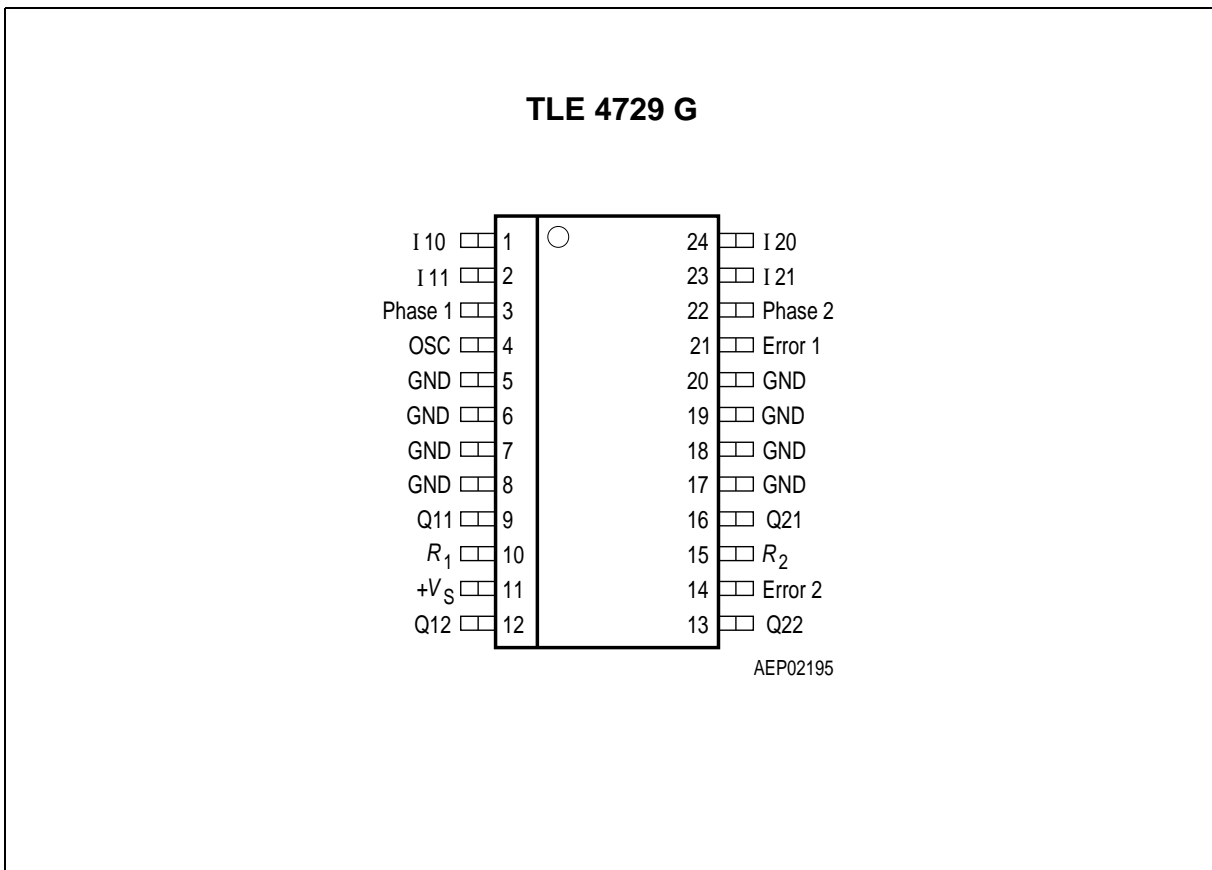


Figure 1

Pin Definitions and Functions

| Pin | Function | | | | | | | | | | | | | | | | | | | | |
|-----------------------|--|-------------------------------|--------------------------|---------------|-------------------------|---|---|---|--------------------------|---|---|-------------------------------|------|---|---|------------------|-------------|---|---|------------------------------|------------|
| 1, 2, 23, 24 | <p>Digital control inputs IX0, IX1 for the magnitude of the current of the particular phase.</p> <p>$I_{\text{set}} = 450 \text{ mA}$ with $R_{\text{sense}} = 1 \, \Omega$</p> <table><tr><th>IX1</th><th>IX0</th><th>Phase Current</th><th>Example of Motor Status</th></tr><tr><td>L</td><td>L</td><td>0</td><td>No current¹⁾</td></tr><tr><td>L</td><td>H</td><td>$0.155 \times I_{\text{set}}$</td><td>Hold</td></tr><tr><td>H</td><td>L</td><td>I_{set}</td><td>Normal mode</td></tr><tr><td>H</td><td>H</td><td>$1.55 \times I_{\text{set}}$</td><td>Accelerate</td></tr></table> <p>¹⁾ "No current" in both bridges inhibits the circuit and current consumption will sink below 50 μA (inhibit-mode)</p> | IX1 | IX0 | Phase Current | Example of Motor Status | L | L | 0 | No current ¹⁾ | L | H | $0.155 \times I_{\text{set}}$ | Hold | H | L | I_{set} | Normal mode | H | H | $1.55 \times I_{\text{set}}$ | Accelerate |
| IX1 | IX0 | Phase Current | Example of Motor Status | | | | | | | | | | | | | | | | | | |
| L | L | 0 | No current ¹⁾ | | | | | | | | | | | | | | | | | | |
| L | H | $0.155 \times I_{\text{set}}$ | Hold | | | | | | | | | | | | | | | | | | |
| H | L | I_{set} | Normal mode | | | | | | | | | | | | | | | | | | |
| H | H | $1.55 \times I_{\text{set}}$ | Accelerate | | | | | | | | | | | | | | | | | | |
| 3 | <p>Input phase 1; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.</p> | | | | | | | | | | | | | | | | | | | | |
| 5 ... 8, 17 ... 20 | <p>Ground; all pins are connected at leadframe internally.</p> | | | | | | | | | | | | | | | | | | | | |
| 4 | <p>Oscillator; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.</p> | | | | | | | | | | | | | | | | | | | | |
| 10 | <p>Resistor R_1 for sensing the current in phase 1.</p> | | | | | | | | | | | | | | | | | | | | |
| 9, 12 | <p>Push-pull outputs Q11, Q12 for phase 1 with integrated free-wheeling diodes.</p> | | | | | | | | | | | | | | | | | | | | |
| 11 | <p>Supply voltage; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 47 μF in parallel with a ceramic capacitor of 100 nF.</p> | | | | | | | | | | | | | | | | | | | | |
| 14 | <p>Error 2 output; signals with "low" the errors: short circuit to ground of one or more outputs or over-temperature.</p> | | | | | | | | | | | | | | | | | | | | |
| 13, 16 | <p>Push-pull outputs Q22, Q21 for phase 2 with integrated free-wheeling diodes.</p> | | | | | | | | | | | | | | | | | | | | |
| 15 | <p>Resistor R_2 for sensing the current in phase 2.</p> | | | | | | | | | | | | | | | | | | | | |
| 21 | <p>Error 1 output; signals with "low" the errors: open load or short circuit to + V_S of one or more outputs or short circuit of the load or over-temperature.</p> | | | | | | | | | | | | | | | | | | | | |
| 22 | <p>Input phase 2; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L-potential in the reverse direction.</p> | | | | | | | | | | | | | | | | | | | | |

Block Diagram

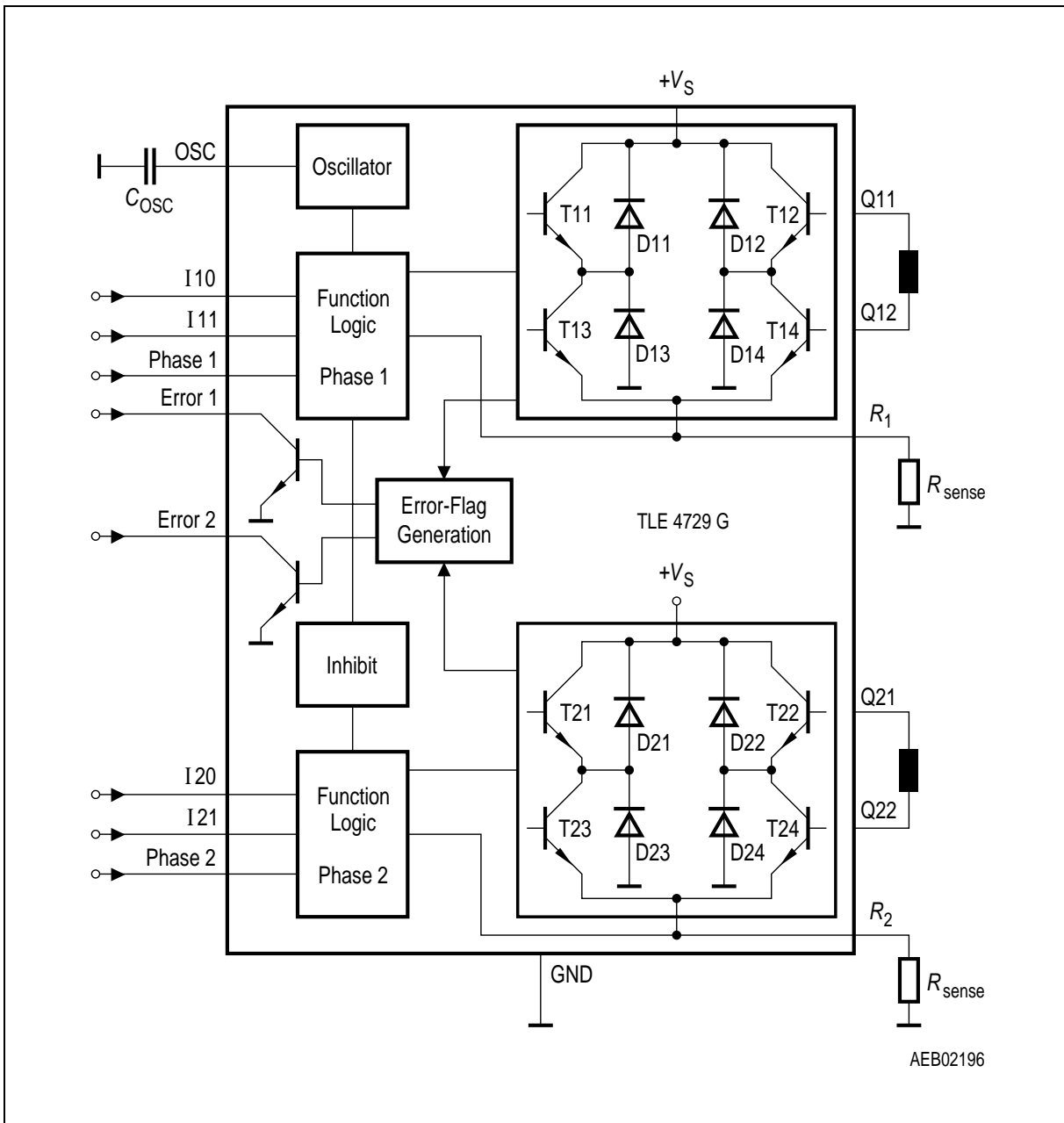


Figure 2

Absolute Maximum Ratings

 $T_j = -40 \text{ to } 150 \text{ }^{\circ}\text{C}$

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|--|--------------------|--------------|------|--------------------|-------------------|
| | | min. | max. | | |
| Supply voltage | V_S | - 0.3 | 45 | V | – |
| Error outputs | V_{Err} | - 0.3 | 45 | V | – |
| | I_{Err} | – | 3 | mA | – |
| Output current | I_Q | - 1 | 1 | A | – |
| Ground current | I_{GND} | - 2 | – | A | – |
| Logic inputs | V_{IXX} | - 15 | 15 | V | IXX; Phase 1, 2 |
| Oscillator voltage | V_{OSC} | - 0.3 | 6 | V | – |
| R_1, R_2 input voltage | V_{RX} | - 0.3 | 5 | V | – |
| Junction temperature | T_j | - 40 | 150 | $^{\circ}\text{C}$ | |
| Storage temperature | T_{stg} | - 50 | 150 | $^{\circ}\text{C}$ | – |
| Thermal resistances | | | | | |
| Junction-ambient | $R_{\text{th ja}}$ | – | 75 | K/W | – |
| Junction-ambient (soldered on a 35 μm thick 20 cm^2 PC board copper area) | $R_{\text{th ja}}$ | – | 50 | K/W | – |
| Junction-case | $R_{\text{th jc}}$ | – | 15 | K/W | Measured on pin 5 |

Operating Range

| | | | | | |
|------------------|------------------|-------|-----|--------------------|--|
| Supply voltage | V_S | 5 | 16 | V | – |
| Case temperature | T_C | - 40 | 110 | $^{\circ}\text{C}$ | Measured on pin 5 $P_{\text{diss}} = 2 \text{ W}$ |
| Output current | I_Q | - 800 | 800 | mA | – |
| Logic inputs | V_{IXX} | - 5 | + 6 | V | IXX; Phase 1, 2 |
| Error outputs | V_{Err} | – | 25 | V | – |
| | I_{Err} | 0 | 1 | mA | – |

Characteristics

$V_S = 6$ to 16 V; $T_j = -40$ to 130 °C

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Current Consumption

| | | | | | | |
|--------------|-------|----|----|----|----|---|
| From + V_S | I_S | – | – | 50 | µA | $IXX = L$; $V_S = 12$ V; $T_j \leq 85$ °C $I_{Q1,2} = 0$ A |
| From + V_S | I_S | 20 | 30 | 50 | mA | |

Oscillator

| | | | | | | |
|-------------------------|------------|-----|-----|-----|-----|--------------------|
| Output charging current | I_{OSC} | 90 | 120 | 150 | µA | – |
| Charging threshold | V_{OSCL} | 0.8 | 1.3 | 1.9 | V | – |
| Discharging threshold | V_{OSCH} | 1.7 | 2.3 | 2.9 | V | – |
| Frequency | f_{OSC} | 18 | 24 | 30 | kHz | $C_{OSC} = 2.2$ nF |

Phase Current ($V_S = 9 \dots 16$ V)

| | | | | | | |
|---|----------|-----|-----|-----|----|-----------------------|
| Mode “no current” | I_Q | – | 0 | – | mA | $IX0 = L$; $IX1 = L$ |
| Voltage threshold of current Comparator at R_{sense} in mode: | | | | | | |
| Hold | V_{ch} | 40 | 70 | 100 | mV | $IX0 = H$; $IX1 = L$ |
| Setpoint | V_{cs} | 410 | 450 | 510 | mV | $IX0 = L$; $IX1 = H$ |
| Accelerate | V_{ca} | 630 | 700 | 800 | mV | $IX0 = H$; $IX1 = H$ |

Logic Inputs (Phase X)

| | | | | | | |
|-----------------|-----------|-------|------|-----|----|---------------|
| Threshold | V_I | 1.2 | 1.7 | 2.2 | V | – |
| Hysteresis | V_{IHy} | – | 200 | – | mV | – |
| L-input current | I_{IL} | – 10 | – 1 | 1 | µA | $V_I = 1.2$ V |
| L-input current | I_{IL} | – 100 | – 20 | – 5 | µA | $V_I = 0$ V |
| H-input current | I_{IH} | – 1 | 0 | 10 | µA | $V_I = 5$ V |

Logic Inputs ($IX1$; $IX0$)

| | | | | | | |
|-----------------|-----------|-------|-----|-----|----|-------------|
| Threshold | V_I | 0.8 | 1.7 | 2.2 | V | – |
| Hysteresis | V_{IHy} | – | 200 | – | mV | – |
| L-input current | I_{IL} | – 100 | – | + 5 | µA | $V_I = 0$ V |
| H-input current | I_{IH} | 5 | 20 | 50 | µA | $V_I = 5$ V |

Characteristics (cont'd)
 $V_S = 6 \text{ to } 16 \text{ V}; T_j = -40 \text{ to } 130 \text{ }^\circ\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Error Outputs

| | | | | | | |
|--------------------|---------------------|----|-----|-----|---------------|---------------------------------|
| Saturation voltage | V_{ErrSat} | 50 | 200 | 500 | mV | $I_{\text{Err}} = 1 \text{ mA}$ |
| Leakage current | I_{ErrL} | – | – | 10 | μA | $V_{\text{Err}} = 25 \text{ V}$ |

Thermal Protection

| | | | | | | |
|---------------------|---------------------|-----|-----|-----|------------------|--|
| Shutdown | T_{jds} | 140 | 150 | 160 | $^\circ\text{C}$ | $I_{Q1, 2} = 0 \text{ A}$ |
| Prealarm | T_{jpa} | 120 | 130 | 140 | $^\circ\text{C}$ | $V_{\text{Err}} = \text{L}$ |
| Delta | ΔT_j | 10 | 20 | 30 | K | $\Delta T_j = T_{\text{jds}} - T_{\text{jpa}}$ |
| Hysteresis shutdown | T_{jdsdhy} | – | 20 | – | K | – |
| Hysteresis prealarm | T_{jpahy} | – | 20 | – | K | – |

Power Outputs
Diode Transistor Sink Pair
(D13, T13; D14, T14; D23, T23; D24, T24)

| | | | | | | |
|--------------------|-------------------|-----|------|------|---------------|----------------------------|
| Saturation voltage | V_{satl} | 0.1 | 0.3 | 0.5 | V | $I_Q = -0.45 \text{ A}$ |
| Saturation voltage | V_{satl} | 0.2 | 0.5 | 0.8 | V | $I_Q = -0.7 \text{ A}$ |
| Reverse current | I_{RI} | 500 | 1000 | 1500 | μA | $V_S = V_Q = 40 \text{ V}$ |
| Forward voltage | V_{FI} | 0.6 | 0.9 | 1.2 | V | $I_Q = 0.45 \text{ A}$ |
| Forward voltage | V_{FI} | 0.7 | 1.0 | 1.3 | V | $I_Q = 0.7 \text{ A}$ |

Diode Transistor Source Pair
(T11, D11; T12, D12; T21, D21; T22, D22)

| | | | | | | |
|-----------------------|--------------------|-----|-----|------|---------------|---|
| Saturation voltage | V_{satuC} | 0.6 | 1.0 | 1.2 | V | $I_Q = 0.45 \text{ A}$; charge |
| Saturation voltage | V_{satuD} | 0.1 | 0.3 | 0.6 | V | $I_Q = 0.45 \text{ A}$; discharge |
| Saturation voltage | V_{satuC} | 0.7 | 1.2 | 1.5 | V | $I_Q = 0.7 \text{ A}$; charge |
| Saturation voltage | V_{satuD} | 0.2 | 0.5 | 0.8 | V | $I_Q = 0.7 \text{ A}$; discharge |
| Reverse current | I_{Ru} | 400 | 800 | 1200 | μA | $V_S = 40 \text{ V}, V_Q = 0 \text{ V}$ |
| Forward voltage | V_{Fu} | 0.7 | 1.0 | 1.3 | V | $I_Q = -0.45 \text{ A}$ |
| Forward voltage | V_{Fu} | 0.8 | 1.1 | 1.4 | V | $I_Q = -0.7 \text{ A}$ |
| Diode leakage current | I_{SL} | 0 | 3 | 10 | mA | $I_F = -0.7 \text{ A}$ |

Characteristics (cont'd)
 $V_S = 6 \text{ to } 16 \text{ V}; T_j = -40 \text{ to } 130 \text{ }^{\circ}\text{C}$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Error Output Timing

| | | | | | | |
|---------------------------|------------|---|----|-----|---------------|---|
| Time Phase X to IXX | t_{PI} | – | 5 | 20 | μs | – |
| Time IXX to Phase X | t_{IP} | – | 12 | 100 | μs | – |
| Delay Phase X to Error 2 | t_{PEsc} | – | 45 | 100 | μs | – |
| Delay Phase X to Error 1 | t_{PEol} | – | 15 | 50 | μs | – |
| Delay IXX to Error 2 | t_{IEsc} | – | 30 | 80 | μs | – |
| Reset delay after Phase X | t_{RP} | – | 3 | 10 | μs | – |
| Reset delay after IXX | t_{RI} | – | 1 | 5 | μs | – |

For details see next four pages.

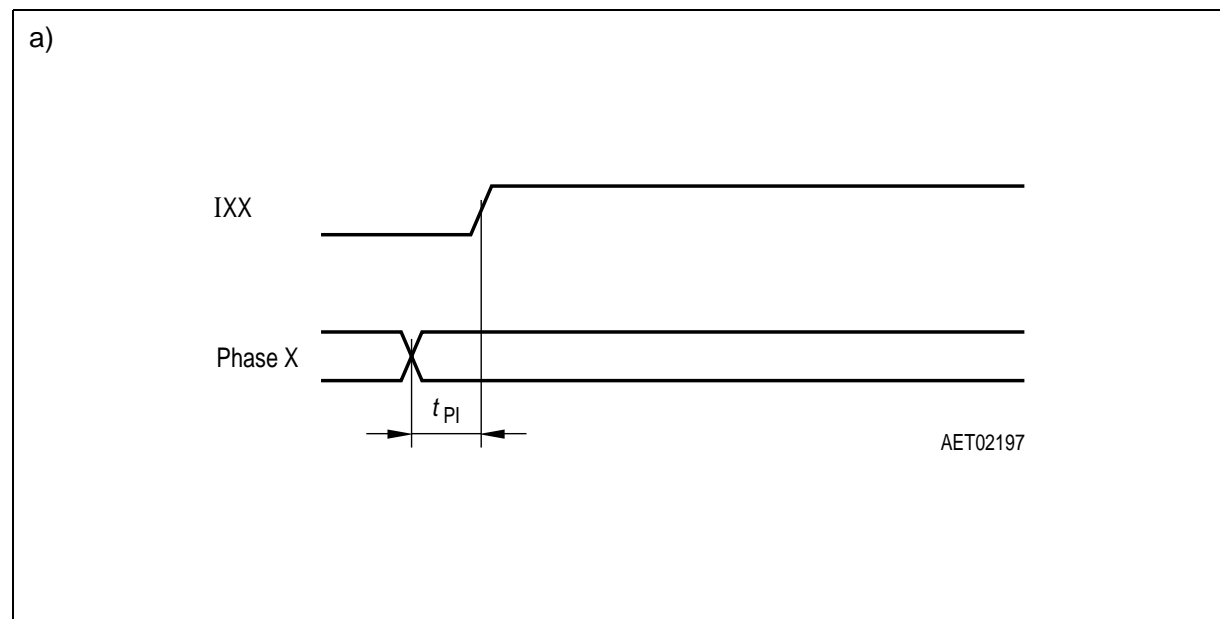
These parameters are not 100% tested in production, but guaranteed by design.

Diagrams

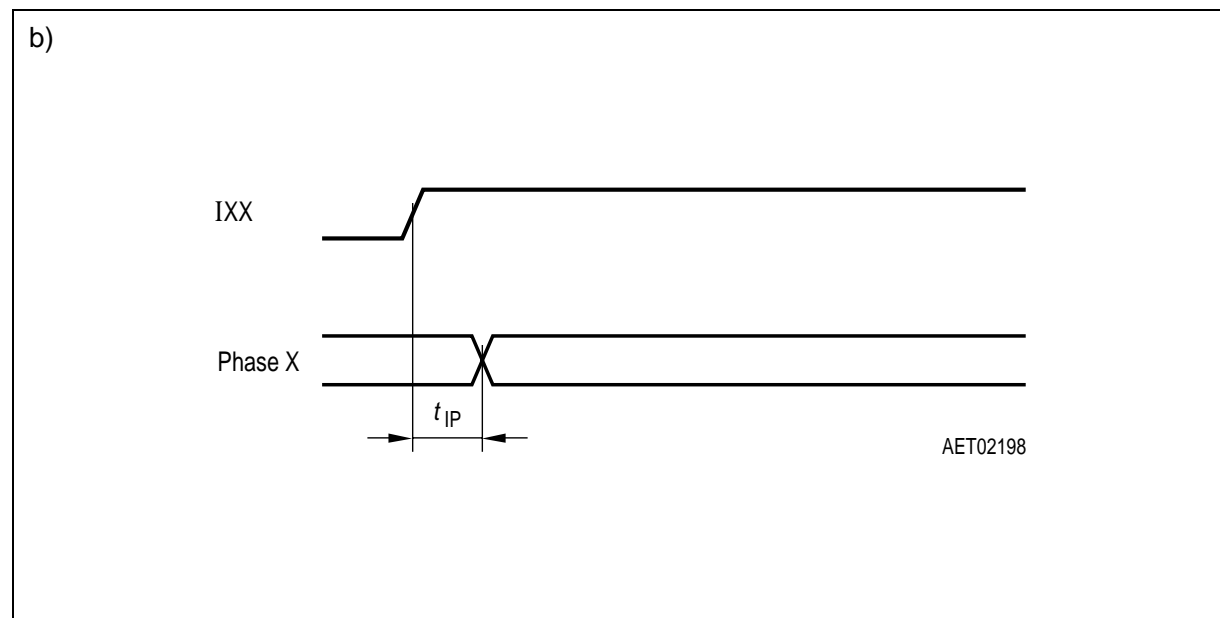
Timing between IXX and Phase X to prevent setting the error flag

Operating conditions:

+ $V_S = 14\text{ V}$, $T_j = 25\text{ °C}$, $I_{\text{err}} = 1\text{ mA}$, load = 3.3 mH , $1\text{ }\Omega$



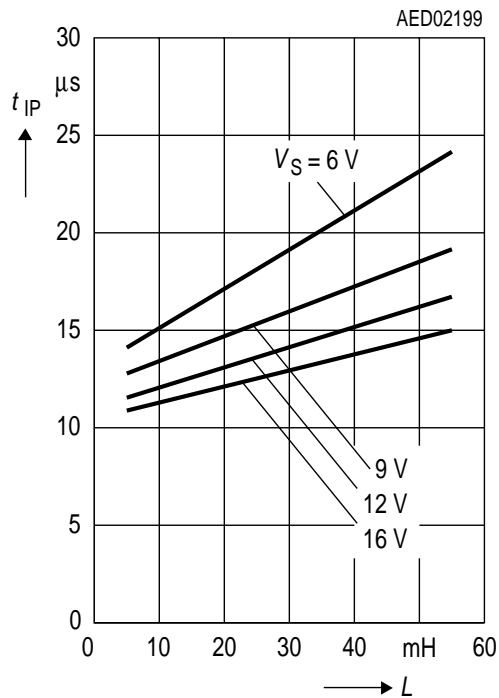
If $t_{PI} < \text{typ. } 5\text{ }\mu\text{s}$, an error “open load” will be set.



If $t_{IP} < \text{typ. } 12\text{ }\mu\text{s}$, an error “open load” will be set.

This time strongly depends on $+V_S$ and inductivity of the load, see diagram below.

Time t_{IP} vs. Load Inductivity

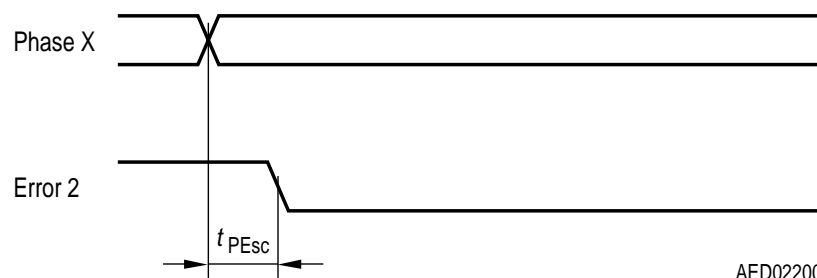


Propagation Delay of the Error Flag

Operating conditions:

$+V_S = 14 V$, $T_j = 25^\circ C$, $I_{err} = 1 mA$, load = 3.3 mH, 1Ω

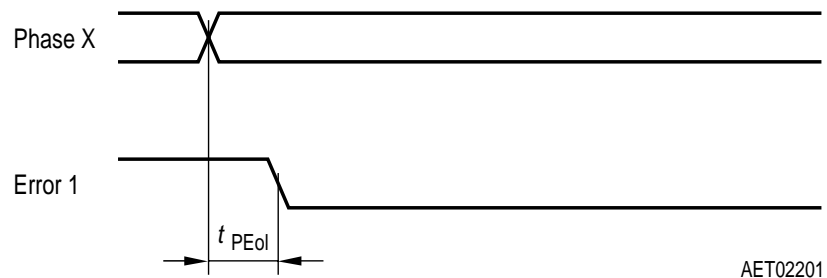
a) IXX = H, error condition: short circuit to GND.



AED02200

typ. t_{PEsc} : 45 μs

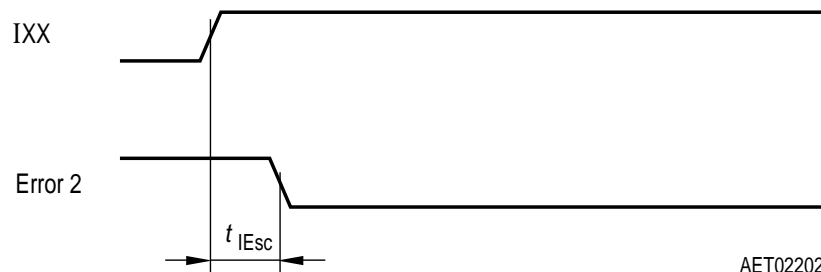
b) IXX = H, error condition: open load (equivalent: short circuit to + V_S).



AET02201

typ. t_{PEol} : 15 μ s

c) Phase X = H or L, const.; error condition: short circuit to GND.

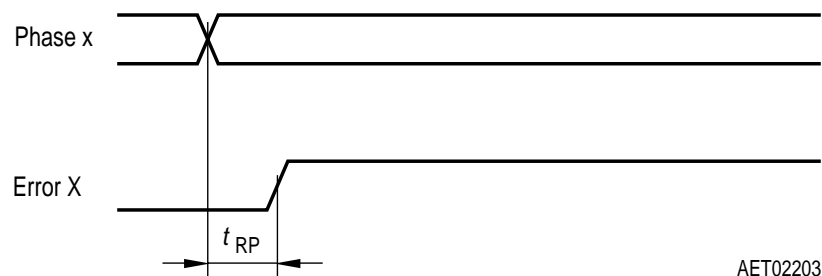


AET02202

typ. t_{IEsc} : 30 μ s

t_{IEsc} is also measured under the condition: begin of short circuit to GND till error flag set.

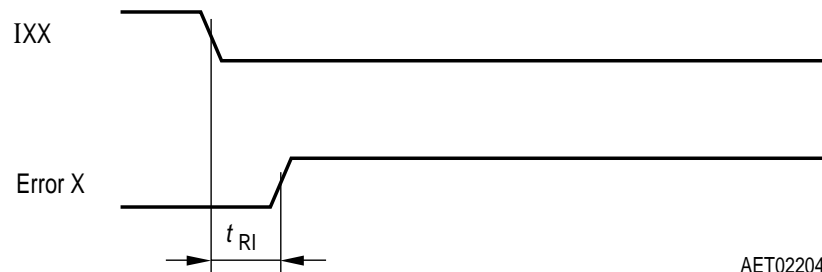
d) IXX = H, reset of error flag when error condition is not true.



AET02203

typ. t_{RP} : 3 μ s

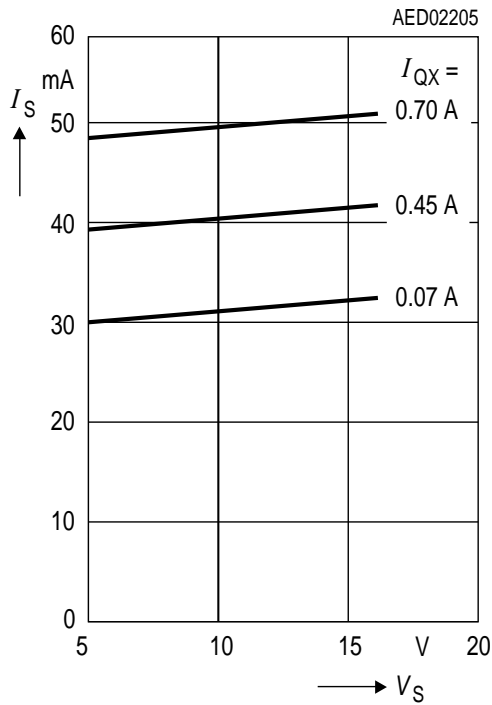
e) Phase X = H or L, const.; reset of error flag when error condition is not true.



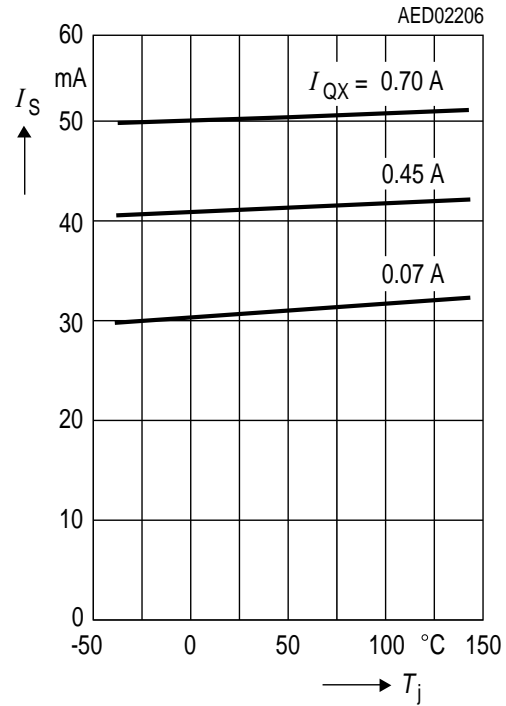
AET02204

typ. t_{RI} : 1 μ s

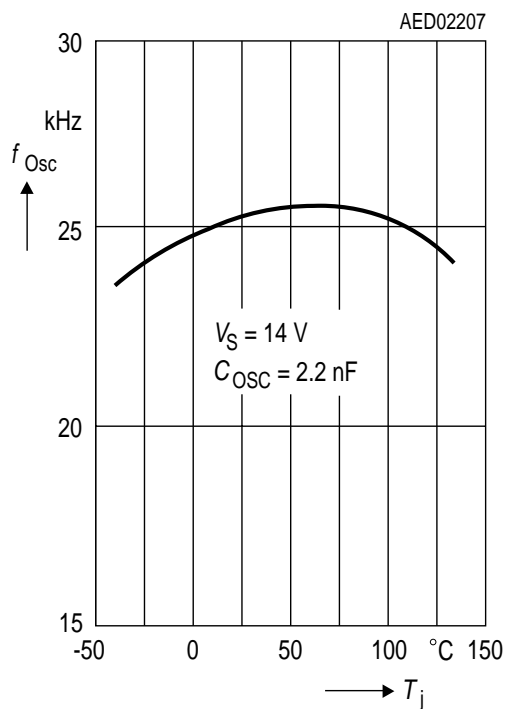
Quiescent Current I_S vs. Supply Voltage V_S ;
bridges not chopping; $T_j = 25\text{ °C}$



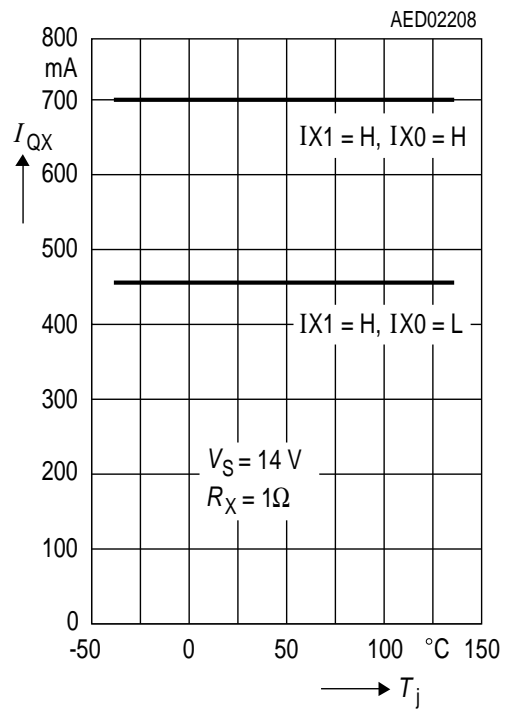
Quiesc. Current I_S vs. Junct. Temp. T_j ;
bridges not chopping, $V_S = 14\text{ V}$

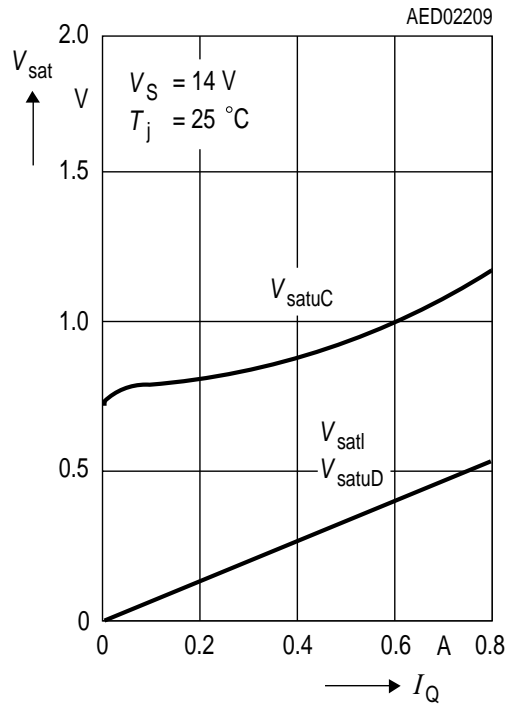
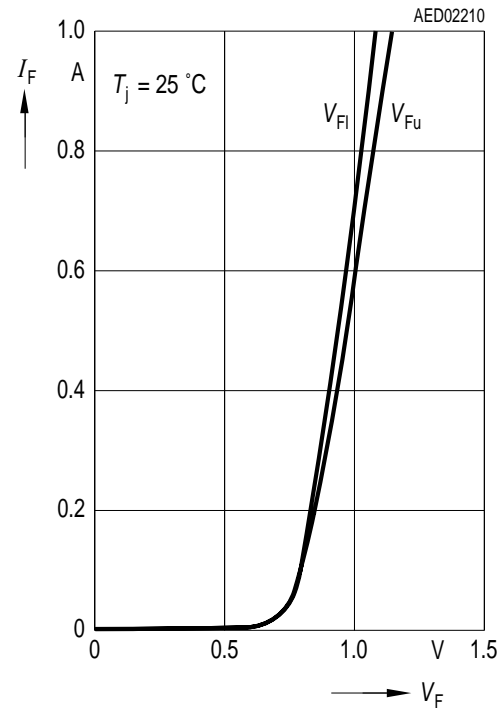
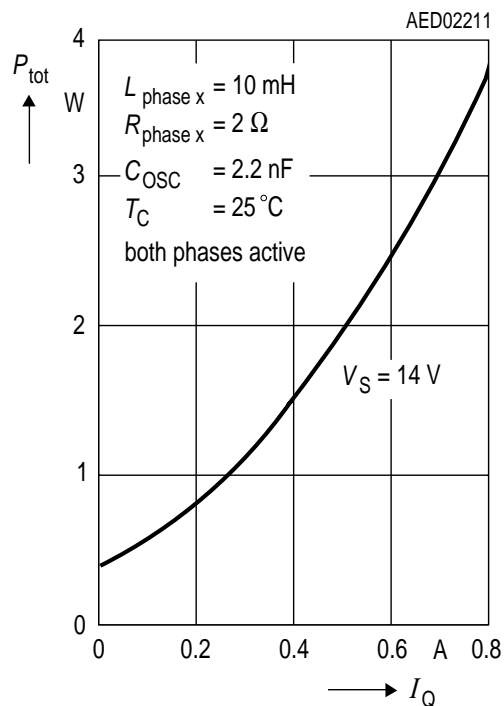
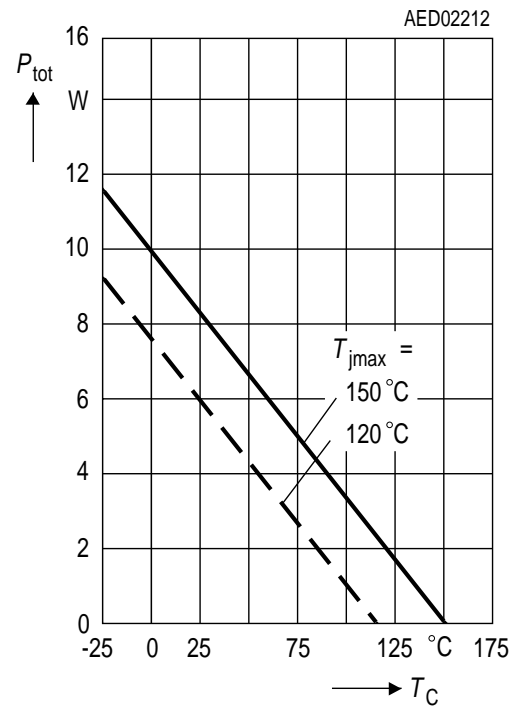


Oscillator Frequency f_{Osc} vs.
Junction Temperature T_j

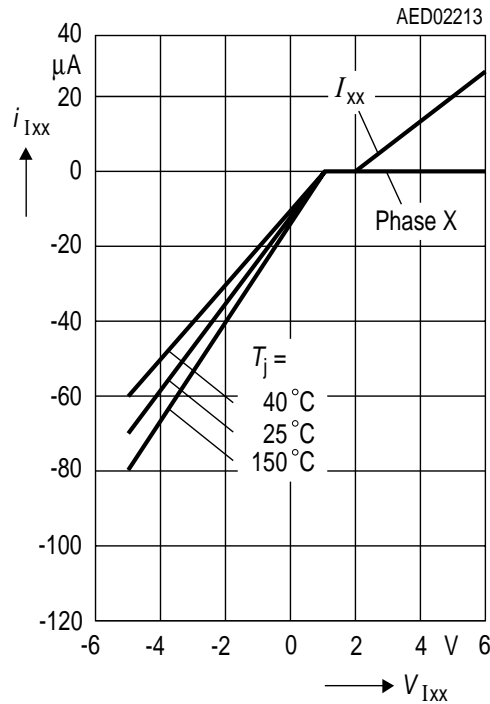


Output Current I_{QX} vs.
Junction Temperature T_j

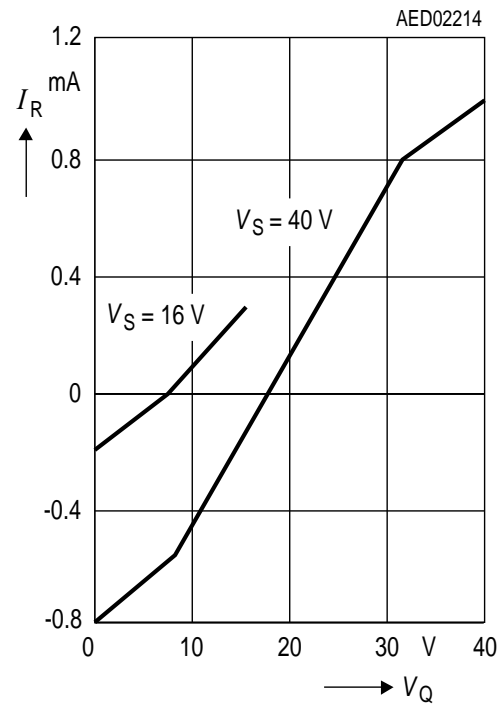


Output Saturation Voltages V_{sat} vs. Output Current I_Q

Forward Current I_F of Free-Wheeling Diodes vs. Forward Voltages V_F

Typical Power Dissipation P_{tot} vs. Output Current I_Q (non stepping)

Permissible Power Dissipation P_{tot} vs. Case Temp. T_C (measured at pin 5)


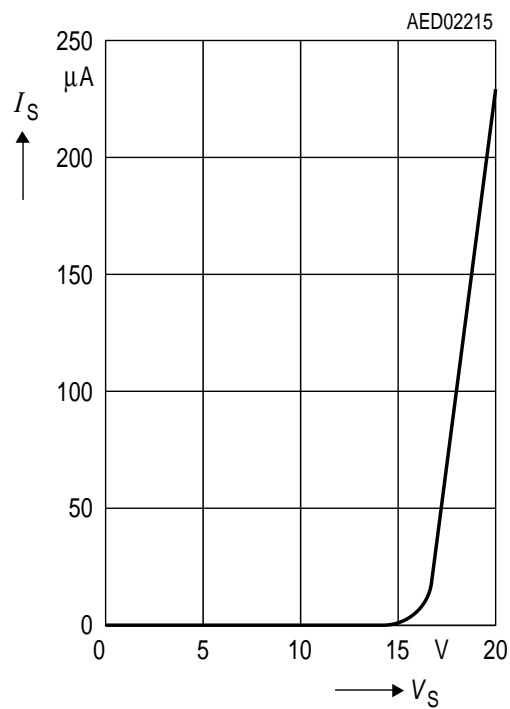
Input Characteristics of I_{XX} , Phase X



Output Leakage Current



Quiescent Current I_S vs. Supply Voltage V_S ; inhibit mode; $T_j = 25^\circ C$



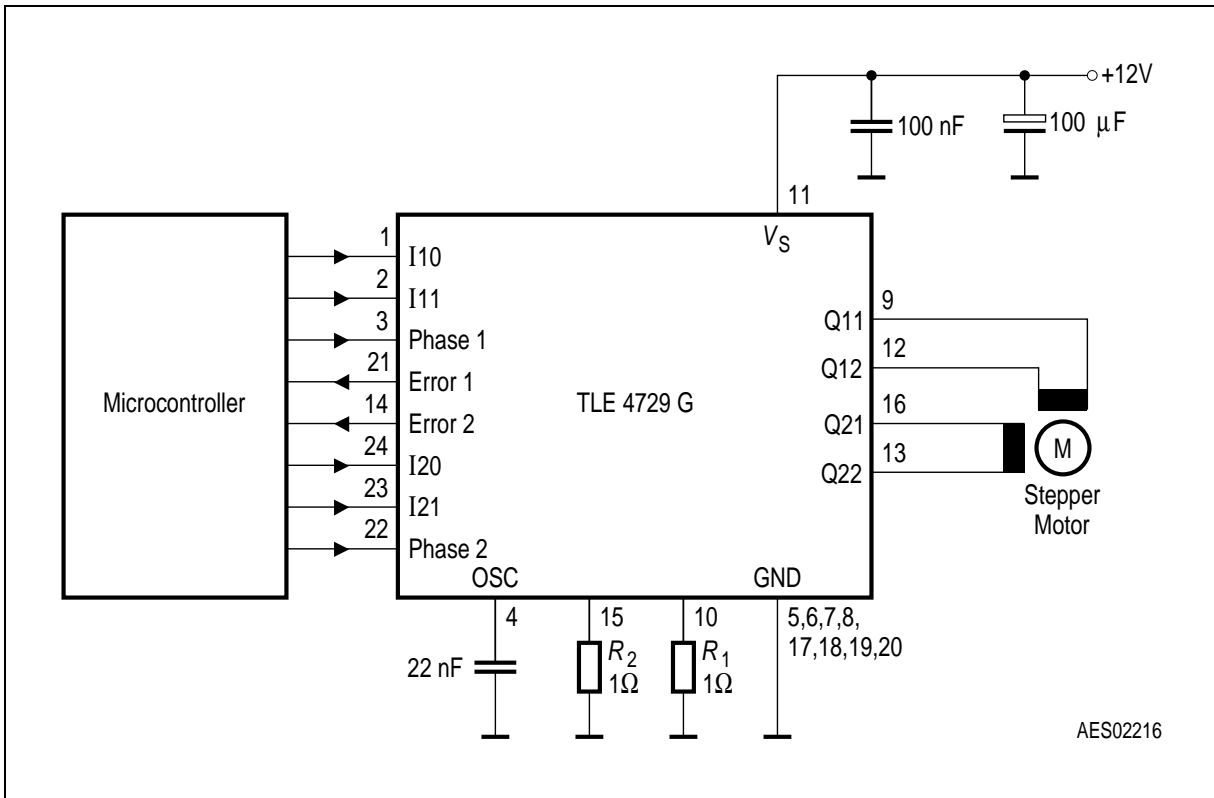


Figure 3 Application Circuit

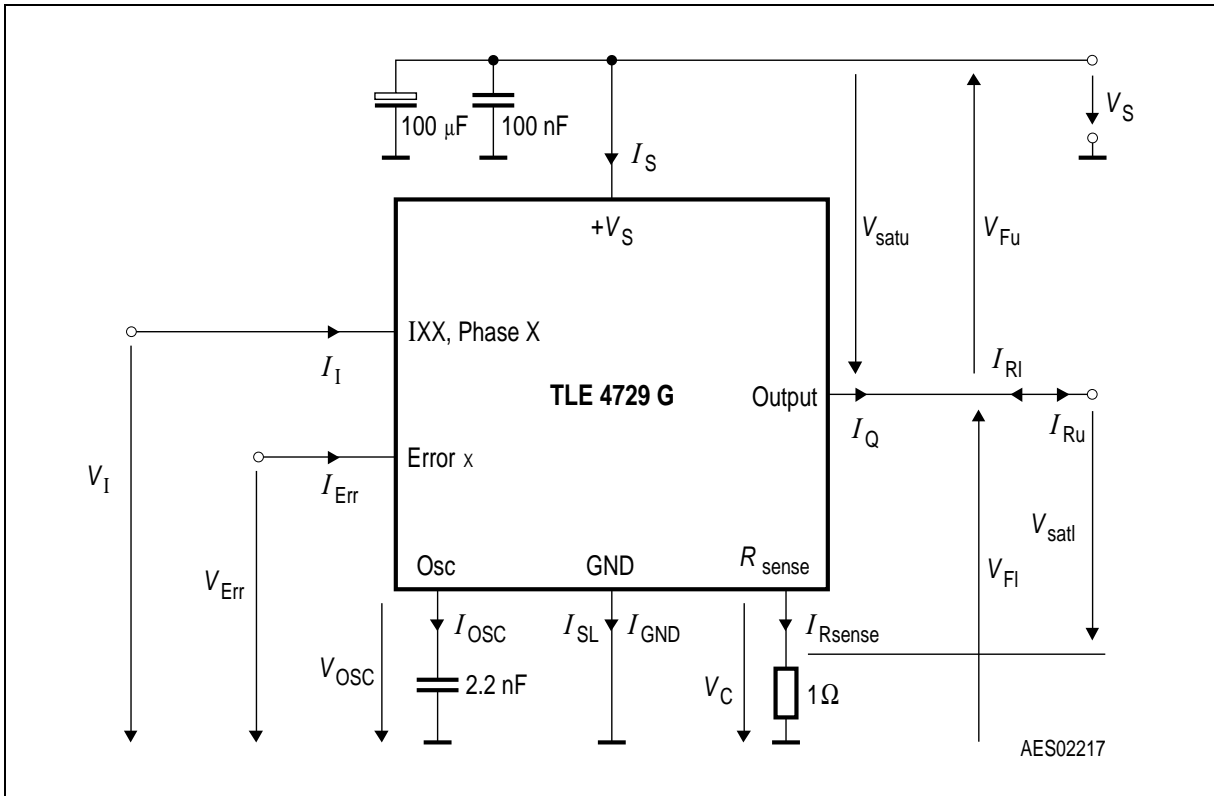


Figure 4 Test Circuit

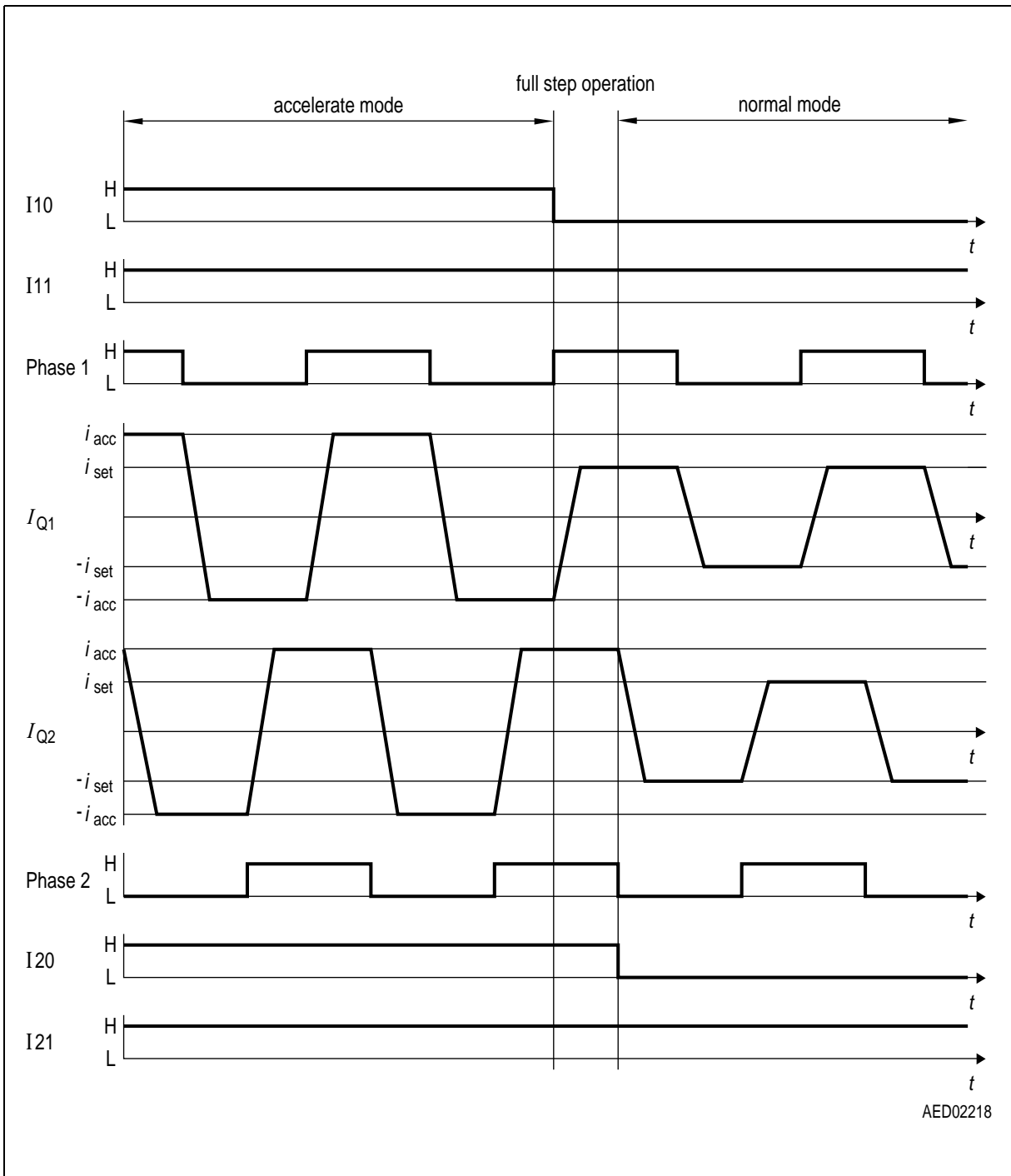


Figure 5 Full Step Operation

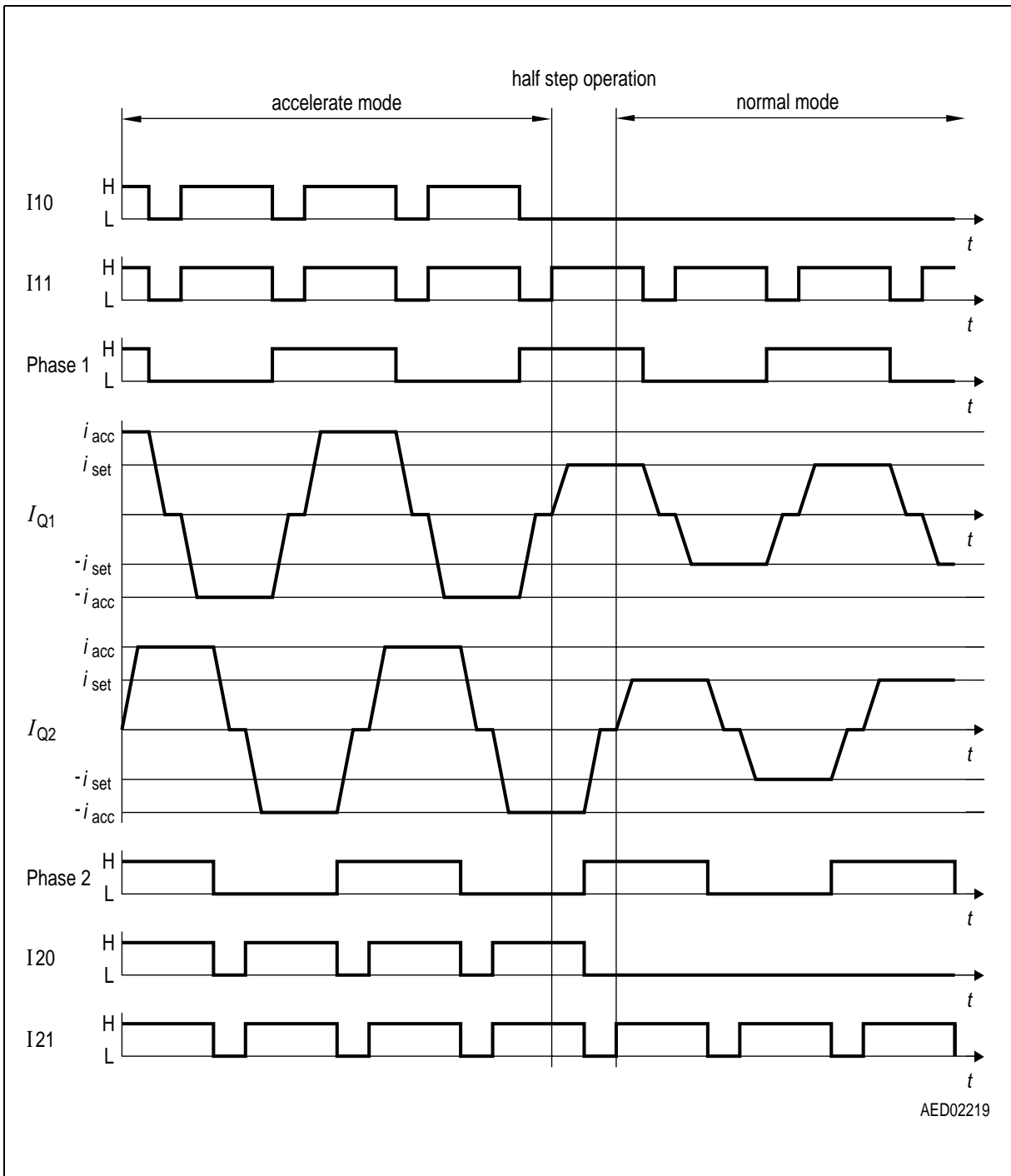


Figure 6 Half Step Operation

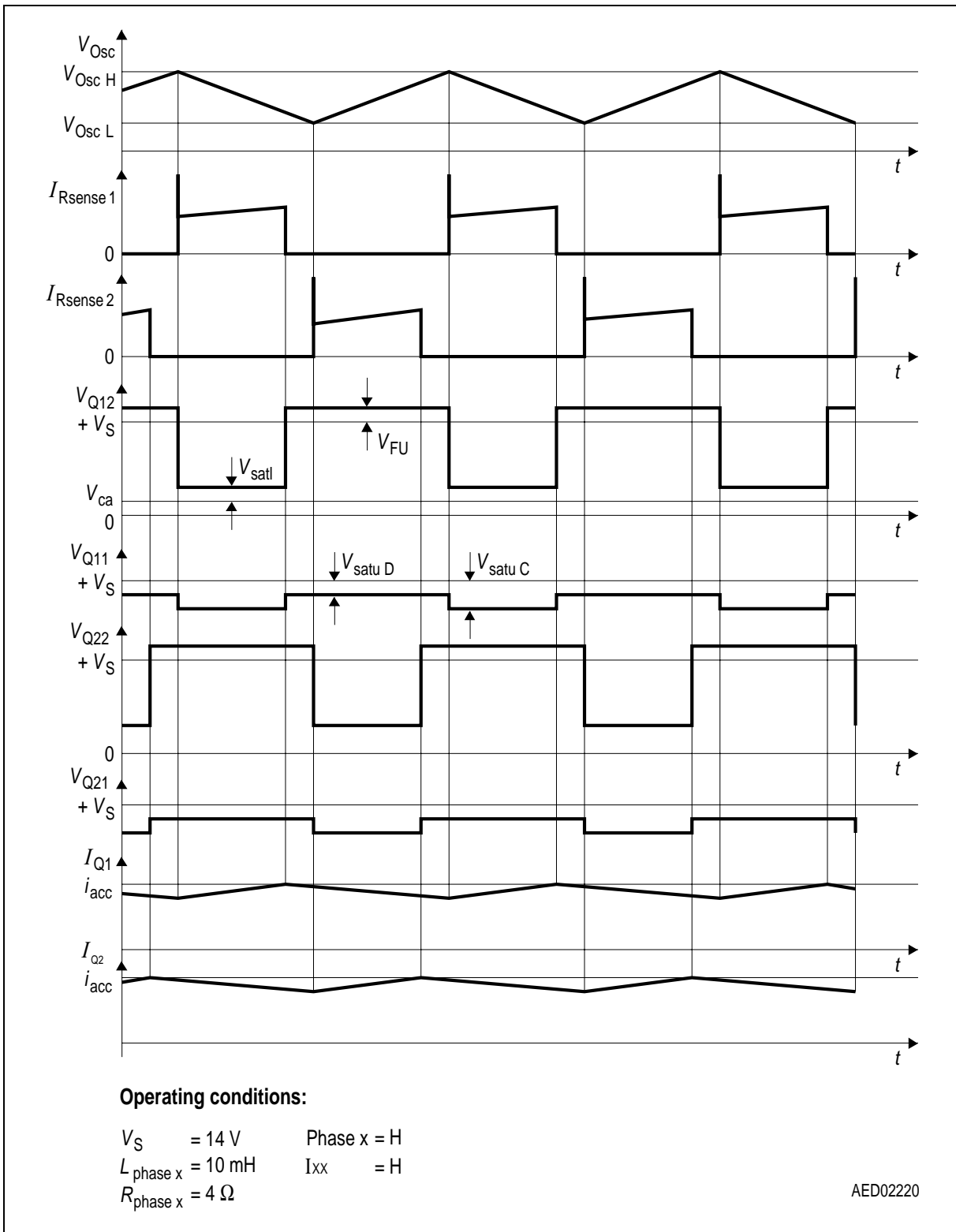


Figure 7 Current Control in Chop-Mode

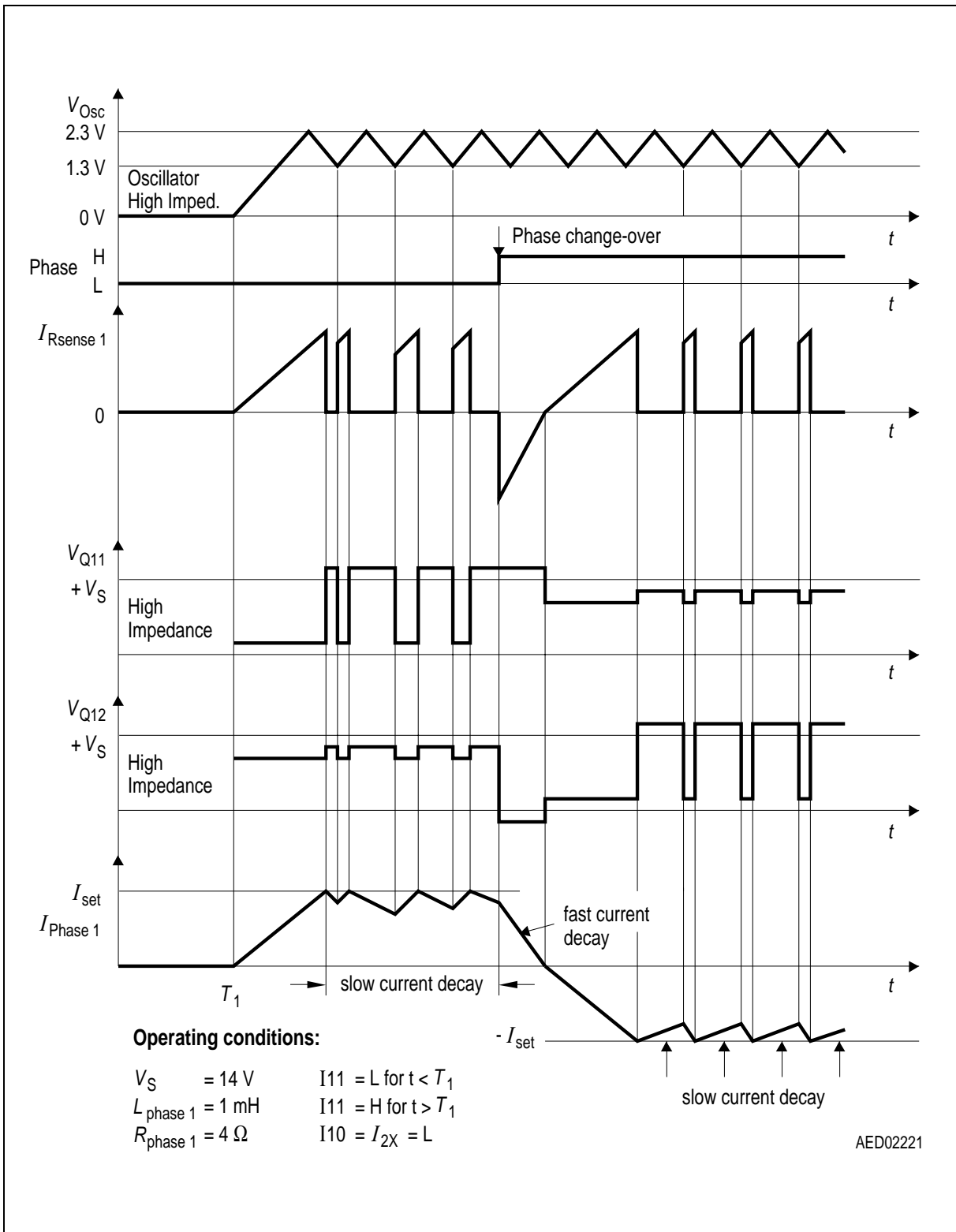


Figure 8 Phase Reversal and Inhibit

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

- Saturation losses P_{sat} (transistor saturation voltage and diode forward voltages),
- Quiescent losses P_{q} (quiescent current times supply voltage) and
- Switching losses P_{s} (turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal.

This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{\text{tot}} = 2 \times P_{\text{sat}} + P_{\text{q}} + 2 \times P_{\text{s}}$$

where

$$P_{\text{sat}} \cong I_{\text{N}} \{V_{\text{satl}} \times d + V_{\text{Fu}} (1 - d) + V_{\text{satuC}} \times d + V_{\text{satuD}} (1 - d)\}$$

$$P_{\text{q}} = I_{\text{q}} \times V_{\text{S}}$$

$$P_{\text{s}} \cong \frac{V_{\text{S}}}{T} \left\{ \frac{i_{\text{D}} \times t_{\text{DON}}}{2} + \frac{(i_{\text{D}} + i_{\text{R}}) \times t_{\text{ON}}}{4} + \frac{I_{\text{N}}}{2} (t_{\text{DOFF}} + t_{\text{OFF}}) \right\}$$

I_{N} = Nominal current (mean value)

I_{q} = Quiescent current

i_{D} = Reverse current during turn-on delay

i_{R} = Peak reverse current

t_{p} = Conducting time of chopper transistor

t_{ON} = Turn-ON time

t_{OFF} = Turn-OFF time

t_{DON} = Turn-ON delay

t_{DOFF} = Turn-OFF delay

T = Cycle duration

d = Duty cycle t_{p} / T

V_{satl} = Saturation voltage of sink transistor (TX3, TX4)

V_{satuC} = Saturation voltage of source transistor (TX1, TX2) during charge cycle

V_{satuD} = Saturation voltage of source transistor (TX1, TX2) during discharge cycle

V_{Fu} = Forward voltage of free-wheeling diode (DX1, DX2)

V_{S} = Supply voltage

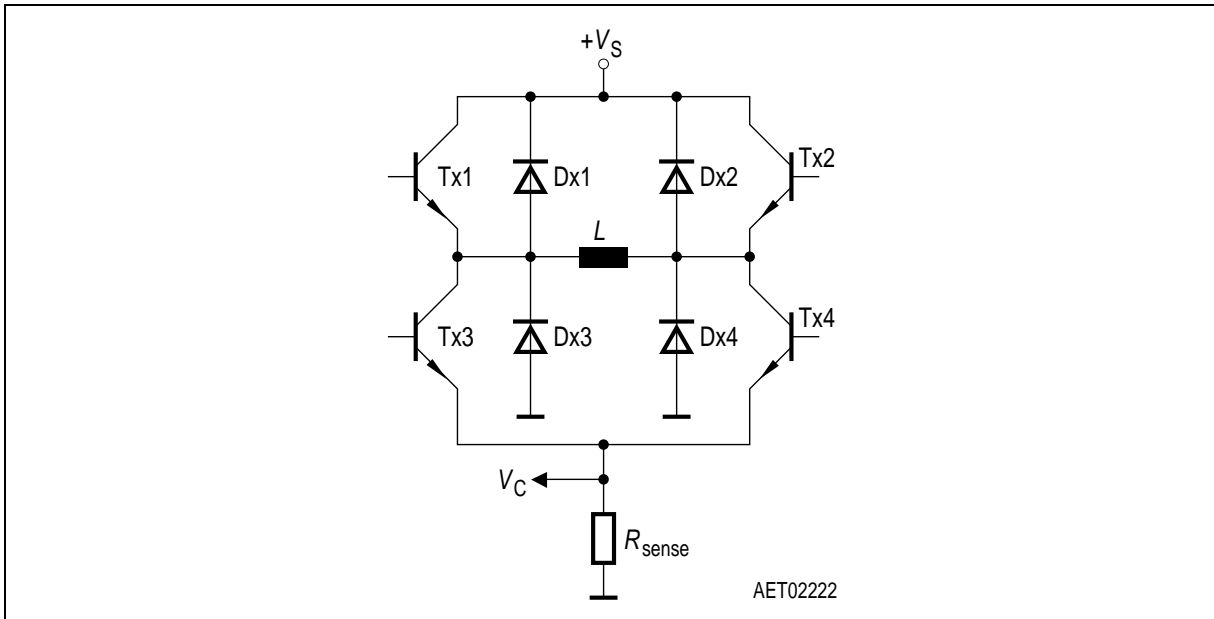


Figure 9

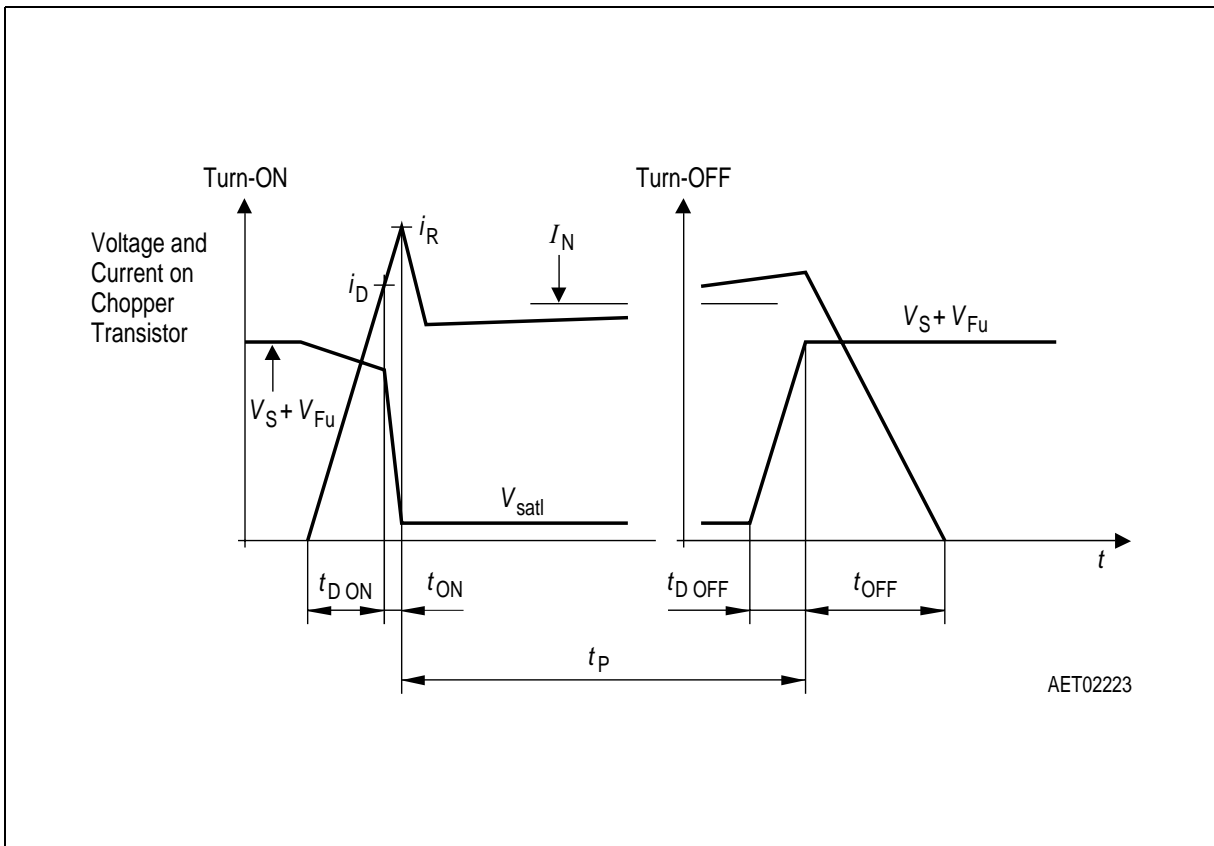


Figure 10 Voltage and Current on Chopper Transistor

Application Hints

The TLE 4729 G is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE 4729 G will work with supply voltages ranging from 5 V to 16 V at pin V_S . Surges exceeding 16 V at V_S won't harm the circuit up to 45 V, but whole function is not guaranteed. As soon as the voltage drops below approximately 16 V the TLE 4729 G works promptly again.

As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.1 μ F ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Inhibit Mode

In the case of low at all four current program inputs IXX the device will switch into inhibit condition; the current consumption is reduced to very low values.

When starting operation again, i.e. putting at least one IXX to high potential, the Error 1 output signals an open load error if the corresponding phase input is high. The error is reset by first recirculation in chop mode.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_{sense} . Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.07 V, 0.45 V and 0.7 V). These thresholds are not affected by variations of V_S . Consequently instabilized supplies will not affect the performance of the regulation. For precise current level it must be considered, that internal bounding wire (typ. 60 m Ω) is a part of R_{sense} .

Due to chopper control fast current rises (up to 10 A/ μ s) will occur at the sensing resistors. To prevent malfunction of the current sensing mechanism R_{sense} should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchronic chopping of several stepper motor drivers may be desirable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE 4729 G by a pulse generator overdriving the oscillator loading currents (approximately $\pm 120 \mu$ A). In these applications low level should be between 0 V and 0.8 V while high level should be between 3 V and 5 V.

Application Hints (cont'd)

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE 4729 G uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the phase inputs should be avoided by proper control signals.

To lower EMI a ceramic capacitor of max. 3 nF is advisable from each output to GND.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented.

Error Monitoring

The error outputs signal corresponding to the logic table the errors described below.

Logic Table

| Kind of Error | | Error Output | |
|---------------|--------------------------|--------------|---------|
| | | Error 1 | Error 2 |
| a) | No error | H | H |
| b) | Short circuit to GND | H | L |
| c) | Open load ¹⁾ | L | H |
| d) | b) and c) simultaneously | H | L |
| e) | Temperature prealarm | L | L |

¹⁾ Also possible: short circuit to + V_S or short circuit of the load.

Over-Temperature is implemented as pre-alarm; it appears approximately 20 K before thermal shut down. To detect an **open load**, the recirculation of the inductive load is watched. If there is no recirculation after a phase change-over, an internal error flipflop is set. Because in most kinds of **short circuits** there won't flow any current through the motor, there will be no recirculation after a phase change-over, and the error flipflop for open load will be set, too. Additionally an **open load error** is signaled after a phase change-over during hold mode.

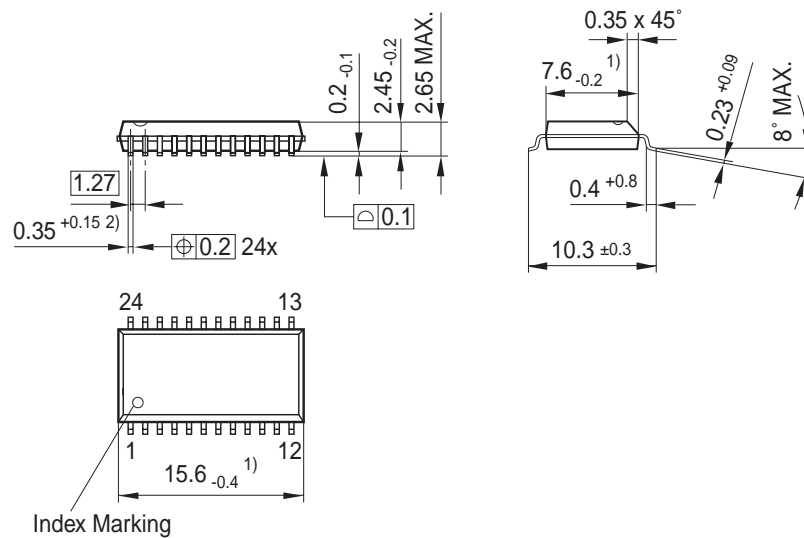
Only in the case of a **short circuit to GND**, the most probably kind of a short circuit in automotive applications, the malfunction is signaled dominant (see d) in logic table) by a separate error flag. Simultaneously the output current is disabled after 30 μ s to prevent disturbances.

A phase change-over or putting both current control inputs of the affected bridge on low potential resets the error flipflop. Being a separate flipflop for every bridge, the error can be located in easy way.

Package Outlines

P-DSO-24-9

(Plastic Dual Small Outline Package)



- ¹⁾ Does not include plastic or metal protrusion of 0.15 max. per side
²⁾ Lead width can be 0.61 max. in dambar area

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm