Features

- Single Supply Voltage, Range 3V to 3.6V
- 3-volt Only Read and Write Operation
- Software Protected Programming
- Low Power Dissipation
  - 15 mA Active Current
  - 40 µA CMOS Standby Current
- Fast Read Access Time – 150 ns
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (64 Bytes/Sector)
  - Internal Address and Data Latches for 64 Bytes
- Fast Sector Program Cycle Time – 20 ms Max.
- Internal Program Control and Timer
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Typical Endurance > 10,000 Cycles
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

256K (32K x 8) 3-volt Only Flash Memory

AT29LV256

Not Recommended for New Designs.

1. Description

The AT29LV256 is a 3-volt-only in-system Flash Programmable Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 54 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 40 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

To allow for simple in-system reprogrammability, the AT29LV256 does not require high input voltages for programming. Three-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29LV256 is performed on a sector basis; 64 bytes of data are loaded into the device and then simultaneously programmed.

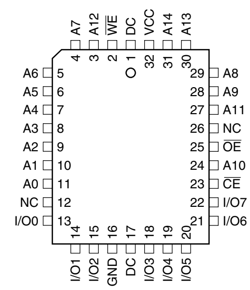
During a reprogram cycle, the address locations and 64 bytes of data are captured at microprocessor speed and internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

0563E–FLASH–2/07

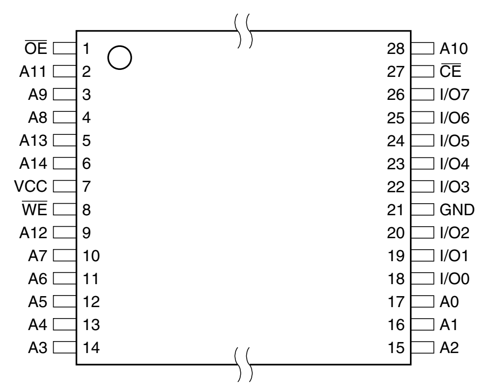
2. Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

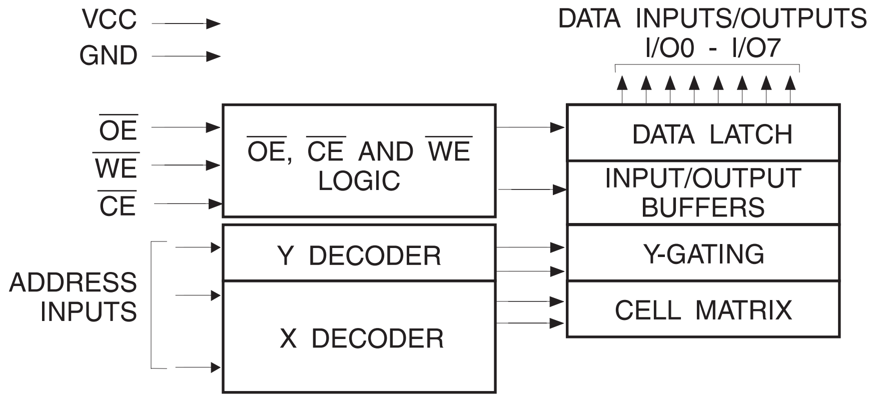
2.1 PLCC Top View



2.2 TSOP Top View – Type 1



3. Block Diagram



4. Device Operation

4.1 Read

The AT29LV256 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Software Data Protection Programming

The AT29LV256 has 512 individual sectors, each 64 bytes. Using the software data protection feature, byte loads are used to enter the 64 bytes of a sector to be programmed. The AT29LV256 can only be programmed or reprogrammed using the software data protection feature. The device is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 64-byte sector must be loaded into the device. The AT29LV256 automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature; however, the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's 3-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

The 64 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high-to-low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low-to-high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high-to-low transition is not detected within 150 µs of the last low-to-high transition, the load period will end and the internal programming period will start. A6 to A14 specify the sector address. The sector address must be valid during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT29LV256 in the following ways: (a) V_{CC} sense – if V_{CC} is below 1.8V (typical), the program function is inhibited; (b) V_{CC} power on delay – once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming; (c) Program inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles; and (d) Noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

4.4 Input Levels

While operating with a 3.3V ±10% power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6 volts.

4.5 Product Identification

The product identification mode identifies the device and manufacturer as Atmel®. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

4.6 $\overline{\text{DATA}}$ Polling

The AT29LV256 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

4.7 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling the AT29LV256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.8 Optional Chip Erase Mode

The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

5. Absolute Maximum Ratings*

Temperature Under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on A9 (including NC Pins) with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. DC and AC Operating Range

		AT29LV256-15	AT29LV256-20	AT29LV256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.3V $\pm$0.3V	3.3V $\pm$0.3V	3.3V $\pm$0.3V

7. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[(2)]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[(1)]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A14 = V_{IL}, A9 = V_H[(3)], A0 = V_{IL}	Manufacturer Code[(4)]
				A1 - A14 = V_{IL}, A9 = V_H[(3)], A0 = V_{IH}	Device Code[(4)]
Software[(5)]				A0 = V_{IL}	Manufacturer Code[(4)]
				A0 = V_{IH}	Device Code[(4)]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.
4. Manufacturer Code is 1F. The Device Code is BC.
5. See details under Software Product Identification Entry/Exit.

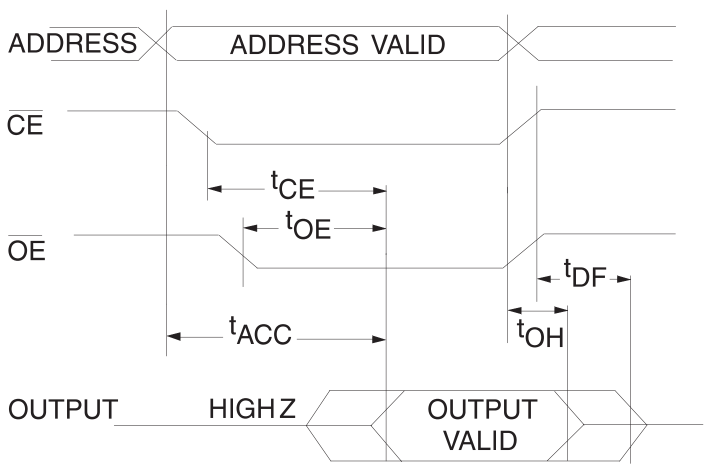
8. DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	Com.		40	µA
			Ind.		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V			15	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = 3.0V		2.4		V

9. AC Read Characteristics

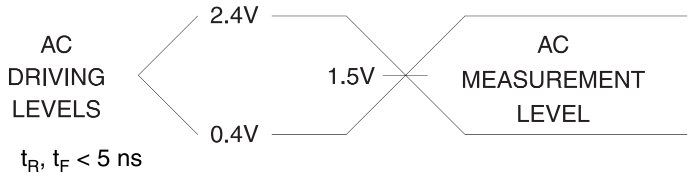
Symbol	Parameter	AT29LV256-15		AT29LV256-20		AT29LV256-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}[1]	$\overline{\text{CE}}$ to Output Delay		150		200		250	ns
t_{OE}[2]	$\overline{\text{OE}}$ to Output Delay	0	70	0	100	0	120	ns
t_{DF}[3][4]	$\overline{\text{CE}}$ or $\overline{\text{OE}}$ to Output Float	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{\text{OE}}$, $\overline{\text{CE}}$ or Address, whichever occurred first	0		0		0		ns

10. AC Read Waveforms[1][2][3][4]

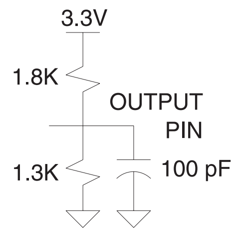


Notes:
1. $\overline{\text{CE}}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{\text{OE}}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{\text{CE}}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{\text{OE}}$ or $\overline{\text{CE}}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

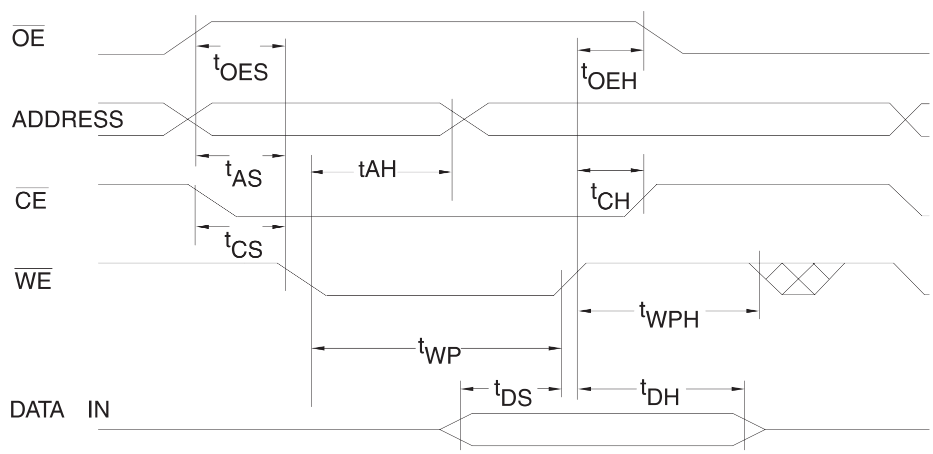
Note: 1. These parameters are characterized and not 100% tested.

14. AC Byte Load Characteristics

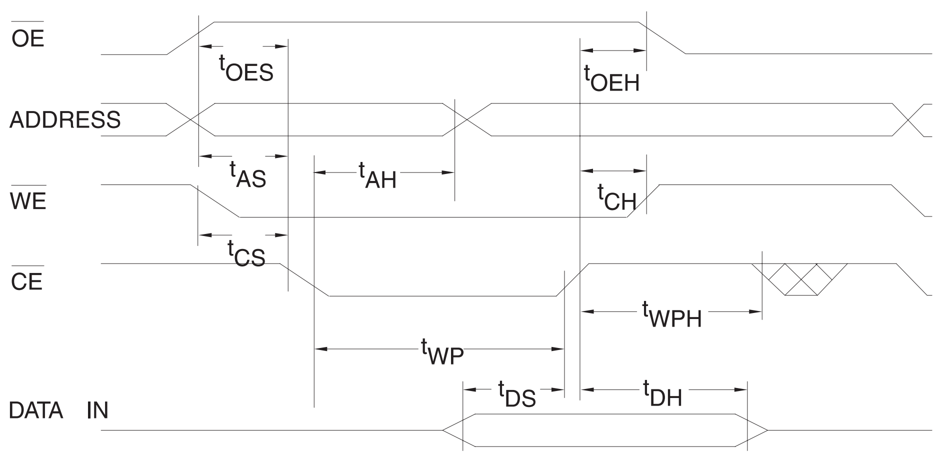
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

15. AC Byte Load Waveforms[(1)(2)]

15.1 $\overline{WE}$ Controlled



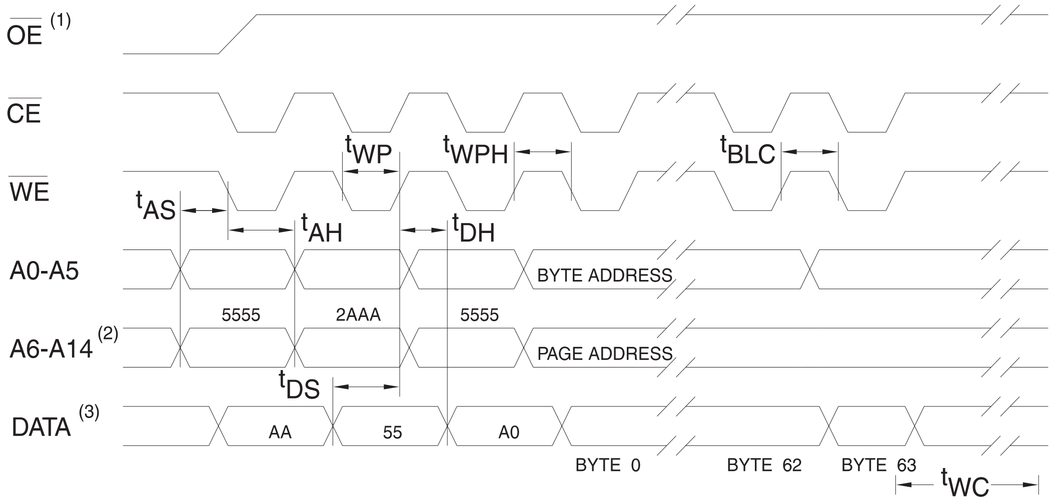
15.2 $\overline{CE}$ Controlled



16. Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	200		ns

17. Software Protected Program Waveform(1)(2)(3)



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.

2. A6 through A14 must specify the sector address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

3. All bytes that are not loaded within the sector being programmed will be indeterminate.

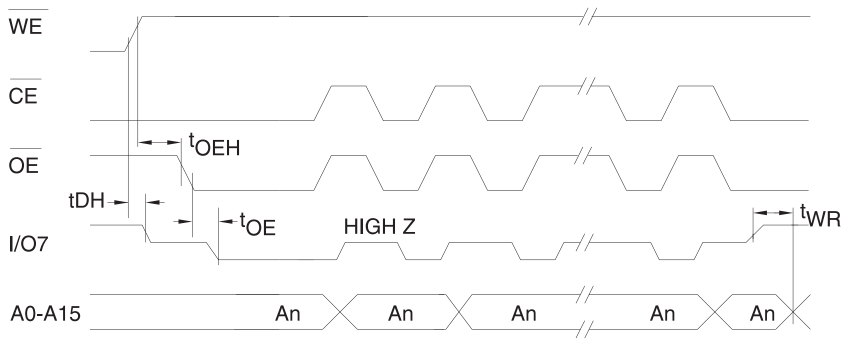
18. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See t_{OE} spec in AC Read Characteristics.

19. $\overline{\text{Data}}$ Polling Waveforms



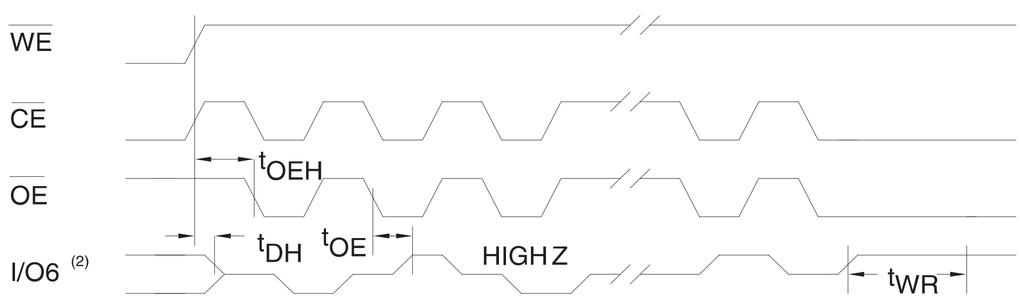
20. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See t_{OE} spec in AC Read Characteristics.

21. Toggle Bit Waveforms[1][3]

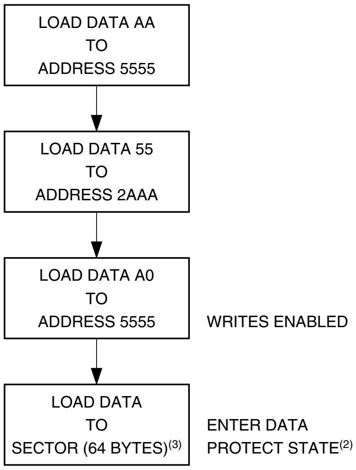


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.

2. Beginning and ending state of I/O6 will vary.

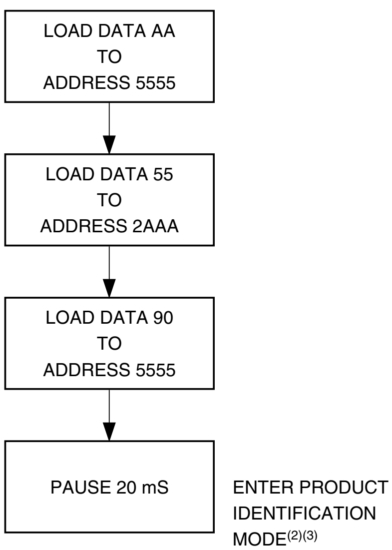
3. Any address location may be used but the address should not vary.

22. Programming Algorithm[(1)]



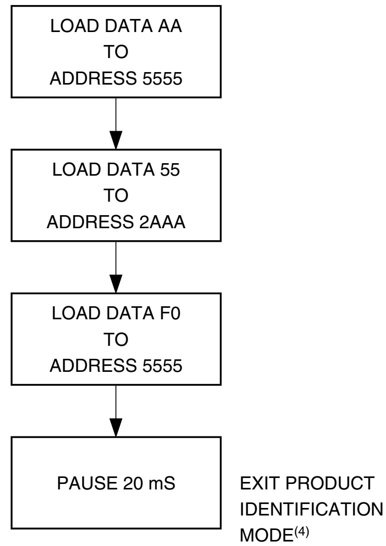
Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 64 bytes of data **MUST BE** loaded.

23. Software Product Identification Entry[(1)]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 1F. The Device Code is BC.

24. Software Product Identification Exit[(1)]



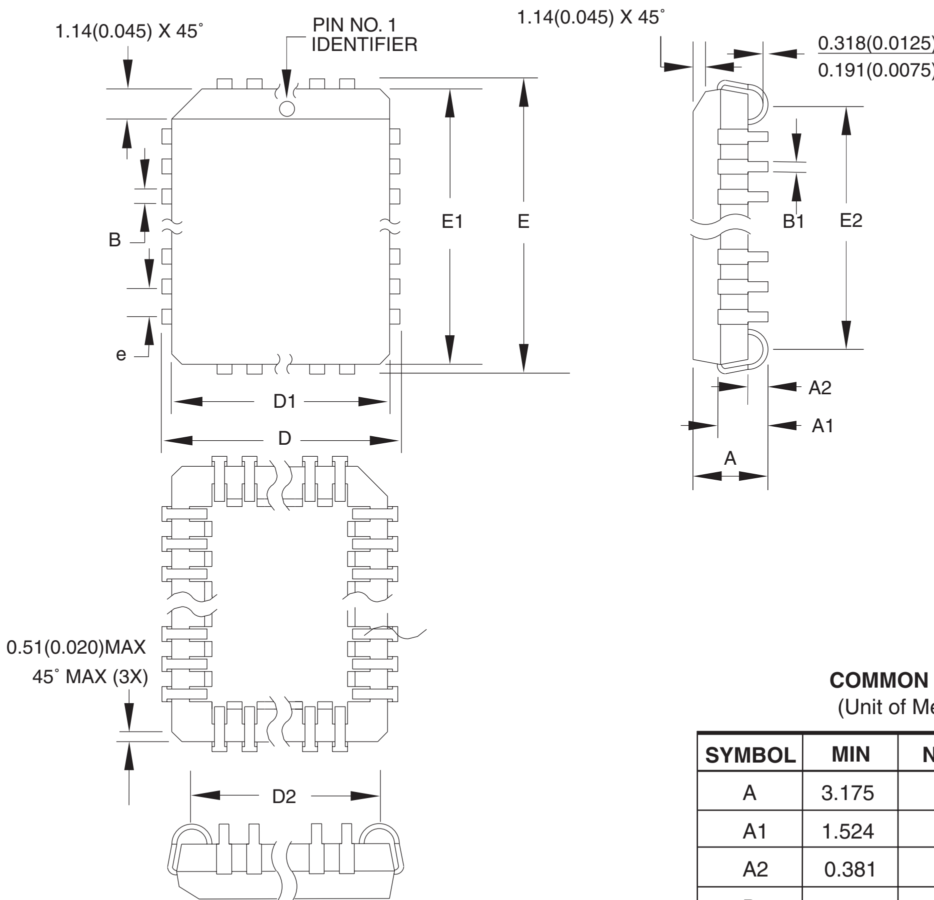
25. Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
150	15	0.04	AT29LV256-15JC AT29LV256-15TC	32J 28T	Commercial (0° to 70° C)
	15	0.05	AT29LV256-15JI AT29LV256-15TI	32J 28T	Industrial (-40° to 85° C)
200	15	0.04	AT29LV256-20JC AT29LV256-20TC	32J 28T	Commercial (0° to 70° C)
	15	0.05	AT29LV256-20JI	32J	Industrial (-40° to 85° C)
250	15	0.04	AT29LV256-25JC AT29LV256-25TC	32J 28T	Commercial (0° to 70° C)
	15	0.05	AT29LV256-25JI	32J	Industrial (-40° to 85° C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28T	28-lead, Thin Small Outline Package (TSOP)

26. Packaging Information

26.1 32J – PLCC



Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

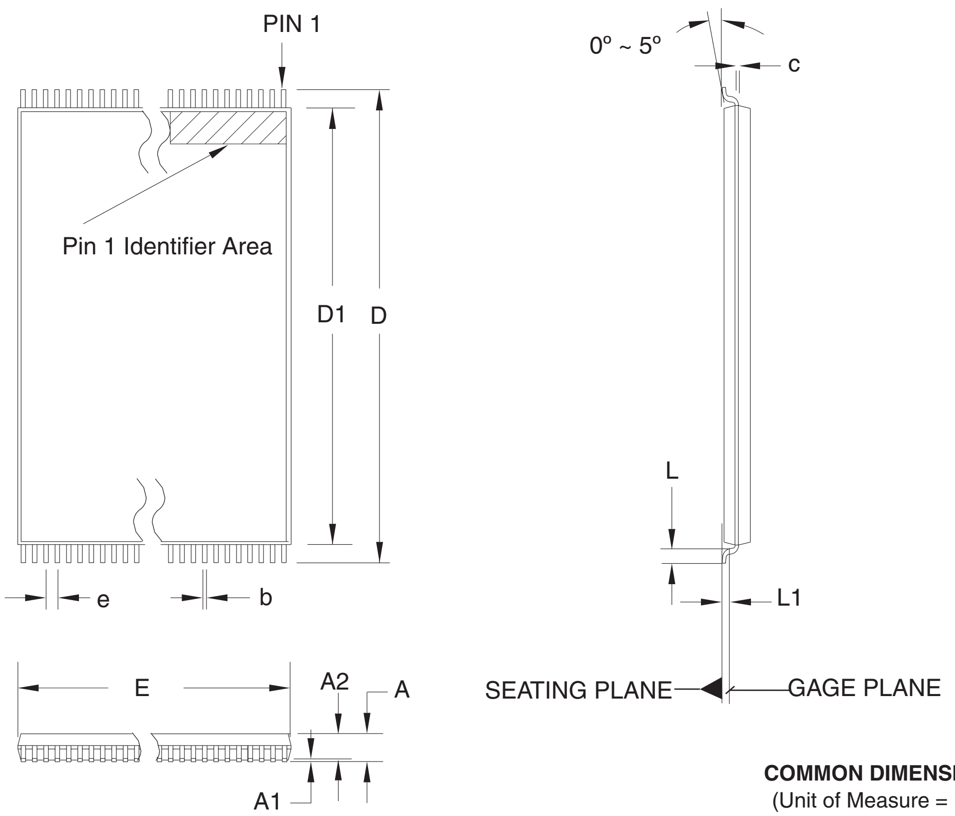
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

10/04/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

26.2 28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	C

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-47-50
Fax: (33) 4-76-58-47-60

Literature Requests
www.atmel.com/literature