TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB6571FG

3-Phase Full-Wave Brushless Motor Controller Featuring Speed Control and Sine Wave PWM Drive

The TB6571FG is a 3-phase full-wave brushless motor controller IC that employs a sine wave PWM drive mechanism with a speed control function.

Sine wave current driving with 2-phase modulation enables the IC to drive a motor with high efficiency and low noise.

It also incorporates a speed control circuit that can vary the motor speed using to an external clock.

Weight: 0.50 g (typ.)

Features

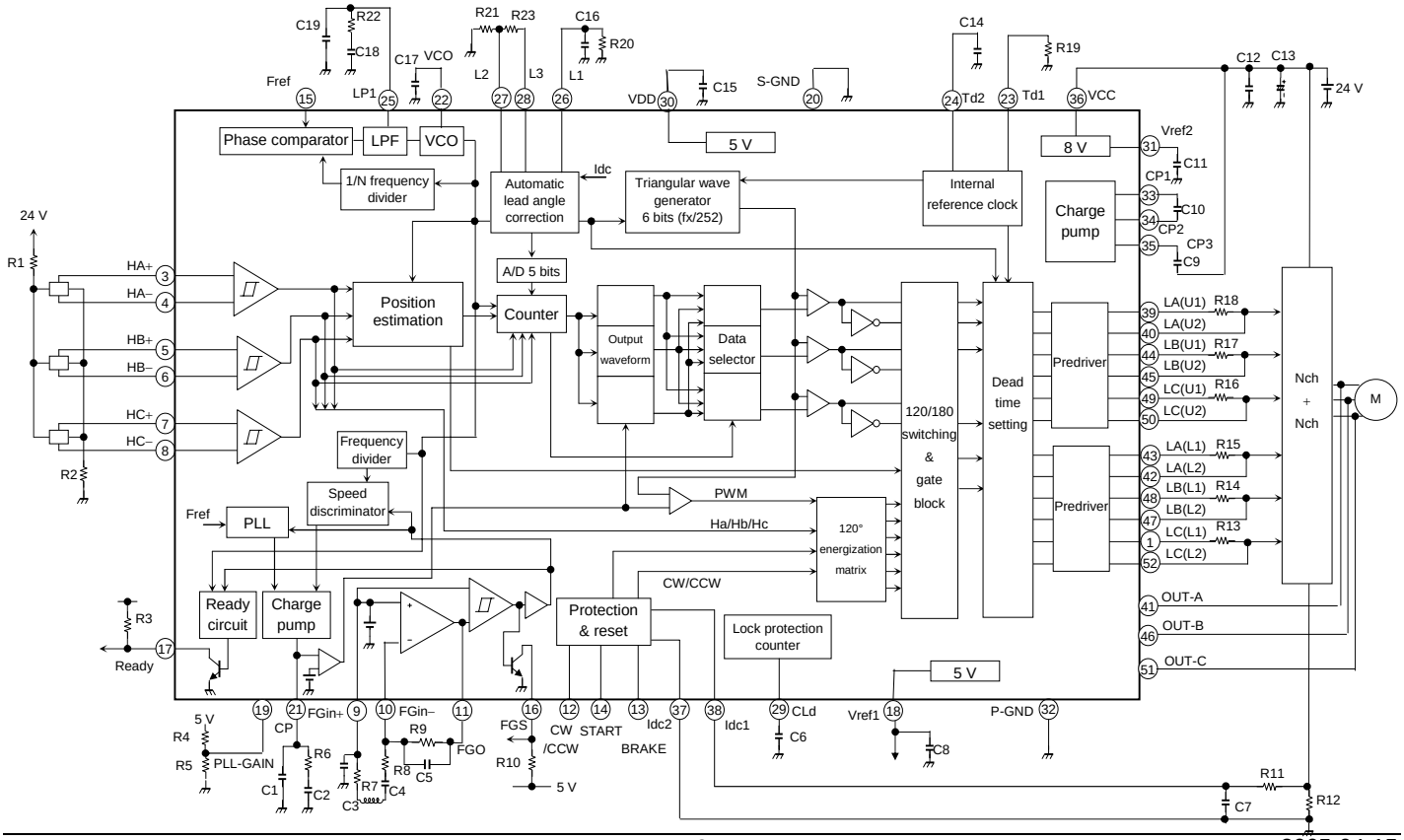
- Sine wave PWM drive
- 2-phase modulation with low switching loss
- Triangular wave generator
- Dead time function
- Speed control function
- External clock input
- Speed discrimination + PLL speed control circuit
- Ready circuit output
- FG amplifier
- Automatic lead angle correction
- Forward/stop/reverse/brake functions
- Current limiter
- Lock protection

TB6571FG:
TB6571FG is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-63Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature=245°C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

- This product has a MOS structure and is sensitive to electrostatic discharge. When handling the product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.
  Install the product correctly. Otherwise, breakdown, damage and/or degradation in the product or equipment may result.

Block Diagram

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

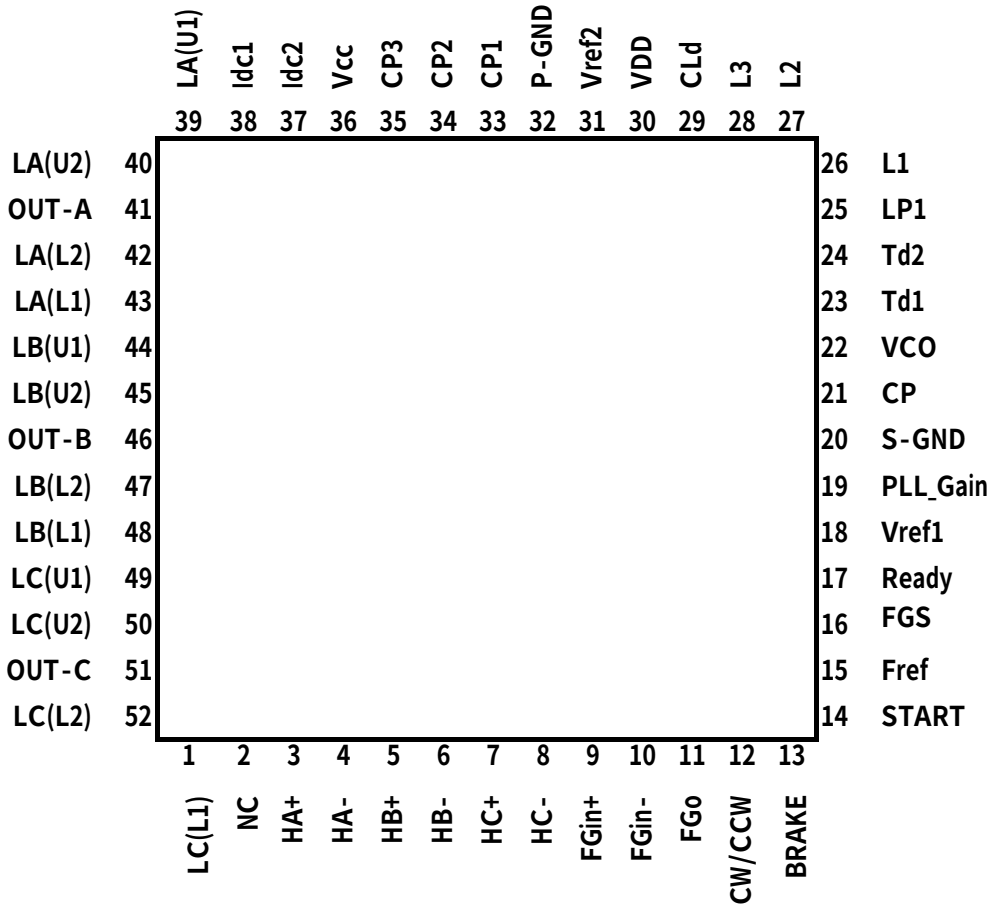


Pin Functions

Pin No.	Name	Pin Functions	Remarks
1	LC (L1)	Phase-C energization signal output (L1)	For source driving for phase-C output FET gate (lower N-ch)
2	NC	No connection	
3	HA+	Phase-A hall signal input + pin	Input the positive phase-A Hall device signal.
4	HA–	Phase-A hall signal input - pin	Input the negative phase-A Hall device signal.
5	HB+	Phase-B hall signal input + pin	Input the positive phase-B Hall device signal.
6	HB–	Phase-B hall signal input - pin	Input the negative phase-B Hall device signal.
7	HC+	Phase-C hall signal input + pin	Input the positive phase-C Hall device signal.
8	HC–	Phase-C hall signal input - pin	Input the negative phase-C Hall device signal.
9	FGin+	FG amplifier input + pin	FG signal input
10	FGin–	FG amplifier input - pin	FG signal input
11	FGo	FG amplifier output pin	
12	CW/CCW	Forward/reverse switching pin	H: Reverse/L: Forward
13	BRAKE	Brake	Pull-up resistor, L for braking (all-phase ON for lower circuit)
14	START	Start	Pull-up resistor, L for start, H for standby
15	Fref	External clock input	Pull-up resistor
16	FGS	FG hysteresis comparator output pin	Open collector output, I_O = 1 mA (max)
17	Ready	Ready output pin	Open collector output. Within ±6%: L, Otherwise: High impedance
18	Vref1	5-V reference power supply	5-V output. Connect to GND through a capacitor.
19	PLL-GAIN	PLL gain adjustment pin	Connect a resistor.
20	S-GND	Ground pin	
21	CP	Charge pump pin for speed control	Connect to GND through a capacitor.
22	VCO	Capacitor pin for VCO	Connect to GND through a capacitor.
23	Td1	Frequency setting pin 1 for internal reference clock	Connect external CR to generate a reference clock.
24	Td2	Frequency setting pin 2 for internal reference clock	
25	LP1	For LPF	
26	L1	Lead angle correction circuit	Connect an external capacitor.
27	L2	Lead angle correction circuit	Connect an external resistor for adjusting the correction gain.
28	L3	Lead angle correction circuit	Connect an external resistor for adjusting the correction gain.
29	CLd	Oscillation pin for lock protection circuit	Connect to GND through a capacitor.
30	VDD	Internal logic power supply pin	5-V output. Connect to GND through a capacitor.
31	Vref2	8-V reference power supply	8-V output. Connect to GND through a capacitor.
32	P-GND	Ground pin	
33	CP1	Charge pump pin	For generating upper N-ch FET gate voltage
34	CP2	Charge pump pin	For generating upper N-ch FET gate voltage
35	CP3	Charge pump pin	For generating upper N-ch FET gate voltage
36	VCC	Voltage input pin for control power supply	V_{CC} (opr.) = 10~28 V
37	Idc2	Input pin for output current detection signal	GND sense pin
38	Idc1	Input pin for output current detection signal	Gate block operation when 0.25 V (typ.) or higher
39	LA (U1)	Phase-A energization signal output (U1)	For source driving for phase-A output FET gate (upper N-ch)
40	LA (U2)	Phase-A energization signal output (U2)	For sink driving for phase-A output FET gate (upper N-ch)

Pin No.	Name	Pin Functions	Remarks
41	OUT-A	Phase-A motor pin	
42	LA (L2)	Phase-A energization signal output (L2)	For sink driving for phase-A output FET gate (lower N-ch)
43	LA (L1)	Phase-A energization signal output (L1)	For source driving for phase-A output FET gate (lower N-ch)
44	LB (U1)	Phase-B energization signal output (U1)	For source driving for phase-B output FET gate (upper N-ch)
45	LB (U2)	Phase-B energization signal output (U2)	For sink driving for phase-B output FET gate (upper N-ch)
46	OUT-B	Phase-B motor pin	
47	LB (L2)	Phase-B energization signal output (L2)	For sink driving for phase-B output FET gate (lower N-ch)
48	LB (L1)	Phase-B energization signal output (L1)	For source driving for phase-B output FET gate (lower N-ch)
49	LC (U1)	Phase-C energization signal output (U1)	For source driving for phase-C output FET gate (upper N-ch)
50	LC (U2)	Phase-C energization signal output (U2)	For sink driving for phase-C output FET gate (upper N-ch)
51	OUT-C	Phase-C motor pin	
52	LC (L2)	Phase-C energization signal output (L2)	For sink driving for phase-C output FET gate (lower N-ch)

Pin Layout



Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	30	V
Input voltage	V_{IN}	5.5 (Note 1)	V
Output voltage	V_{OUT}	5.5 (Note 2)	V
		40 (Note 3)	
Output current	I_{OUT}	20 (Note 4)	mA
		10 (Note 5)	
Power dissipation	P_D	1.3 (Note 6)	W
Operating temperature	T_{opr}	−30~85	°C
Storage temperature	T_{stg}	−55~150	°C

Note 1: CW/CCW, STB,START,BRAKE, Idc,Fref

Note 2: Ready, FGS

Note 3: LA (U), LB (U), LC (U)

Note 4: LA (U), LB (U), LC (U), LA (L), LB (L), LC (L)

Note 5: Vref1

Note 6: When mounted on the board
(glass epoxy, 50 mm × 50 mm × 1.6 mm, copper foil 36%, thickness = 18 μm, single-sided)

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Operating Conditions (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	10~28	V
External clock frequency	Fref	200~2 k	Hz

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.

Sine Wave PWM Drive

<Energization Switching>

Upon start-up, the TB6571FG drives the motor with square waves for 120° energization using phase detection signals (hall device signals).

If the frequency (f) of the position detection signal (hall device signal) for a single phase exceeds the specified value (f_H), the TB6571FG switches to 180° energization.

The following formula determines: $f_H = fx1 / (2^{10} \times 32 \times 6)$

fx1: The system clock frequency (fx1) is obtained by multiplying the external clock frequency (fref).

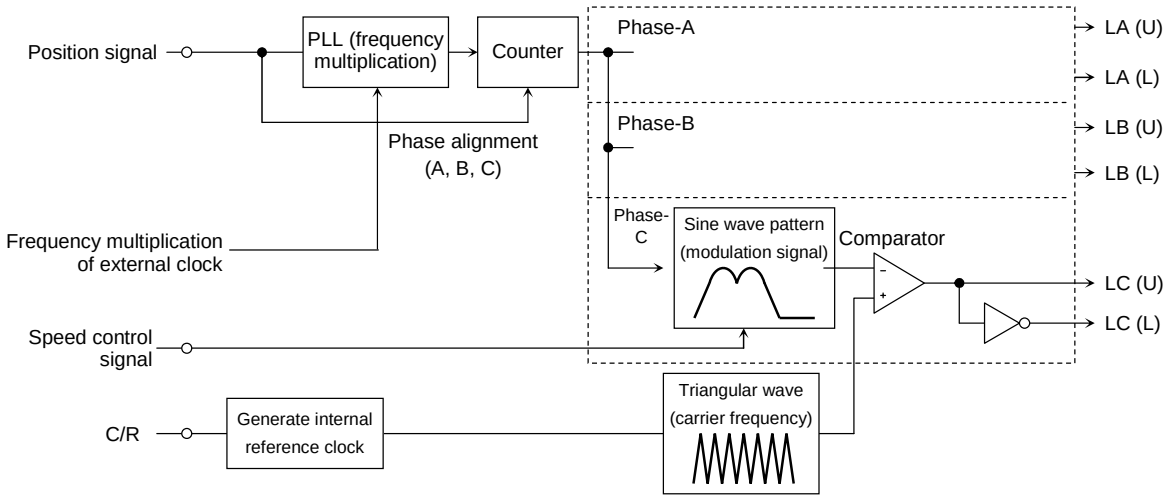
$fx\ 1 = 4 \times 1024 \times fref$

Thus, a transition from 120° energization to 180° energization occurs according to the external clock frequency.

Mode Table

Rotation State	Drive Mode
$f_H > f$	Square wave drive (120°energization)
$f_H < f$	Sine wave PWM drive (180°energization)

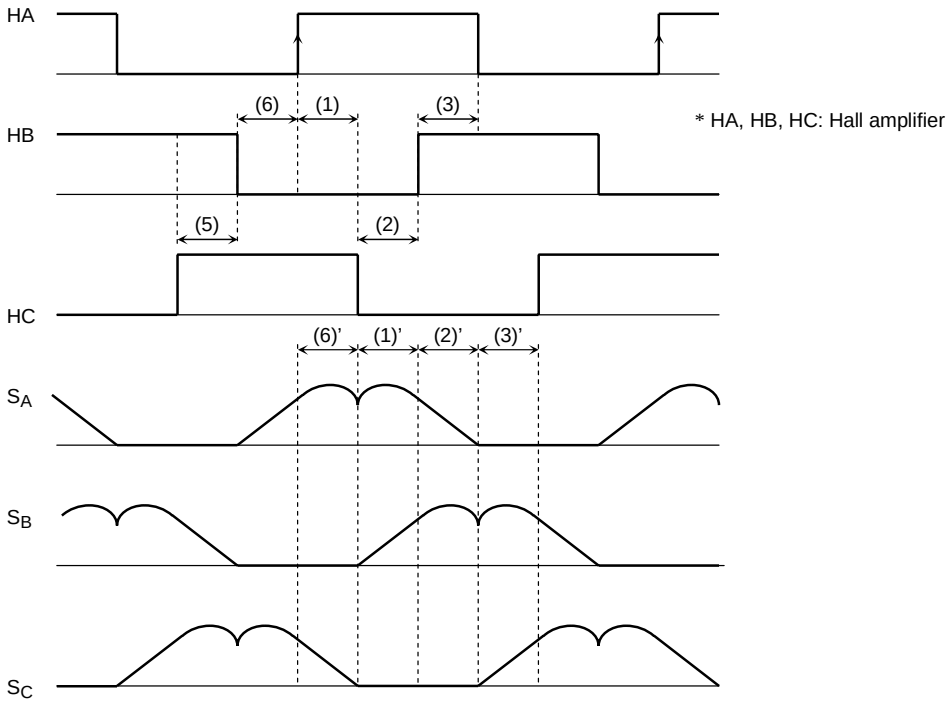
<Operation Flow>



The TB6571FG uses position detection signals to create modulation waveforms, which it compares with triangular waves to generate sine wave PWM signals.

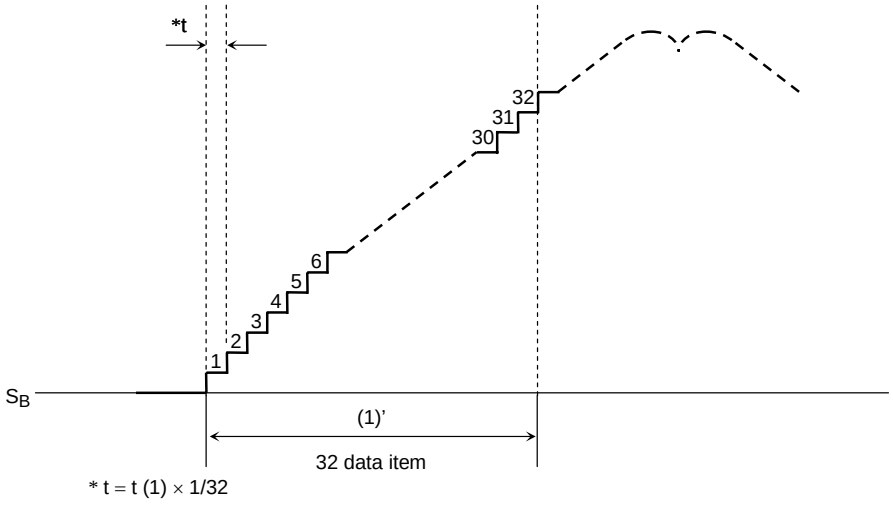
It counts the time between zero-crossing points for the three position detection signals (electrical angle: 60°) and uses the time as data for the next 60° phase of the modulation waveforms.

A 60° phase part of a modulation waveform consists of 32 data items. The time width for a single data item in a 60° phase part is 1/32 of that for the preceding 60° phase part. The modulation waveform proceeds with that width.

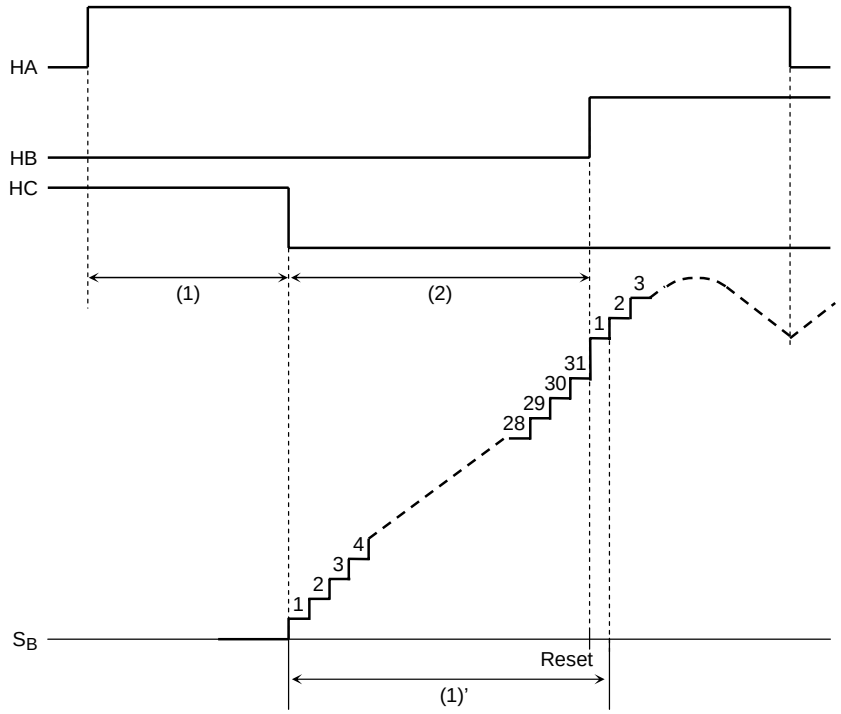


In the above chart, the time between HA rising and HC falling is marked (1). The modulation waveform within the (1)' period proceeds with a width that is 1/32 of (1). In the same way, the waveform within the (2)' period proceeds with 1/32 of (2), which is the time between HC falling and HB rising.

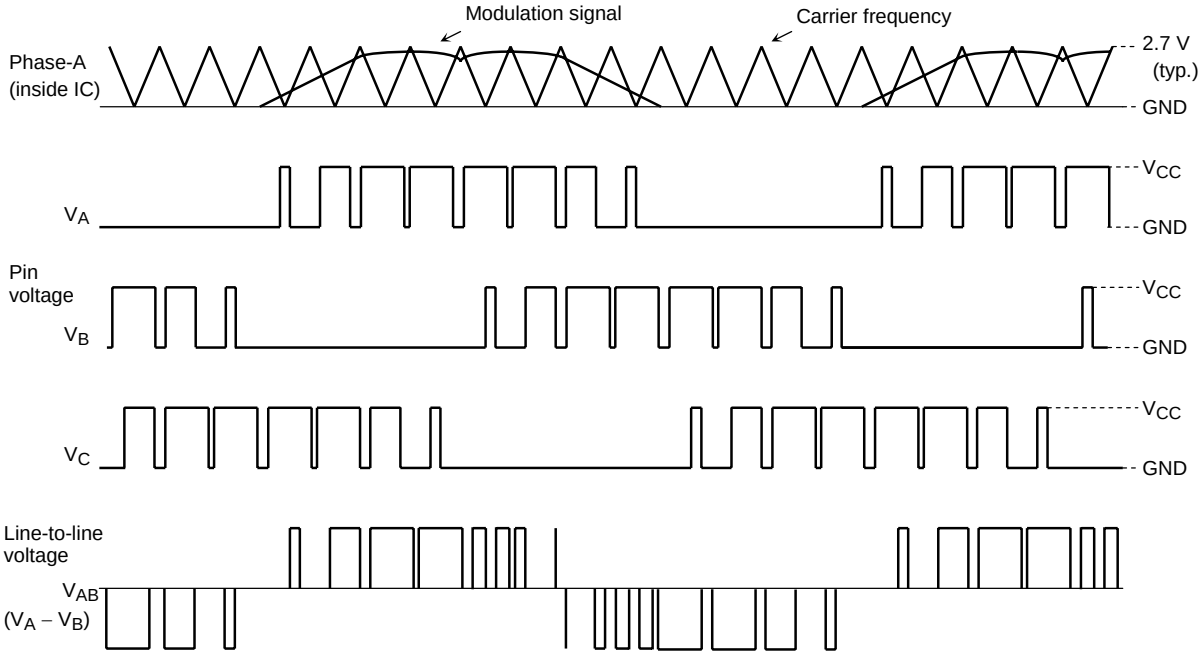
If next zero-crossing does not take place appear after 32 data items, the next 32 data items proceed with the same time width until next zero-crossing occurs.



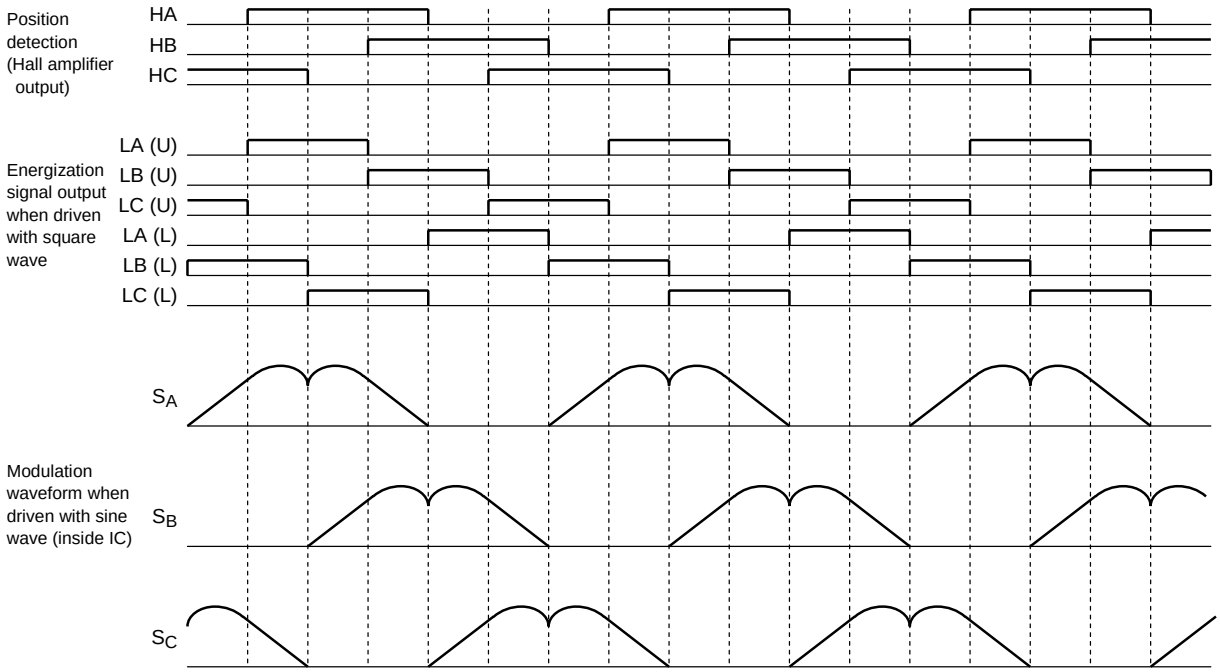
In addition, the TB6571FG performs phase alignment with the modulation waveforms at each zero-crossing in the position detection signals.
For every 60° of electrical angle, it synchronizes with the rising and falling edges of the position detection signals (Hall amplifier output signals), thus resetting the modulation waveforms.
If zero-crossing timing is shifted in position detection signals, causing next zero-crossing to occur before 32 data items are reached for the 60° phase, the data is reset and data for the next 60° phase is started. In that case, the modulation waveforms become discontinuous at a reset.



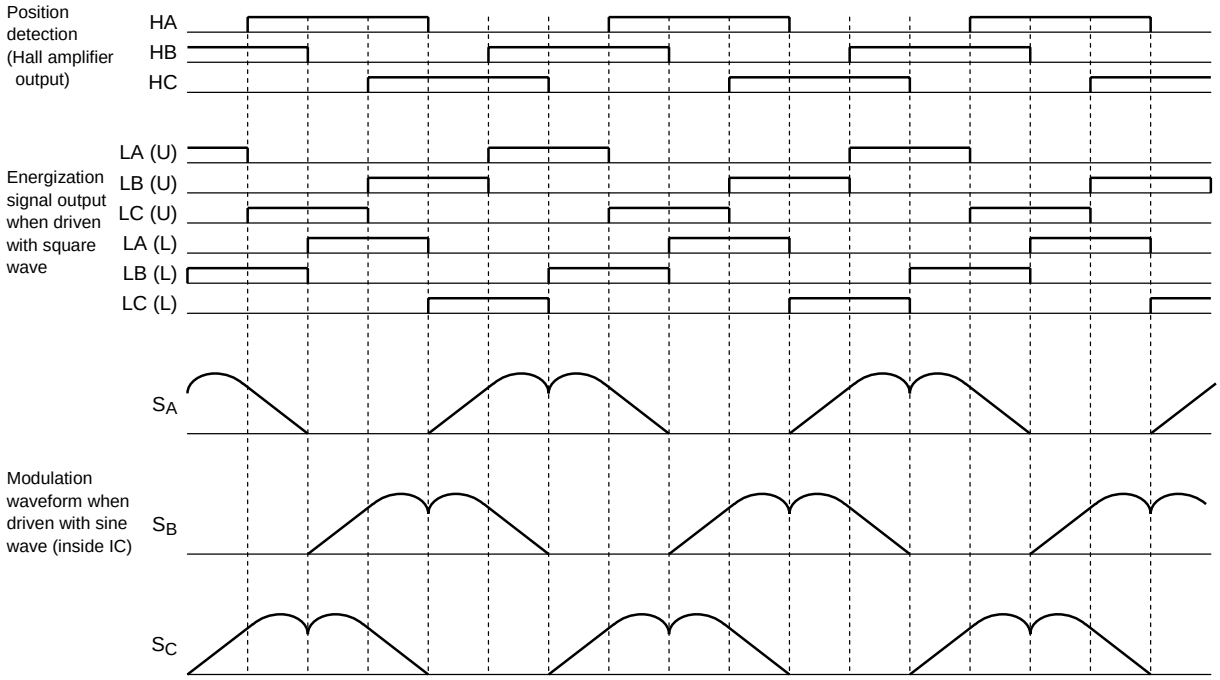
Operating Waveforms for Sine wave PWM Drive



Timing Charts



Forward rotation



Reverse rotation

* HA, HB, HC: Hall amplifier outputs

Generating an Internal Reference Clock

The TB6571FG uses external C and R to generate a reference clock internally.
It uses the reference clock to generate triangular waves, which determine the carrier frequency, and set a dead time.
The clock also functions as a reference clock for the charge pump (booster) and lead angle circuit ADC.

Generating Triangular Waves

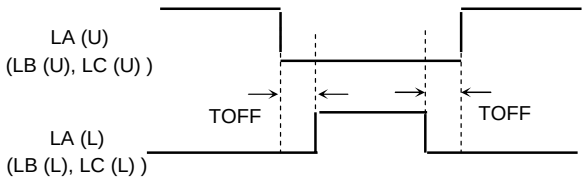
The TB6571FG compares the modulation waveforms with triangular waves to generate PWM signals.
The carrier frequency for PWM control depends on the frequency of the triangular waves.
The triangular waves are switched according to the internal reference clock frequency.

The following formula obtains the PWM frequency, where fx2 is the internal reference clock frequency:
PWM frequency fpwm = fx2/252 (= triangular wave frequency)
For example: When fx2 = 5 MHz: fpwm = 19.8 kHz
When fx2 = 4 MHz: fpwm = 15.8 kHz
When fx2 = 3 MHz: fpwm = 11.9 kHz

Dead time Setup Circuit

To apply PWM control with synchronous regeneration for output FETs, the TB6571FG sets a dead time for energization signal outputs, thus preventing the upper and lower output power FETs from turning on simultaneously.
It uses the internal reference clock, generated from external CR, to set a dead time.

Dead Time



The following formula obtains the dead time, where fx2 is the internal reference clock frequency:
Dead time td = (1/fx2) × 4
For example: When fx2 = 5 MHz: td = 0.8 μs
When fx2 = 4 MHz: td = 1.0 μs
When fx2 = 3 MHz: td = 1.3 μs

Charge Pump

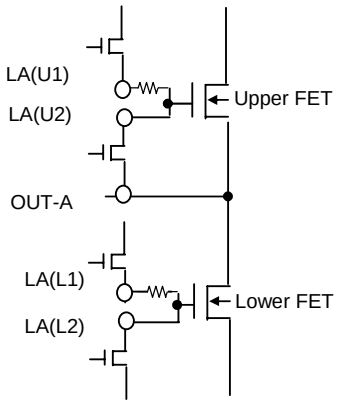
The TB6571FG incorporates a charge pump to drive two N-ch FETs in the external output FET configuration, in particular, to generate the gate voltage for the upper N-ch FET.
The booster voltage is V_{CC} + 8.0 V and the upper gate drive voltage is V_{CC} + 7.75 V.
The charge pump boosts the voltage using a frequency that is 1/16 of the internal reference clock frequency, fx2 (250 kHz when fx2 = 4 MHz).

Motor Output Pins

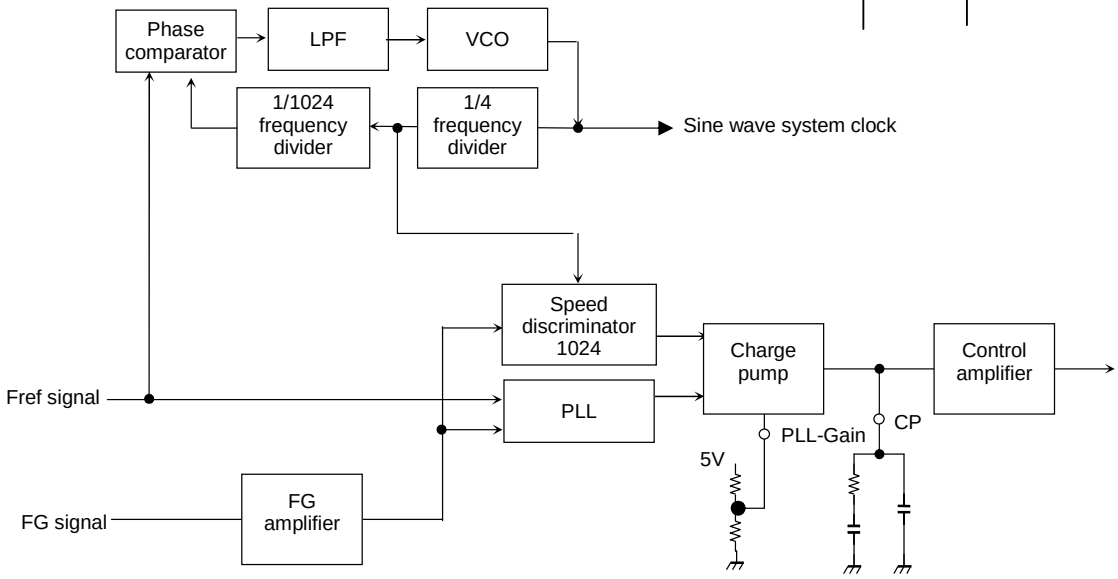
During PWM operation, the source voltage for the upper external N-ch FET swings between GND and VM.
VGS for the Nch-FET is clamped so that it does not exceed VGS (max) = 20 V.

External FET Gate Drive Output

The output for driving the upper FET is divided into two pins so that resistor adjustment is enabled only for gate driving (sourcing), thus reducing impedance for extraction.
The output for driving the lower FET is also divided.
The upper FET is driven with the LA(U1) pin on the source and the LA(U2) pin on the sink. The lower FET is driven with LA(L1) on the source and LA(L2) on the sink.



Speed Control

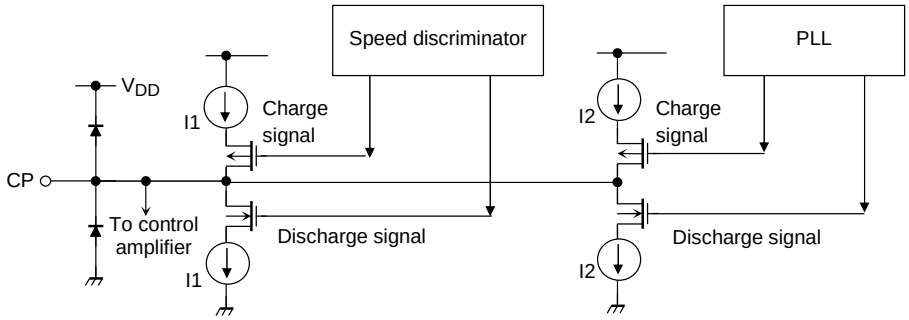


- The TB6571FG uses a speed discriminator and PLL to control speed.
- The speed discriminator has two counter stages, each of which alternately counts a single period of the FG signal. The resulting difference signal is output as two signals (charge pulses and discharge pulses).
- The PLL counts the phase difference between the 1/2 FG signal and reference signal. The resulting difference signal is output as two signals (charge pulses and discharge pulses). The phase difference is assumed to be zero when the FG frequency is outside the lock range (±6% of the specified value).
- The gain ratio between the speed discriminator and PLL is set using an external resistor.
- The total gain is set using an external constant for the charge pump.
- VCO PLL
  The maximum guaranteed range for the VCO oscillation frequency is a quadruple width, with a single external constant as a condition.
- FG frequency = speed control clock/speed discriminator
  → Speed control clock = FG frequency × speed discriminator
  FG frequency = 200 to 2 k, speed discriminator = 1024
  Speed control clock = 0.2048 to 2.048 MHz
  System clock = speed control clock × 4
  = 0.8192 to 8.192 MHz
- When the Fref input is open, the output is turned off.
- Note that a sudden variation in rotation speed may cause a motor current to be regenerated into the power supply, resulting in the rise of the motor voltage.

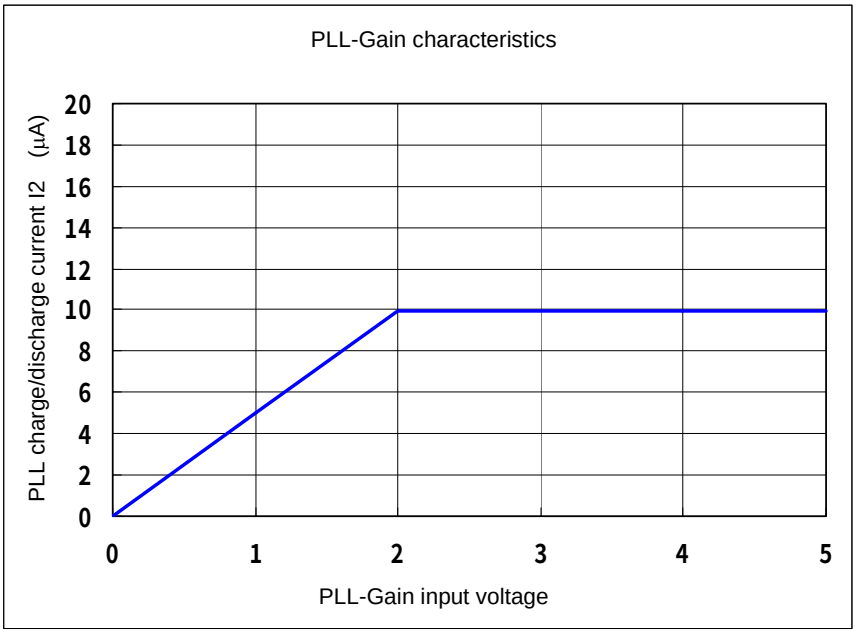
(Note)

- When the system clock is saturated, a READY signal may remain being L output even if external clock frequency and FG frequency shift. Please confirm optimization of a VCO system PLL circuit constant(25pin,22pin).

Charge Pump

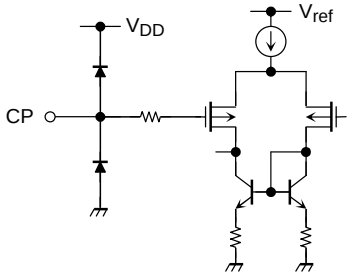


- The charge pump consists of MOS transistors, which enable fast switching, thus allowing control with higher resolution.
  For the speed discriminator and PLL gains, the ratio of the charge/discharge current is specified using an external resistor (PLL-Gain).
  The charge/discharge current for the speed discriminator, I1, is 100 μA (typ.) and the PLL charge/discharge current, I2, can be specified using the external PLL-Gain voltage.



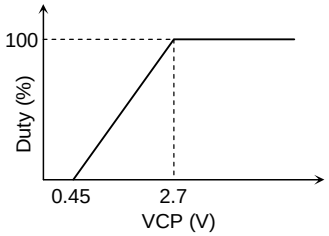
- The charge pump is placed in discharge mode upon stop or braking.
  Because the external capacitance becomes zero upon stop or braking, the charge-up time upon start is constant, so that the time required for the motor to start is also stable.
- Upon start, the charge pump is forcibly charged.

Control amplifier

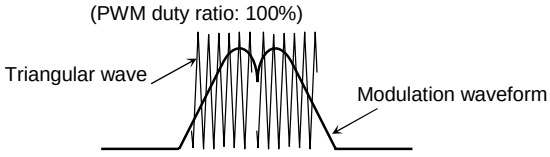


- The voltage integrated in the charge pump is input to the control amplifier.
  The input is placed in high-impedance state because it is a P-ch gate.

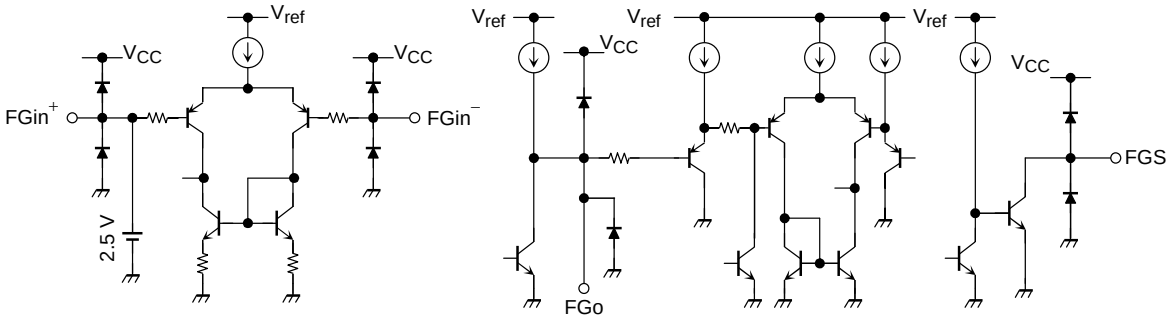
- The control amplifier circuit has an offset of 0.45 V (typ.). If the CP pin voltage exceeds the offset value, the energization signal outputs become active. It incorporates a clamp circuit that saturates the PWM duty ratio for the energization signal outputs when the CP pin voltage becomes 2.7 V (typ.).



- The PWM duty ratio indicates the value at the peak of the modulation waveform. A duty ratio of 100% indicates that the peak value coincides with the peak of the triangular wave.



FG amplifier/hysteresis comparator

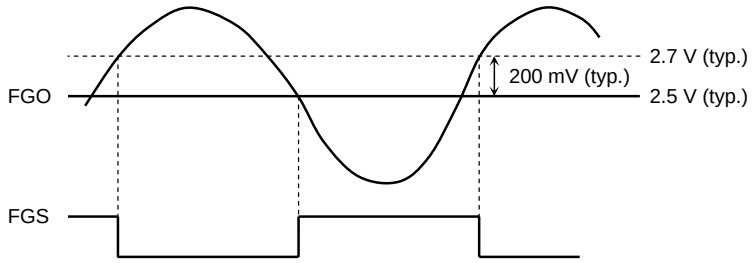


- The FG amplifier supports pattern FG and incorporates an internal reference voltage of 2.5 V.
  Entering a sine wave of 50 mVpp or greater results in a signal multiplied by the gain being output.
  The open loop gain is 45 dB (min) (design target value).

- The FG amplifier is followed by a hysteresis comparator, which compares the FG output and delivers it to the FGS.
  The comparator has a single-side hysteresis of 200 mV for the 2.5 V reference voltage. The square wave signal output from the FGS enters the internal counter.

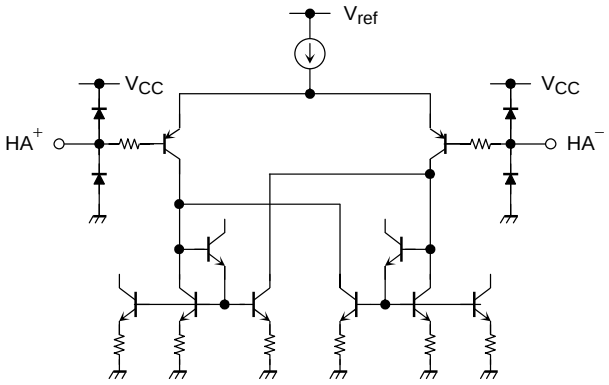
- The FGO output dynamic range is as follows:

  1.0 V~V_{ref} −1.0 V at IFGO = ±200 μA



- The FGS has an open-collector output. Connect a pull-up resistor considering the following characteristics. The input current is 1 mA (max).
  VFGS = 0.7 V (max) at IFGS = 1 mA

Hall amplifier

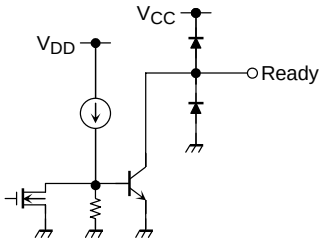


- The Hall amplifier accepts Hall device output signals. If input signals contain noise, connect a capacitor between inputs.
- The common-mode input voltage range is: VCMRH = 1.5 to 3.5 V.
  The Hall amplifier has an input hysteresis of ±8 mV(typ).
- The Hall amplifier converts Hall device signals into square waves, which then enter the internal logic.
- If positive/negative inputs are open, all external MOS FETs is turned off.

Ready circuit

- The Ready circuit indicates the motor rotation speed state using two states (L and HZ) of an open-collector output.
  When the motor is rotating, the circuit counts FG signals and outputs the following states according to whether the frequency is within or outside ±6% of the specified value:
  - Within ±6% of motor rotation speed: L output
  - Outside ±6% of motor rotation speed: HZ (high impedance)

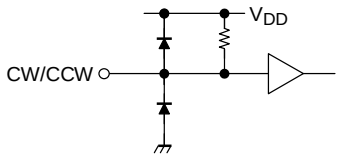
- Connect a pull-up resistor to the Ready output pin. Determine the resistance considering the following characteristics. The input current is 2 mA (max).
  VCER = 0.5 V (max) at IR = 2 mA



(Note)

- When the system clock is saturated, a READY signal may remain being L output even if external clock frequency and FG frequency shift. Please confirm optimization of a VCO system PLL circuit constant(25pin,22pin).

Forward/reverse rotation circuit



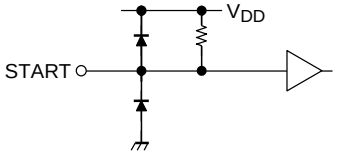
The circuit accepts a TTL input and incorporates a pull-up resistor.

CW/CCW Input	Mode
H	Reverse
L	Forwared

Forward: Hall device signals $HA^{+} \rightarrow HB^{+} \rightarrow HC^{+}$

Note that abrupt switching between forward and reverse rotation may result in an output FET being damaged due to reverse torque.

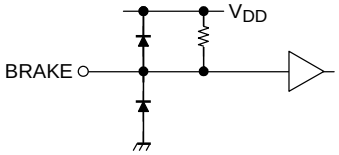
Start circuit



The circuit accepts a TTL input and incorporates a pull-up resistor.

START Input	Mode
H	Stop
L	Start

Brake

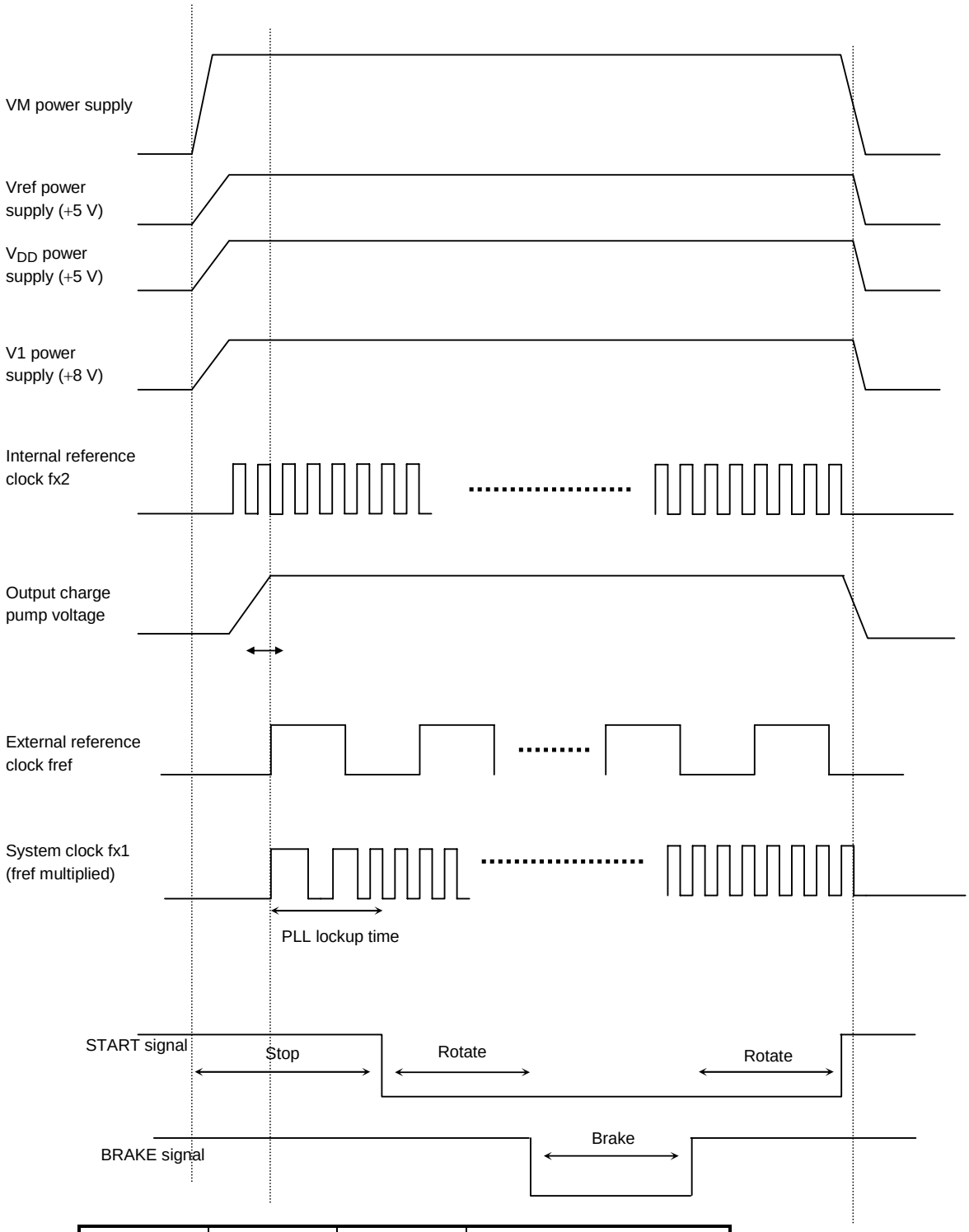


The circuit accepts a TTL input and incorporates a pull-up resistor.

BRAKE Input	Mode
H	OPERATION
L	BRAKE

Note that abrupt braking from high-speed rotation may result in an output FET being damaged.

Operation sequence

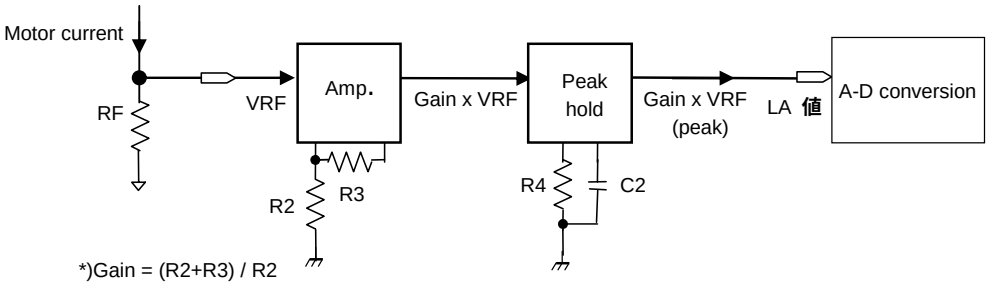


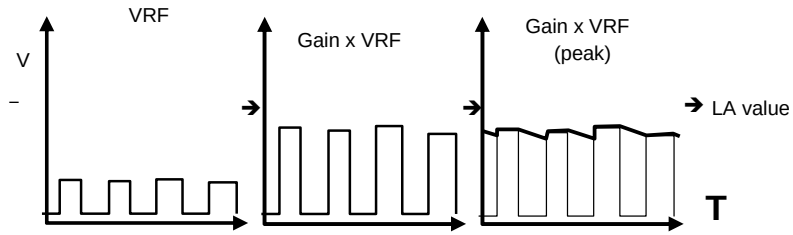
START 信号	BRAKE 信号	Mode	Description
H	H or L	Stop	Turn all external FETs off.
L	**H**	Rotate	Energize
L	**L**	Brake	Turn all lower external FETs on.

Automatic phase lead angle correction circuit

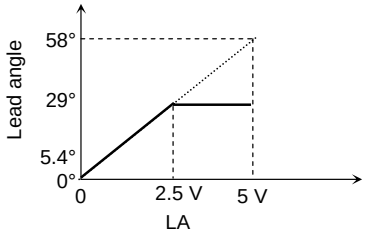
- The circuit corrects the lead angle using the motor current value.

Automatic lead angle correction





- The circuit can advance the phase of an energization signal relative to the induced voltage for input of 0 to 2.5 V (16 steps).
  0 V → 0°
  2.5 V → 29°(29° for an input voltage higher than 2.5 V)



- The circuit clamps the lead angle at 29°.
- It logically clamps the angle between 0° and 29°, rather than clamping the input voltage.

Lock protection circuit

- The circuit turns the output power FET off if the motor is locked.
- It turns off both upper and lower output power FETs if it detects the Ready signal with the following condition satisfied.
  The circuit latched state is terminated once the TB6571FG is placed in the stop or brake state.

Detected signal	Condition for triggering lock protection
Ready signal	The Ready signal output remains high for at least 5.5 seconds (typ.).

- A reference oscillation waveform for lock protection is generated using an external capacitor connected to the CLD pin and counted with the internal 5-bit counter.
- When CLD = 0.1 μF, the oscillation frequency is approximately 25 Hz, so that the lock protection triggering time is 5.5 seconds (typ.).

Constant voltage circuit

(1) Vref1

- The circuit creates 5 V for biasing the internal analog circuit and outputs it from the Vref pin. Connect a capacitor (0.1 μF to 1 μF) between the Vref pin and L-GND to prevent oscillation and absorb noise.
  The output load current is 10 mA.

  Vref = 5 V (typ.) ± 0.5 V at Io = 10 mA

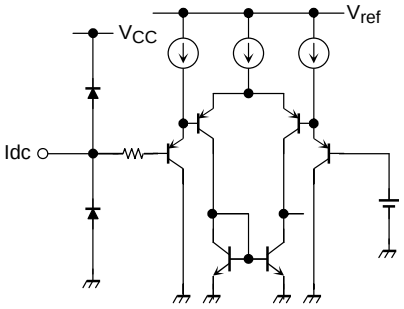
(2) V_{DD}

- The circuit outputs 5 V for biasing the internal logic circuit from the V_{DD} pin.
  Connect a capacitor (1 μF recommended) between the V_{DD} pin and L-GND to prevent oscillation and absorb noise.
  Connect no load to the V_{DD} pin.

(3) Vref2

- The circuit creates 8 V for output FET gate driving and outputs it from the Vref2 pin.
  Connect a capacitor (1 μF or larger) between the Vref2 pin and L-GND to prevent oscillation and absorb noise.

Overcurrent protection circuit



- The circuit turns the external output power FET off if the detected voltage is higher than 0.25 V (typ.). It re-activates the FET according to the carrier frequency.
  Note that the Idc pin accepts a direct analog comparator input and is highly sensitive. Use C and R, therefore, for filtering so that output current noise due to chopping does not activate the overcurrent protection circuit.

Power supply monitor circuit

The circuit monitors the Vref and Vcc voltages and turns the external power FET off if any of the following conditions are satisfied:
V_{CC} (H) ≤ 9 V, V_{CC} (L) ≤ 8.5 V, Vref1 (H) ≤ 4.5 V, Vref1 (L) ≤ 4.0 V

Thermal shutdown circuit

The circuit turns the external output power FET off if the junction temperature TSD (ON) exceeds 160°C. The thermal shutdown state is terminated once the TB6571FG is placed in the stop or brake state.

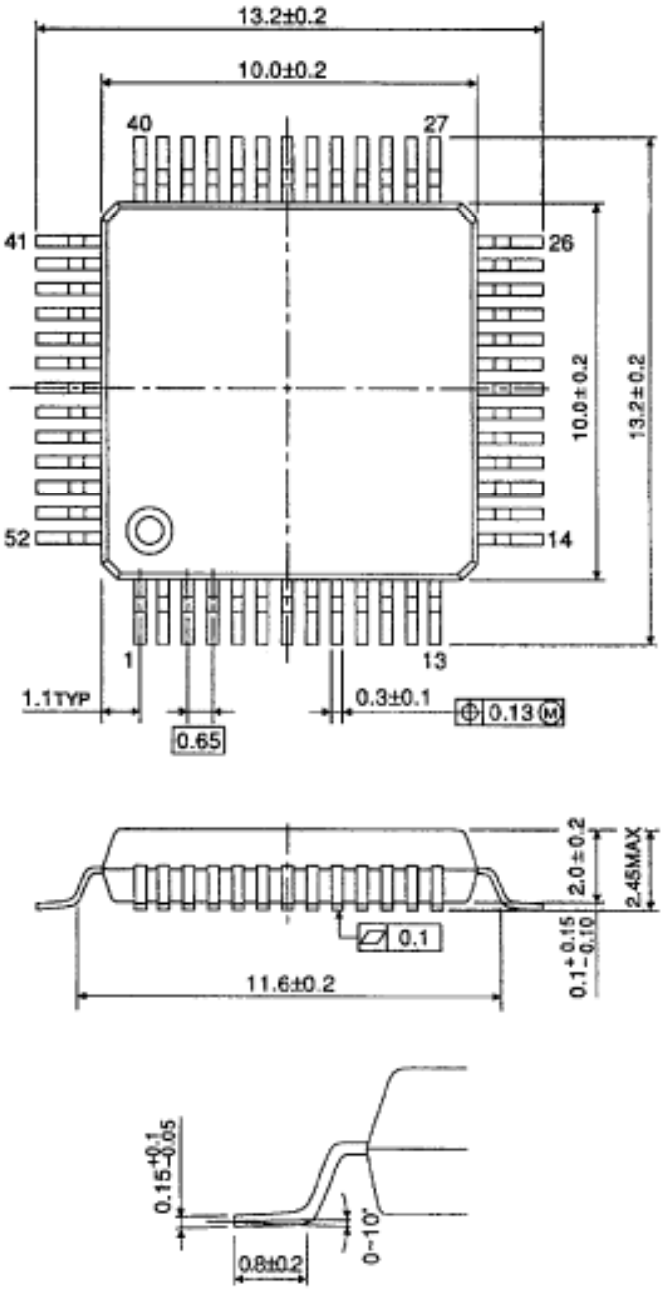
Electrical characteristics (V_{CC} = 24 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test conditions	Min	Typ.	Max	Units
Supply current		I_{CC1}		Start	6.0	12.0	18.0	mA
		I_{CC2}		Stop	5.4	9.0	12.6	
Hall amplifier	Common-mode input voltage range	VCMRH			1.5	—	3.5	V
	Input amplitude range	VH			50	—	—	mVpp
	Input hysteresis	VhysH	—	(Design target value)	± 4	± 8	± 12	mV
	Input current	IinH		VCMRH = 2.5 V, 1-phase	—	—	1	μA
Ready circuit	Remaining output voltage	VCER		Open collector output, ICER = 2 mA	—	—	0.5	V
	Output leakage current	ILR		Vready = 6 V	—	—	1	μA
FG amplifier	Input offset voltage	VOSFG			—		± 7	mV
	Remaining output voltage (upper)	VOFG (H)		IFG = 100 μA (source current)	Vref1 −1.2	—	Vref1	V
	Remaining output voltage (lower)	VOFG (L)		IFG = 100 μA (sink current)	—	—	1.2	
	Reference voltage	VrefFG			2.2	Vref1/ 2	2.8	V
FG hysteresis comparat-or	Hysteresis width	VhysS			0.15	0.2	0.25	V
	Remaining output voltage	VCES		Open collector output, ICES = 1 mA	—	—	0.5	V
	Output leakage current	VLS		VFGS = 6 V	—	—	1	μA
Control input circuit	Input voltage (H)	Vin(H)		CW/CCW, STB, BRAKE, START	2.0	—	5.5	V
	Input voltage (L)	Vin(L)		CW/CCW, STB, BRAKE, START	0	—	0.8	
	Input current (H)	IinCW (H)		Vin = 5 V	—	—	1	μA
	Input current (L)	IinCW (L)		Vin = GND	70	100	130	
Fref input circuit	Input voltage (H)	VinSB (H)		Fref	2.0	—	5.5	V
	Input voltage (L)	VinSB (L)		Fref	0	—	0.8	
	Input current (H)	Iin (H)		Vin = 5 V	—	—	1	μA
	Input current (L)	Iin (L)		Vin = GND	70	100	130	
Charge pump voltage		VG			V_{CC} + 7	V_{CC} + 8	V_{CC} + 9	V
Energization signal output voltage		VO (U)-(H)		LA (U)/LB (U)/LC (U), Io = 20 mA	VG −1.0	—	VG	V
		VO (U)-(L)			—	—	0.5	
		VO (L)-(H)		LA (L) /LB (L) /LC (L), Io = 20 mA	7.25	7.75	8.25	
		VO (L)-(L)			—	—	0.5	
Internal supply voltage output		V_{DD}			4.5	5.0	5.5	V
		Vref1			4.5	5.0	5.5	
		Vref2			8.2	8.7	9.2	
Current limiter circuit reference voltage		Vdc			0.23	0.25	0.27	V
Internal clock frequency		fx2		R=10 kΩ,C=51pF	3.4	3.8	4.2	MHz
Dead time		TOFF1		R=10 kΩ,C=51pF	1.2	1.7	2.2	μs
		TOFF2		R=10 kΩ,C=51pF	1.2	1.7	2.2	
Phase lead angle controller	Upper clamp limit	ACLH			—	29	—	°

Characteristics		Symbol	Test Circuit	Test conditions	Min	Typ.	Max	Units
Control amplifier	Rising voltage	VCR			0.3	0.5	0.6	V
	Saturation voltage	VCLP			2.7	2.85	3.0	
	Input current	IinCP			—	0	—	μA
Charge pump	Charge current	Icp +		(source current), Vcp = 3.1 V, V(PLL-GAIN)=0V	70	100	150	μA
	Discharge current	Icp −		(sink current), Vcp = 0.35 V, V(PLL-GAIN)=0V	70	100	150	
Lock protection circuit	Reference clock frequency	FLd		CLd = 0.1 μF	17.5	25	30	Hz
	Operating time	tLd			4.2	5.5	7.0	s

Package Dimensions

QFP52-P-1010-0.65 Unit : mm



Weight: 0.0 g (typ.)

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