MIC502

Fan Management IC

General Description

The MIC502 is a thermal and fan management IC which supports the features for NLX/ATX power supplies and other control applications.

Fan speed is determined by an external temperature sensor, typically a thermistor-resistor divider, and (optionally) a second signal, such as the NLX “FanC” signal. The MIC502 produces a low-frequency pulse-width modulated output for driving an external motor drive transistor. Low-frequency PWM speed control allows operation of standard brushless dc fans at low duty cycle for reduced acoustic noise and permits the use of a very small power transistor. The PWM time base is determined by an external capacitor.

An open-collector overtemperature fault output is asserted if the primary control input is driven above the normal control range.

The MIC502 features a low-power sleep mode with a user-determined threshold. Sleep mode completely turns off the fan and occurs when the system is asleep or off (both control inputs very low). A complete shutdown or reset can also be initiated by external circuitry as desired.

The MIC502 is available as 8-pin plastic DIP and SOIC packages in the –40°C to +85°C industrial temperature range.

Data sheets and support documentation can be found on Micrel’s web site at www.micrel.com.

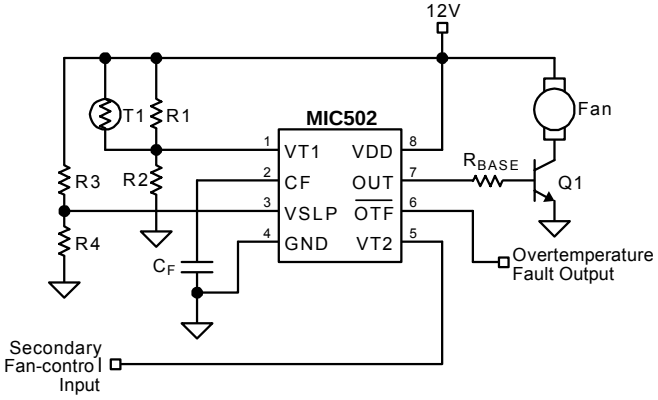
Features

- Temperature-proportional fan speed control
- Low-cost, efficient PWM fan drive
- 4.5V to 13.2V IC supply range
- Controls any voltage fan
- Overtemperature detection with fault output
- Integrated fan startup timer
- Automatic user-specified sleep mode
- Supports low-cost NTC/PTC thermistors
- 8-pin DIP and SOIC packages

Applications

- NLX and ATX power supplies
- Personal computers
- File servers
- Telecom and networking hardware
- Printers, copiers, and office equipment
- Instrumentation
- Uninterruptible power supplies
- Power amplifiers

Typical Application



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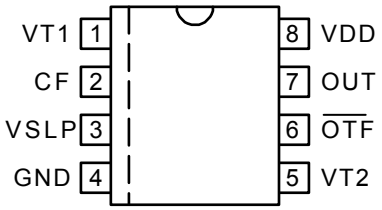
Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC502BN	–40° to +85°C	8-Pin Plastic DIP	Standard
MIC502YN	–40° to +85°C	8-Pin Plastic DIP	Pb-Free
MIC502BM	–40° to +85°C	8-Pin SOIC	Standard
MIC502YM	–40° to +85°C	8-Pin SOIC	Pb-Free

Pin Configuration



8-Pin SOIC (M)

8-Pin DIP (N)

Pin Description

Pin Number	Pin Name	Pin Function
1	VT1	Thermistor 1 (Input): Analog input of approximately 30% to 70% of V_{DD} produces active duty cycle of 0% to 100% at driver output (OUT). Connect to external thermistor network (or other temperature sensor). Pull low for shutdown.
2	CF	PWM Timing Capacitor (External Component): Positive terminal for the PWM triangle-wave generator timing capacitor. The recommended C_F is 0.1µF for 30Hz PWM operation.
3	VSLP	Sleep Threshold (Input): The voltage on this pin is compared to VT1 and VT2. When $V_{T1} < V_{SLP}$ and $V_{T2} < V_{SLP}$ the MIC502 enters sleep mode until V_{T1} orV_{T2} rises above V_{WAKE}. ($V_{WAKE} = V_{SLP} + V_{HYST}$). Grounding V_{SLP} disables the sleep-mode function.
4	GND	Ground.
5	VT2	Thermistor 2 (Input): Analog input of approximately 30% to 70% of V_{DD} produces active duty cycle of 0% to 100% at driver output (OUT). Connect to motherboard fan control signal or second temperature sensor.
6	/OTF	Overtemperature Fault (Output): Open-collector output (active low).Indicates overtemperature fault condition ($V_{T1} > V_{OT}$) when active.
7	OUT	Driver Output: Asymmetrical-drive active-high complimentary PWM output. Typically connect to base of external NPN motor control transistor.
8	VDD	Power Supply (Input): IC supply input; may be independent of fan power supply.

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Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +14V
Output Sink Current ($I_{OUT(sink)}$) 10mA
Output Source Current ($I_{OUT(source)}$) 25mA
Input Voltage (any pin) ..... –0.3V to V_{DD} +0.3V
Junction Temperature (T_J) ..... +125°C
Lead Temperature (soldering, 5 sec.) ..... 260°C
Storage Temperature (T_A) ..... –65°C to +150°C
ESD Rating[3]

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +4V to 13.2V
Sleep Voltage (V_{SLP}) ..... GND to V_{DD}
Temperature Range (T_A) ..... –40°C to +85°C
Power Dissipation at 25°C
SOIC 800mW
DIP 740mW
Derating Factors
SOIC ..... 8.3mW/°C
Plastic DIP ..... 7.7mW/°C

Electrical Characteristics

4.5V ≤ V_{DD} ≤ 13.2V, **Note 4**; T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current, Operating	V_{SLP} = GND, OTF, OUT = open, C_F = 0.1µF, V_{T1} = V_{T2} = 0.7 V_{DD}			1.5	mA
$I_{DD(slp)}$	Supply Current, Sleep	V_{T1} = GND, V_{SLP}, OTF, OUT = open, C_F = 0.1µF			500	µA
Driver Output						
t_R	Output Rise Time, **Note 5**	I_{OH} = 10mA			50	µs
t_F	Output Fall Time, **Note 5**	I_{OL} = 1mA			50	µs
I_{OL}	Output Sink Current	V_{OL} = 0.5V	**0.9**			mA
I_{OH}	Output Source Current	4.5V ≤ V_{DD} ≤ 5.5V, V_{OH} = 2.4V	**10**			mA
		10.8V ≤ V_{DD} ≤ 13.2V, V_{OH} = 3.2V	**10**			mA
I_{OS}	Sleep-Mode Output Leakage	V_{OUT} = 0V		1		µA
Thermistor and Sleep Inputs						
$V_{PWM(max)}$	100% PWM Duty Cycle Input Voltage		**67**	70	**73**	%V_{DD}
$V_{PWM(span)}$	$V_{PWM(max)}$ – $V_{PWM(min)}$		**37**	40	**43**	%V_{DD}
V_{HYST}	Sleep Comparator Hysteresis		**8**	11	**14**	%V_{DD}
V_{IL}	VT1 Shutdown Threshold				**0.7**	V
V_{IH}	VT1 Startup Threshold		**1.1**			V
V_{OT}	VT1 Overtemperature Fault Threshold	**Note 6**	**74**	77	**80**	%V_{DD}
I_{VT}, I_{VSLP}	VT1, VT2, VSLP Input Current		–2.5		1	µA
t_{RESET}	Reset Setup Time	minimum time V_{T1} < V_{IL}, to guarantee reset, **Note 5**	**30**			µs
Oscillator						
f	Oscillator Frequency, **Note 7**	4.5V ≤ V_{DD} ≤ 5.5V, C_F = 0.1µF	**24**	27	**30**	Hz
		10.8V ≤ V_{DD} ≤ 13.2V, C_F = 0.1µF	**27**	30	**33**	Hz
f_{MIN}, f_{MAX}	Oscillator Frequency Range	**Note 7**	15		90	Hz
$t_{STARTUP}$	Startup Interval			64/f		S

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Symbol	Parameter	Condition	Min	Typ	Max	Units
Overtemperature Fault Output						
V_{OL}	Active (Low) Output Voltage	I_{OL} = 2mA			0.3	V
I_{OH}	Off-State Leakage	$V_{/OTF} = V_{DD}$		1		µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Part is functional over this V_{DD} range; however, it is characterized for operation at 4.5V ≤ V_{DD} ≤ 5.5V and 10.8V ≤ V_{DD} ≤ 13.2V ranges. These ranges correspond to nominal V_{DD} of 5V and 12V, respectively.
5. Guaranteed by design.
6. V_{OT} is guaranteed by design to always be higher than $V_{PWM(max)}$.
7. Logic time base and PWM frequency. For other values of C_F, f(Hz) = 30Hz $\frac{0.1\mu F}{C}$, where C is in µF.

Timing Diagrams

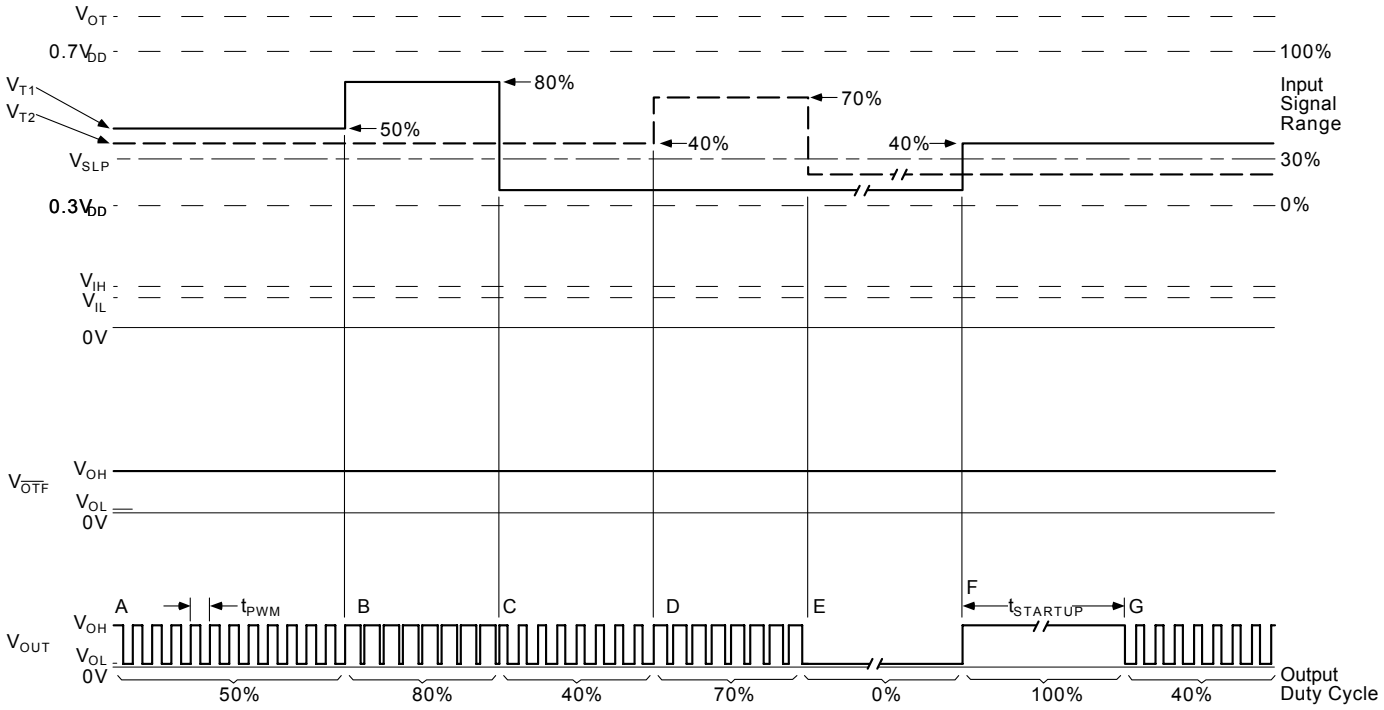

Figure 1. Typical System Behavior

Note A. Output duty-cycle is initially determined by V_{T1}, as it is greater than V_{T2}.

Note B. PWM duty-cycle follows V_{T1} as it increases.

Note C. V_{T1} drops below V_{T2}. V_{T2} now determines the output duty-cycle.

Note D. The PWM duty-cycle follows V_{T2} as it increases.

Note E. Both V_{T1} and V_{T2} decrease below V_{SLP} but above VIL. The device enters sleep mode.

Note F. The PWM 'wakes up' because one of the control inputs (V_{T1} in this case) has risen above V_{WAKE}. The startup timer is triggered, forcing OUT high for 64 clock periods. ($V_{WAKE} = V_{SLP} + V_{HYST}$. See "Electrical Characteristics").

Note G. Following the startup interval, the PWM duty-cycle is the higher of V_{T1} and V_{T2}.

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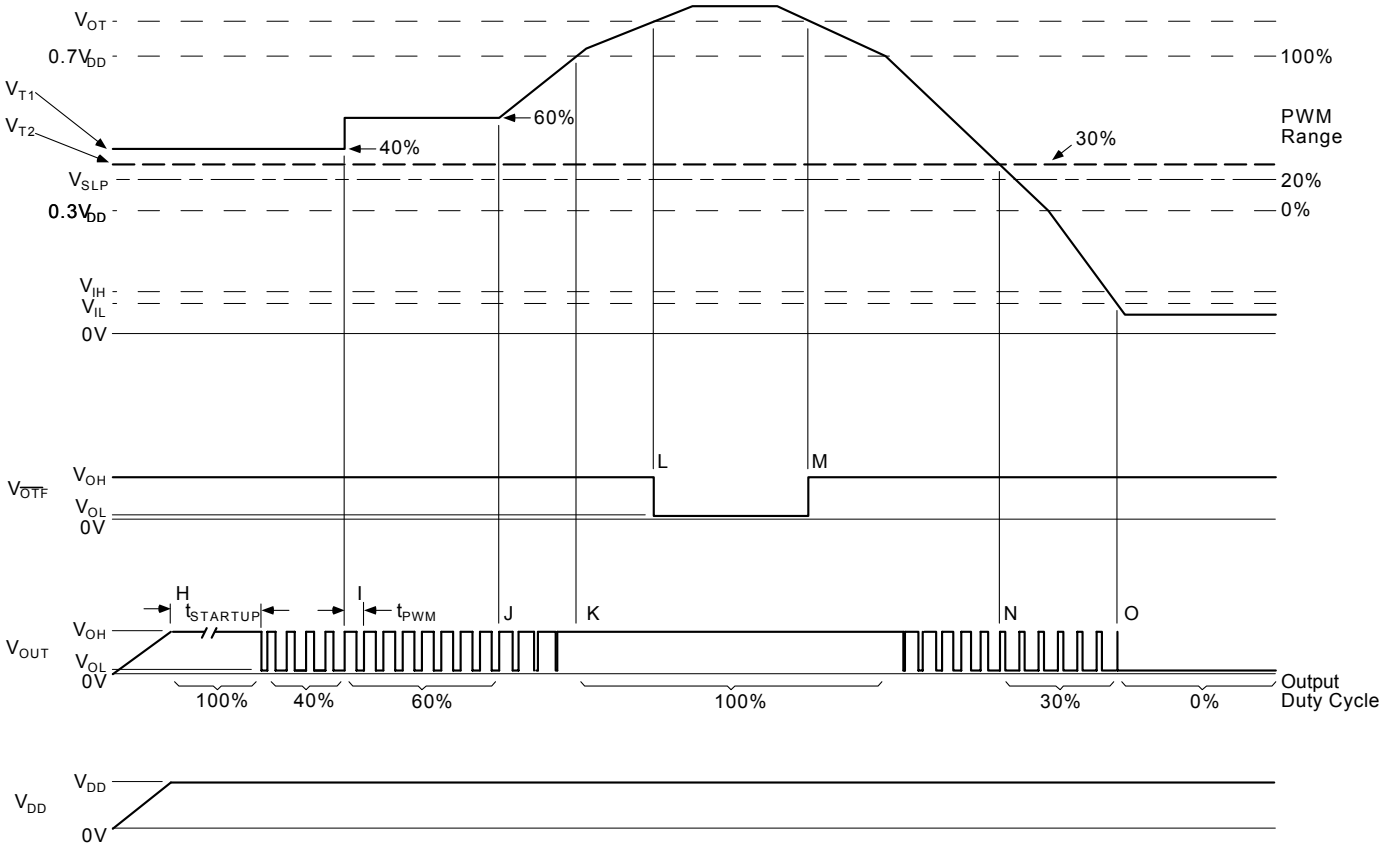

Figure 2. MIC502 Typical Power-Up System Behavior

Note H. At power-on, the startup timer forces OUT on for 64 PWM cycles of the internal timebase (t_{PWM}). This insures that the fan will start from a dead stop.

Note I. The PWM duty-cycle follows the higher of V_{T1} and V_{T2}, in the case, V_{T1}.

Note J. The PWM duty-cycle follows V_{T1} as it increases.

Note K. PWM duty-cycle is 100% (OUT constantly on) anytime $V_{T1} > V_{PWM(max)}$.

Note L. /OTF is asserted anytime $V_{T1} > V_{OT}$. (The fan continues to run at 100% duty-cycle).

Note M. /OTF is deasserted when V_{T1} falls below V_{OT}; duty-cycle once again follows V_{T1}.

Note N. Duty-cycle follows V_{T1} until $V_{T1} < V_{T2}$, at which time V_{T2} becomes the controlling input signal. Note that V_{T1} is below V_{SLP} but above V_{IH}; so normal operation continues. (Both V_{T1} and V_{T2} must be below V_{SLP} to active sleep mode).

Note O. All functions cease when $V_{T1} < V_{IL}$; this occurs regardless of the state of V_{T2}.

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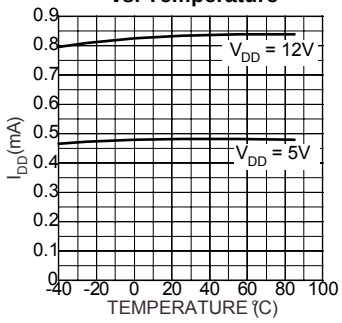
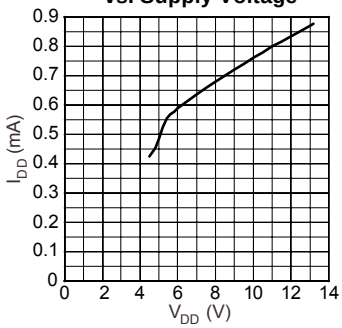
Typical Characteristics

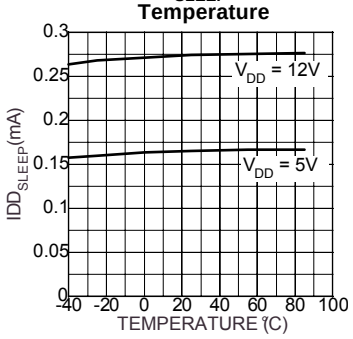
Supply Current vs. Temperature



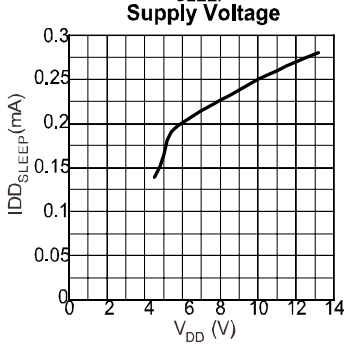
Supply Current vs. Supply Voltage



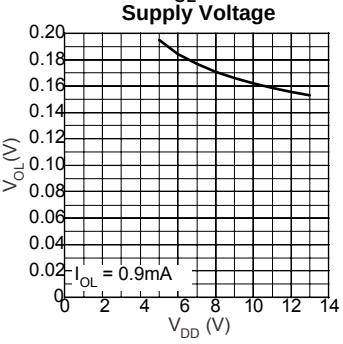
IDD_{SLEEP} vs. Temperature



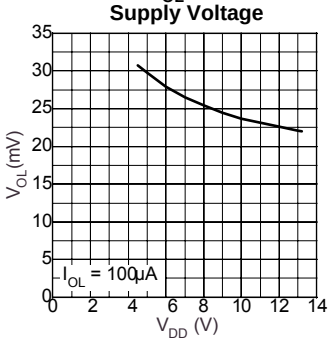
IDD_{SLEEP} vs. Supply Voltage



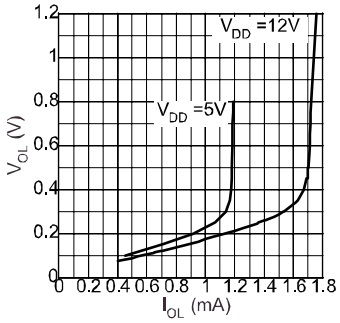
V_{OL} vs. Supply Voltage



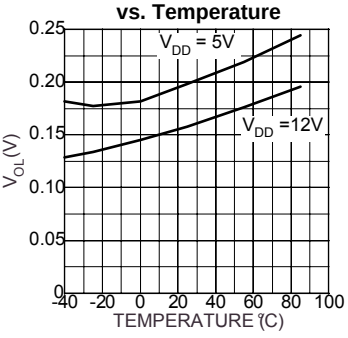
V_{OL} vs. Supply Voltage



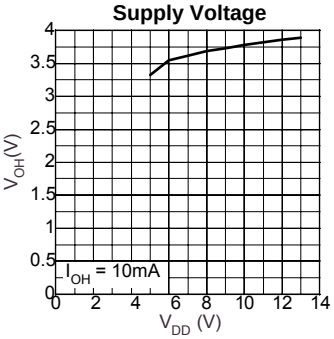
V_{OL} vs. I_{OL}



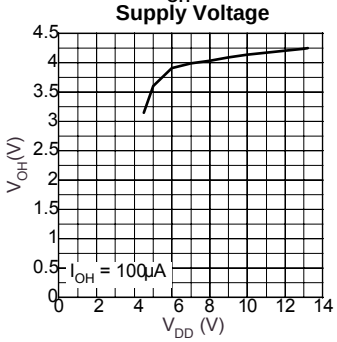
V_{OL} vs. Temperature



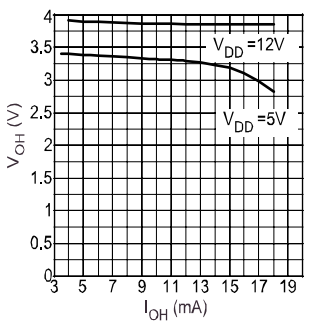
V_{OH} vs. Supply Voltage



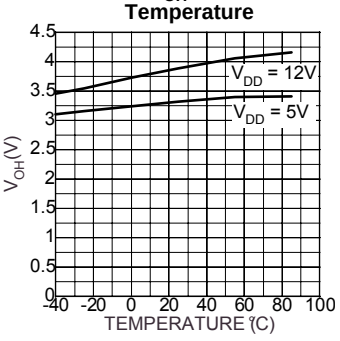
V_{OH} vs. Supply Voltage



V_{OH} vs. I_{OH}



V_{OH} vs. Temperature



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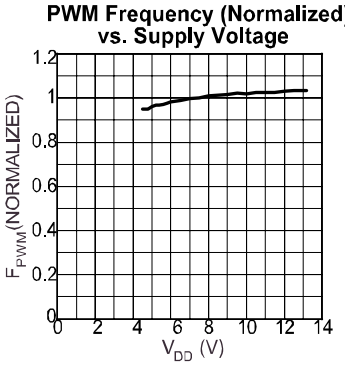
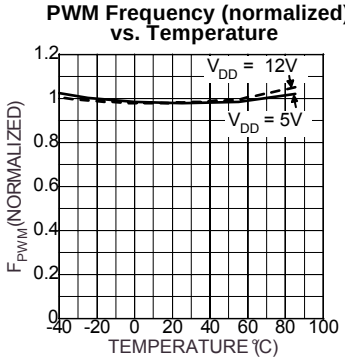
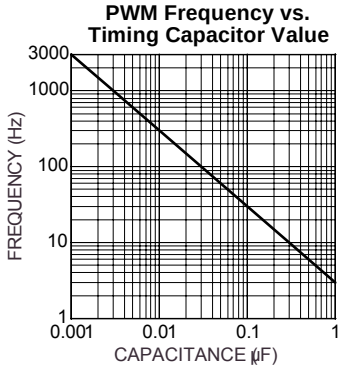
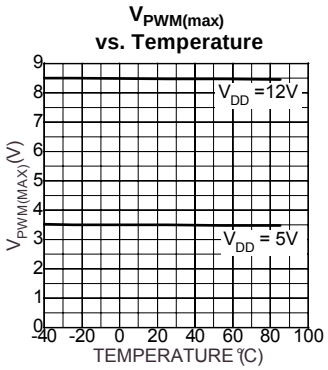
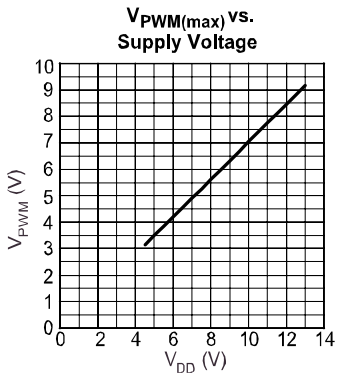
Typical Characteristics (cont.)

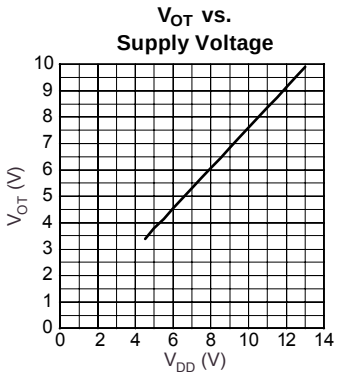


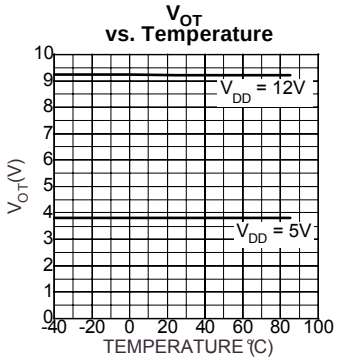












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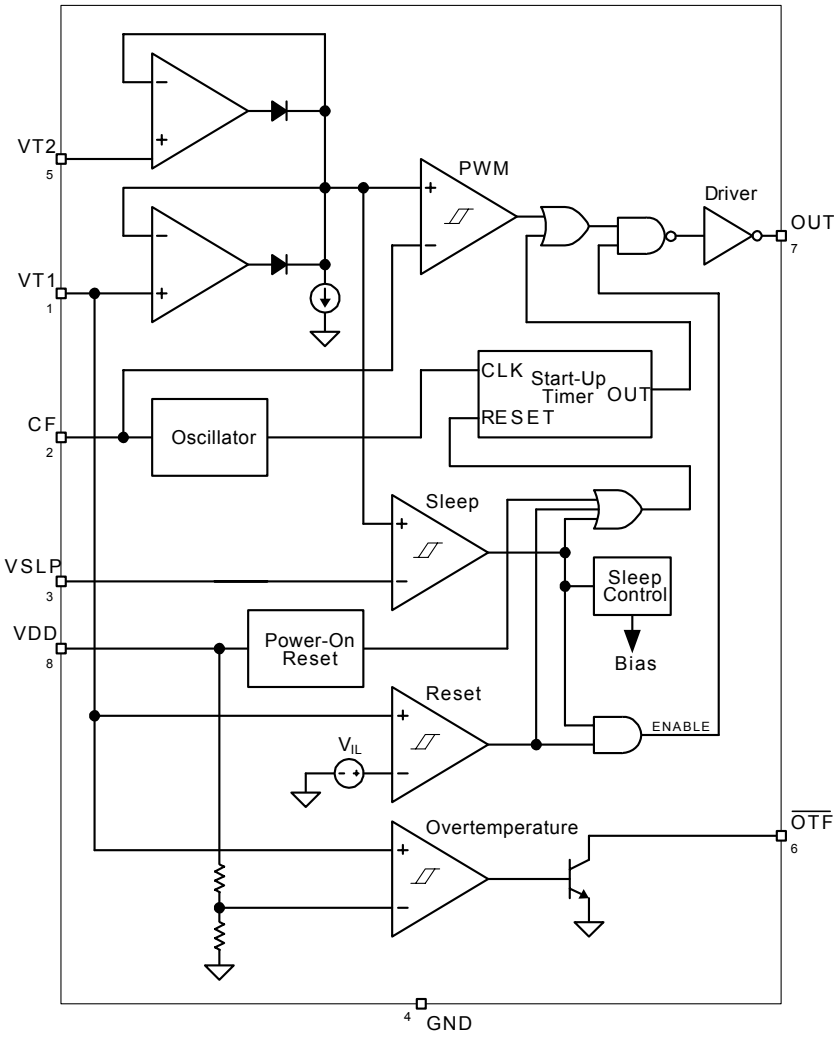
Functional Diagram



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Functional Description

Oscillator

A capacitor connected to CF determines the frequency of the internal time base which drives the state-machine logic and determines the PWM frequency. This operating frequency will be typically 30Hz to 60Hz. (C_F = 0.1µF for 30Hz.)

Pulse-Width Modulator

A triangle-wave generator and threshold detector comprise the internal pulse-width modulator (PWM). The PWM's output duty-cycle is determined by the higher of V_{T1} or V_{T2}. A typical voltage range of 30% to 70% of V_{DD} applied to the V_{T1} and V_{T2} pins corresponds to 0% to 100% duty-cycle. Since at least one of the control voltage inputs is generally from a thermistor-resistor divider connected to V_{DD}, the PWM out-put duty cycle will not be affected by changes in the supply voltage.

Driver Output

OUT is a complementary push-pull digital output with asymmetric drive (approximately 10mA source, 1mA sink, see "Electrical Characteristics"). It is optimized for directly driving an NPN transistor switch in the fan's ground-return. See "Applications Information" for circuit details.

Shutdown/Reset

Internal circuitry automatically performs a reset of the MIC502 when power is applied. The MIC502 may be shut down at anytime by forcing V_{T1} below its V_{IL} threshold. This is typically accomplished by connecting the V_{T1} pin to open-drain or open-collector logic and results in an immediate and asynchronous shutdown of the MIC502. The OUT and /OTF pins will float while V_{T1} is below V_{IL}.

If V_{T1} then rises above V_{IH}, a device reset occurs. Reset is equivalent to a power-up condition: the state of /OTF is cleared, a startup interval is triggered, and normal fan operation begins.

Startup Interval

Any time the fan is started from the off state (power-on or coming out of sleep mode or shutdown mode), the PWM output is automatically forced high for a startup interval of 64× t_{PWM}. Once the startup interval is complete, PWM operation will commence and the duty-cycle of the output will be determined by the higher of V_{T1} or V_{T2}.

Overtemperature Fault Output

/OTF is an active-low, open-collector logic output. An over-temperature condition will cause /OTF to be asserted. An overtemperature condition is determined by V_{T1} exceeding the normal operating range of 30% to 70% of V_{DD} by > 7% of V_{DD}. Note that V_{OT} is guaranteed by design to always be higher than $V_{PWM(max)}$.

Sleep Mode

When V_{T1} and V_{T2} fall below V_{SLP}, the system is deemed capable of operating without fan cooling and the MIC502 enters sleep mode and discontinues fan operation. The threshold where the MIC502 enters sleep mode is determined by V_{SLP}. Connecting the V_{SLP} pin to ground disables sleep mode.

Once in sleep mode, all device functions cease (/OTF inactive, PWM output off) unless V_{T1} or V_{T2} rise above V_{WAKE}. (V_{WAKE} = V_{SLP} + V_{HYST}). V_{HYST} is a fixed amount of hysteresis added to the sleep comparator which prevents erratic operation around the V_{SLP} operating point. The result is stable and predictable thermostatic action: whenever possible the fan is shut down to reduce energy consumption and acoustic noise, but will always be activated if the system temperature rises.

If the device powers-up or exits its reset state, the fan will not start unless V_{T1} or V_{T2} rises above V_{WAKE}.

System Operation

Power Up

- A complete reset occurs when power is applied.
- OUT is off (low) and /OTF is inactive (high/floating).
- If $V_{T1} < V_{IL}$, the MIC502 remains in shutdown.
- The startup interval begins. OUT will be on (high) for 64 clock cycles (64 × t_{PWM}).
- Following the startup interval, normal operation begins.

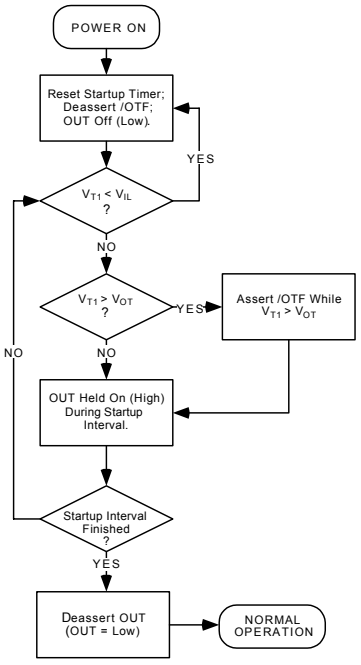

Figure 3. Power-Up Behavior

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Normal Operation

Normal operation consists of the PWM operating to control the speed of the fan according to V_{T1} and V_{T2}. Exceptions to this otherwise indefinite behavior can be caused by any of three conditions: V_{T1} exceeding V_{OT}, an overtemperature condition; V_{T1} being pulled below V_{IL} initiating a device shutdown and reset; or both V_{T1} and V_{T2} falling below V_{SLP}, activating sleep mode. Each of these exceptions is treated as follows:

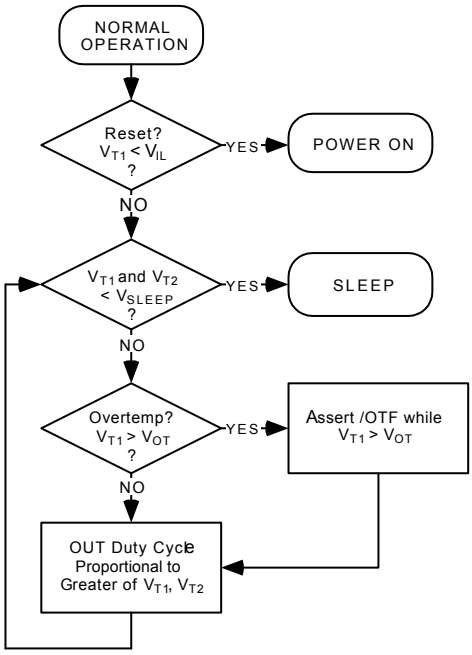

Figure 4. Normal System Behavior

- *Overtemperature*: If the system temperature rises typically 7% above the 100% duty-cycle operating point, /OTF will be activated to indicate an overtemperature fault. ($V_{T1} > V_{OT}$) Overtemperature detection is essentially independent of other operations — the PWM continues its normal behavior; with $V_{T1} > V_{PWM(max)}$, the output duty-cycle will be 100%. If V_{T1} falls below V_{OT}, the overtemperature condition is cleared and /OTF is no longer asserted. It is assumed that in most systems, the /OTF output will initiate power supply shutdown.
- *Shutdown/Reset:* If V_{T1} is driven below V_{IL} an immediate, asynchronous shutdown occurs. While in shutdown mode, OUT is off (low), and /OTF is unconditionally inactive (high/floating). If V_{T1} subsequently rises above V_{IH}, a device reset will occur. Reset is indistinguishable from a power-up condition. The state of /OTF is cleared, a startup interval is triggered, and normal fan operation begins.
- *Sleep:* If V_{T1} and V_{T2} fall below V_{SLP}, the device enters sleep mode. All internal functions cease unless V_{T1} or V_{T2} rise above V_{WAKE}. ($V_{WAKE} = V_{SLP} + V_{HYST}$). The /OTF output is unconditionally inactive (high/floating) and the PWM is disabled during sleep (OUT will float).

Sleep Mode

During normal operation, if V_{T1} and V_{T2} fall below V_{SLP}, the device will go into sleep mode and fan operation will stop. The MIC502 will exit sleep mode when V_{T1} or V_{T2} rise above V_{SLP} by the hysteresis voltage, V_{HYST}. When this occurs, normal operation will resume. The resumption of normal operation upon exiting sleep is indistinguishable from a power-on reset. (See “Sleep: Normal Operation,” above.)

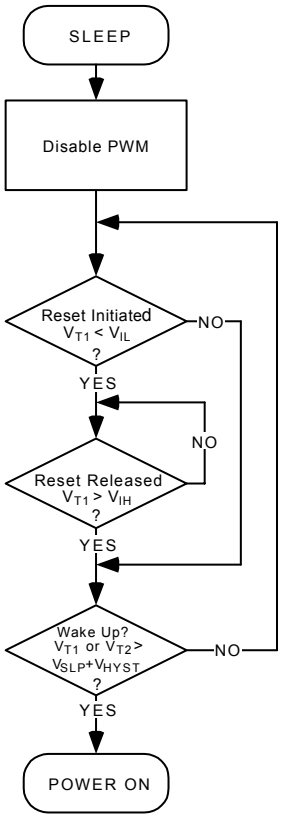

Figure 5. Sleep-Mode Behavior

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Application Information

The Typical Application drawing on page 1 illustrates a typical application circuit for the MIC502. Interfacing the MIC502 with a system consists of the following steps:

1. Selecting a temperature sensor
2. Interfacing the temperature sensor to the V_{T1} input
3. Selecting a fan-drive transistor, and base-drive current limit resistor
4. Deciding what to do with the Secondary Fan-Control Input
5. Making use of the Overtemperature Fault Output

Temperature Sensor Selection

Temperature sensor T1 is a negative temperature coefficient (NTC) thermistor. The MIC502 can be interfaced with either a negative or positive tempco thermistor; however, a negative temperature coefficient thermistor typically costs less than its equivalent positive tempco counterpart. While a variety of thermistors can be used in this application, the following paragraphs reveal that those with an R25 rating (resistance at 25°C) of from about 50kΩ to 100kΩ lend themselves nicely to an interface network that requires only a modest current drain. Keeping the thermistor bias current low not only indicates prudent design; it also prevents self-heating of the sensor from becoming an additional design consideration. It is assumed that the thermistor will be located within the system power supply, which most likely also houses the speed-controlled fan.

Temperature Sensor Interface

As shown by the Electrical Characteristics table, the working voltage for input V_{T1} is specified as a percentage of V_{DD}. This conveniently frees the designer from having to be concerned with interactions resulting from variations in the supply voltage. By design, the operating range of V_{T1} is from about 30%of V_{DD} to about 70% of V_{DD}.

$$V_{PWM(min)} = V_{PWM(min)} - V_{PWM(span)}$$

When $V_{T1} = V_{PWM(max)} \approx 0.7V_{DD}$, a 100% duty-cycle motor-drive signal is generated. Conversely, when $V_{T1} = V_{PWM(min)} \approx 0.3V_{DD}$, the motor-drive signal has a 0% duty cycle. Resistor voltage divider R1 || T1, R2 in the Typical Application diagram is designed to preset V_{T1} to a value of V_{PWM} that corresponds to the slowest desired fan speed when the resistance of thermistor T1 is at its highest (cold) value. As temperature rises the resistance of T1 decreases and V_{T1} increases because of the parallel connection of R1 and T1.

Since $V_{T1} = V_{PWM(min)}$ represents a stopped fan (0% duty-cycle drive), and since it is foreseen that at least some cooling will almost always be required, the lowest voltage applied to the V_{T1} input will normally be somewhat higher than $0.3V_{DD}$ (or $>V_{PWM(min)}$). It is assumed that the system will be in sleep mode rather than operate the fan at a very low duty cycle (<25%). Operation at very low duty cycle results in relatively little airflow. Sleep mode should be used to reduce acoustic noise when the system is cool. For a given minimum desired fan speed, a corresponding $V_{T1(min)}$ can be determined via the following observation:

since

$$V_{PWM(max)} = 70\% \text{ of } V_{DD} \propto 100\% \text{ RPM}$$

and

$$V_{PWM(min)} = 30\% \text{ of } V_{DD} \propto 0\% \text{ RPM}$$

then

$$V_{PWM(span)} = 40\% \text{ of } V_{DD} \propto 100\% \text{ RPM } \textit{range}.$$

Figure 6 shows the following linear relationship between the voltage applied to the V_{T1} input, motor drive duty cycle, and *approximate* motor speed.

since

$$V_{T1} = 0.7V_{DD} \propto 100\% \text{ PWM}$$

then

$$V_{T1} = 0.6V_{DD} \propto 75\% \text{ PWM}$$

and

$$V_{T1} = 0.5V_{DD} \propto 50\% \text{ PWM}$$

and

$$V_{T1} = 0.4V_{DD} \propto 25\% \text{ PWM}$$

In addition to the R25 thermistor rating, sometimes a datasheet will provide the ratio of R25/R50 (resistance at 25°C divided by resistance at 50°C) is given. Sometimes this is given as an R0/R50 ratio. Other datasheet contents either specify or help the user determine device resistance at arbitrary temperatures. The thermistor interface to the MIC502 usually consists of the thermistor and two resistors.

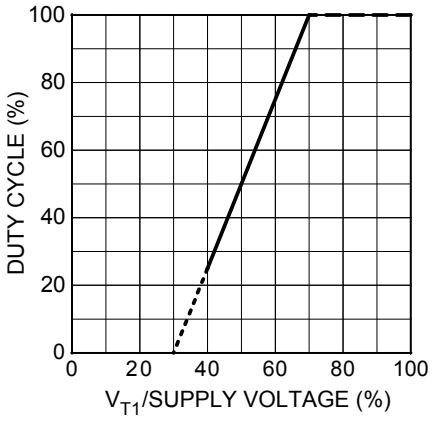

Figure 6. Control Voltage vs. Fan Speed

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Design Example

The thermistor-resistor interface network is shown in the Typical Application drawing. The following example describes the design process: A thermistor datasheet specifies a thermistor that is a candidate for this design as having an R25 resistance of 100kΩ. The datasheet also supports calculation of resistance at arbitrary temperatures, and it was discovered the candidate thermistor has a resistance of 13.6k at 70°C (R70). Accuracy is more important at the higher temperature end of the operating range (70°C) than the lower end because we wish the overtemperature fault output (/OTF) to be reasonably accurate — it may be critical to operating a power supply crowbar or other shutdown mechanism, for example. The lower temperature end of the range is less important because it simply establishes minimum fan speed, which is when less cooling is required.

Referring to the "Typical Application," the following approach can be used to design the required thermistor interface network:

let

$R1 = \infty$

$R_{T1} = 13.6k$ (at 70°C)

and

$V_T = 0.7V_{DD}$ (70% of VDD)

since

$$V_T = \frac{V_{DD} \times R2}{(R_{T1} \,||\, R1 + R2)}$$

$$0.7 = \frac{R2}{(R_{T1} + R2)}$$

$0.7R_{T1} + 0.7R2 = R2$

$0.7R_{T1} = 0.3R2$

and

$R2 = 2.33R_{T1} = 2.33 \times 13.6k = 31.7k \approx 33k$

Let's continue by determining what the temperature-proportional voltage is at 25°C.

let

$R1 = \infty$

and

$R_{T1} = 100k$ (at 25°C).

from

$$V_T = \frac{V_{DD} \times R2}{(R_{T1} + R2)}$$

$$V_T = \frac{V_{DD} \times 33k}{(100k + 33k)}$$

$V_T = 0.248V_{DD}$

Recalling from above discussion that the desired V_T for 25°C should be about 40% of V_{DD}, the above value of 24.8% is far too low. This would produce a voltage that would stop the fan (recall from the above that this occurs when V_T is about 30% of V_{DD}. To choose an appropriate value for R1 we need to learn what the parallel combination of R_{T1} and R1 should beat 25°C:

again

$$V_T = \frac{V_{DD} \times R2}{(R_{T1} \,||\, R1 + R2)}$$

$$0.4 = \frac{R2}{(R_{T1} \,||\, R1 + R2)}$$

$0.4(R_{T1} \,||\, R1) + 0.4R2 = R2$

$0.4(R_{T1} \,||\, R1) = 0.6R2$

and

$R_{T1} \,||\, R1 = 1.5R2 = 1.5 \times 33k = 49.5k$

since

$R_{T1} = 100k$

and

$R_{T1} \,||\, R1 = 49.5k \approx 50k$

let

$R1 = 100k$

While that solves the low temperature end of the range, there is a small effect on the other end of the scale. The new value of V_T for 70°C is 0.734, or about 73% of V_{DD}. This represents only a 3% shift from the design goal of 70% of V_{DD}. In summary, R1 = 100k, and R2 = 33k. The candidate thermistor used in this design example is the RL2010-54.1K-138-D1, manufactured by Keystone Thermometrics.

The R25 resistance (100kΩ) of the chosen thermistor is probably on the high side of the range of potential thermistor resistances. The result is a moderately high-impedance network for connecting to the V_{T1} and/or V_{T2} input(s). Because these inputs can have up to 1µA of leakage current, care must be taken if the input network impedance becomes higher than the example. Leakage current and resistor accuracy could require consideration in such designs. Note that the V_{SLP} input has this same leakage current specification.

Secondary Fan-Control Input

The above discussions also apply to the secondary fan-control input, V_{T2}, pin 5. It is possible that a second thermistor, mounted at another temperature-critical location outside the power supply, may be appropriate. There is also the possibility of accommodating the NLX "FanC" signal via this input. If a second thermistor is the desired solution, the V_{T2} input may be treated exactly like the V_{T1} input. The above discussions then apply directly. If, however, the NLX FanC signal is to be

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incorporated into the design then the operating voltage (V_{DD} = 5V vs. V_{DD} = 12V) becomes a concern. The FanC signal is derived from a 12V supply and is specified to swing at least to 10.5V. A minimum implementation of the FanC signal would provide the capability of asserting full-speed operation of the fan; this is the case when 10.5V ≤ FanC ≤ 12V. This FanC signal can be applied directly to the V_{T2} input of the MIC502, but only when its V_{DD} is 12V. If this signal is required when the MIC502 V_{DD} = 5V a resistor divider is necessary to reduce this input voltage so it does not exceed the MIC502 V_{DD} voltage. A good number is 4V (80%V_{DD}).

Because of input leakage considerations, the impedance of the resistive divider should be kept at ≤ 100kΩ. A series resistor of 120kΩ driven by the FanC signal and a 100kΩ shunt resistor to ground make a good divider for driving the V_{T2} input.

Transistor and Base-Drive Resistor Selection

The OUT motor-drive output, pin 7, is intended for driving a medium-power device, such as an NPN transistor. A rather ubiquitous transistor, the 2N2222A, is capable of switching up to about 400mA. It is also available as the PN2222A in a plastic TO-92 package. Since 400mA is about the maximum current for most popular computer power supply fans (with many drawing substantially less current) and since the MIC502 provides a minimum of 10mA output current, the PN2222A, with its minimum β of 40, is the chosen motor-drive transistor.

The design consists solely of choosing the value R_{BASE} in Figures 7 and 8. To minimize on-chip power dissipation in the MIC502, the value of R_{BASE} should be determined by the power supply voltage. The Electrical Characteristics table specifies a minimum output current of 10mA. However, different output voltage drops (V_{DD} – V_{OUT}) exist for 5V vs.12V operation. The value R_{BASE} should be as high as possible for a given required transistor base-drive current in order to reduce on-chip power dissipation.

Referring to the “Typical Application” and to the “Electrical Characteristics” table, the value for R_{BASE} is calculated as follows. For V_{DD} = 5V systems, I_{OH} of OUT (pin 7) is guaranteed to be a minimum of 10mA with a V_{OH} of 2.4V.

R_{BASE} then equals (2.4V – V_{BE}) ÷ 10mA = 170Ω.

For V_{DD} = 12V systems, R_{BASE} = (3.4 – 0.7) ÷ 0.01 = 250Ω.

Overtemperature Fault Output

The /OTF output, pin 6, is an open-collector NPN output. It is compatible with CMOS and TTL logic and is intended for alerting a system about an overtemperature condition or triggering a power supply crowbar circuit. If V_{DD} for the MIC502 is 5V the output should not be pulled to a higher voltage. This output can sink up to 2mA and remain compatible with the TTL logic-low level.

Timing Capacitors vs. PWM Frequency

The recommended C_F (see first page) is 0.1µF for operation at a PWM frequency of 30Hz. This frequency is factory trimmed within ±3Hz using a 0.1% accurate capacitor. If it is desired to operate at a different frequency, the new value for C_F is calculated as follows:

$$C = \frac{3}{f}, \text{ where C is in µF and f is in Hz}$$

The composition, voltage rating, ESR, etc., parameters of the capacitor are not critical. However, if tight control of frequency vs. temperature is an issue, the temperature coefficient may become a consideration.

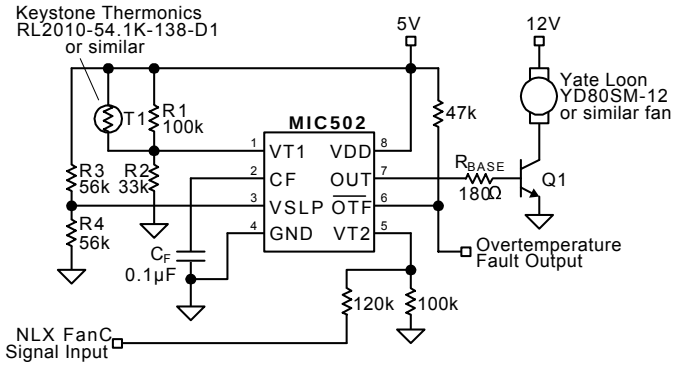

Figure 7. Typical 5V V_{DD} Application Circuit

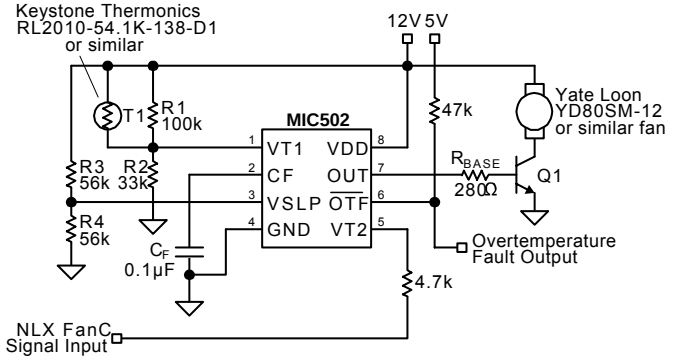

Figure 8. Typical 12V V_{DD} Application Circuit

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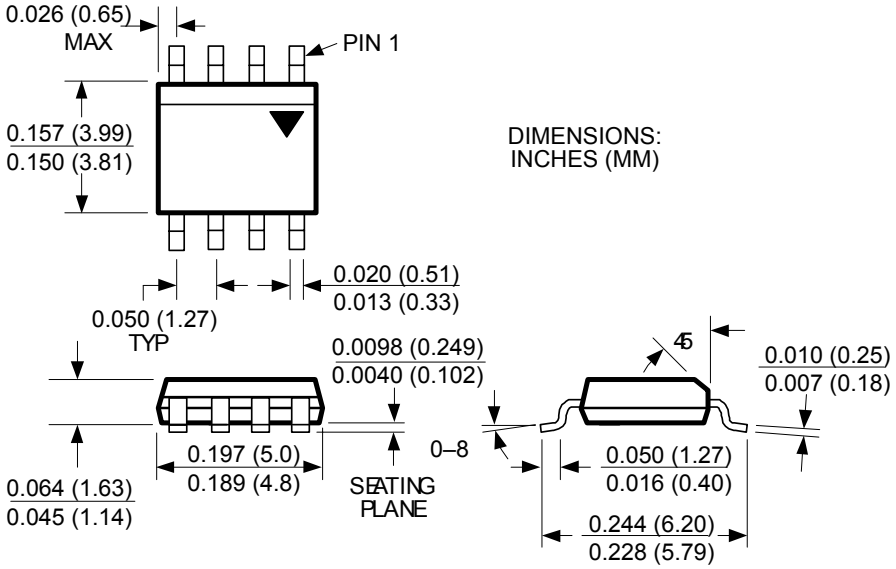
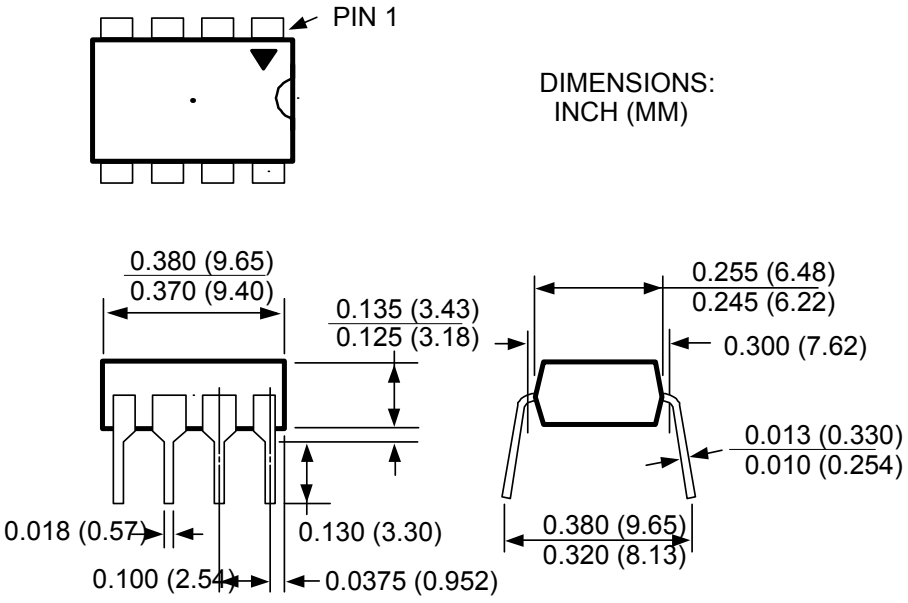
Package Information



8-Pin SOIC (M)



8-Pin Plastic DIP (N)

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TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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