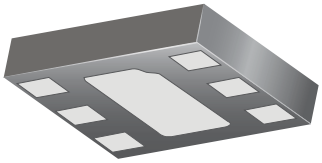
Low-Voltage, Full-Bridge Brushless DC Motor Driver with Integrated Hall Sensor IC, PWM Speed Control, Soft-Switching, and Reverse Battery and Short Circuit Protection

Features and Benefits

- Low-voltage operation, 1.8 to 4.2 V
- Multifunction CONTROL pin input:
  - Direct input PWM for speed control
  - Active braking for fast stop cycle
  - Sleep function to reduce average power consumption
- Reverse voltage protection on VDD and CONTROL pins
- Output thermal shutdown protection for robust performance
- Soft switching algorithm to reduce audible switching noise and EMI
- Hall chopper stabilization technique for precise signal response over operating range
- Antistall feature guarantees continuous rotation and prevents overheating
- Single-chip solution for high reliability
- Miniature MLP/DFN package with industry-leading 0.40 mm maximum overall thickness

Package:

6-contact MLP/DFN
1.5 mm × 2 mm
0.40 mm maximum overall height
(EW package)



Approximate size

Description

The A1448 is a full-bridge motor driver designed to drive low-voltage, brushless DC motors. The device is designed to allow the user to control several functions with a single input control pin. The pin allows for direct input PWM for speed control, is used to initiate the active braking function to reduce motor stop time, and acts as an enable pin to engage micro-power sleep mode to reduce average power consumption when not in use. The A1448 is designed for use in vibration motor applications in portable devices that require fast stop-start cycles, such as haptic applications and vibration ring tones.

Commutation of the motor is achieved by use of a single Hall element to detect the rotational position of an alternating-pole ring magnet. A high density CMOS semiconductor process allows the integration of all the necessary electronics. This includes the Hall element, the motor control circuitry, and the output full bridge. Low-voltage design techniques have been employed to achieve full device functionality down to 1.8 V V_{DD}. This fully integrated single chip solution provides enhanced reliability (including reverse battery protection and output short circuit protection) and eliminates the need for any external support components.

The A1448 employs a soft-switching algorithm to reduce audible switching noise and EMI interference. The micropower sleep mode can be initiated on the CONTROL pin, and reduces current consumption for battery management in

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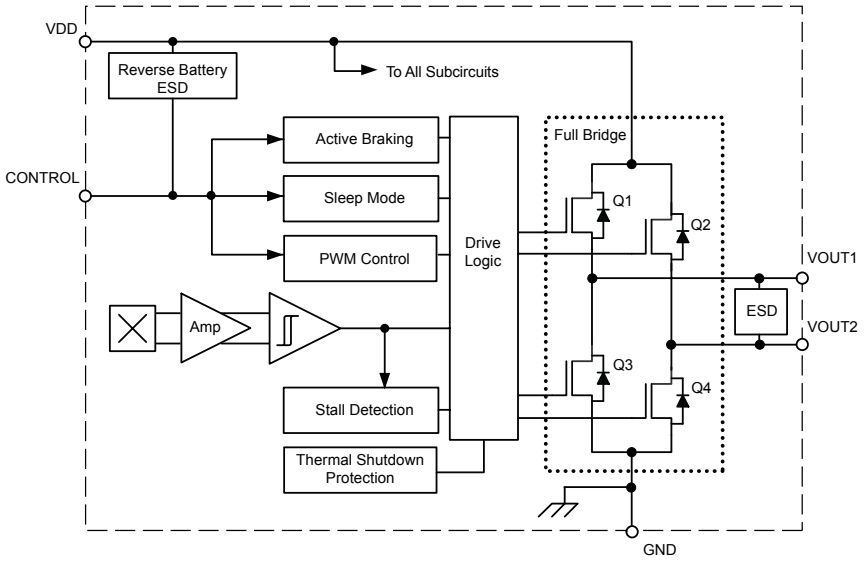
Functional Block Diagram



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Description (continued)

portable electronic devices. This feature allows the removal of a FET transistor for switching the device on and off.

The A1448 is optimized for vibration motor applications in cellular phones, pagers, electronic toothbrushes, hand-held video game controllers, and can also be used as a micro-fan driver for fans motors up to 1 W.

The Allegro DFN (EW) package is the thinnest DFN in the industry with a 0.40 mm maximum thickness that allows for very thin BLDC coin motor designs. The small package outline and low profile make this device ideally suited for use in applications where printed circuit board area and component headroom are at a premium. It is available in a lead (Pb) free, 6-contact MLP/DFN micro-leadframe package, with an exposed pad for enhanced thermal dissipation. Leadframe is 100% matte tin plated.

Selection Guide

Part Number	Packing*	Package
A1448EEWLT-P	3000 pieces per 7-in. reel	1.5 mm × 2 mm , 0.40 mm maximum overall package height, 6-contact MLP/DFN with exposed thermal pad

*Contact Allegro for additional packing options

Absolute Maximum Ratings

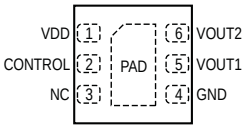
Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{DD}		5.5	V
Reverse Supply Voltage	V_{RDD}		–5.0	V
Forward Output Voltage	V_{OUT}	V_{DD} > 0 V	0 to V_{DD} + 0.3	V
Reverse Output Voltage	V_{ROUT}	V_{DD} > 0 V	–0.3	V
Forward CONTROL Pin Input Voltage	V_{IN}		0 to V_{DD} + 0.3	V
Reverse CONTROL Pin Input Voltage	V_{RIN}		V_{DD} – 6.0 V	V
Continuous Output Current	I_{OUT}	Positive I_{LOAD} flow is from VOUT1 to VOUT2, $T_J < T_J(max)$	±200	mA
Peak Output Current	$I_{OUT(pk)}$	<1 ms	±400	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	$T_J(max)$		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer PCB, with 0.23 in.^{2} copper area each side	125	ºC/W
		On 4-layer PCB based on JEDEC standard	64	ºC/W

*Additional thermal information available on the Allegro website

Pin-out Diagram



Terminal List

Number	Name	Function
1	VDD	Supply voltage
2	CONTROL	Input for PWM, braking, and sleep mode
3	NC	No connection
4	GND	Ground
5	VOUT1	First output
6	VOUT2	Second output

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OPERATING CHARACTERISTICS Valid over supply voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Electrical Characteristics						
Supply Voltage	V_{DD}	$T_J < T_J(max)$	2.0	–	4.2	V
Extended Range of Supply Voltage[1]	V_{DDE}	$T_J < T_J(max)$	1.8	–	4.2	V
Supply Current	I_{DD}	$V_{IN} > V_{INHI}$, T_A = 25°C, no load	–	4	6	mA
		$V_{IN} < V_{INLO}$, T_A = 25°C	–	–	10	µA
Total Output On-Resistance[2]	$R_{DS(on)}$	I_{OUT} = 70 mA, V_{DD} = 2 V, T_A = 25°C	–	3.9	–	Ω
		I_{OUT} = 70 mA, V_{DD} = 3 V, T_A = 25°C	–	2.6	–	Ω
		I_{OUT} = 70 mA, V_{DD} = 4 V, T_A = 25°C	–	2.2	–	Ω
Reverse Battery Current	I_{RDD}	V_{RDD} = –4.2 V	–	–	–10	mA
CONTROL Pin Input Threshold	V_{INHI}		0.7 × V_{DD}	–	–	V
	V_{INLO}		–	–	0.2 × V_{DD}	V
CONTROL Pin Input Current	I_{IN}	V_{IN} = 3.0 V	–	1.0	5	µA
CONTROL Pin Input Frequency	f_{PWM}		100	384	800	kHz
CONTROL Prebraking Time[3]	t_{PB}		–	–	2.5	ms
Thermal Shutdown Limit	T_{JTSD}	Device is active	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(HYS)}$	Device is active	–	20	–	°C
Magnetic Characteristics[4]						
Magnetic Switchpoints	B_{OP}		–	35	75	G
	B_{RP}		–75	–35	–	G
	B_{HYS}		–	70	–	G
Output Polarity	VOUT1	$B < B_{RP}$	–	LOW	–	V
		$B > B_{OP}$	–	HIGH	–	V
	VOUT2	$B < B_{RP}$	–	HIGH	–	V
		$B > B_{OP}$	–	LOW	–	V

[1]Extended V_{DD} range affects $R_{DS(on)}$ and B_x.
[2]Total Output On-Resistance = $R_{DS(on)Q1} + R_{DS(on)Q4}$, or $R_{DS(on)Q2} + R_{DS(on)Q3}$, where Qx refers to the internal full-bridge transistors.
[3]Device initiates braking algorithm if the CONTROL pin is pulled to GND for longer than the maximum specified CONTROL Prebraking Time.
[4]1 G (gauss) = 0.1 mT (millitesla).

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Functional Description

Soft Switching

The A1448 device includes a soft-switching algorithm that controls the output switching slew rate for both output pins. As a result, the A1448 device is ideal for use in applications requiring low audible switching noise and low EMI. The resistance of the output transistors is controlled to ensure the smooth switching of the outputs, as illustrated in figure 1.

CONTROL Pin Functionality: PWM, Braking, and Sleep Mode Input

The CONTROL input pin accepts an external signal that can control the speed of the output bridge, initiate active braking, and put the device into sleep mode. Signals higher than the V_{INHI} threshold will turn on the output bridge according to the applied magnetic field. Applying a PWM signal to the CONTROL pin will turn the bridge on and off according to the PWM duty cycle. When the CONTROL pin is pulled to GND, the device initiates its internal active braking algorithm to stop the motor. After braking, the device enters micro-power sleep mode. The device becomes active again when the CONTROL pin is pulled higher than V_{INHI}.

Antistall Algorithm

If a stall condition occurs, the device will execute an antistall algorithm to re-start the motor.

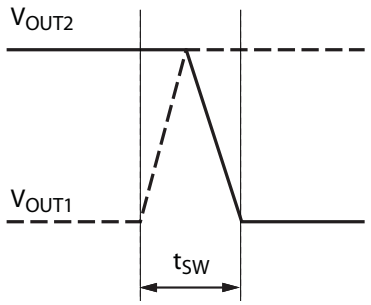

Figure 1. A1448 output soft switching with a 30 Ω resistive load

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Application Information

Figure 2 shows a typical vibration motor application in which speed control, active braking, and sleep mode are required on the CONTROL pin.

Figure 3 shows an application circuit in which 100% duty cycle is required. Tying the CONTROL pin to V_{DD} disables the braking function and the sleep mode. The user must control supply in order to control the speed of the motor. This represents a 2-wire motor design.

Note that:

- No external diode is required for reverse battery protection because the protection is fully integrated into the IC.
- Thermal shutdown also is integrated, to protect the device against inadvertent output shorts during manufacturing or testing.
- A bypass capacitor of 0.1 µF is required. This capacitor is usually included on the end user PCB and therefore not necessary on the motor PCB.

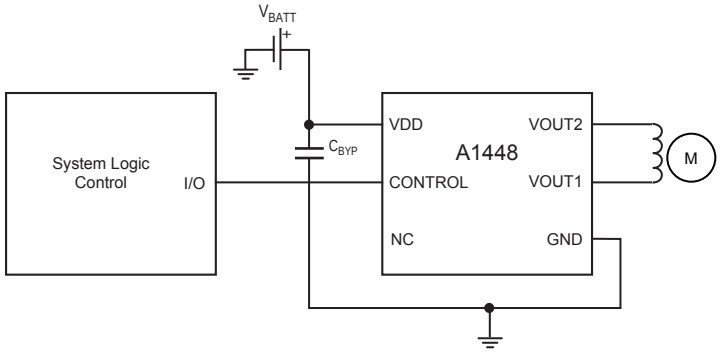

Figure 2. Three-wire vibration motor application circuit

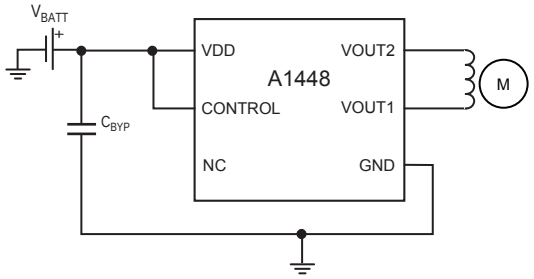

Figure 3. Two-wire vibration motor application circuit

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Power Derating

The device must be operated below the maximum junction temperature of the device, T_J (max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at various P_D levels.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For a load of 30 Ω, and given common conditions such as: T_A= 25°C, V_{DD} = 3 V, I_{DD} = 83 mA, V_{LOAD} = 2.43 V, I_{LOAD} = 81 mA, and $R_{\theta JA}$ = 125 °C/W, (see figure 5)

then:

$$P_D = V_{DD} \times I_{DD} - V_{LOAD} \times I_{LOAD}$$

$$= 3\ V \times 83\ mA - 2.43\ V \times 81\ mA$$

$$= 52.17\ mW$$

$$\Delta T = P_D \times R_{\theta JA}$$

$$= 52.17\ mW \times 125\ °C/W$$

$$= 7°C$$

$$T_J = T_A + \Delta T$$

$$= 25°C + 7°C$$

$$= 32°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level, without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

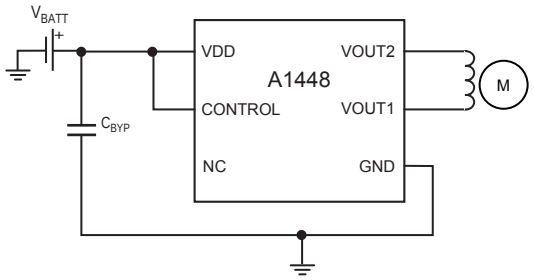

Figure 5. A1448 typical application

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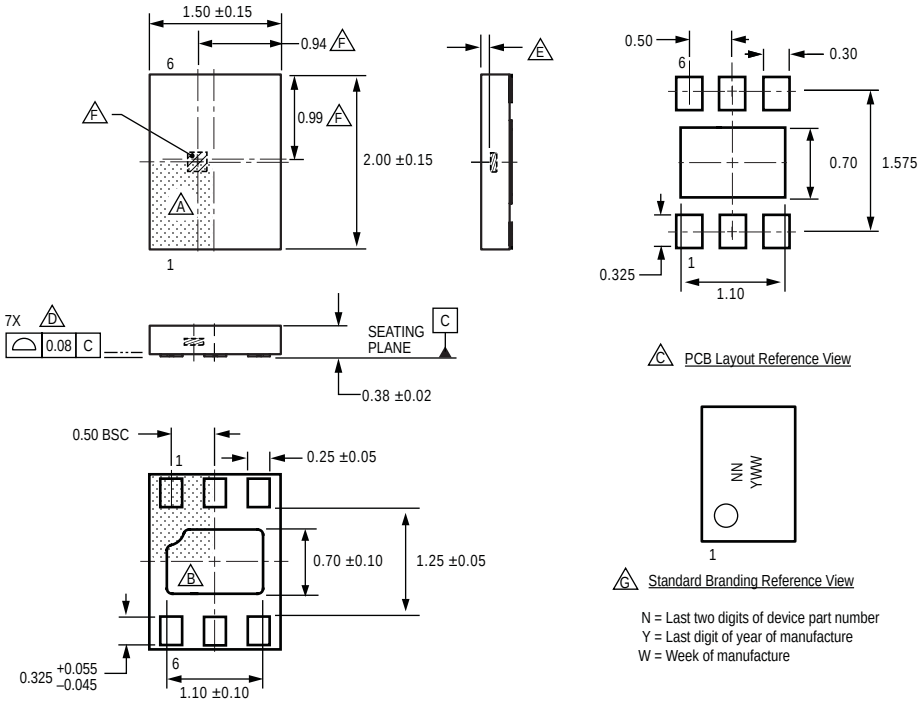
Package EW, 6-Pin MLP/DFN



C PCB Layout Reference View

G Standard Branding Reference View

N = Last two digits of device part number
Y = Last digit of year of manufacture
W = Week of manufacture

For Reference Only, not for tooling use (refernce DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Active Area Depth 0.15 mm REF

F Hall Element (not to scale)

G Branding scale and appearance at supplier discretion

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