# VN770P

## QUAD SMART POWER SOLID STATE RELAY FOR COMPLETE H BRIDGE CONFIGURATIONS

| TYPE | $R_{DS(on)}$ * | $I_{OUT}$ | $V_{CC}$ |
|------|------------|------|------|
| VN770P | 0.270 Ω | 9 A | 26 V |

* Total resistance of one side in bridge configuration

- IDEAL AS A  LOW VOLTAGE BRIDGE
- LINEAR CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- SHORT CIRCUIT PROTECTED
- STATUS FLAG DIAGNOSTICS
- OPEN DRAIN DIAGNOSTICS OUTPUT
- INTEGRATED CLAMPING CIRCUITS
- UNDER-VOLTAGE PROTECTION
- ESD PROTECTION



SO-28

## DESCRIPTION

The VN770P is a device formed by three monolithic chips housed in a standard SO28 package: a double high side and two low side switches. Both the double high side and low side switches are made using STMicroelectronics VIPower technology. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application. The dual high side switches have built-in thermal shut-down to protect the chip from over temperature and short circuit, status output to provide indication for open load in off and on state, overtemperature conditions and stuck-on to $V_{CC}$. The low side switches are two OMNIFET types (fully autoprotected Power MOSFET in VIPower™ technology). They have built-in thermal shut-down, linear current limitation and overvoltage clamping. Fault feedback for thermal intervention can be detected by monitoring the voltage at the input pin.

DUAL HIGH-SIDE SWITCH

From the falling edge of the input signal, the status output, initially low  to signal a fault condition (overtemperature or open load on-state), will go back to a high state with a different delay in case of overtemperature (tpovl) and in case of open open load ($_{tpol}$) respectively. This feature allows to discriminate the nature of the detected fault. To protect the device against
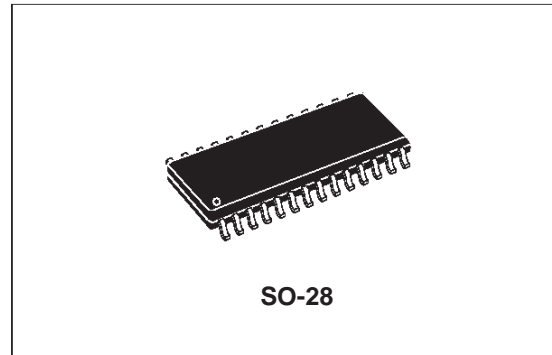
short circuit and over current condition, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When this temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor (one for each channel) being located inside each of the two Power MOS areas. This positioning allows the device to operate with one channel in automatic thermal cycling and the other one on a normal load. An internal function of the devices ensures the fast demagnetization of inductive loads with a typical voltage  ($V_{demag}$) of -18V. This function allows to greatly reduces the power dissipation according to the formula:

$$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$$
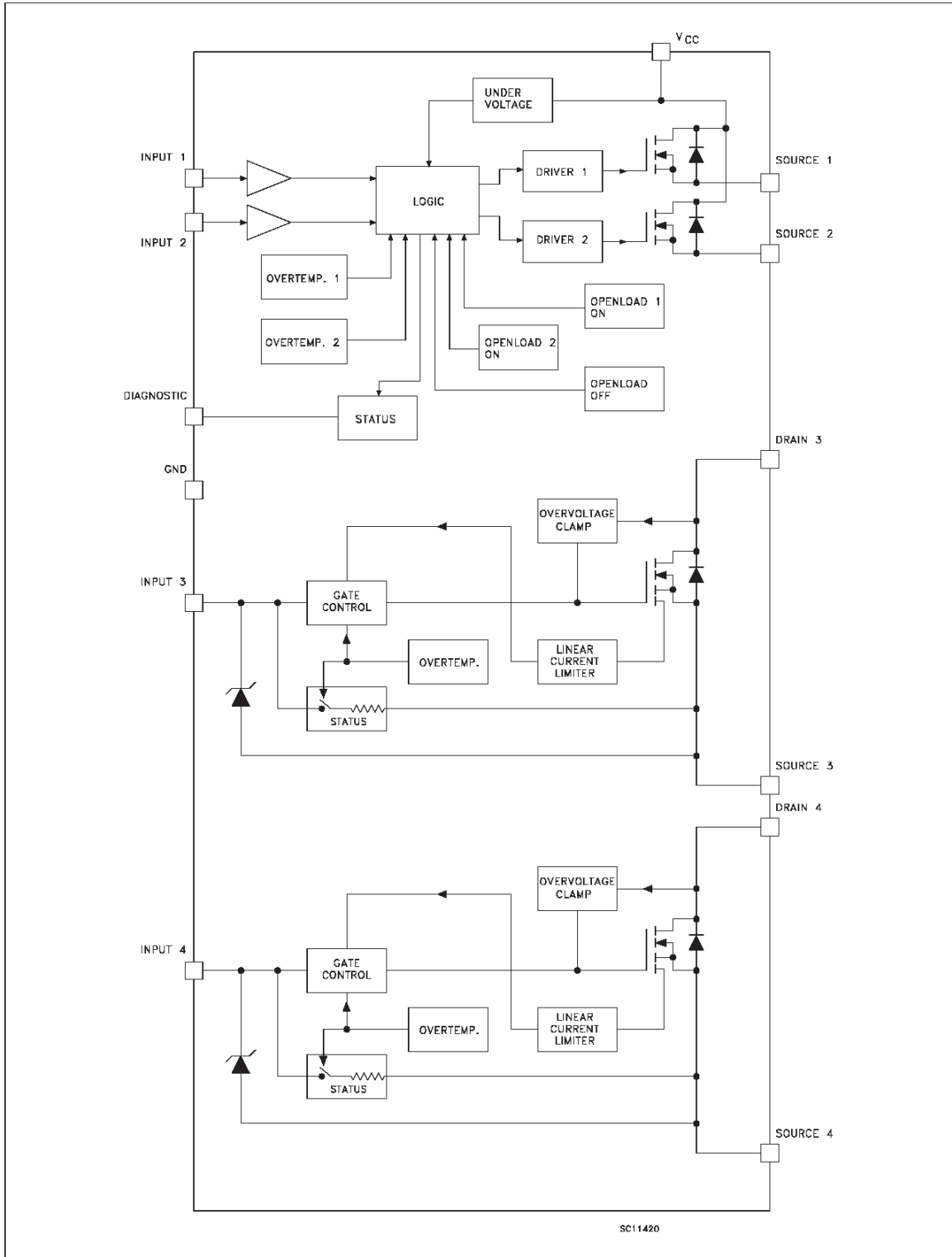
where f = switching frequency and
$V_{demag}$ = demagnetization voltage.

In this device if the GND pin is disconnected, with $V_{CC}$ not exceeding 16V, both channel will switch off.
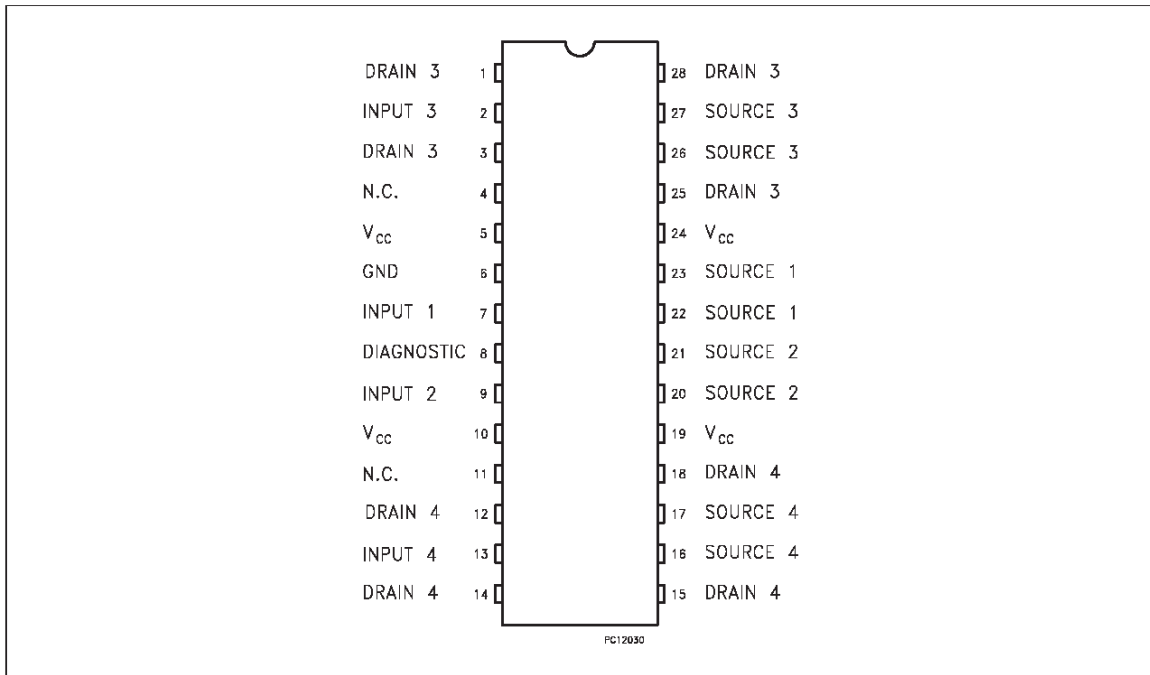
LOW-SIDE SWITCHES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current ($I_{iss}$) flows into the Input pin in order to supply the internal circuitry.

## BLOCK DIAGRAM



SC11420

## CONNECTION DIAGRAM

```
              DRAIN  3    1 ▯        ▯ 28  DRAIN  3
              INPUT  3    2 ▯        ▯ 27  SOURCE  3
              DRAIN  3    3 ▯        ▯ 26  SOURCE  3
              N.C.        4 ▯        ▯ 25  DRAIN  3
              V_CC        5 ▯        ▯ 24  V_CC
              GND         6 ▯        ▯ 23  SOURCE  1
              INPUT  1    7 ▯        ▯ 22  SOURCE  1
              DIAGNOSTIC  8 ▯        ▯ 21  SOURCE  2
              INPUT  2    9 ▯        ▯ 20  SOURCE  2
              V_CC       10 ▯        ▯ 19  V_CC
              N.C.       11 ▯        ▯ 18  DRAIN  4
              DRAIN  4   12 ▯        ▯ 17  SOURCE  4
              INPUT  4   13 ▯        ▯ 16  SOURCE  4
              DRAIN  4   14 ▯        ▯ 15  DRAIN  4
                            PC12030
```

## PIN FUNCTION

| No | NAME | FUNCTION |
|---|---|---|
| 1, 3, 25, 28 | DRAIN 3 | Drain of Switch 3 (low-side switch) |
| 2 | INPUT 3 | Input of Switch 3 (low-side switch) |
| 4, 11 | N.C. | Not Connected |
| 5, 10, 19, 24 | $V_{CC}$ | Drain of Switches 1and 2 (high-side switches) and Power Supply Voltage |
| 6 | GND | Ground of Switches 1 and 2 (high-side switches) |
| 7 | INPUT 1 | Input of Switch 1 (high-side switch) |
| 8 | DIAGNOSTIC | Diagnostic of Switches 1 and 2 (high-side switches) |
| 9 | INPUT 2 | Input of Switch 2 (high-side switch) |
| 12, 14, 15, 18 | DRAIN 4 | Drain of Switch 4 (low-side switch) |
| 13 | INPUT 4 | Input of Switch 4 (low-side switch) |
| 16, 17 | SOURCE 4 | Source of Switch 4 (low-side switch) |
| 20, 21 | SOURCE 2 | Source of Switch 2 (high-side switch) |
| 22, 23 | SOURCE 1 | Source of Switch 1 (high-side switch) |
| 26, 27 | SOURCE 3 | Source of Switch 3 (low-side switch) |

## PROTECTION CIRCUITS

DUAL HIGH SIDE SWITCH

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a a small resistor between pin 2 (GND) and ground. The suggested resistance value is about 150Ω. In any case the maximum voltage drop on this resistor should not overcome 0.5V.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to the device ground (see application circuit in fig. 3), which becomes the common signal GND for the whole control board avoiding shift of $V_{ih}$, $V_{il}$ and $V_{stat}$.

LOW SIDE SWITCHES

The devices integrate:

- OVERVOLTAGE CLAMP PROTECTION: internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.

- STATUS FEEDBACK: In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of these devices are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

**TRUTH TABLE** (for Dual high-side switch only)

| | | INPUT 1 | INPUT 2 | SOURCE 1 | SOURCE 2 | DIAGNOSTIC |
|---|---|---|---|---|---|---|
| Normal Operation | | L | L | L | L | H |
| | | H | H | H | H | H |
| | | L | H | L | H | H |
| | | H | L | H | L | H |
| Under-voltage | | X | X | L | L | H |
| Thermal Shutdown | Channel 1 | H | X | L | X | L |
| | Channel 2 | X | H | X | L | L |
| Open Load | Channel 1 | H | X | H | X | L |
| | | L | L | L | L | L |
| | Channel 2 | X | H | X | H | L |
| | | L | L | L | L | L |
| Output Shorted to $V_{CC}$ | Channel 1 | H | X | H | X | L |
| | | L | L | H | L | L |
| | Channel 2 | X | H | X | H | L |
| | | L | L | L | H | L |

NOTE: The low-side switches have the fault feedback which can be detected by monitoring the voltage at the input pins.

L = Logic LOW, H = Logic HIGH, X = Don't care

### ABSOLUTE MAXIMUM RATING  (-40 $^{o}$C < T$_j$ < 150 $^{o}$C)

HIGH SIDE SWITCH

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| V$_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 40 | V |
| I$_{OUT}$ | Output Current (cont.) | 9 | A |
| I$_R$ | Reverse Output Current | -9 | A |
| I$_{IN}$ | Input Current | ±10 | mA |
| -V$_{CC}$ | Reverse Supply Voltage | -4 | V |
| I$_{STAT}$ | Status Current | ±10 | mA |
| V$_{ESD}$ | Electrostatic Discharge (C = 100 pF, R =1.5 KΩ) | 2000 | V |
| P$_{tot}$ | Power Dissipation at T$_c$ = 25 $^{o}$C | Internally Limited | W |
| T$_j$ | Junction Operating Temperature | -40 to 150 | $^{o}$C |
| T$_{stg}$ | Storage Temperature | -55 to 150 | $^{o}$C |

LOW SIDE SWITCH

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| V$_{(BR)DSS}$ | Drain-Source Breakdown Voltage | Internally Clamped | V |
| V$_{IN}$ | Input Voltage | 18 | V |
| I$_D$ | Drain Current | Internally Limited | A |
| I$_R$ | Reverse DC Output Current | -14 | A |
| V$_{ESD}$ | Electrostatic Discharge (C = 100 pF, R =1.5 KΩ) | 2000 | V |
| P$_{tot}$ | Total Dissipation at T$_c$ = 25 $^{o}$C | Internally Limited | W |
| T$_j$ | Operating Junction Temperature | Internally Limited | $^{o}$C |
| T$_{stg}$ | Storage Temperature | -55 to 150 | $^{o}$C |

### THERMAL DATA

| | | | | |
|---|---|---|---|---|
| R$_{thj-case}$ | Thermal  Resistance  Junction-case (High-side switch) | Max | 20 | $^{o}$C/W |
| R$_{thj-case}$ | Thermal  Resistance  Junction-case (Low-side switch) | Max | 20 | $^{o}$C/W |
| R$_{thj-amb}$ | Thermal  Resistance  Junction-ambient | Max | 60 | $^{o}$C/W |

### ELECTRICAL  CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH
(8 < V$_{CC}$ < 16 V; -40 ≤ T$_j$ ≤ 125 $^{o}$C unless otherwise specified)
POWER

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| V$_{CC}$ | Supply Voltage | | 6 | 13 | 26 | V |
| In(*) | Nominal Current | T$_c$ = 85 $^{o}$C  V$_{DS(on)}$ ≤ 0.5  V$_{CC}$ = 13 V | 1.6 | | 2.6 | A |
| R$_{on}$ | On State Resistance | I$_{OUT}$ = I$_n$  V$_{CC}$ = 13 V  T$_j$ = 25 $^{o}$C | 0.13 | | 0.2 | Ω |
| I$_S$ | Supply Current | Off State    T$_j$ = 25 $^{o}$C   V$_{CC}$ = 13 V | | 35 | 100 | μA |
| V$_{DS(MAX)}$ | Maximum Voltage Drop | I$_{OUT}$ = 7.5 A   T$_j$ = 85 $^{o}$C   V$_{CC}$ = 13 V | 1.44 | | 2.3 | V |

## ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH (continued)

| | | | | | | |
|---|---|---|---|---|---|---|
| $R_i$ | Output to GND internal Impedance | $T_j$ = 25 $^o$C | 5 | 10 | 20 | K$\Omega$ |

SWITCHING

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$(^) | Turn-on Delay Time Of Output Current | $R_{out}$ = 5.4 $\Omega$ | 5 | 25 | 200 | µs |
| $t_r$(^) | Rise Time Of Output Current | $R_{out}$ = 5.4 $\Omega$ | 10 | 50 | 180 | µs |
| $t_{d(off)}$(^) | Turn-off Delay Time Of Output Current | $R_{out}$ = 5.4 $\Omega$ | 10 | 75 | 250 | µs |
| $t_f$(^) | Fall Time Of Output Current | $R_{out}$ = 5.4 $\Omega$ | 10 | 35 | 180 | µs |
| $(di/dt)_{on}$ | Turn-on Current Slope | $R_{out}$ = 5.4 $\Omega$ | 0.003 | | 0.1 | A/µs |
| $(di/dt)_{off}$ | Turn-off Current Slope | $R_{out}$ = 5.4 $\Omega$ | 0.005 | | 0.1 | A/µs |

LOGIC INPUT

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Level Voltage | | | | 1.5 | V |
| $V_{IH}$ | Input High Level Voltage | | 3.5 | | (•) | V |
| $V_{I(hyst.)}$ | Input Hysteresis Voltage | | 0.2 | 0.9 | 1.5 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = 5 V    $T_j$ = 25 $^o$C | | 30 | 100 | µA |
| $V_{ICL}$ | Input Clamp Voltage | $I_{IN}$ = 10 mA<br>$I_{IN}$ = -10 mA | 5 | 6<br>-0.7 | 7 | V<br>V |

PROTECTION AND DIAGNOSTICS

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{STAT}$ | Status Voltage Output Low | $I_{STAT}$ = 1.6 mA | | | 0.4 | V |
| $V_{USD}$ | Under Voltage Shut Down | | 3.5 | 4.5 | 6 | V |
| $V_{SCL}$ | Status Clamp Voltage | $I_{STAT}$ = 10 mA<br>$I_{STAT}$ = -10 mA | 5 | 6<br>-0.7 | 7 | V<br>V |
| $T_{TSD}$ | Thermal Shut-down Temperature | | 140 | 160 | 180 | $^o$C |
| $T_{SD(hyst.)}$ | Thermal Shut-down Hysteresis | | | | 50 | $^o$C |
| $T_R$ | Reset Temperature | | 125 | | | $^o$C |
| $V_{OL}$ | Open Voltage Level | Off-State  (note 2) | 2.5 | 4 | 5 | V |

### ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH (continued)

PROTECTION AND DIAGNOSTICS

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OL}$ | Open Load Current Level | On-State | 5 | | 180 | mA |
| $t_{povl}$ | Status Delay | (note 3) | | 5 | 10 | µs |
| $t_{pol}$ | Status Delay | (note 3) | 50 | 500 | 2500 | µs |

(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(^) See switching time waveform
() The $V_{IH}$ is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at $T_c = 85\ ^oC$ for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$
note 3: $t_{povl}\ t_{pol}$: ISO definition

### ELECTRICAL CHARACTERISTICS FOR LOW SIDE SWITCHES

($T_{case} = 25\ ^oC$ unless otherwise specified)
OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CLAMP}$ | Drain-source Clamp Voltage | $I_D = 7\ A \quad V_{in} = 0$ | 36 | 42 | 48 | V |
| $V_{CLTH}$ | Drain-source Clamp Threshold Voltage | $I_D = 2\ mA \quad V_{in} = 0$ | 35 | | | V |
| $V_{INCL}$ | Input-Source Reverse Clamp Voltage | $I_{in} = -1\ mA$ | -1 | | -0.3 | V |
| $I_{DSS}$ | Zero Input Voltage Drain Current ($V_{in} = 0$) | $V_{DS} = 13\ V \quad V_{in} = 0$<br>$V_{DS} = 25\ V \quad V_{in} = 0$ | | | 50<br>200 | µA<br>µA |
| $I_{ISS}$ | Supply Current from Input Pin | $V_{DS} = 0\ V \quad V_{in} = 10\ V$ | | 250 | 500 | µA |

ON (∗)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN(th)}$ | Input Threshold Voltage | $V_{DS} = V_{in} \quad I_D + I_{in} = 1\ mA$ | 0.8 | | 3 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{in} = 10\ V \quad I_D = 7\ A$<br>$V_{in} = 5\ V \quad I_D = 7\ A$ | | | 0.07<br>0.1 | Ω<br>Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

### ELECTRICAL  CHARACTERISTICS FOR LOW SIDE SWITCHES (continued)

| $g_{fs}$ (∗) | Forward Transconductance | $V_{DS}$ = 13 V    $I_D$ = 7 A | 8 | 10 | | S |
|---|---|---|---|---|---|---|
| $C_{oss}$ | Output Capacitance | $V_{DS}$ = 13 V    f = 1 MHz    $V_{in}$ = 0 | | 400 | 500 | pF |

SWITCHING (∗∗)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 15 V        $I_d$ = 7A<br>$V_{gen}$ = 10 V    $R_{gen}$ = 10 Ω<br>(see figure 3) | | 60<br>160<br>250<br>100 | 120<br>300<br>400<br>200 | ns<br>ns<br>ns<br>ns |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 15 V        $I_d$ = 7 A<br>$V_{gen}$ = 10 V    $R_{gen}$ = 1000 Ω<br>(see figure 3) | | 300<br>1.5<br>5.5<br>1.8 | 500<br>2.2<br>7.5<br>2.5 | ns<br>μs<br>μs<br>μs |
| $(di/dt)_{on}$ | Turn-on Current Slope | $V_{DD}$ = 15 V        $I_D$ = 7A<br>$V_{in}$ = 10 V        $R_{gen}$ = 10 Ω | | 120 | | A/μs |
| $Q_i$ | Total Input Charge | $V_{DD}$ = 12 V    $I_D$ = 7 A    $V_{in}$ = 10 V | | 30 | | nC |

### SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (∗) | Forward On Voltage | $I_{SD}$ = 10 A    $V_{in}$ = 0 | | | 1.6 | V |
| $t_{rr}$ (∗∗) | Reverse Recovery Time | $I_{SD}$ = 7 A      di/dt = 100 A/μs<br>$V_{DD}$ = 30 V    $T_j$ = 25 °C<br>(see test circuit, figure 5) | | 110 | | ns |
| $Q_{rr}$ (∗∗) | Reverse Recovery Charge | | | 0.34 | | μC |
| $I_{RRM}$ (∗∗) | Reverse Recovery Current | | | 6.1 | | A |

### PROTECTION

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{jsh}$ (∗∗) | Overtemperature Shutdown | | 150 | | | °C |
| $T_{jrs}$ (∗∗) | Overtemperature Reset | | 135 | | | °C |
| $I_{gf}$ (∗∗) | Fault Sink Current | $V_{in}$ = 10 V    $V_{DS}$ = 13 V<br>$V_{in}$ = 5 V      $V_{DS}$ = 13 V | | 50<br>20 | | mA<br>mA |
| $I_{lim}$ | Drain Current Limit | $V_{in}$ = 10 V    $V_{DS}$ = 13 V<br>$V_{in}$ = 5 V      $V_{DS}$ = 13 V | 10<br>10 | 14<br>14 | 20<br>20 | A<br>A |
| $t_{dlim}$ (∗∗) | Step Response Current Limit | $V_{in}$ = 10 V<br>$V_{in}$ = 5 V | | 30<br>80 | 60<br>150 | μs<br>μs |

## TYPICAL APPLICATION DIAGRAM
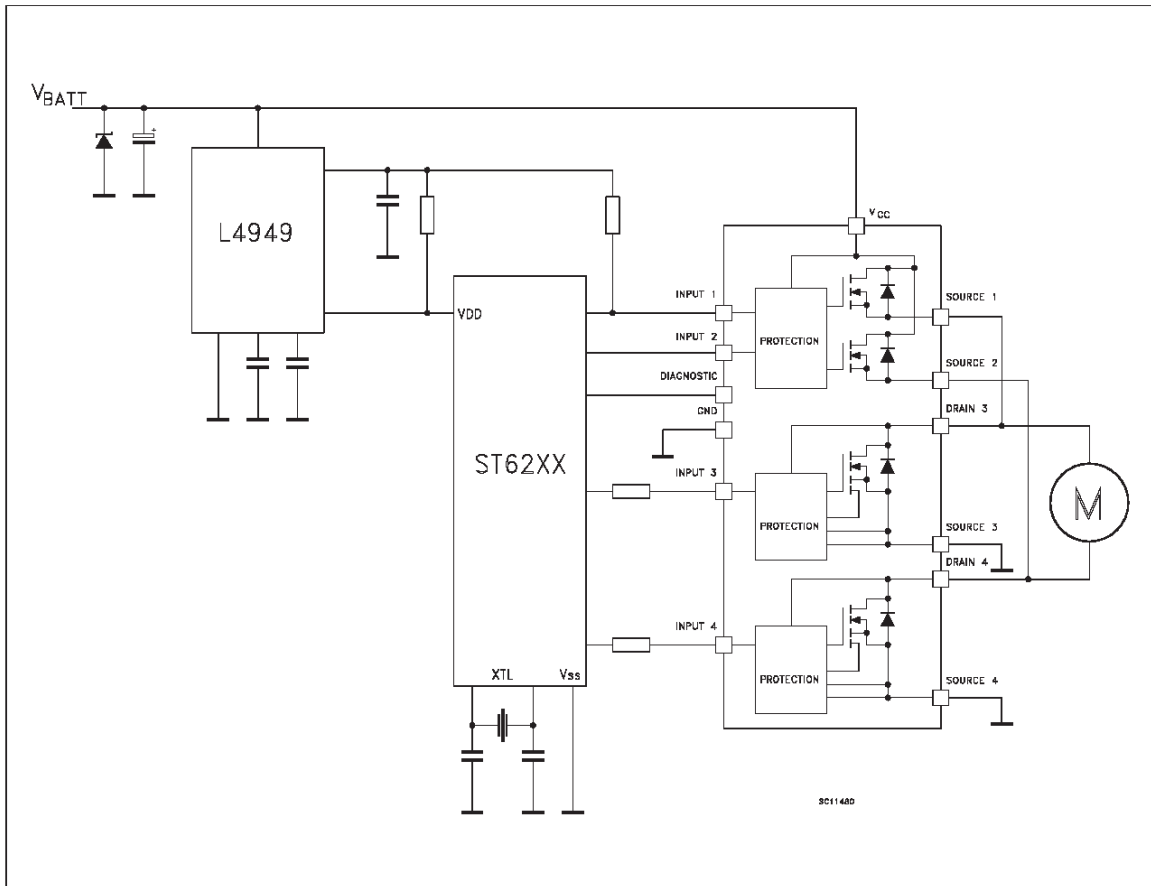
## SO-28 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-----|------|------|------|------|------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.10 | | 0.30 | 0.004 | | 0.012 |
| b | 0.35 | | 0.49 | 0.013 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.50 | | | 0.020 | |
| c1 | 45 (typ.) | | | | | |
| D | 17.7 | | 18.1 | 0.697 | | 0.713 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 16.51 | | | 0.650 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.299 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| S | 8 (max.) | | | | | |



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