



# VND5050AJ-E VND5050AK-E

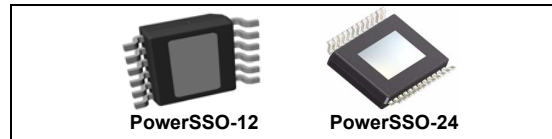
## Double channel high side driver with analog current sense for automotive applications

### Features

|                                   |            |                          |
|-----------------------------------|------------|--------------------------|
| Max transient supply voltage      | $V_{CC}$   | 41 V                     |
| Operating voltage range           | $V_{CC}$   | 4.5 to 36 V              |
| Max on-state resistance (per ch.) | $R_{ON}$   | 50 m $\Omega$            |
| Current limitation (typ)          | $I_{LIMH}$ | 18 A                     |
| Off-state supply current          | $I_S$      | 2 $\mu$ A <sup>(1)</sup> |

1. Typical value with all loads connected

- Main
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/ec european directive
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Current sense disable
  - Thermal shutdown indication
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Thermal shutdown
  - Reverse battery protection (see [Application schematic on page 21](#))
  - Electrostatic discharge protection



### Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

### Description

The VND5050AJ-E, VND5050AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open. When CS\_DIS is driven high, the current sense pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

**Table 1. Device summary**

| Package     | Order codes |               |
|-------------|-------------|---------------|
|             | Tube        | Tape and reel |
| PowerSSO-12 | VND5050AJ-E | VND5050AJTR-E |
| PowerSSO-24 | VND5050AK-E | VND5050AKTR-E |

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# 1 Block diagram and pin description

Figure 1. Block diagram

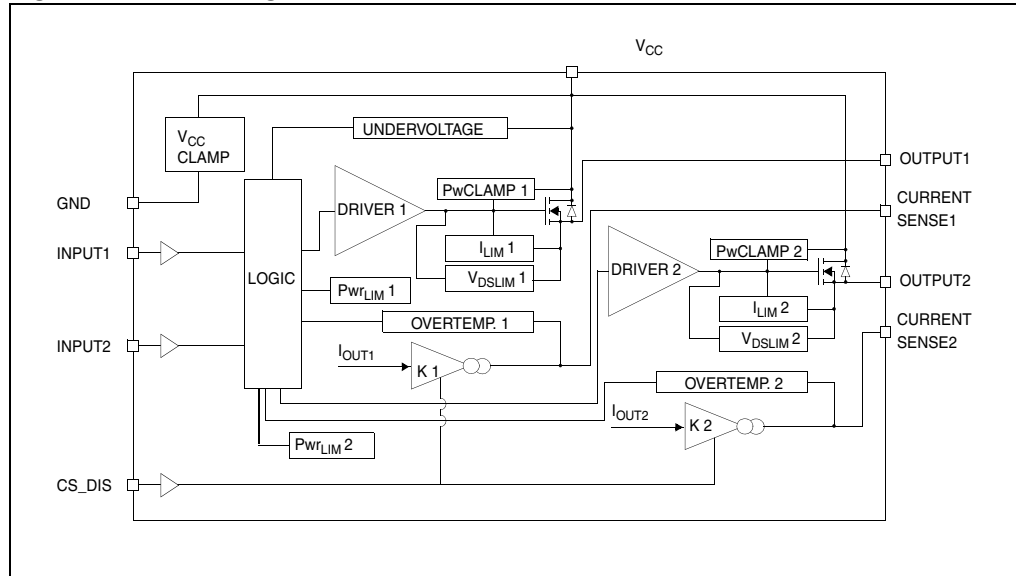


Table 2. Pin function

| Name                         | Function   |
|------------------------------|--|
| $V_{CC}$                     | Battery connection.  |
| OUTPUT <sub>1,2</sub>        | Power output.  |
| GND                          | Ground connection. Must be reverse battery protected by an external diode/resistor network.  |
| INPUT <sub>1,2</sub>         | Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state. |
| CURRENT SENSE <sub>1,2</sub> | Analog current sense pin, delivers a current proportional to the load current                |
| CS_DIS                       | Active high CMOS compatible pin, to disable the current sense pin.                           |

Figure 2. Configuration diagram (top view)

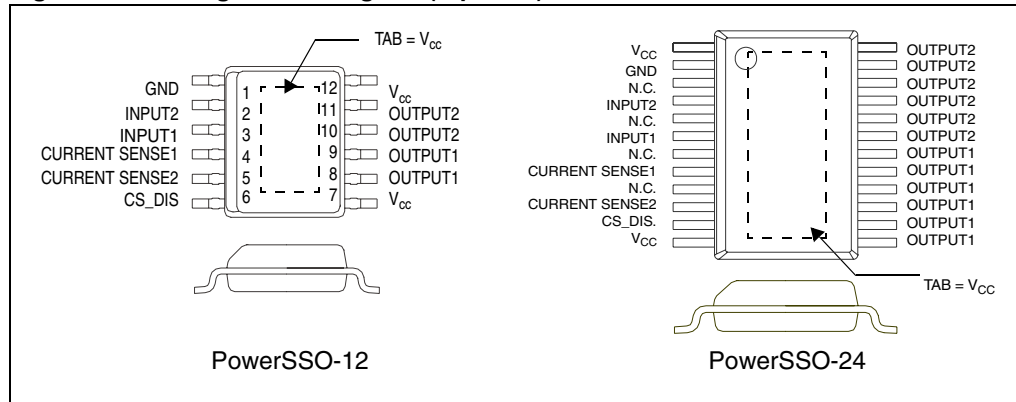


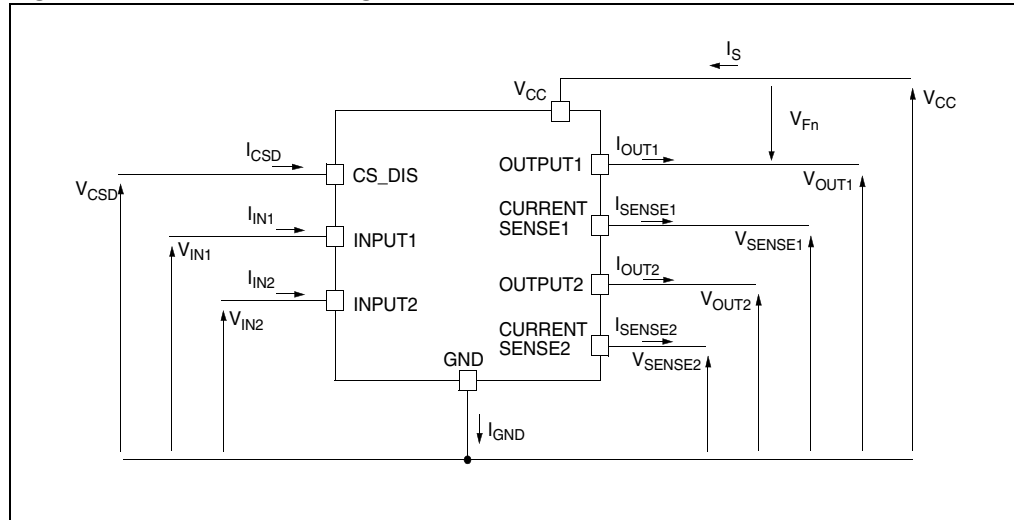
Table 3. Suggested connections for unused and not connected pins

| Connection/pin | Current sense         | N.C. | Output              | Input                  | CS_DIS                 |
|----------------|-----------------------|------|---------------------|------------------------|------------------------|
| Floating       | N.R. <sup>(1)</sup>   | X    | X                   | X                      | X                      |
| To ground      | Through 1 KΩ resistor | X    | N.R. <sup>(1)</sup> | Through 10 KΩ resistor | Through 10 KΩ resistor |

1. Not recommended.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

| Symbol        | Parameter   | Value                    | Unit   |
|---------------|---|--------------------------|--------|
| $V_{CC}$      | DC supply voltage   | 41                       | V      |
| $-V_{CC}$     | Reverse DC supply voltage   | 0.3                      | V      |
| $-I_{GND}$    | DC reverse ground pin current   | 200                      | mA     |
| $I_{OUT}$     | DC output current   | Internally limited       | A      |
| $-I_{OUT}$    | Reverse DC output current   | 12                       | A      |
| $I_{IN}$      | DC input current  | -1 to 10                 | mA     |
| $I_{CSD}$     | DC current sense disable input current  | -1 to 10                 | mA     |
| $-I_{CSENSE}$ | DC reverse CS pin current   | 200                      | mA     |
| $V_{CSENSE}$  | Current sense maximum voltage   | $V_{CC}-41$<br>$+V_{CC}$ | V<br>V |
| $E_{MAX}$     | Maximum switching energy<br>( $L = 3\text{mH}$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5\text{V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_{OUT} = I_{limL}(Typ.)$ ) | 104                      | mJ     |

**Table 4. Absolute maximum ratings (continued)**

| Symbol           | Parameter   | Value      | Unit |
|------------------|---|------------|------|
| V <sub>ESD</sub> | Electrostatic discharge (Human Body Model: R=1.5KΩ;<br>C=100pF) |            |      |
|                  | – Input   | 4000       | V    |
|                  | – Current sense   | 2000       | V    |
|                  | – CS_DIS  | 4000       | V    |
|                  | – Output  | 5000       | V    |
|                  | – V <sub>CC</sub>   | 5000       | V    |
| V <sub>ESD</sub> | Charge device model (CDM-AEC-Q100-011)                          | 750        | V    |
| T <sub>j</sub>   | Junction operating temperature                                  | -40 to 150 | °C   |
| T <sub>stg</sub> | Storage temperature   | -55 to 150 | °C   |

## 2.2 Thermal data

**Table 5. Thermal data**

| Symbol                | Parameter   | Value                         |                               | Unit |
|-----------------------|---|-------------------------------|-------------------------------|------|
|                       |   | PowerSSO-12                   | PowerSSO-24                   |      |
| R <sub>thj-case</sub> | Thermal resistance junction case (max)<br>(with one channel on) | 2.7                           | 2.7                           | °C/W |
| R <sub>thj-amb</sub>  | Thermal resistance junction ambient<br>(max)                    | See <a href="#">Figure 29</a> | See <a href="#">Figure 33</a> | °C/W |

## 2.3 Electrical characteristics

8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>j</sub> < 150 °C, unless otherwise specified.

**Table 6. Power section**

| Symbol               | Parameter                          | Test conditions  | Min. | Typ.                  | Max.                  | Unit           |
|----------------------|------------------------------------|--|------|-----------------------|-----------------------|----------------|
| V <sub>CC</sub>      | Operating supply voltage           |  | 4.5  | 13                    | 36                    | V              |
| V <sub>USD</sub>     | Undervoltage shutdown              |  |      | 3.5                   | 4.5                   | V              |
| V <sub>USDhyst</sub> | Undervoltage shutdown hysteresis   |  |      | 0.5                   |                       | V              |
| R <sub>ON</sub>      | On-state resistance <sup>(1)</sup> | I <sub>OUT</sub> = 2A; T <sub>j</sub> = 25°C<br>I <sub>OUT</sub> = 2A; T <sub>j</sub> = 150°C<br>I <sub>OUT</sub> = 2A; V <sub>CC</sub> = 5V; T <sub>j</sub> = 25°C  |      |                       | 50<br>100<br>65       | mΩ<br>mΩ<br>mΩ |
| V <sub>clamp</sub>   | Clamp voltage                      | I <sub>S</sub> = 20mA  | 41   | 46                    | 52                    | V              |
| I <sub>S</sub>       | Supply current                     | Off-state; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C;<br>V <sub>IN</sub> =V <sub>OUT</sub> =V <sub>SENSE</sub> =V <sub>CSD</sub> =0V<br>On-state; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V;<br>I <sub>OUT</sub> = 0A |      | 2 <sup>(2)</sup><br>3 | 5 <sup>(2)</sup><br>6 | μA<br>mA       |



**Table 6. Power section (continued)**

| Symbol       | Parameter                                      | Test conditions  | Min. | Typ. | Max. | Unit    |
|--------------|--|--|------|------|------|---------|
| $I_{L(off)}$ | Off-state output current <sup>(1)</sup>        | $V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ;<br>$T_j=25^{\circ}C$  | 0    | 0.01 | 3    | $\mu A$ |
|              |  | $V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ;<br>$T_j=125^{\circ}C$ | 0    |      | 5    |         |
| $V_F$        | Output - $V_{CC}$ diode voltage <sup>(1)</sup> | $-I_{OUT}=4A$ ; $T_j=150^{\circ}C$                         |      |      | 0.7  | V       |

1. For each channel.
2. PowerMOS leakage included.

**Table 7. Switching ( $V_{CC} = 13V$ ;  $T_j = 25^{\circ}C$ )**

| Symbol                | Parameter                                 | Test conditions                                   | Min.                          | Typ. | Max. | Unit       |
|-----------------------|---|---|-------------------------------|------|------|------------|
| $t_{d(on)}$           | Turn-on delay time                        | $R_L = 6.5\Omega$ (see <a href="#">Figure 8</a> ) |                               | 25   |      | $\mu s$    |
| $t_{d(off)}$          | Turn-off delay time                       | $R_L = 6.5\Omega$ (see <a href="#">Figure 8</a> ) |                               | 35   |      | $\mu s$    |
| $dV_{OUT}/dt_{(on)}$  | Turn-on voltage slope                     | $R_L = 6.5\Omega$                                 | See <a href="#">Figure 21</a> |      |      | V/ $\mu s$ |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope                    | $R_L = 6.5\Omega$                                 | See <a href="#">Figure 22</a> |      |      | V/ $\mu s$ |
| $W_{ON}$              | Switching energy losses during $t_{won}$  | $R_L = 6.5\Omega$ (see <a href="#">Figure 8</a> ) |                               | 0.24 |      | mJ         |
| $W_{OFF}$             | Switching energy losses during $t_{woff}$ | $R_L = 6.5\Omega$ (see <a href="#">Figure 8</a> ) |                               | 0.2  |      | mJ         |

**Table 8. Logic input**

| Symbol        | Parameter                 | Test conditions                   | Min. | Typ. | Max. | Unit    |
|---------------|---------------------------|-----------------------------------|------|------|------|---------|
| $V_{IL}$      | Input low level voltage   |                                   |      |      | 0.9  | V       |
| $I_{IL}$      | Low level input current   | $V_{IN} = 0.9V$                   | 1    |      |      | $\mu A$ |
| $V_{IH}$      | Input high level voltage  |                                   | 2.1  |      |      | V       |
| $I_{IH}$      | High level input current  | $V_{IN} = 2.1V$                   |      |      | 10   | $\mu A$ |
| $V_{I(hyst)}$ | Input hysteresis voltage  |                                   | 0.25 |      |      | V       |
| $V_{ICL}$     | Input clamp voltage       | $I_{IN} = 1mA$<br>$I_{IN} = -1mA$ | 5.5  | -0.7 | 7    | V<br>V  |
| $V_{CSDL}$    | CS_DIS low level voltage  |                                   |      |      | 0.9  | V       |
| $I_{CSDL}$    | Low level CS_DIS current  | $V_{CSD} = 0.9V$                  | 1    |      |      | $\mu A$ |
| $V_{CSDH}$    | CS_DIS high level voltage |                                   | 2.1  |      |      | V       |
| $I_{CSDH}$    | High level CS_DIS current | $V_{CSD} = 2.1V$                  |      |      | 10   | $\mu A$ |

**Table 8. Logic input (continued)**

| Symbol          | Parameter                 | Test conditions                     | Min. | Typ. | Max. | Unit   |
|-----------------|---------------------------|-------------------------------------|------|------|------|--------|
| $V_{CSD(hyst)}$ | CS_DIS hysteresis voltage |                                     | 0.25 |      |      | V      |
| $V_{CSCL}$      | CS_DIS clamp voltage      | $I_{CSD} = 1mA$<br>$I_{CSD} = -1mA$ | 5.5  | -0.7 | 7    | V<br>V |

**Table 9. Protections and diagnostics (1)**

| Symbol      | Parameter                                    | Test conditions   | Min.          | Typ.          | Max.          | Unit   |
|-------------|--|---|---------------|---------------|---------------|--------|
| $I_{limH}$  | DC short circuit current                     | $V_{CC} = 13V$<br>$5V < V_{CC} < 36V$   | 12            | 18            | 24<br>24      | A<br>A |
| $I_{limL}$  | Short circuit current during thermal cycling | $V_{CC} = 13V$ ; $T_R < T_J < T_{TSD}$  |               | 7             |               | A      |
| $T_{TSD}$   | Shutdown temperature                         |   | 150           | 175           | 200           | °C     |
| $T_R$       | Reset temperature                            |   | $T_{RS} + 1$  | $T_{RS} + 5$  |               | °C     |
| $T_{RS}$    | Thermal reset of STATUS                      |   | 135           |               |               | °C     |
| $T_{HYST}$  | Thermal hysteresis ( $T_{TSD} - T_R$ )       |   |               | 7             |               | °C     |
| $V_{DEMAG}$ | Turn-off output voltage clamp                | $I_{OUT} = 2A$ ; $V_{IN} = 0$ ; $L = 6mH$   | $V_{CC} - 41$ | $V_{CC} - 46$ | $V_{CC} - 52$ | V      |
| $V_{ON}$    | Output voltage drop limitation               | $I_{OUT} = 0.1A$ ;<br>$T_J = -40°C \dots +150°C$<br>(see <a href="#">Figure 9</a> ) |               | 25            |               | mV     |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 10. Current sense (8V <  $V_{CC}$  < 16V)**

| Symbol           | Parameter                 | Test conditions   | Min.         | Typ.         | Max.         | Unit |
|------------------|---------------------------|---|--------------|--------------|--------------|------|
| $K_0$            | $I_{OUT}/I_{SENSE}$       | $I_{OUT} = 0.05A$ ;<br>$V_{SENSE} = 0.5V$ ; $V_{CSD} = 0V$ ;<br>$T_J = -40°C \dots 150°C$           | 1270         | 2360         | 3450         |      |
| $K_1$            | $I_{OUT}/I_{SENSE}$       | $I_{OUT} = 1A$ ; $V_{SENSE} = 0.5V$ ; $V_{CSD} = 0V$ ;<br>$T_J = -40°C$<br>$T_J = 25°C \dots 150°C$ | 1470<br>1570 | 2020<br>2020 | 2610<br>2470 |      |
| $dK_1/K_1^{(1)}$ | Current sense ratio drift | $I_{OUT} = 1A$ ; $V_{SENSE} = 0.5V$ ;<br>$V_{CSD} = 0V$ ;<br>$T_J = -40°C$ to $150°C$               | -7           |              | +7           | %    |
| $K_2$            | $I_{OUT}/I_{SENSE}$       | $I_{OUT} = 2A$ ; $V_{SENSE} = 4V$ ; $V_{CSD} = 0V$ ;<br>$T_J = -40°C$<br>$T_J = 25°C \dots 150°C$   | 1740<br>1790 | 2020<br>2020 | 2320<br>2250 |      |

**Table 10. Current sense (8V<V<sub>CC</sub><16V) (continued)**

| Symbol           | Parameter   | Test conditions  | Min.         | Typ.         | Max.         | Unit          |
|------------------|---|--|--------------|--------------|--------------|---------------|
| $dK_2/K_2^{(1)}$ | Current sense ratio drift                                 | $I_{OUT}=2\text{ A}$ ; $V_{SENSE}=4\text{ V}$ ;<br>$V_{CSD}=0\text{V}$ ;<br>$T_J=-40\text{ }^\circ\text{C to }150\text{ }^\circ\text{C}$     | -4           |              | +4           | %             |
| $K_3$            | $I_{OUT}/I_{SENSE}$                                       | $I_{OUT}=4\text{A}$ ; $V_{SENSE}=4\text{V}$ ; $V_{CSD}=0\text{V}$ ;<br>$T_J=-40^\circ\text{C}$<br>$T_J=25^\circ\text{C}...150^\circ\text{C}$ | 1880<br>1900 | 2010<br>2010 | 2160<br>2120 |               |
| $dK_3/K_3^{(1)}$ | Current sense ratio drift                                 | $I_{OUT}=4\text{ A}$ ; $V_{SENSE}=4\text{ V}$ ;<br>$V_{CSD}=0\text{V}$ ;<br>$T_J=-40\text{ }^\circ\text{C to }150\text{ }^\circ\text{C}$     | -2           |              | +2           | %             |
| $I_{SENSE0}$     | Analog sense leakage current                              | $I_{OUT}=0\text{A}$ ; $V_{SENSE}=0\text{V}$ ;<br>$V_{CSD}=5\text{V}$ ; $V_{IN}=0\text{V}$ ;<br>$T_J=-40^\circ\text{C}...150^\circ\text{C}$   | 0            |              | 1            | $\mu\text{A}$ |
|                  |   | $V_{CSD}=0\text{V}$ ; $V_{IN}=5\text{V}$ ;<br>$T_J=-40^\circ\text{C}...150^\circ\text{C}$  | 0            |              | 2            | $\mu\text{A}$ |
|                  |   | $I_{OUT}=2\text{A}$ ; $V_{SENSE}=0\text{V}$ ;<br>$V_{CSD}=5\text{V}$ ; $V_{IN}=5\text{V}$ ;<br>$T_J=-40^\circ\text{C}...150^\circ\text{C}$   | 0            |              | 1            | $\mu\text{A}$ |
| $I_{OL}$         | Openload on-state current detection threshold             | $V_{IN} = 5\text{V}$ , $I_{SENSE} = 5\text{ }\mu\text{A}$  | 4            |              | 20           | mA            |
| $V_{SENSE}$      | Max analog sense output voltage                           | $I_{OUT}=4\text{A}$ ; $V_{CSD}=0\text{V}$  | 5            |              |              | V             |
| $V_{SENSEH}$     | Analog sense output voltage in over temperature condition | $V_{CC}=13\text{V}$ ; $R_{SENSE}=10\text{K}\Omega$   |              | 9            |              | V             |
| $I_{SENSEH}$     | Analog sense output current in over temperature condition | $V_{CC}=13\text{V}$ ; $V_{SENSE}=5\text{V}$  |              | 8            |              | mA            |
| $t_{DSENSE1H}$   | Delay response time from falling edge of CS_DIS pin       | $V_{SENSE}<4\text{V}$ , $0.5\text{A}<I_{OUT}<4\text{A}$<br>$I_{SENSE}=90\%$ of $I_{SENSE\text{ max}}$<br>(see <a href="#">Figure 4</a> )     |              | 50           | 100          | $\mu\text{s}$ |
| $t_{DSENSE1L}$   | Delay response time from rising edge of CS_DIS pin        | $V_{SENSE}<4\text{V}$ , $0.5\text{A}<I_{OUT}<4\text{A}$<br>$I_{SENSE}=10\%$ of $I_{SENSE\text{ max}}$<br>(see <a href="#">Figure 4</a> )     |              | 5            | 20           | $\mu\text{s}$ |
| $t_{DSENSE2H}$   | Delay response time from rising edge of INPUT pin         | $V_{SENSE}<4\text{V}$ , $0.5\text{A}<I_{OUT}<4\text{A}$<br>$I_{SENSE}=90\%$ of $I_{SENSE\text{ max}}$<br>(see <a href="#">Figure 4</a> )     |              | 80           | 250          | $\mu\text{s}$ |

**Table 10. Current sense (8V<V<sub>CC</sub><16V) (continued)**

| Symbol                | Parameter  | Test conditions   | Min. | Typ. | Max. | Unit    |
|-----------------------|--|---|------|------|------|---------|
| $\Delta t_{DSENSE2H}$ | Delay response time between rising edge of output current and rising edge of current sense | $V_{SENSE} < 4V$ ,<br>$I_{SENSE} = 90\%$ of $I_{SENSEMAX}$ ,<br>$I_{OUT} = 90\%$ of $I_{OUTMAX}$<br>$I_{OUTMAX}=2A$ (see <a href="#">Figure 5</a> ) |      |      | 65   | $\mu s$ |
| $t_{DSENSE2L}$        | Delay response time from falling edge of INPUT pin   | $V_{SENSE} < 4V$ , $0.5A < I_{OUT} < 4A$<br>$I_{SENSE} = 10\%$ of $I_{SENSE\ max}$<br>(see <a href="#">Figure 4</a> )                               |      | 100  | 250  | $\mu s$ |

1. Parameter guaranteed by design; it is not tested.

**Figure 4. Current sense delay characteristics**

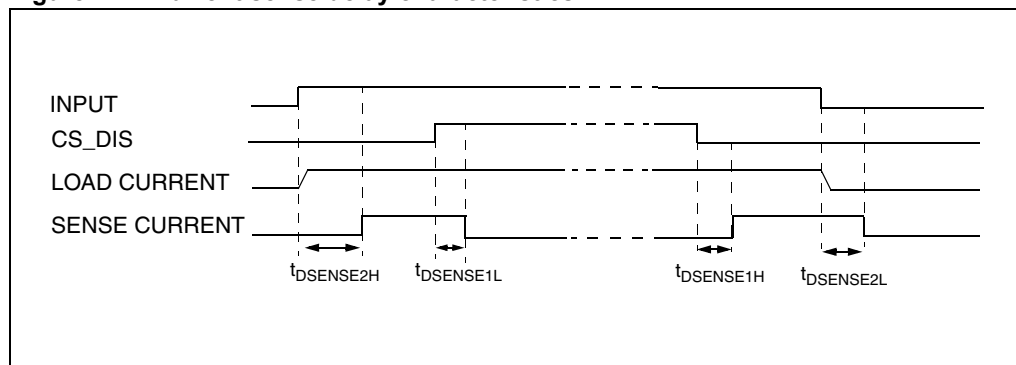


Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

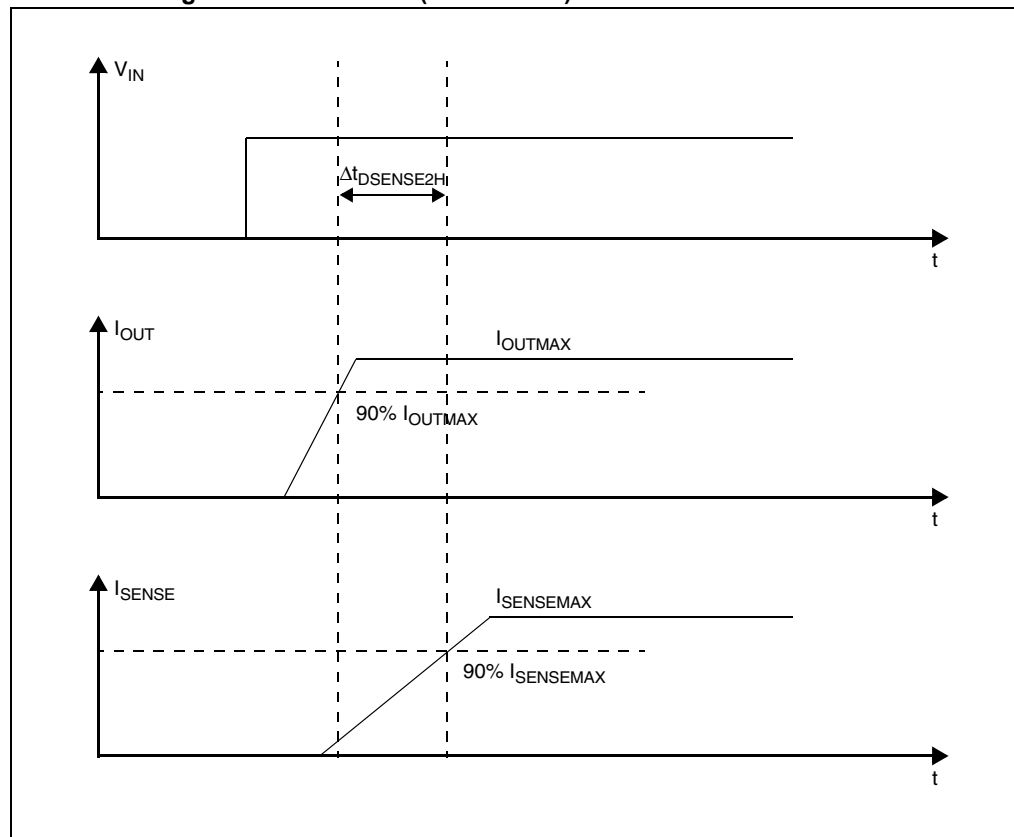


Figure 6.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$

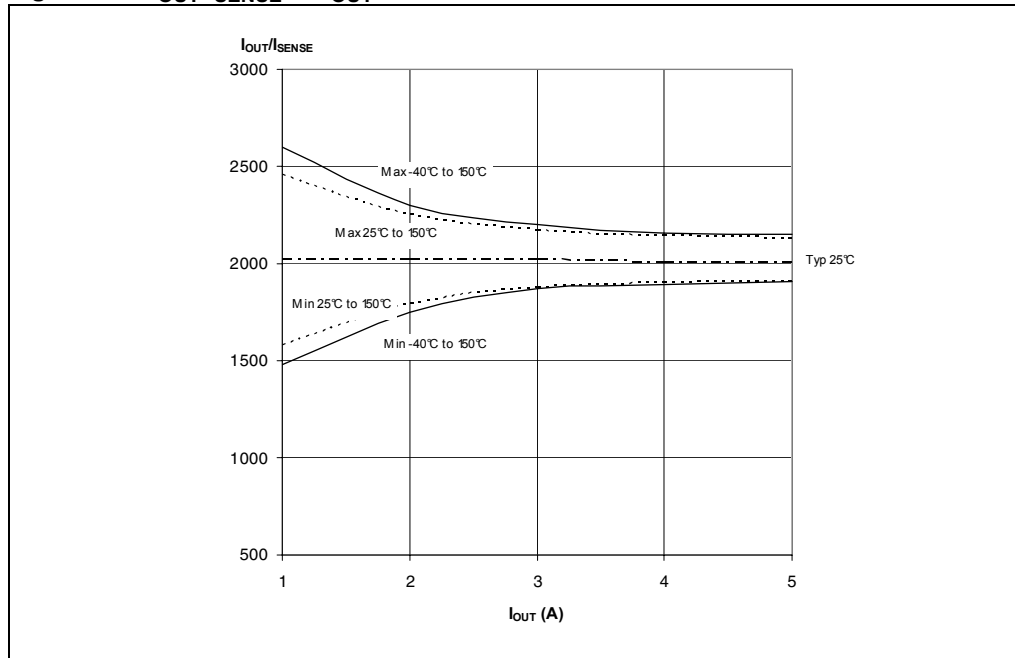
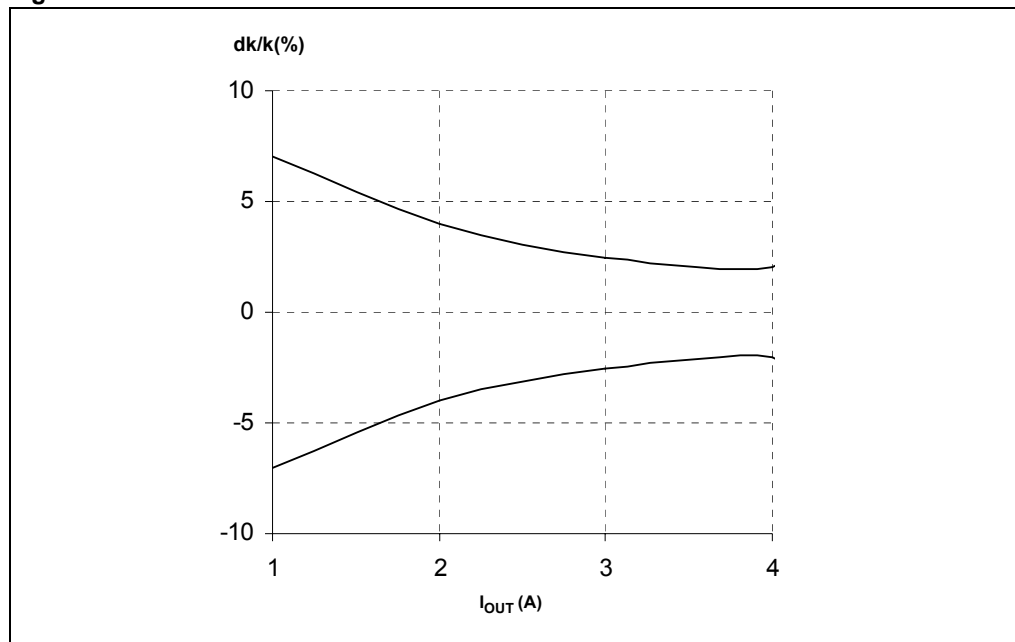


Figure 7. Maximum current sense ratio drift vs load current



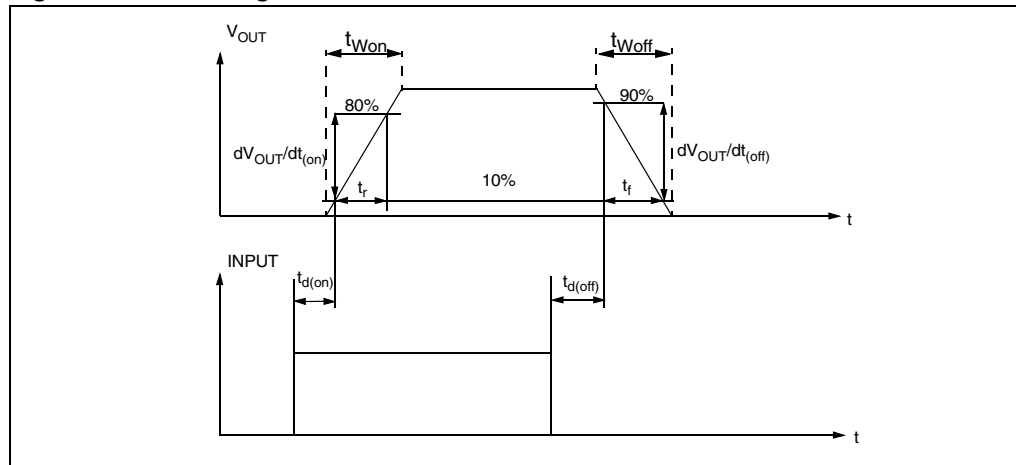
Note: Parameter guaranteed by design; it is not tested.

**Table 11. Truth table**

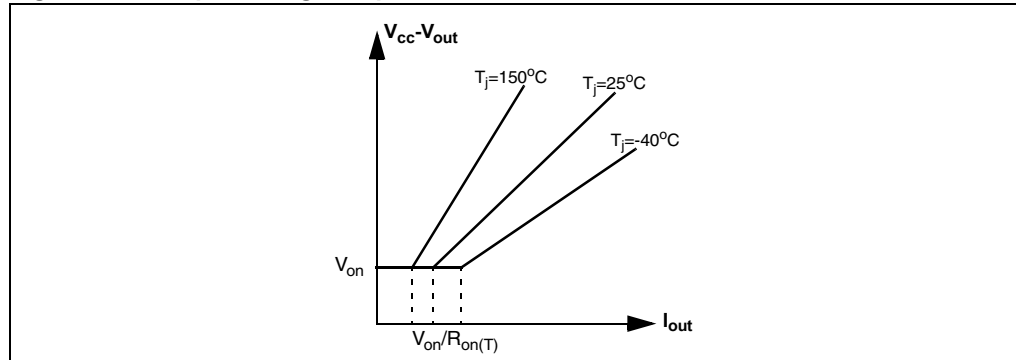
| Conditions  | Input | Output | Sense ( $V_{CSD}=0V$ ) <sup>(1)</sup> |
|---|-------|--------|---------------------------------------|
| Normal operation  | L     | L      | 0                                     |
|   | H     | H      | Nominal                               |
| Over temperature  | L     | L      | 0                                     |
|   | H     | L      | $V_{SENSEH}$                          |
| Undervoltage  | L     | L      | 0                                     |
|   | H     | L      | 0                                     |
| Short circuit to GND<br>( $R_{sc} \leq 10\text{ m}\Omega$ ) | L     | L      | 0                                     |
|   | H     | L      | 0 if $T_j < T_{TSD}$                  |
|   | H     | L      | $V_{SENSEH}$ if $T_j > T_{TSD}$       |
| Short circuit to $V_{CC}$                                   | L     | H      | 0                                     |
|   | H     | H      | < Nominal                             |
| Negative output voltage clamp                               | L     | L      | 0                                     |

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

**Figure 8. Switching characteristics**



**Figure 9. Output voltage drop limitation**



**Table 12. Electrical transient requirements (part 1/3)**

| ISO 7637-2:<br>2004(E)<br>test pulse | Test levels <sup>(1)</sup> |       | Number of<br>pulses or<br>test times | Burst cycle/pulse<br>repetition time |        | Delays and<br>impedance  |
|--------------------------------------|----------------------------|-------|--------------------------------------|--------------------------------------|--------|--------------------------|
|                                      | III                        | IV    |                                      |                                      |        |                          |
| 1                                    | -75V                       | -100V | 5000<br>pulses                       | 0.5 s                                | 5 s    | 2 ms, 10 $\Omega$        |
| 2a                                   | +37V                       | +50V  | 5000<br>pulses                       | 0.2 s                                | 5 s    | 50 $\mu$ s, 2 $\Omega$   |
| 3a                                   | -100V                      | -150V | 1h                                   | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$ |
| 3b                                   | +75V                       | +100V | 1h                                   | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$ |
| 4                                    | -6V                        | -7V   | 1 pulse                              |                                      |        | 100 ms, 0.01<br>$\Omega$ |
| 5b <sup>(2)</sup>                    | +65V                       | +87V  | 1 pulse                              |                                      |        | 400 ms, 2 $\Omega$       |

1. The above test levels must be considered referred to  $V_{cc} = 13.5V$  except for pulse 5b.

**Table 13. Electrical transient requirements (part 2/3)**

| ISO 7637-2:<br>2004(E)<br>test pulse | Test level results <sup>(1)</sup> |    |
|--------------------------------------|-----------------------------------|----|
|                                      | III                               | IV |
| 1                                    | C                                 | C  |
| 2a                                   | C                                 | C  |
| 3a                                   | C                                 | C  |
| 3b                                   | C                                 | C  |
| 4                                    | C                                 | C  |
| 5b <sup>(2)</sup>                    | C                                 | C  |

1. The above test levels must be considered referred to  $V_{cc} = 13.5V$  except for pulse 5b.

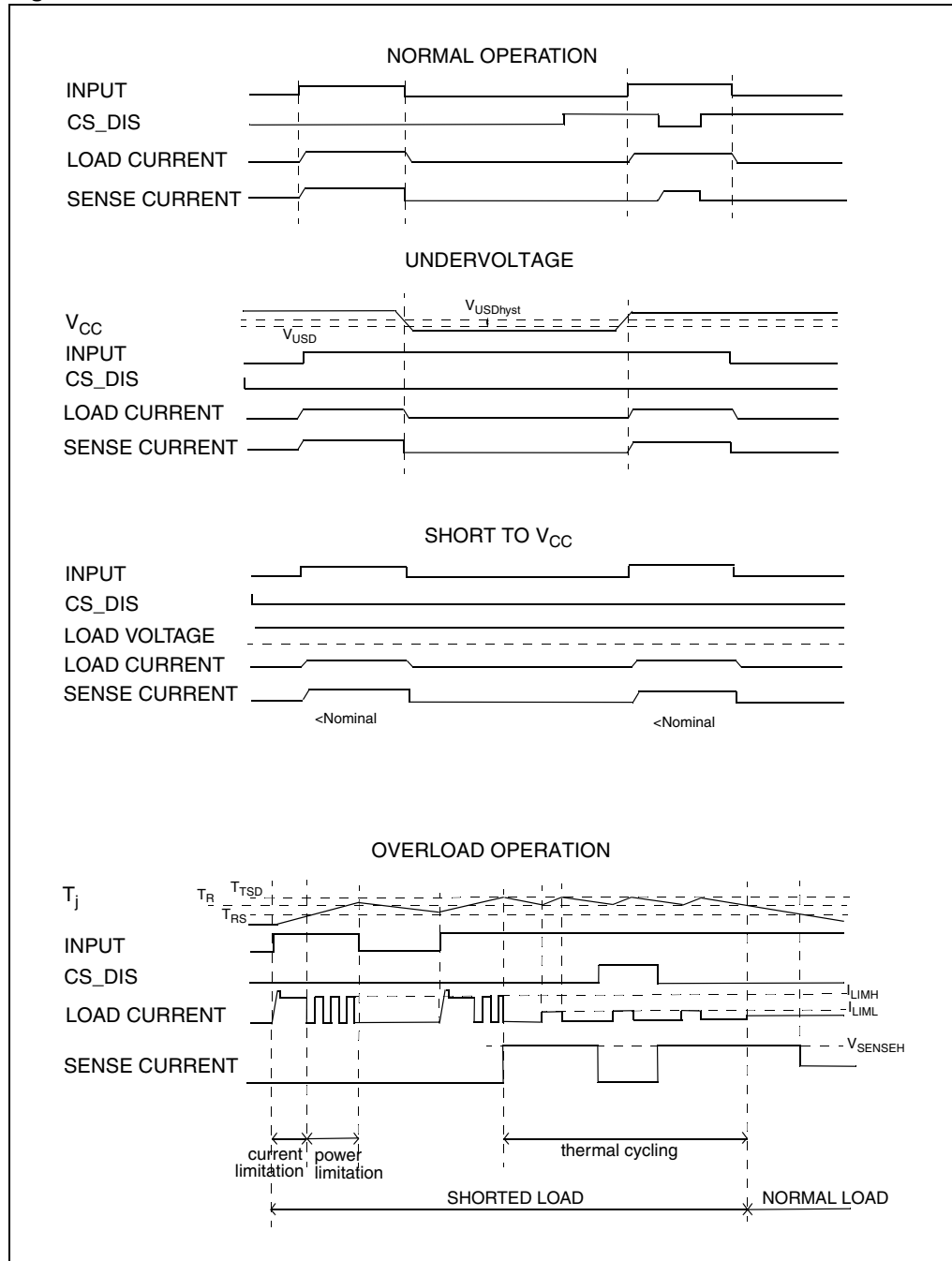
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 14. Electrical transient requirements (part 3/3)**

| Class | Contents   |
|-------|--|
| C     | All functions of the device are performed as designed after exposure to disturbance.   |
| E     | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |



Figure 10. Waveforms



## 2.4 Electrical characteristics curves

Figure 11. Off-state output current

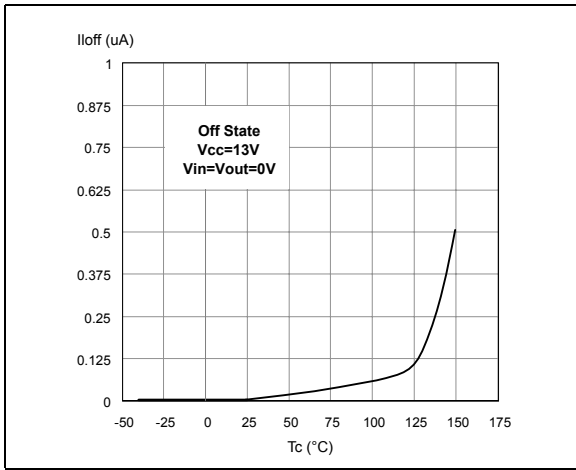


Figure 12. High level input current

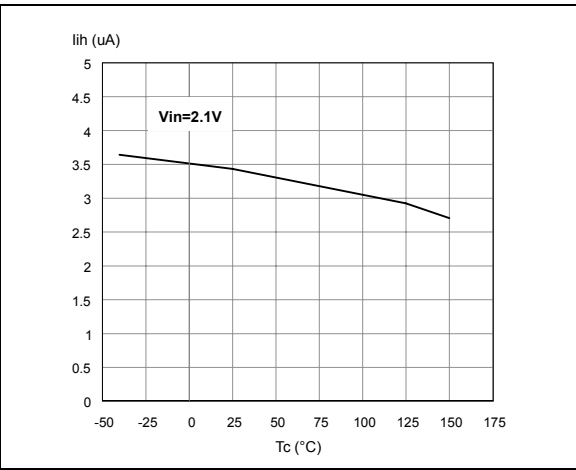


Figure 13. Input clamp voltage

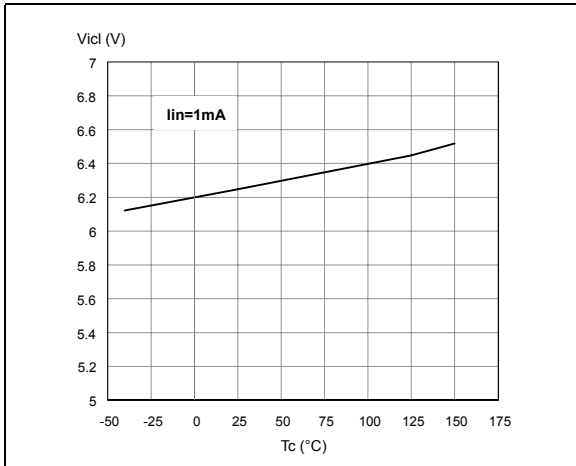


Figure 14. Input high level

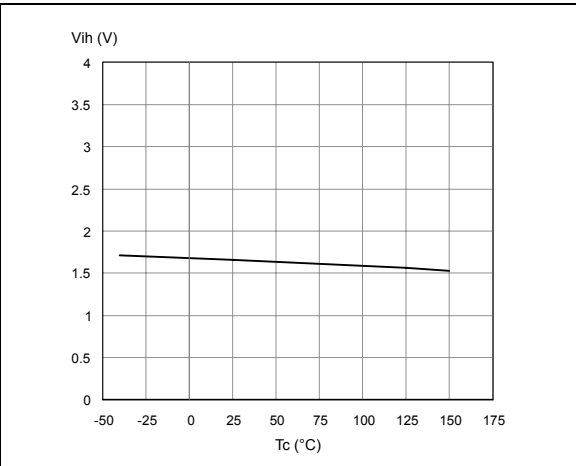


Figure 15. Input low level

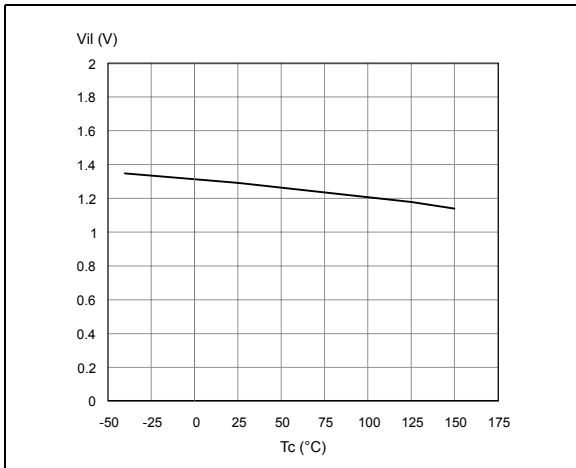


Figure 16. Input hysteresis voltage

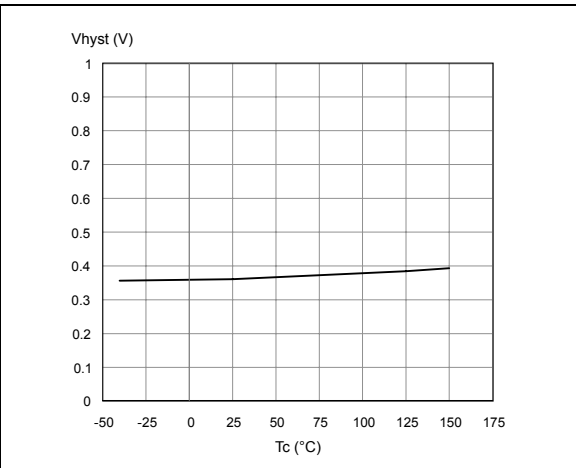


Figure 17. On-state resistance vs  $T_{case}$

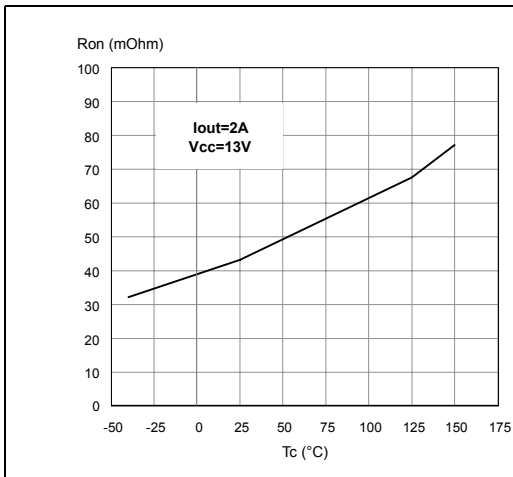


Figure 18. On-state resistance vs  $V_{CC}$

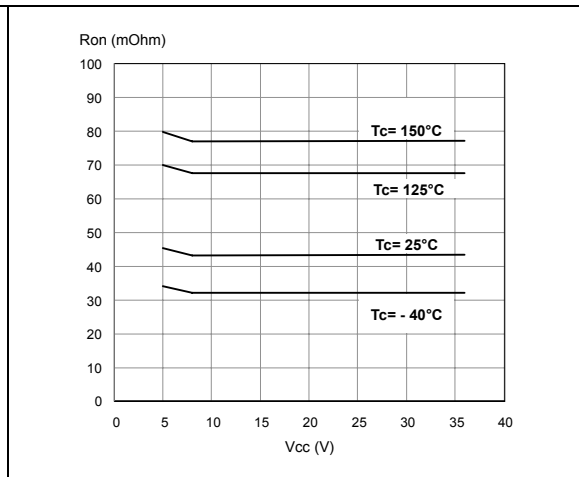


Figure 19. Undervoltage shutdown

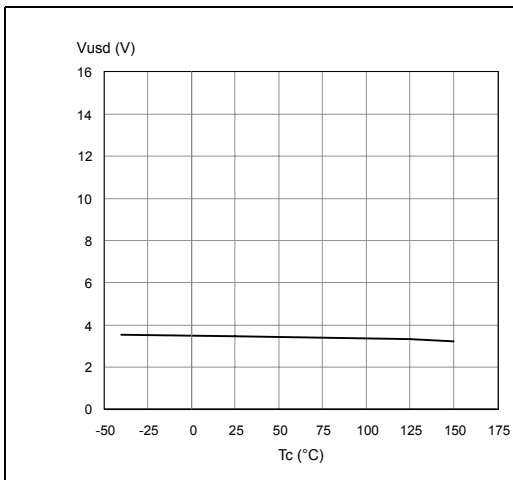


Figure 20.  $I_{LIMH}$  vs  $T_{case}$

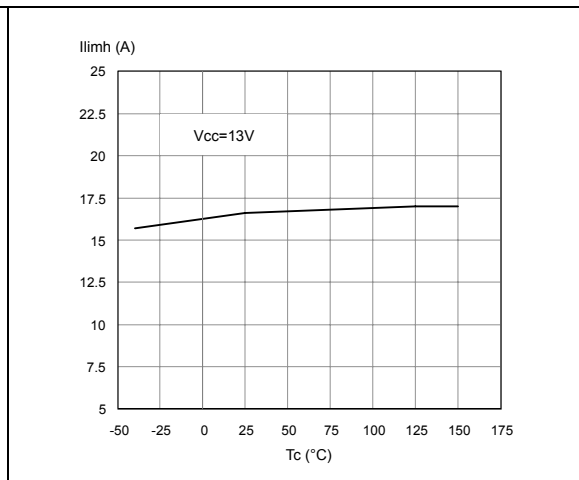


Figure 21. Turn-on voltage slope

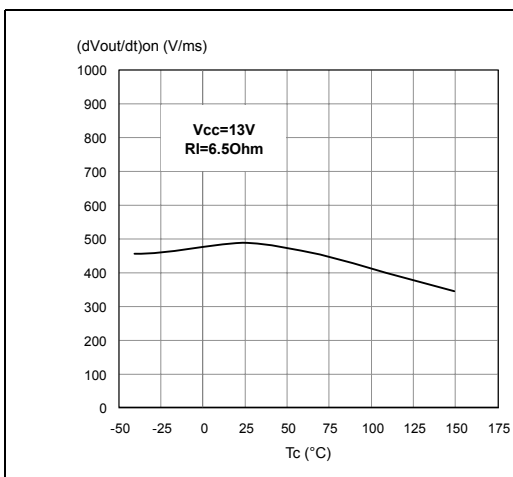


Figure 22. Turn-off voltage slope

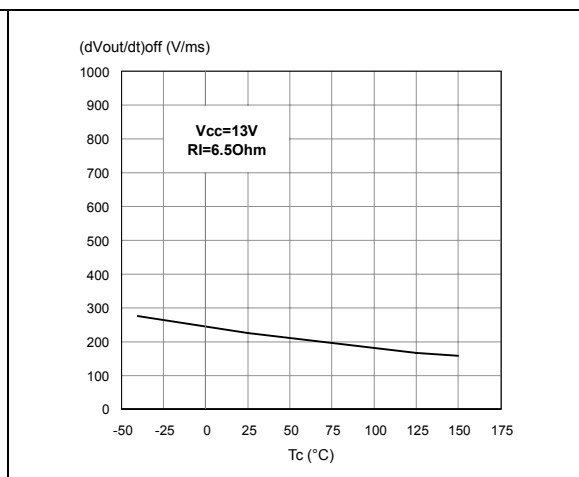


Figure 23. STAT\_DIS clamp voltage

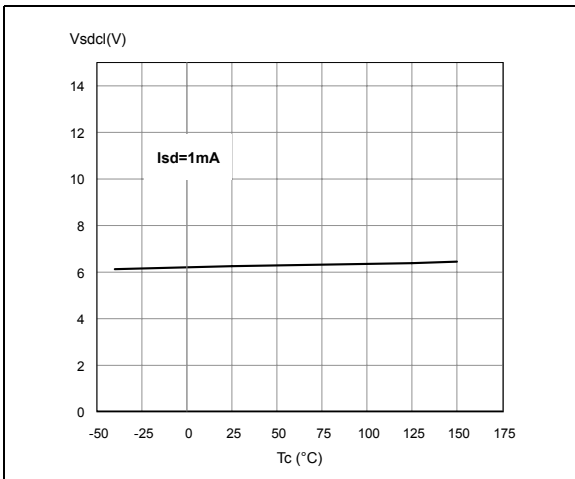


Figure 24. Low level STAT\_DIS voltage

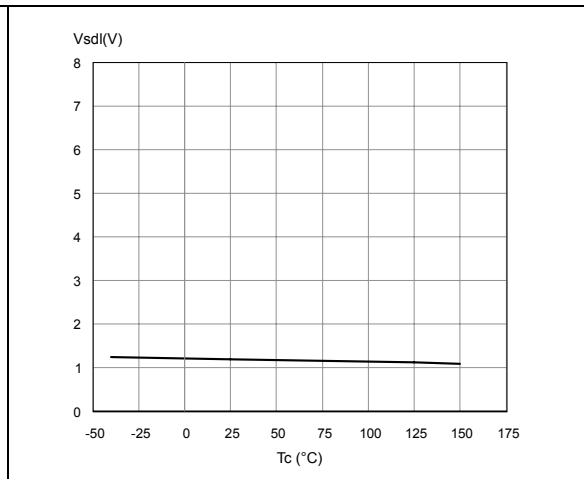
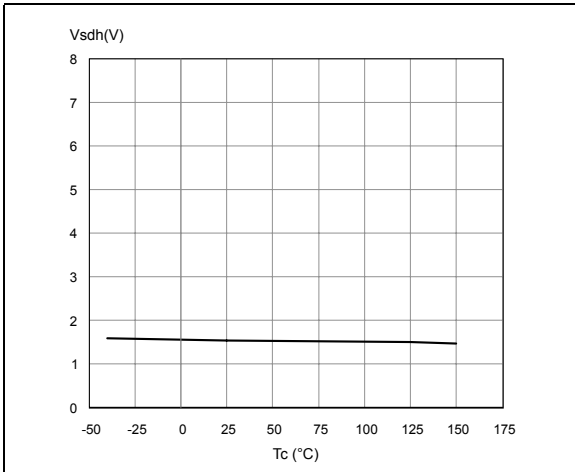
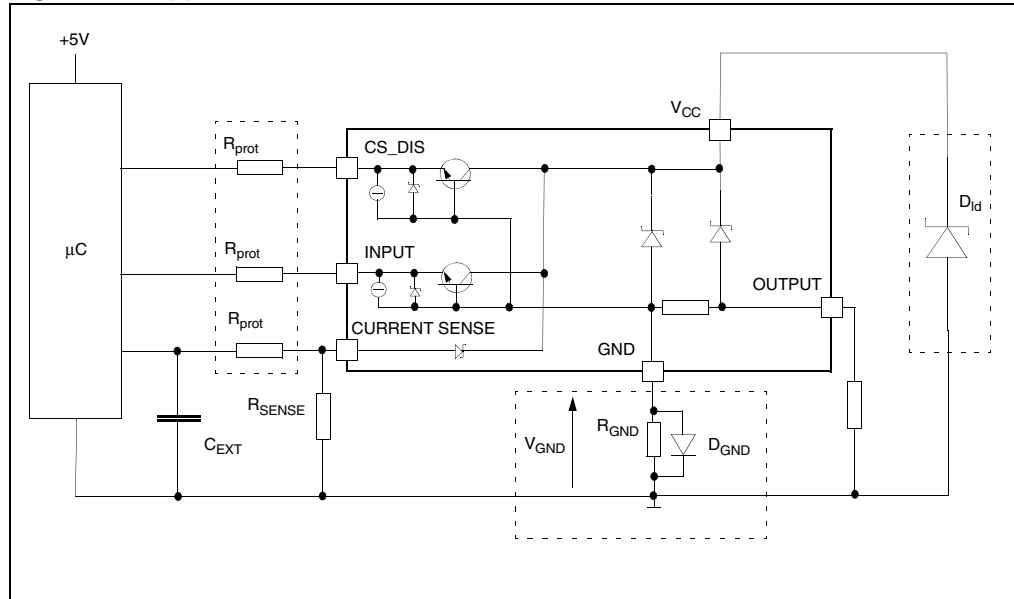


Figure 25. High level STAT\_DIS voltage



### 3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

#### 3.1 GND protection network against reverse battery

##### 3.1.1 Solution 1: resistor in the ground line ( $R_{GND}$ only)

This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 3.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

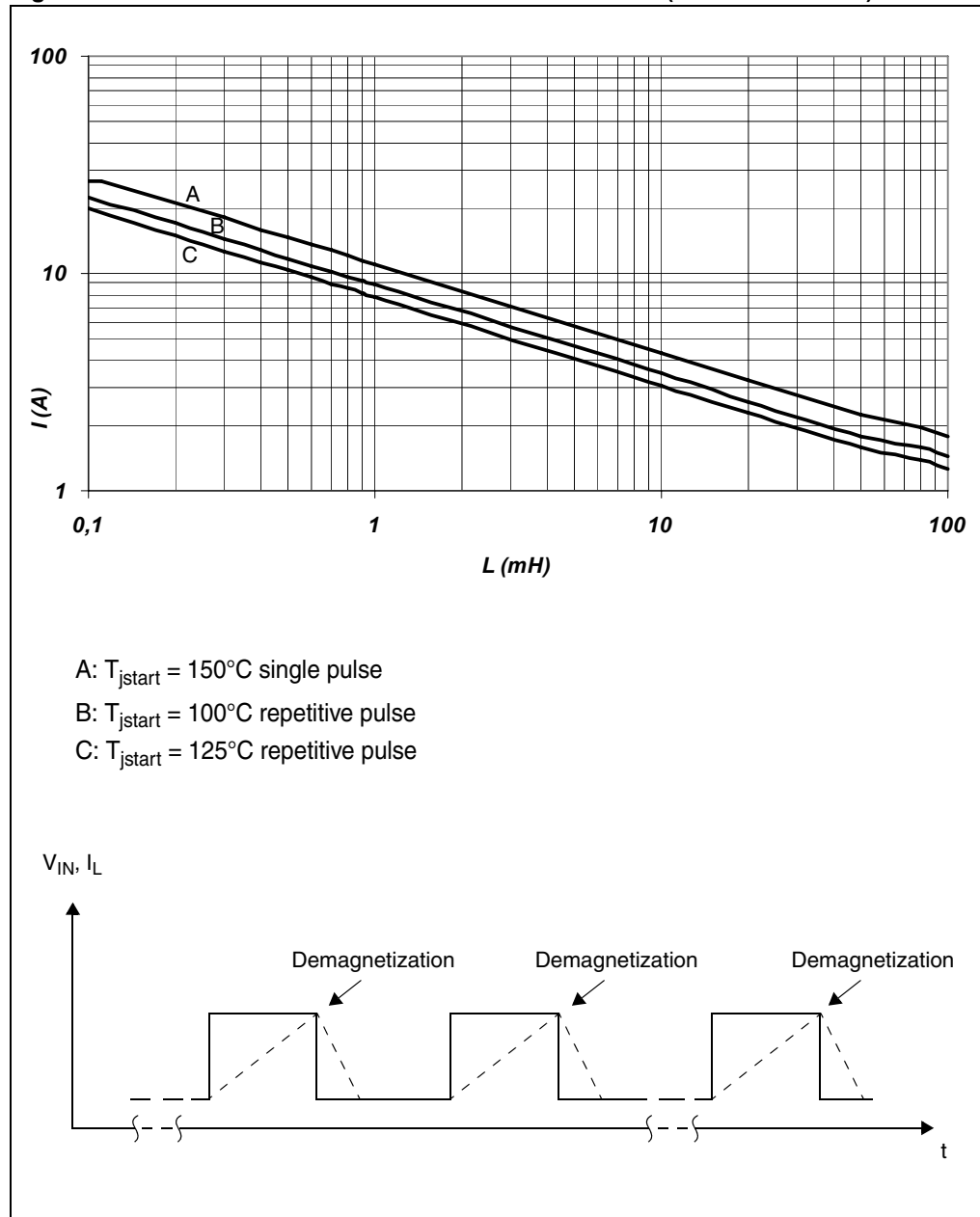
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values:  $R_{prot} = 10k\Omega$ ,  $C_{EXT} = 10nF$ .

### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 27. Maximum turn-off current versus inductance (for each channel)

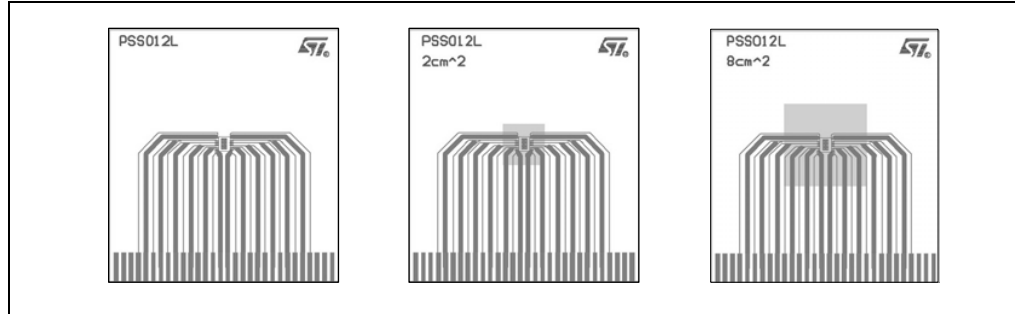


Note: Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

### 4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6 mm, Cu thickness=70  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 29.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)

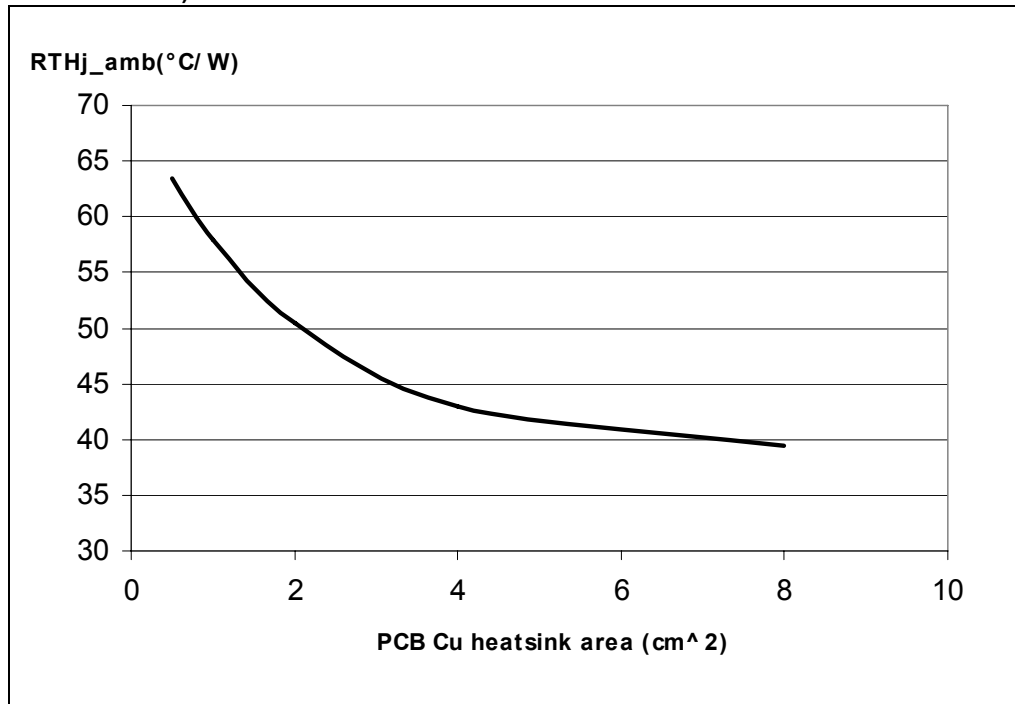
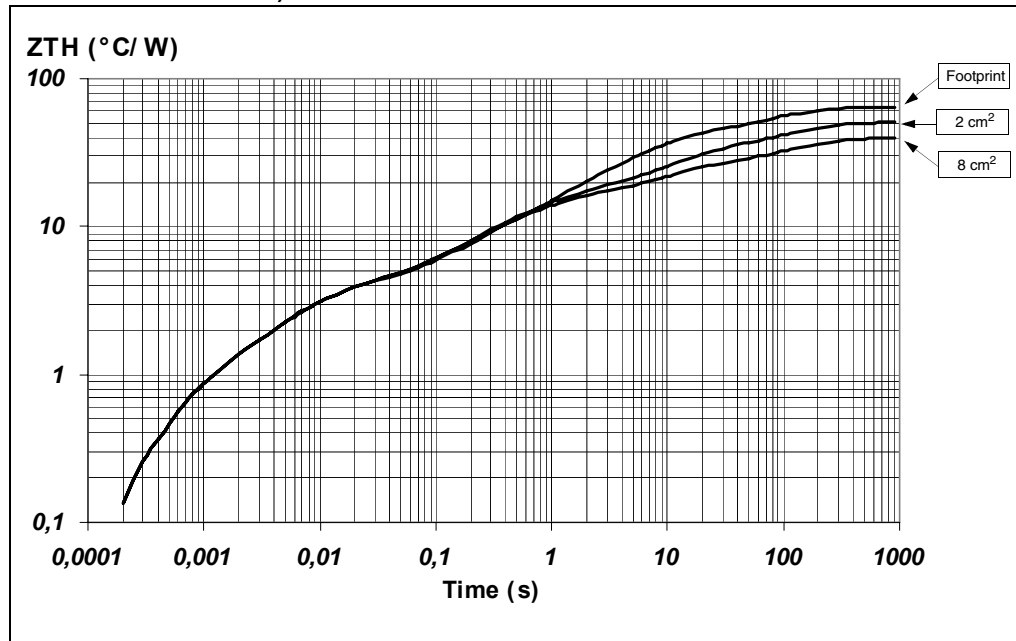




Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on)

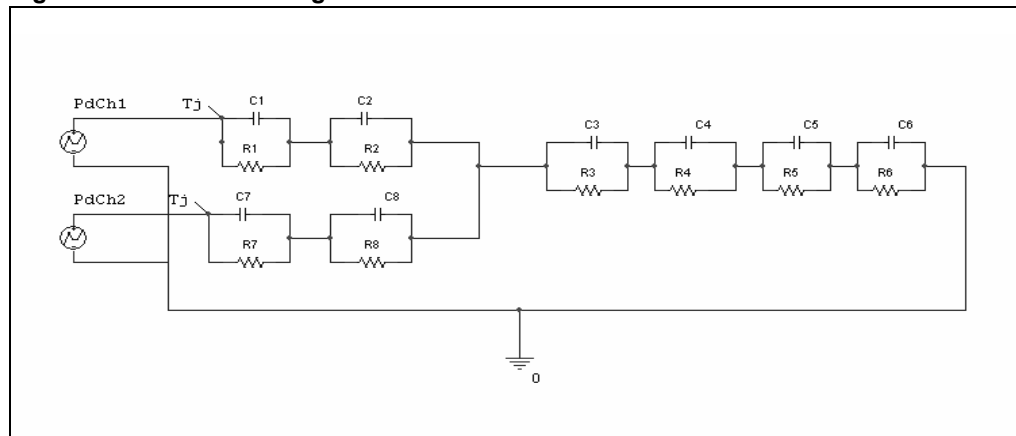


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ (a)



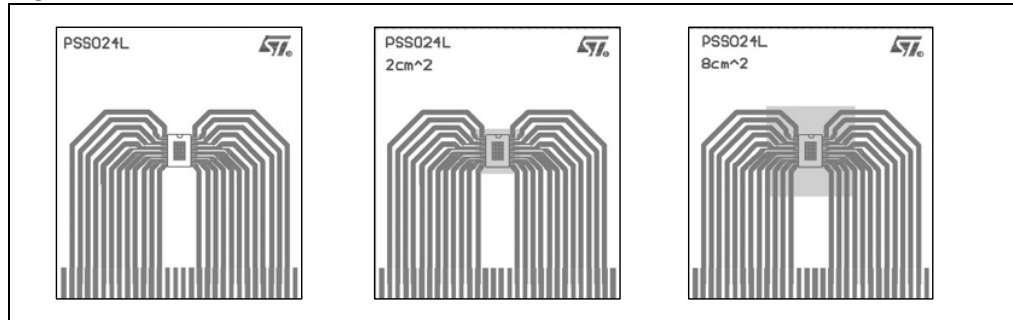
- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. PowerSSO-12™ thermal parameter

| Area/island (cm <sup>2</sup> ) | Footprint | 2   | 8   |
|--------------------------------|-----------|-----|-----|
| R1= R7 (°C/W)                  | 0.7       |     |     |
| R2= R8 (°C/W)                  | 2.8       |     |     |
| R3 (°C/W)                      | 4         |     |     |
| R4 (°C/W)                      | 8         | 8   | 7   |
| R5 (°C/W)                      | 22        | 15  | 10  |
| R6 (°C/W)                      | 26        | 20  | 15  |
| C1= C7 (W.s/°C)                | 0.001     |     |     |
| C2= C8 (W.s/°C)                | 0.0025    |     |     |
| C3 (W.s/°C)                    | 0.05      |     |     |
| C4 (W.s/°C)                    | 0.2       | 0.1 | 0.1 |
| C5 (W.s/°C)                    | 0.27      | 0.8 | 1   |
| C6 (W.s/°C)                    | 3         | 6   | 9   |

## 4.2 PowerSSO-24™ thermal data

Figure 32. PowerSSO-24™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6mm, Cu thickness=70  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 33.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)

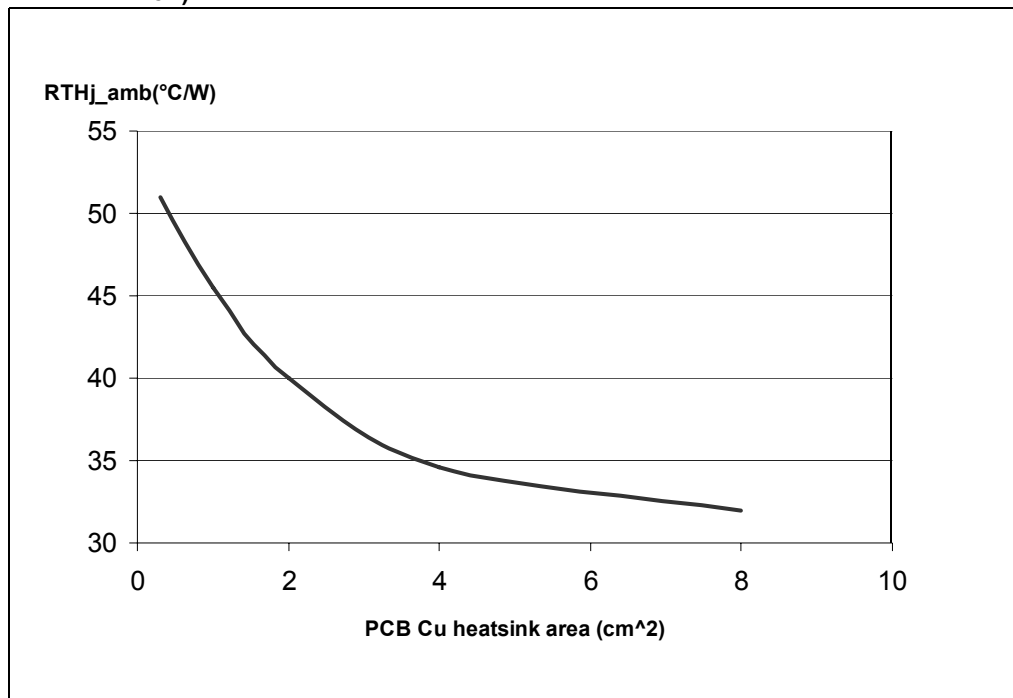
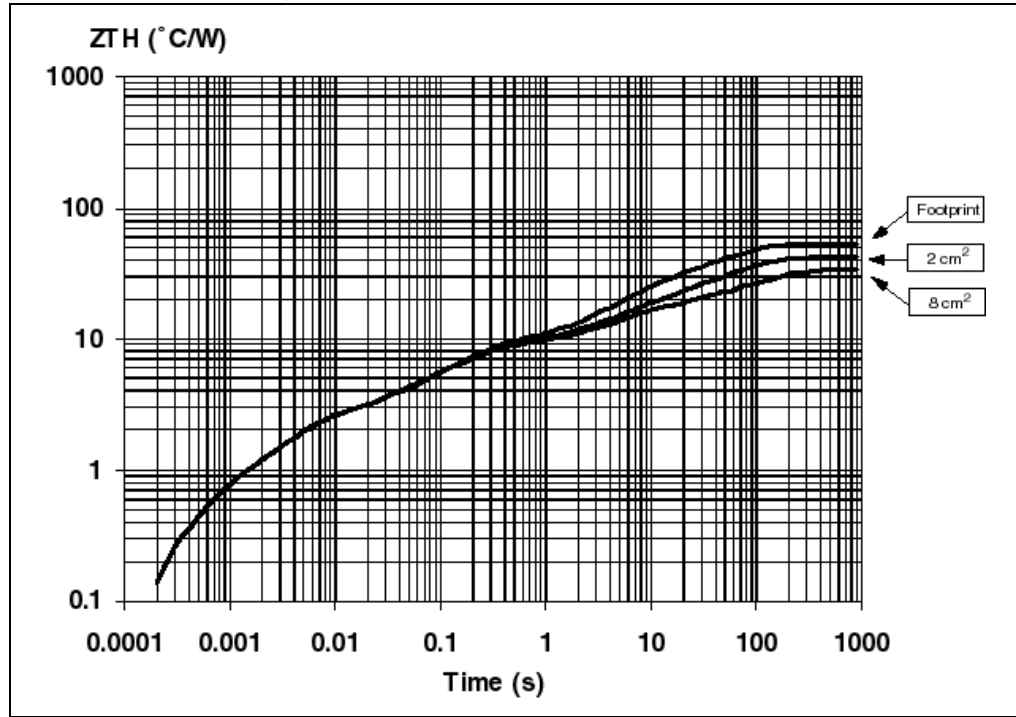


Figure 34. PowerSSO-24™ Thermal impedance junction ambient single pulse (one channel on)

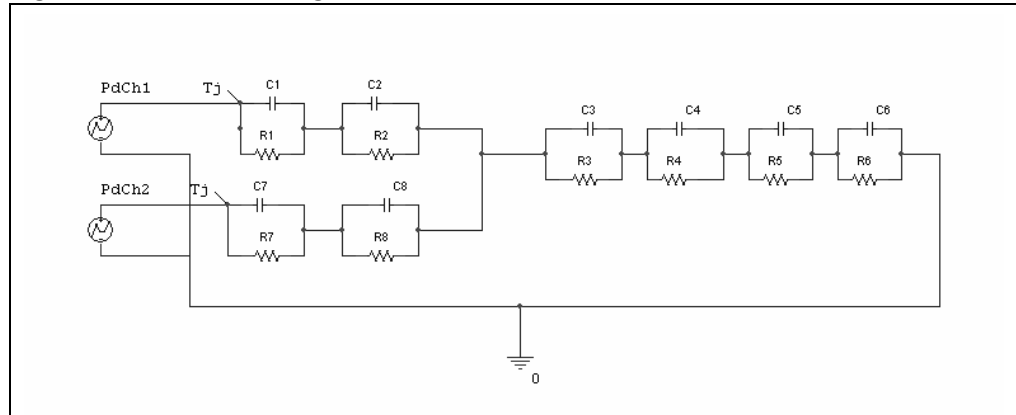


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-24™(b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. PowerSSO-24™ thermal parameter

| Area/island (cm <sup>2</sup> ) | Footprint | 2  | 8  |
|--------------------------------|-----------|----|----|
| R1=R7 (°C/W)                   | 0.4       |    |    |
| R2=R8 (°C/W)                   | 2         |    |    |
| R3 (°C/W)                      | 6         |    |    |
| R4 (°C/W)                      | 7.7       |    |    |
| R5 (°C/W)                      | 9         | 9  | 8  |
| R6 (°C/W)                      | 28        | 17 | 10 |
| C1=C7 (W.s/°C)                 | 0.001     |    |    |
| C2=C8 (W.s/°C)                 | 0.0022    |    |    |
| C3 (W.s/°C)                    | 0.025     |    |    |
| C4 (W.s/°C)                    | 0.75      |    |    |
| C5 (W.s/°C)                    | 1         | 4  | 9  |
| C6 (W.s/°C)                    | 2.2       | 5  | 17 |

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.2 PowerSSO-12™ package information

Figure 36. PowerSSO-12™ package dimensions

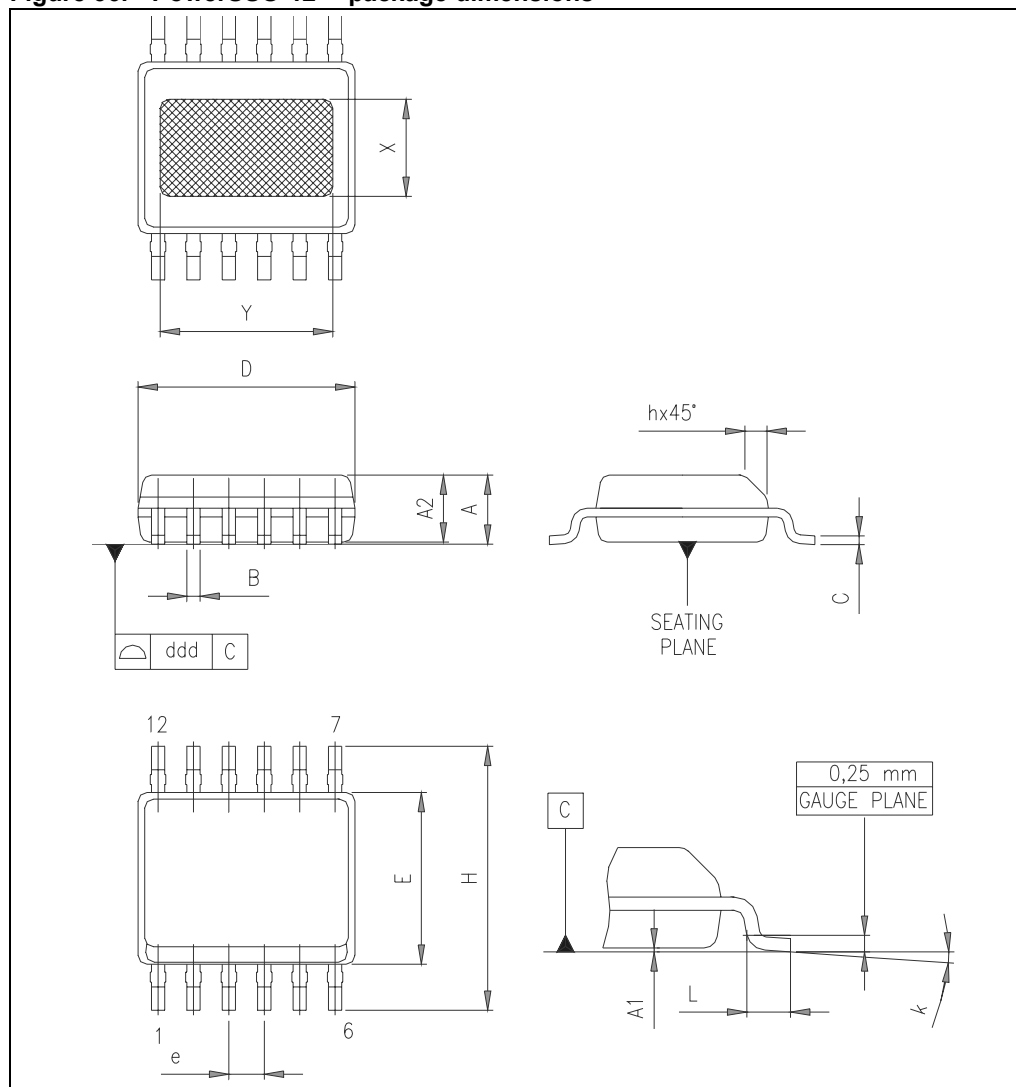


Table 17. PowerSSO-12™ mechanical data

| Symbol | Millimeters |      |      |
|--------|-------------|------|------|
|        | Min.        | Typ. | Max. |
| A      | 1.25        |      | 1.62 |
| A1     | 0           |      | 0.1  |
| A2     | 1.10        |      | 1.65 |
| B      | 0.23        |      | 0.41 |
| C      | 0.19        |      | 0.25 |
| D      | 4.8         |      | 5.0  |
| E      | 3.8         |      | 4.0  |
| e      |             | 0.8  |      |
| H      | 5.8         |      | 6.2  |
| h      | 0.25        |      | 0.5  |
| L      | 0.4         |      | 1.27 |
| k      | 0°          |      | 8°   |
| X      | 1.9         |      | 2.5  |
| Y      | 3.6         |      | 4.2  |
| ddd    |             |      | 0.1  |

### 5.3 PowerSSO-24™ package information

Figure 37. PowerSSO-24™ package dimensions

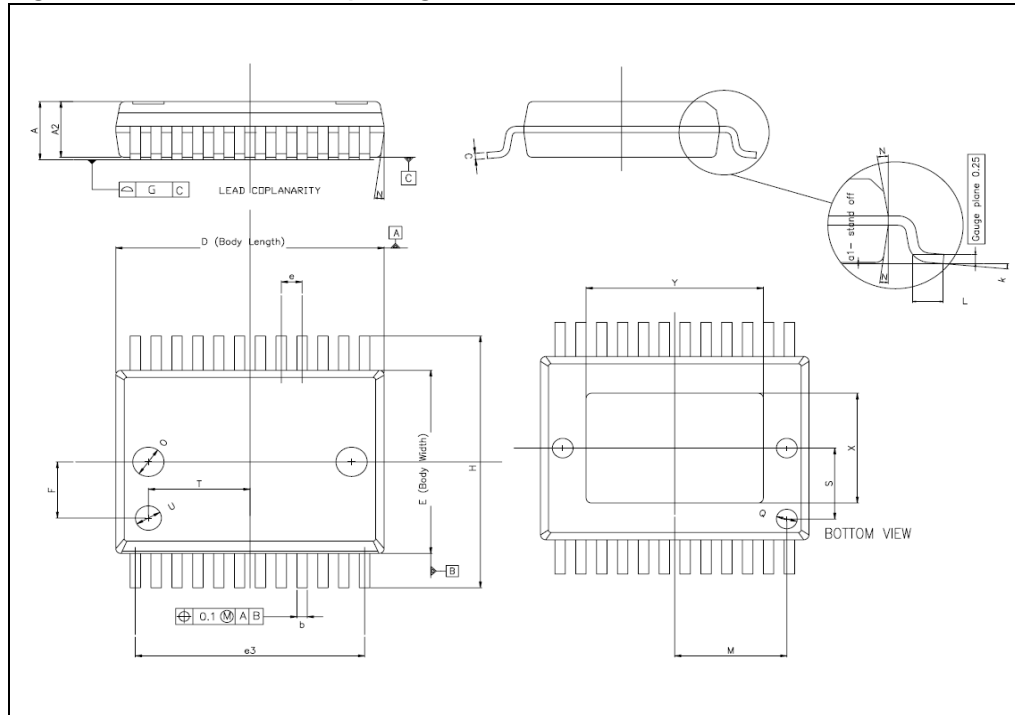


Table 18. PowerSSO-24™ mechanical data

| Symbol | Millimeters |      |       |
|--------|-------------|------|-------|
|        | Min.        | Typ. | Max.  |
| A      | -           |      | 2.45  |
| A2     | 2.15        |      | 2.35  |
| a1     | 0           |      | 0.1   |
| b      | 0.33        |      | 0.51  |
| c      | 0.23        |      | 0.32  |
| D      | 10.10       |      | 10.50 |
| E      | 7.4         |      | 7.6   |
| e      |             | 0.8  |       |
| e3     |             | 8.8  |       |
| F      |             | 2.3  |       |
| G      |             |      | 0.1   |
| H      | 10.1        |      | 10.5  |



Table 18. PowerSSO-24™ mechanical data (continued)

| Symbol | Millimeters |      |      |
|--------|-------------|------|------|
|        | Min.        | Typ. | Max. |
| h      |             |      | 0.4  |
| k      | 0°          |      | 8°   |
| L      | 0.55        |      | 0.85 |
| O      |             | 1.2  |      |
| Q      |             | 0.8  |      |
| S      |             | 2.9  |      |
| T      |             | 3.65 |      |
| U      |             | 1.0  |      |
| N      |             |      | 10°  |
| X      | 4.1         |      | 4.7  |
| Y      | 6.5         |      | 7.1  |

### 5.4 PowerSSO-12™ packing information

Figure 38. PowerSSO-12™ tube shipment (no suffix)

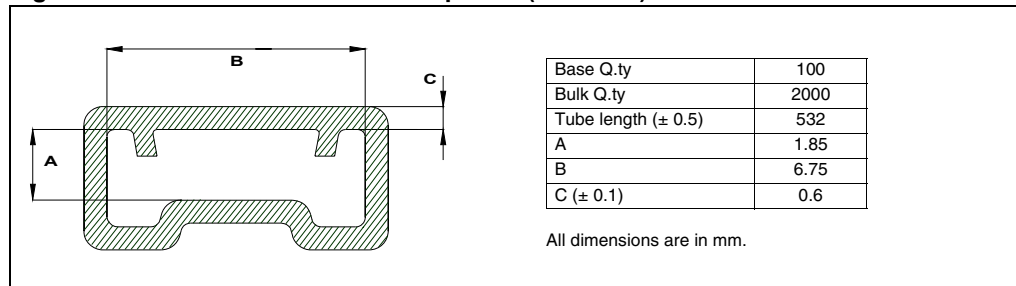
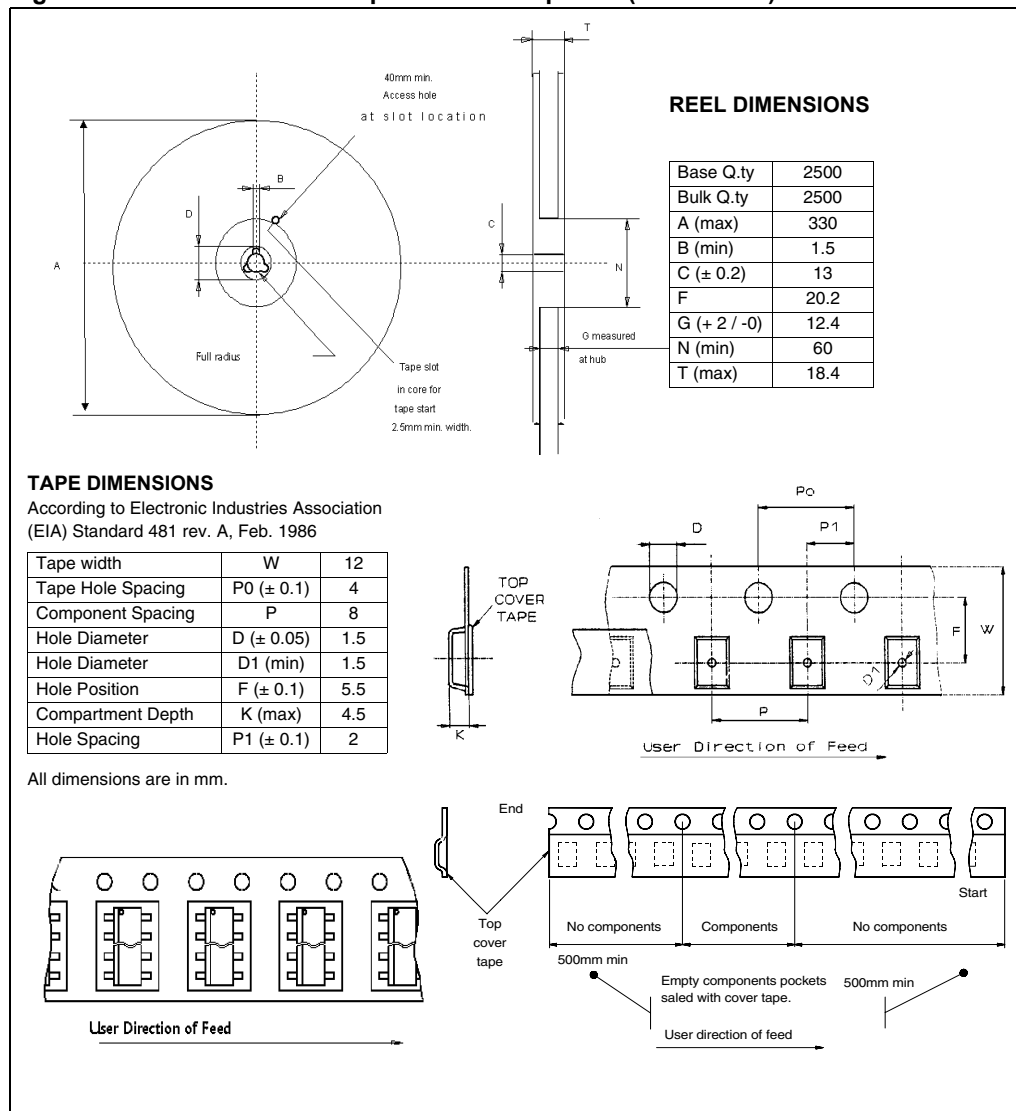


Figure 39. PowerSSO-12™ tape and reel shipment (suffix “TR”)



### 5.5 PowerSSO-24™ packing information

Figure 40. PowerSSO-24™ tube shipment (no suffix)

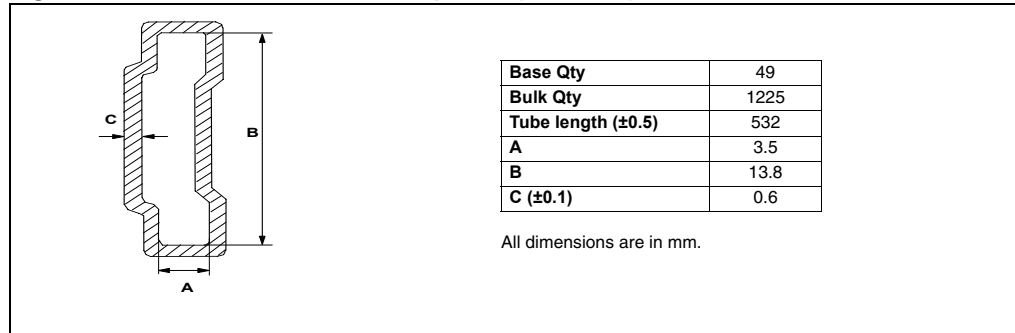
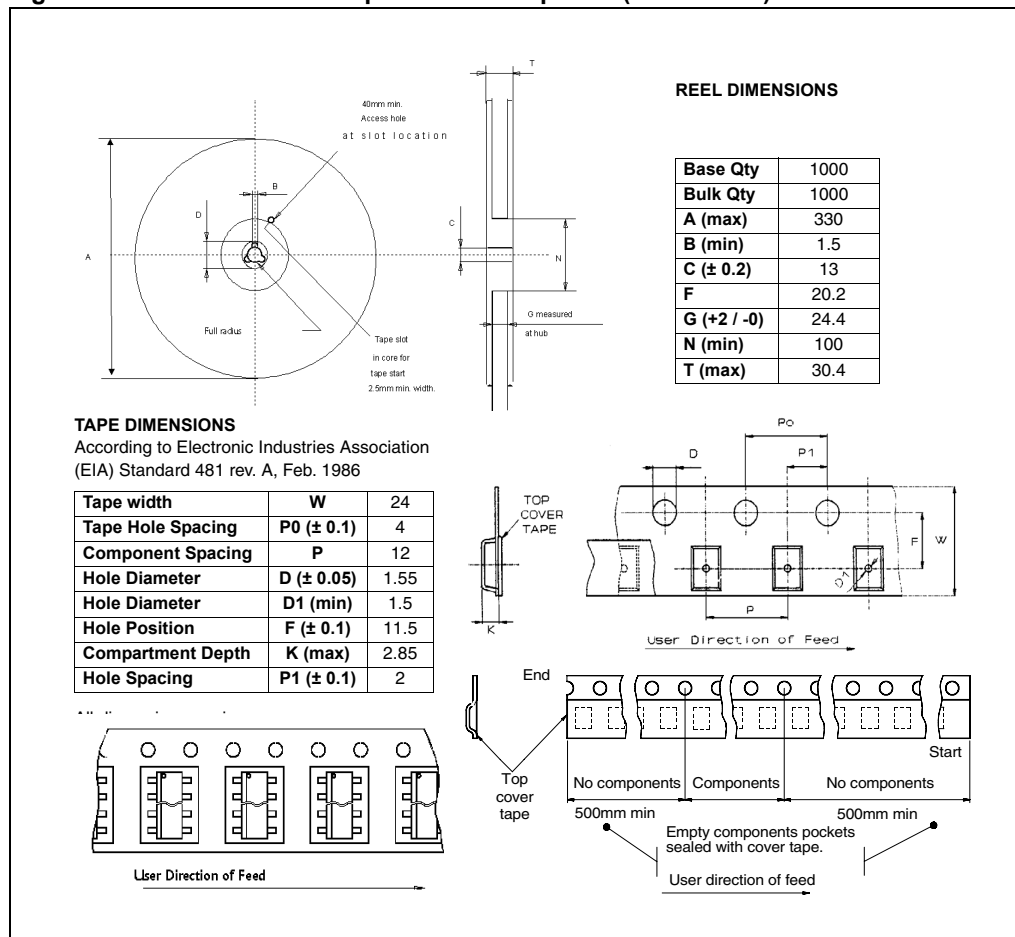


Figure 41. PowerSSO-24™ tape and reel shipment (suffix “TR”)



## 6 Revision history

Table 19. Document revision history

| Date        | Revision | Changes  |
|-------------|----------|--|
| 30-Mar-2006 | 1        | Initial release.   |
| 14-Apr-2006 | 2        | PowerSSO-24 dimensions table update.   |
| 26-Apr-2007 | 3        | Reformatted<br><i>Figure 31</i> title corrected  |
| 14-May-2007 | 4        | <i>Table 4</i> : corrected $E_{MAX}$ value.<br><i>Table 10</i> : added dk1/k1, dk2/k2, dk3/k3, $\Delta t_{DSENSE2H}$ .<br>Added <i>Figure 5</i> .<br>Updated <i>Figure 6</i> .<br>Added <i>Figure 7</i> .<br><i>Table 12</i> : Updated test level values III and IV for test pulse 5b and notes.<br>Added <i>Section 3.4: Maximum demagnetization energy (VCC = 13.5V)</i> .   |
| 01-Jun-2007 | 5        | <i>Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™</i> , <i>Figure 35: Thermal fitting model of a double channel HSD in PowerSSO-24™</i> : added notes.   |
| 04-Dec-2007 | 6        | Updated <i>Table 10: Current sense (8V &lt; V<sub>CC</sub> &lt; 16V)</i> :<br>– changed $t_{DSENSE2H}$ max value from 300 $\mu$ s to 250 $\mu$ s.<br>– added $I_{OL}$ parameter.<br>Updated <i>Section 4.1: PowerSSO-12™ thermal data</i> :<br>– Changed <i>Figure 29: R<sub>thj-amb</sub> vs PCB copper area in open box free air condition (one channel on)</i> .<br>– Changed <i>Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on)</i> .<br>– Updated <i>Table</i> : :<br>R3 value changed from 7 to 4 °C/W.<br>R4 values changed from 10 /10 /10 to 8 /8 /7 °C/W. |
| 12-Feb-2008 | 7        | Corrected typing error in <i>Table 10: Current sense (8V &lt; V<sub>CC</sub> &lt; 16V)</i> :<br>changed $I_{OL}$ test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$ .  |
| 16-Jun-2009 | 8        | <i>Table 18: PowerSSO-24™ mechanical data</i> :<br>– Deleted A (min) value<br>– Changed A (max) value from 2.47 to 2.45<br>– Changed A2 (max) value from 2.40 to 2.35<br>– Changed a1 (max) value from 0.075 to 0.1<br>– Added F and k rows  |
| 21-Jul-2009 | 9        | Updated <i>Figure 37: PowerSSO-24™ package dimensions</i> .<br>Updated <i>Table 18: PowerSSO-24™ mechanical data</i> :<br>– Deleted G1 row<br>– Added O, Q, S, T, and U rows   |

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