MX877
8-Channel, 60V Driver with Push-Pull Output, 3 Wire Interface

Features

- Eight (8) Outputs Rated at 60V, ±80mA
- Push-Pull Driver Configuration
- 6V to 60V Driver Supply Range
- 2.7V to 5.5V Logic Supply Range
- 3-Wire Serial Interface plus Chip Select
- Captures Serial & Parallel Input Data
- Outputs Can Be Paralleled
- 28-Lead QFN Package

Applications

- White Goods
- ATE
- Industrial Equipment

Description

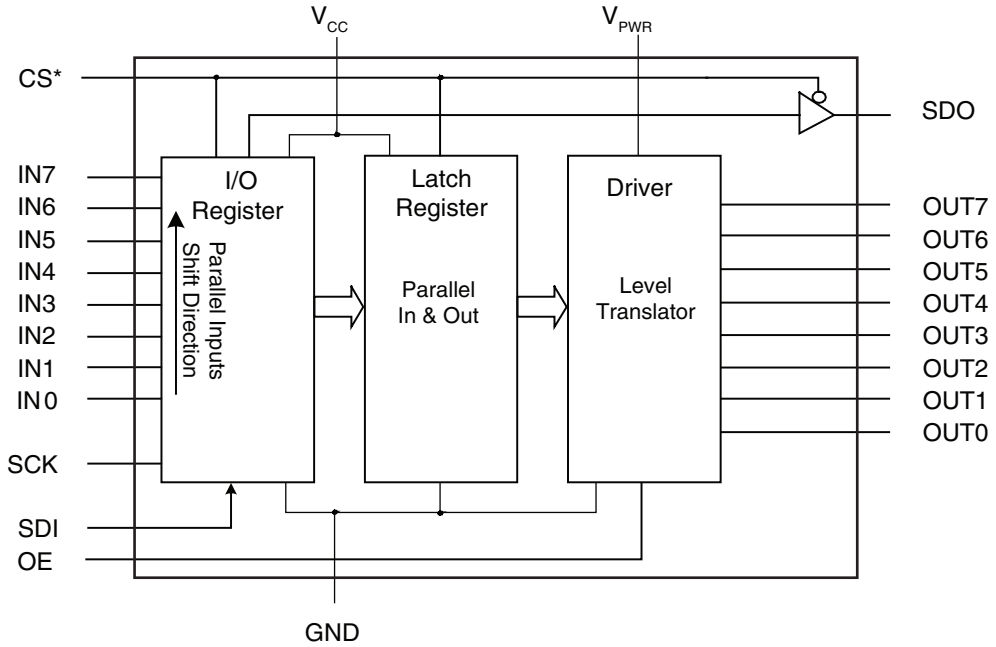
The MX877 is an 8-channel, high voltage switch with 8-bit parallel or serial input control. The MX877 connects directly to a microprocessor through a standard 3-wire serial interface. The push-pull output configuration can drive up to 60 volts at 80mA. Outputs can be paralleled for increased drive current up to a device total of 400mA, sink or source.

The MX877 is designed to operate over a temperature range of -40°C to +85°C, and is available in a 28-lead QFN Package.

Ordering Information

Part	Description
MX877R	QFN-28 (73/Tube)
MX877RTR	QFN-28 Tape & Reel (2500/Reel)

Functional Block Diagram



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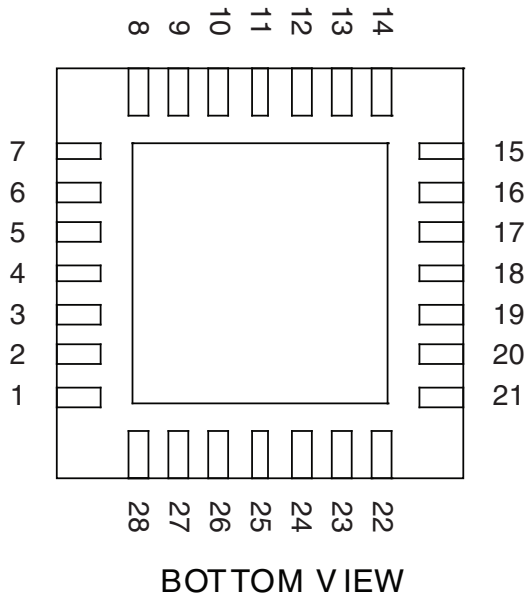
1 Specifications

1.1 Package Pinout



BOTTOM VIEW

1.2 Pin Description

Pin#	Name	Description
1	OUT7	Parallel Output
2	N/C	No Connection
3	GND	Ground
4	V_{PWR}	High Voltage Supply (6V to 60V)
5	N/C	No Connection
6	V_{CC}	Logic Supply (2.7V to 5.5V)
7	SDO	Serial Data Output
8	IN7	Parallel Input
9	IN6	Parallel Input
10	IN5	Parallel Input
11	IN4	Parallel Input
12	IN3	Parallel Input
13	IN2	Parallel Input
14	IN1	Parallel Input
15	IN0	Parallel Input
16	SCK	Serial Clock
17	V_{PWR}	High Voltage Supply (6V to 60V)
18	SDI	Serial Data Input
19	CS*	Chip Select (Active Low)
20	OE	Output Enable
21	GND	Ground
22	OUT0	Parallel Output
23	OUT1	Parallel Output
24	OUT2	Parallel Output
25	OUT3	Parallel Output
26	OUT4	Parallel Output
27	OUT5	Parallel Output
28	OUT6	Parallel Output

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
V_{PWR} Supply Voltage	V_{PWR}	-	60	V
Logic Supply Voltage	V_{CC}	-	6	V
Input Pin Voltage	VIN	-	6	V
Continuous Output Current OUT0 - OUT7	I_{OUTn}	-	±100	mA
Operating Junction Temperature	T_J	-	150	°C
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	110 Typical		°C/W
Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{STG}	-55	150	°C

Absolute maximum electrical ratings are at 25°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

Voltages with respect to GND=0V.

ESD Warning: *ESD (electrostatic discharge) sensitive device. Although the MX877 features proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.*

1.4 DC Electrical Characteristics

V_{CC}=5V, V_{PWR}=42V, T_A=25°C, unless otherwise specified.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Logic Supply Voltage	-	V_{CC}	2.7	-	5.5	V
Logic Supply Current	f_{SCK}=5MHz	I_{CC}	-	50	-	µA
Quiescent Logic Supply Current	f_{SCK}=0	I_{CC}	-	-	1	µA
V_{PWR} Voltage	-	V_{PWR}	6	-	60	V
V_{PWR} Current	Total of all Outputs	I_{PWR}	-	-	400	mA
GND Current	Total of all Outputs	-	-	-	400	mA
Quiescent V_{PWR} Current	V_{PWR}=42V, No Load	I_{PWR}	-	0.75	-	mA
High Level Input Voltage	IN0-IN7, SCK, SDI, OE, CS*	V_{IH}	V_{CC}-0.5	-	-	V
Low Level Input Voltage	-	V_{IL}	-	-	0.5	V
Input Leakage Current	-		-	-	1	µA
SDO Tri-State Leakage Current	CS*=Logic High		-	-	1	µA
OUT0-OUT7 Current	Any One Output, Sink or Source	I_{OUTn}	-	-	±80	mA
OUT0-OUT7 ON Resistance	V_{PWR}=42V	R_{OUTn}	-	9	-	Ω
OUT0-7 Tri-State Leakage Current	OE=Logic Low	I_{OUTn}	-	-	1	µA

Notes: To avoid unwanted output during V_{PWR} application and system initialization, keep OE at a logic low until CS* has completed one cycle.

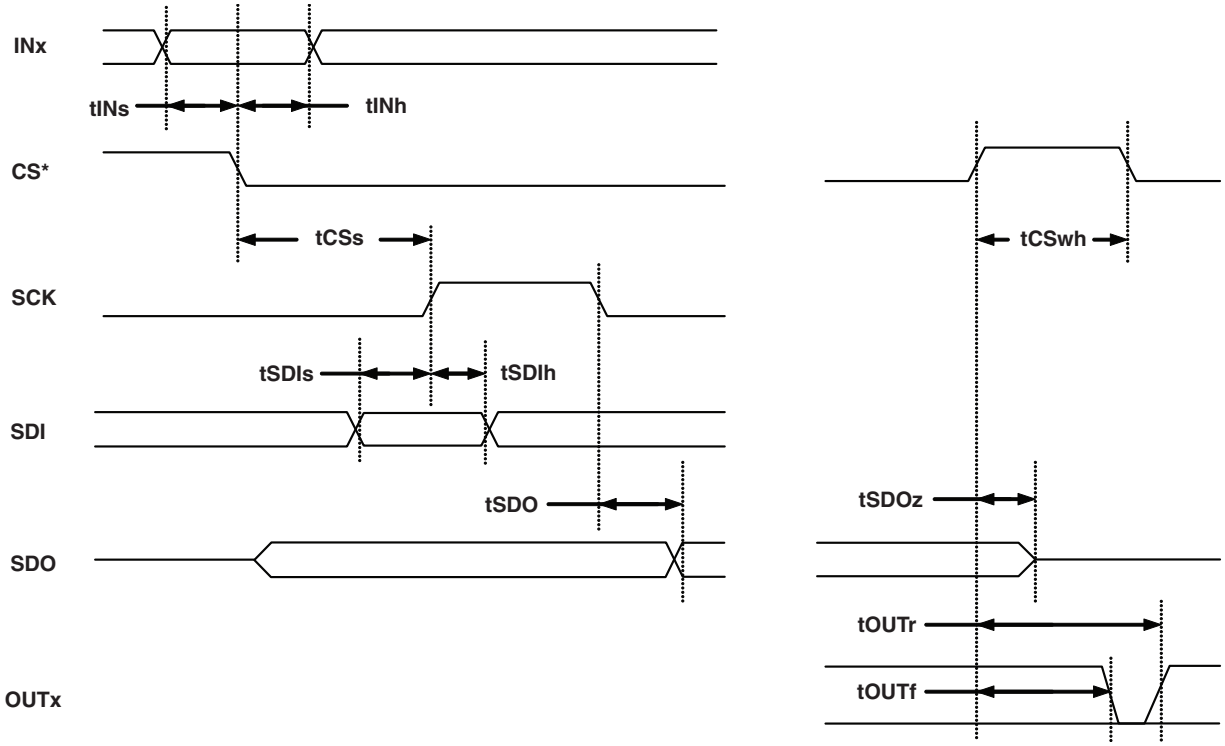
Thermal Resistance is measured in still air with the device soldered to a 6 square inch board without a ground plane. Applications may require derating of the specified maximum currents to avoid exceeding the maximum operation junction temperature.

1.5 Dynamic Electrical Characteristics

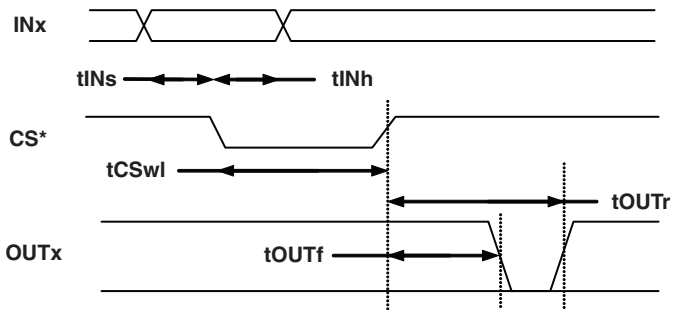
V_{CC}=5V, V_{PWR}=42V, T_A=25°C, unless otherwise specified.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
SCK Period	-	-	100	-	DC	ns
SCK High Time	-	-	40	-	-	ns
SCK Low Time	-	-	40	-	-	ns
CS* High Time	-	tCSwh	50	-	-	ns
CS* Falling to SCK Rising	Setup Time	tCSs	150	-	-	ns
CS* Low Time	SCK Low (Parallel Input Mode)	tCSwl	150	-	-	ns
INx to CS Falling (SETUP TIME)	-	tINs	15	-	-	ns
INx to CS Falling (HOLD TIME)	-	tINh	30	-	-	ns
SDI to SCK Rising (SETUP TIME)	-	tSDIs	20	-	-	ns
SDI to SCK Rising (HOLD TIME)	-	tSDIh	25	-	-	ns
SCK Falling to to SDO Data Valid	-	tSDO	-	10	-	ns
CS* Rising to SDO High Z	-	tSDOz	-	12	-	ns
CS* Rising to OUTx Rising	To 50%, C(OUTx)=1000pF	tOUTr	-	750	-	ns
CS* Rising to OUTx Falling	To 50%, C(OUTx)=1000pF	tOUTf	-	570	-	ns
OUTx Rise Time	From 10% to 90%, C(OUTx)=1000pF	-	-	110	-	ns
OUTx Fall Time	From 10% to 90%, C(OUTx)=1000pF	-	-	75	-	ns
OE Rising to OUTx Rising	To 90%	-	-	580	-	ns
OE Rising to OUTx Falling	To 90%	-	-	390	-	ns
OE Falling to OUTx High Z	To 10%, OUTx High	-	-	130	-	ns
	To 10%, OUTx Low	-	-	90	-	ns

1.6 Serial Timing



1.7 Parallel Timing



2 Functional Description

The MX877 is an 8 channel high voltage driver with 8-bit input control. The MX877 interfaces to a microprocessor through a standard 3 wire serial interface and an active-low chip select, or can be used in a parallel-in, parallel-out configuration.

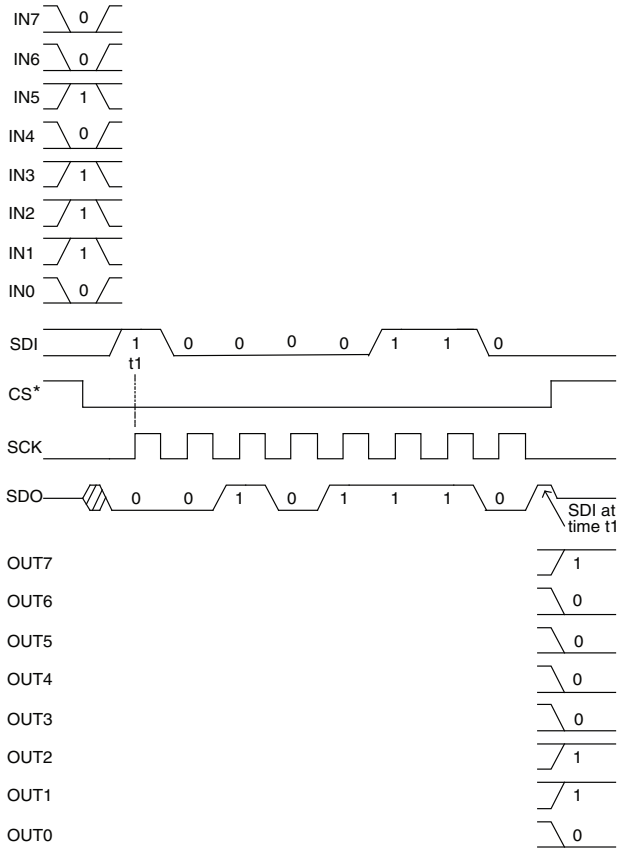
Parallel data is transferred to the I/O register of the MX877 through the parallel input pins, IN0 through IN7 on the falling edge of the chip select pin, CS*. When CS* is in a logic low state, serial data can be transferred to the I/O register through the serial input pin, SDI, and from the I/O register through the serial output pin, SDO. Parallel or serial input data is transferred from the I/O register to the latch and high voltage output drivers, OUT0 through OUT7, on the positive edge of CS*. This data remains latched until the next positive edge of CS*.

The 8-bit I/O shift register is clocked by the serial clock pin, SCK. Serial data presented at the SDI pin is transferred to the shift register on the positive edge of SCK. Data shifts out of the register through the SDO pin on the negative edge of SCK. SDI and SCK are ignored, and SDO transitions to a high impedance condition when CS* is at a logic high state.

Serial data is received by the MX877 through the SDI pin. This data is accepted on the rising edge of SCK. A specific output is programmed to a logic high state if SDI is at a logic high state during the rising edge of SCK. Conversely, a specific output is programmed to a logic low state if SDI is at a logic low state during the rising edge of SCK. Outputs transition to their programmed states on the positive edge of CS* if the output enable pin, OE is in a logic high state.

The MSB input data (IN7) is presented at the serial output pin, SDO on the falling edge of CS*. Input data from IN6 through IN0 is sequentially presented at SDO on negative SCK transitions if CS* remains in a logic low state. If CS* is at a logic low state beyond 8 cycles of SCK, SDI data that has propagated through the I/O register will then be presented at SDO. The SDO pin transitions to a high impedance state when CS* is in a logic level high state, thus allowing multiple serial peripherals to share the microprocessor data pin.

Figure 1. Serial Data Transfer Example



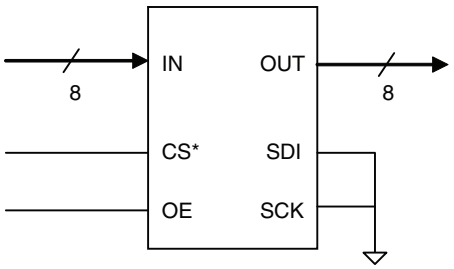
Devices may be serially cascaded by connecting SDO to SDI of the next device. Pins SCK and CS* are common to all devices in serial cascade. For n-cascaded devices the CS* should remain low for 8n cycles of SCK.

An output enable pin, OE enables the driver outputs OUT0 through OUT7 when logic high. A logic low level on OE forces the OUT0 through OUT7 outputs to a high impedance state.

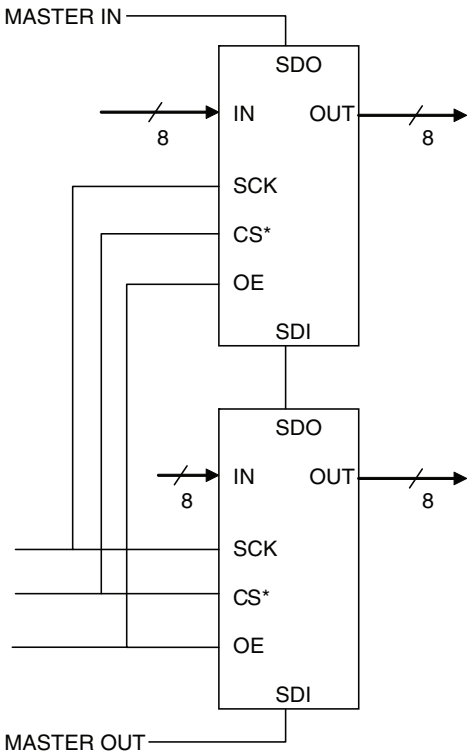
The MX877 can also operate as a parallel-in, parallel-out level shifter and driver. SCK must remain at a logic low state when operating in this mode. Parallel input data presented to IN0 through IN7 is captured on the falling edge of CS*. This data is transferred to OUT0 through OUT7 on the rising edge of CS*, and remains latched until the next rising edge of CS*.

3 Application Examples

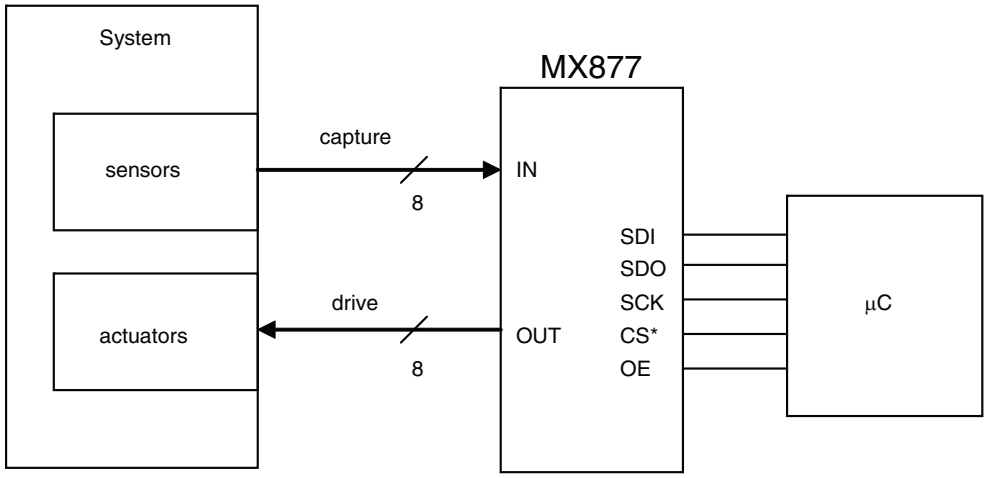
3.1 Parallel In / Parallel Out Application



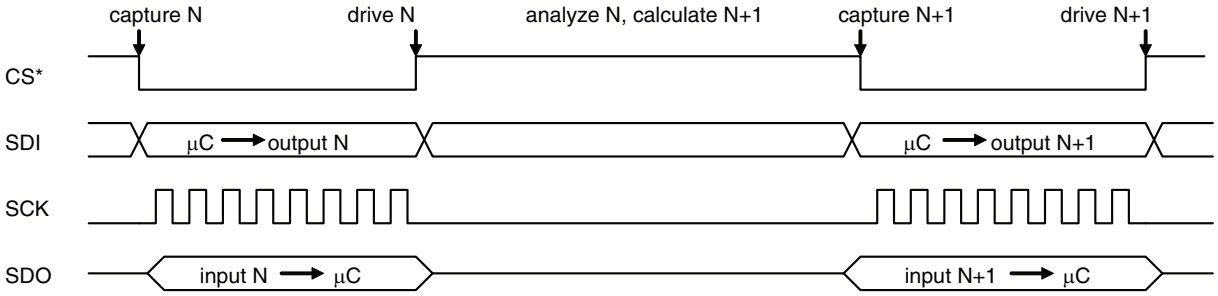
3.2 Serial Cascade Application



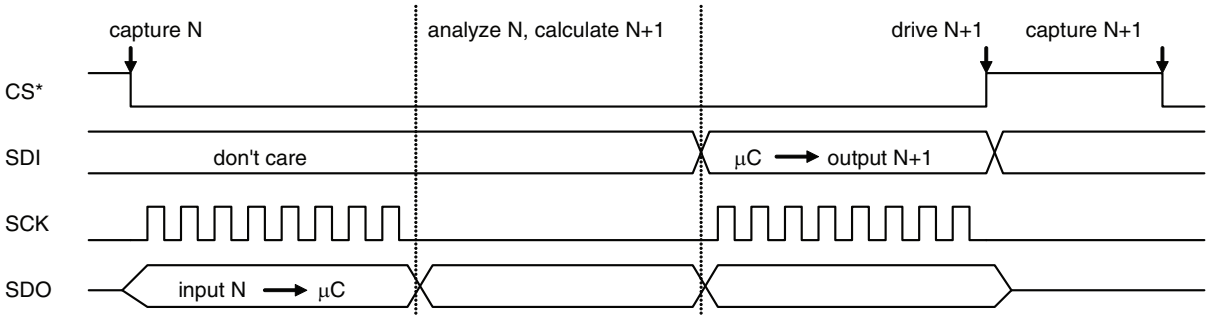
3.3 Control System Application



Type 1 timing:



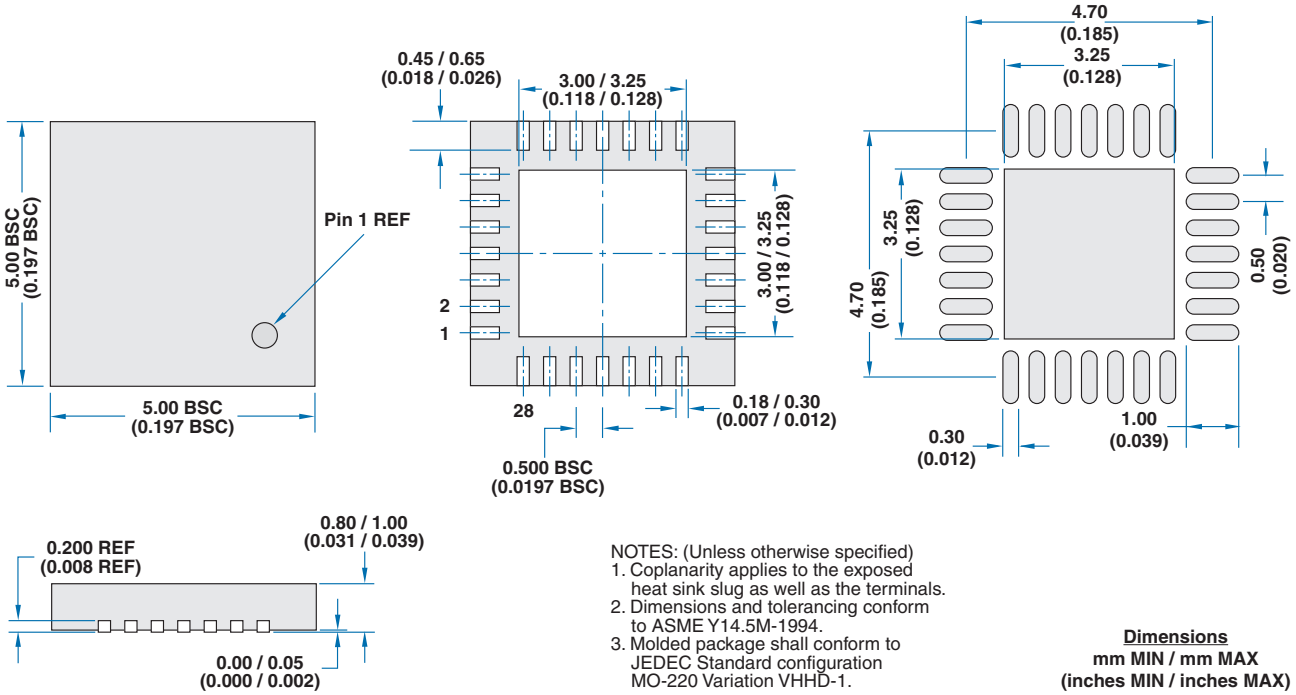
Type 2 timing:



4 Manufacturing Information

4.1 Mechanical Dimensions

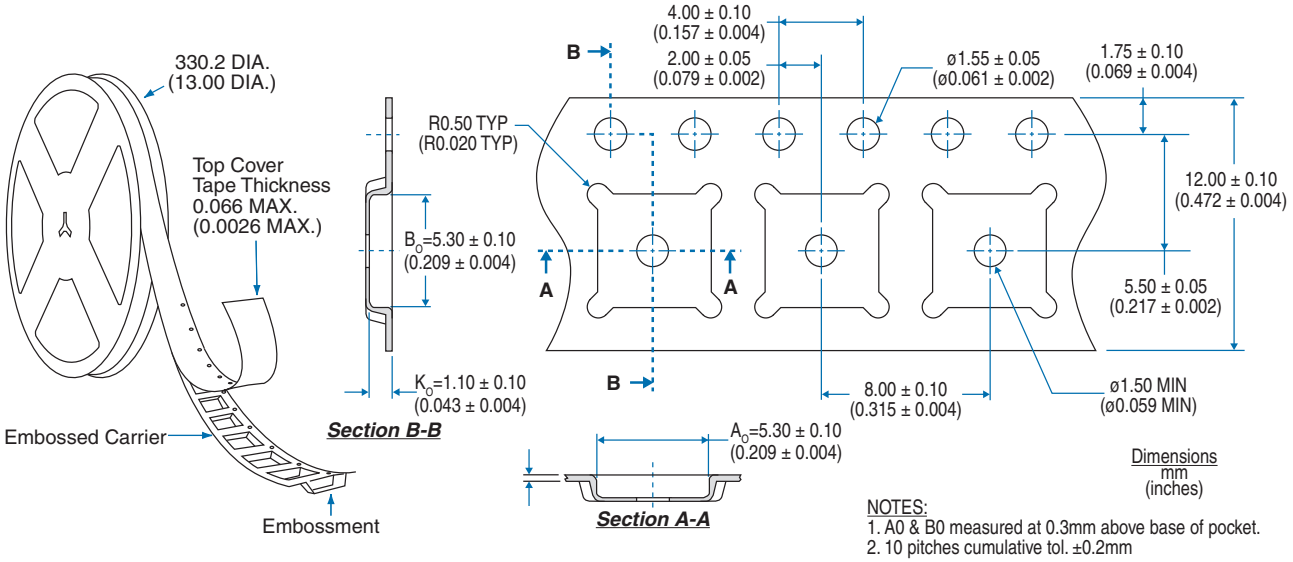
4.1.1 QFN-28 Package & Recommended PCB Land Pattern



NOTES: (Unless otherwise specified)
1. Coplanarity applies to the exposed heat sink slug as well as the terminals.
2. Dimensions and tolerancing conform to ASME Y14.5M-1994.
3. Molded package shall conform to JEDEC Standard configuration MO-220 Variation VHHD-1.

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

4.1.2 Tape & Reel Dimensions



Dimensions
mm
(inches)

NOTES:
1. A0 & B0 measured at 0.3mm above base of pocket.
2. 10 pitches cumulative tol. ±0.2mm

4.2 Soldering

For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

4.3 Washing

Clare does not recommend ultrasonic cleaning or the use of chlorinated hydrocarbons.

For additional information please visit our website at: www.clare.com

Specification: DS-MX877-R00B

12/17/09