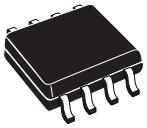
VN751S

High side driver

Features

Type	$R_{DS(on)}$	I_{out}	V_{CC}
VN751S	60 mΩ	2.5 A	36 V

- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output

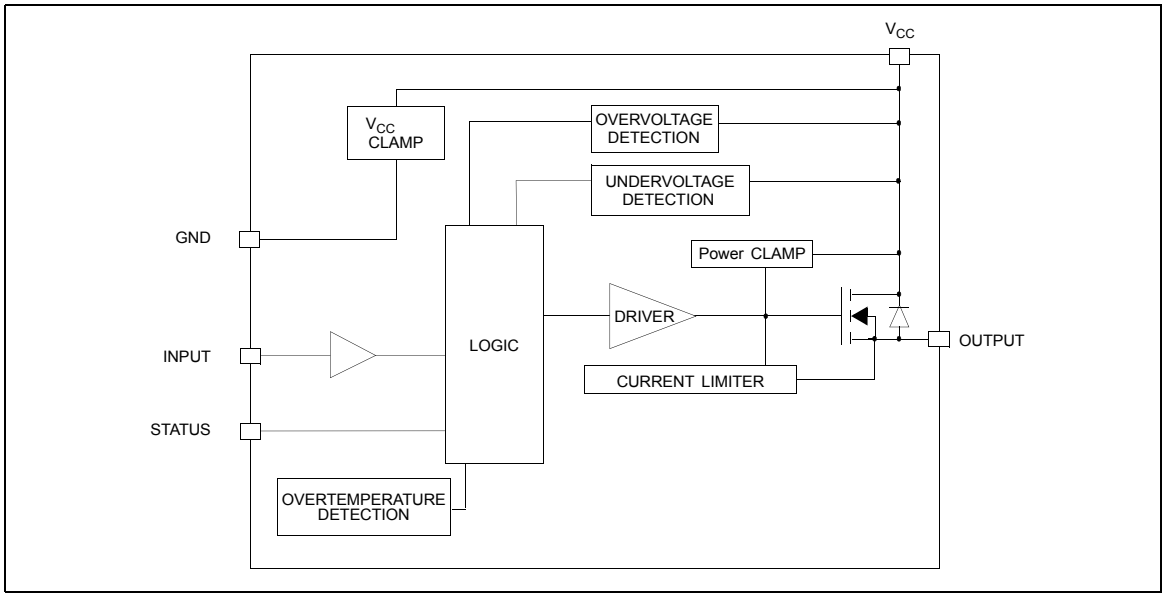


SO-8

Description

The VN751S is a monolithic device designed in STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controllers international standard.

Figure 1. Block diagram



Contents

1 Maximum ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (overvoltage protected)	45	V
- V_{CC}	Reverse DC supply voltage	-0.3	V
- I_{GND}	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	-5	A
I_{IN}	DC input current	+/- 10	mA
I_{STAT}	DC status current	+/- 10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	5000	V
P_{tot}	Power dissipation T_C = 25 °C	Internally limited	W
T_J	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C
E_{AS}	Single-pulse avalanche energy	0.8	J

Table 2. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Thermal resistance junction-ambient	Max	93(1)	°C/W
			82(2)	°C/W
R_{thJC}	Thermal resistance junction-case	Max	15	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35µm) thick connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 2 cm^2 of Cu (at least 35µm) thick connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2 Pin connections

Figure 2. Connection diagram (top view)

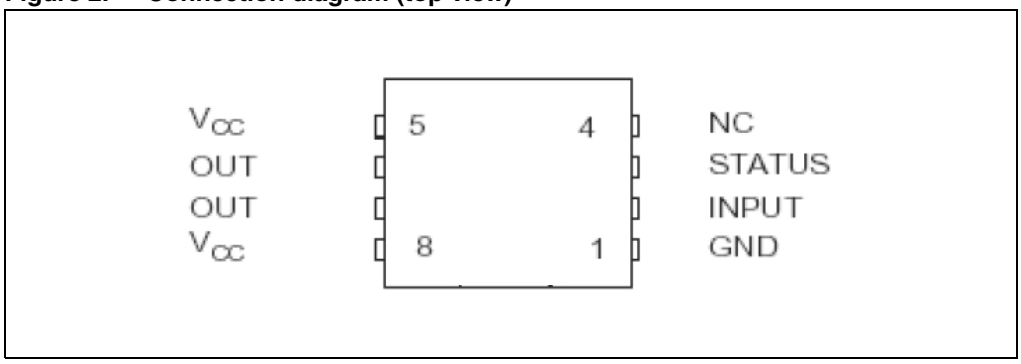
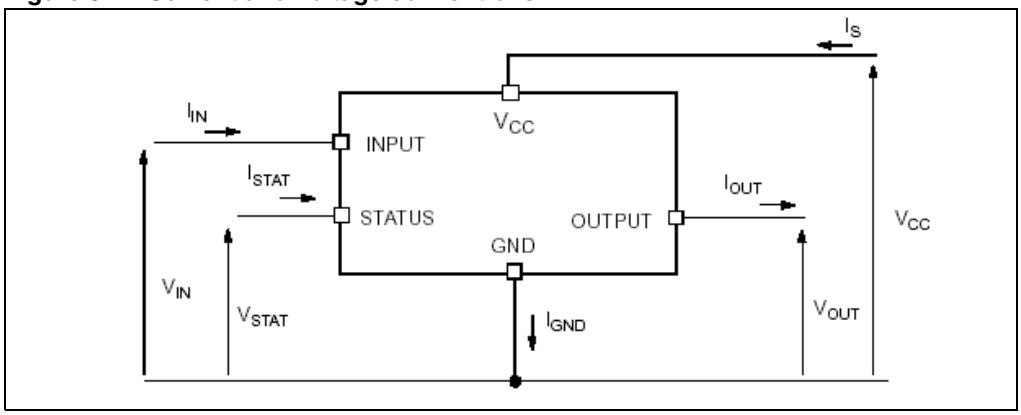


Figure 3. Current and voltage conventions



3 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified

Table 3. Power

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5		36	V
V_{USD}	Undervoltage shut-down		3	4	5.5	V
V_{OV}	Overvoltage shut-down		36			V
R_{ON}	On state resistance	I_{OUT} = 2 A; T_J = 25 °C I_{OUT} = 2 A		60	 180	mΩ mΩ
I_S	Supply current	Off state; V_{CC} = 24 V; T_{CASE} =25 °C On state; V_{CC} = 24 V On state; V_{CC} = 24 V;T_{CASE} =100 °C		10 1.5	20 1.8	µA mA mA
$I_{L(off)}$	Off state output current	V_{IN} = V_{OUT} = 0 V	0		10	µA

Table 4. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 12 Ω from V_{IN} rising edge to V_{OUT} = 2.4 V		12		µs
$t_{d(off)}$	Turn-off delay time	R_L = 12 Ω from V_{IN} falling edge to V_{OUT} = 21.6 V		35		µs
$dV_{OUT}/dt_{(on)}$	Turn -on voltage slope	R_L = 12Ω from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V		0.80		V/µs
$dV_{OUT}/dt_{(off)}$	Turn -off voltage slope	R_L = 12 Ω from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V		0.30		V/µs

Table 5. Input pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
I_{IN}	Input current	$V_{IN} = V_{CC}$ = 5 V			10	µA
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = -1 mA	6	6.8 -0.7	8	V V

Table 6. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA; I_{STAT} =-1 mA	6	6.8 -0.7	8	V V

Table 7. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	20		°C
I_{lim}	Current limitation	V_{CC} = 24 V, R_{LOAD} = 10 mΩ, t = 0.4 ms	2.7		6.0	A
V_{demag}	Turn-off output clamp voltage	R_L =12 Ω; L = 6 mH	V_{CC}-47	V_{CC}-52	V_{CC}-57	V

4 Waveforms and truth table

Figure 4. Switching time waveforms

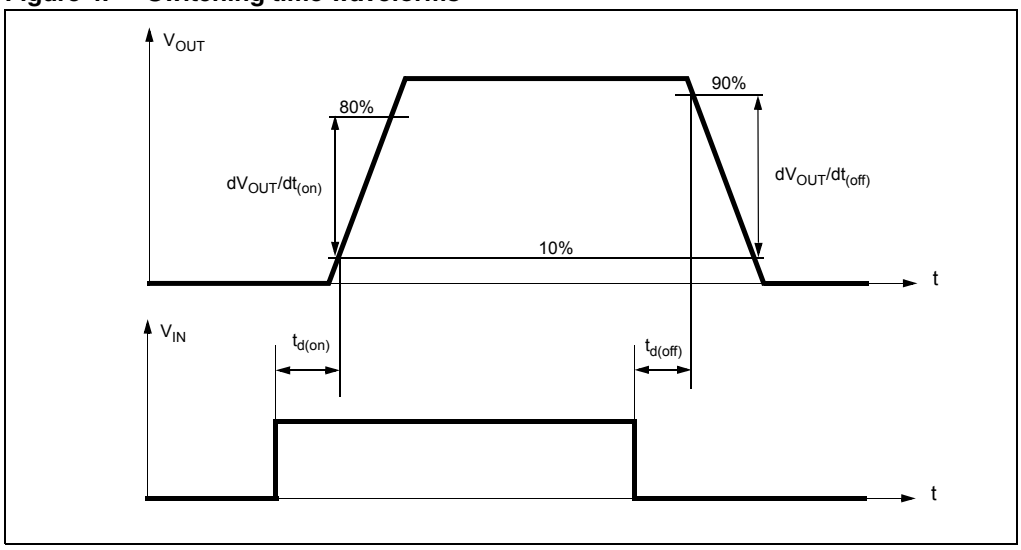
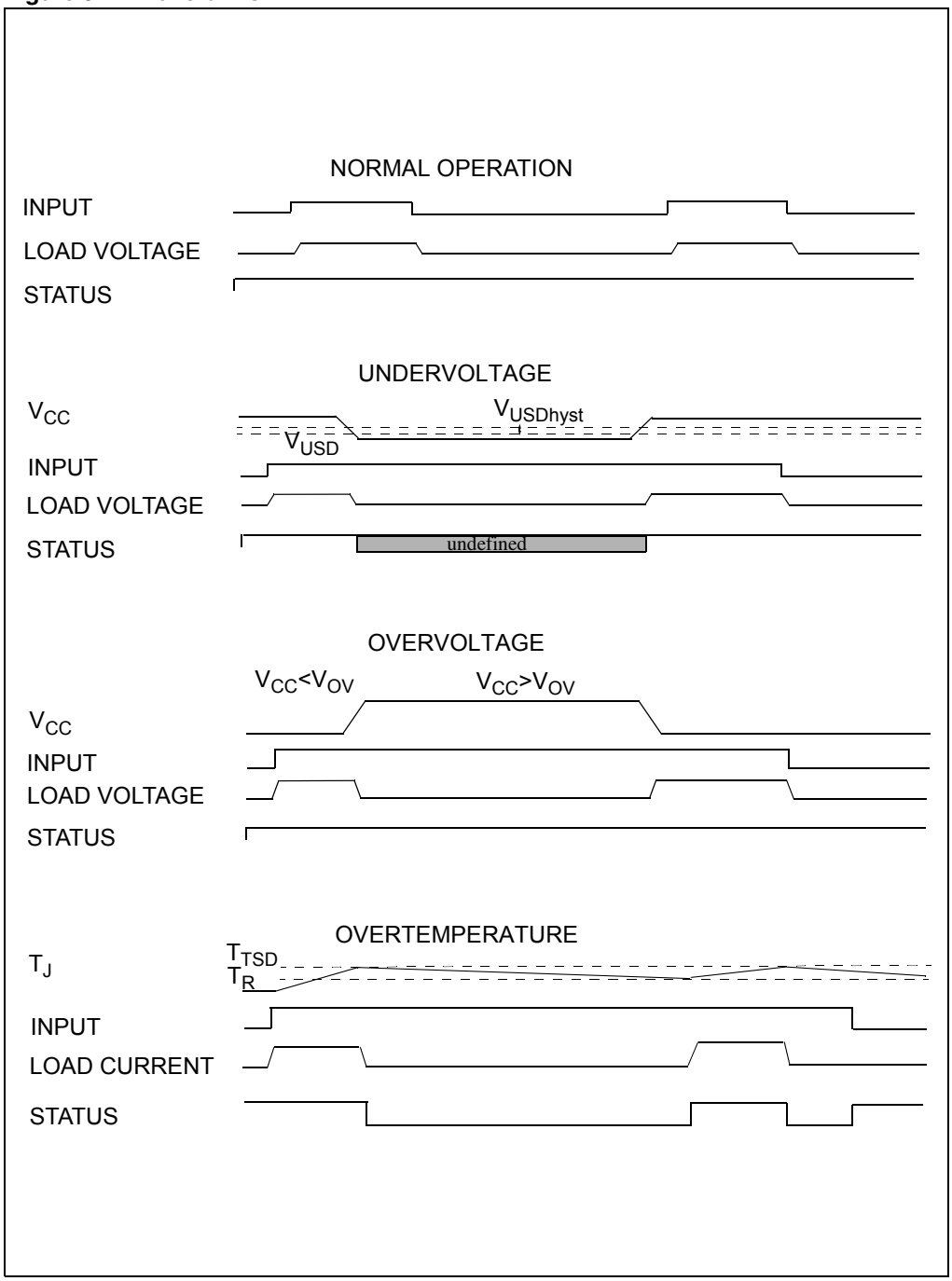


Table 8. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_J < T_{TSD}$) H ($T_J > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H

Figure 5. Waveforms



5 Test circuit

Figure 6. Peak short circuit current test circuit

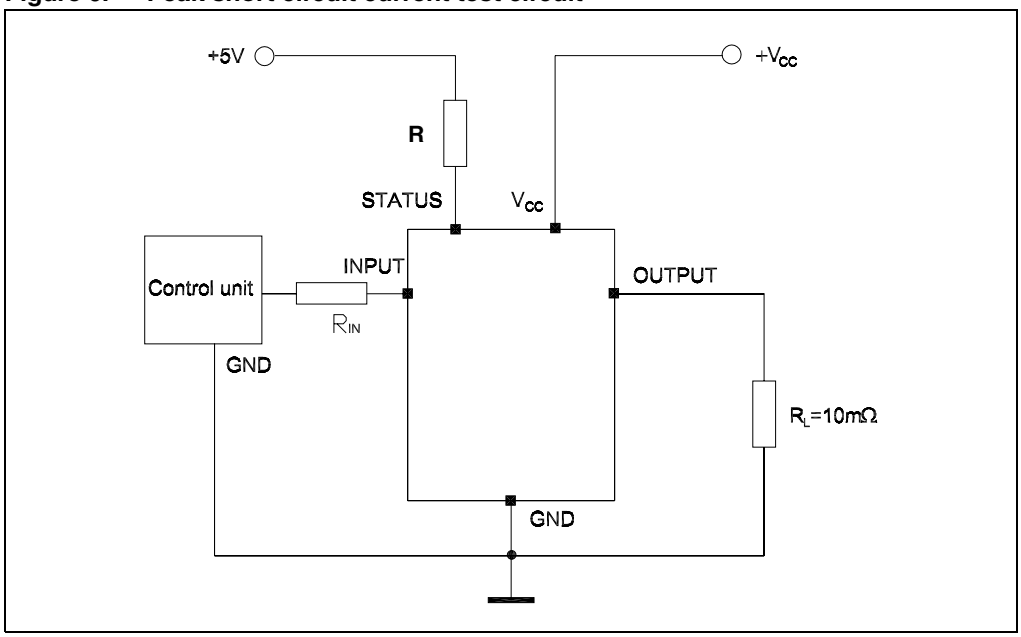
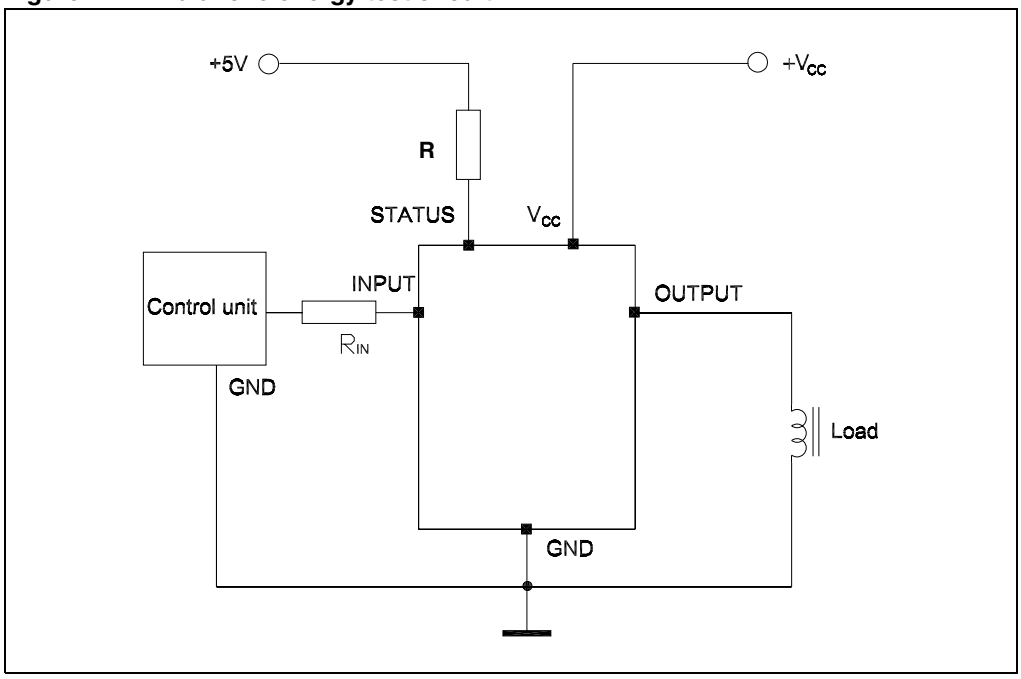
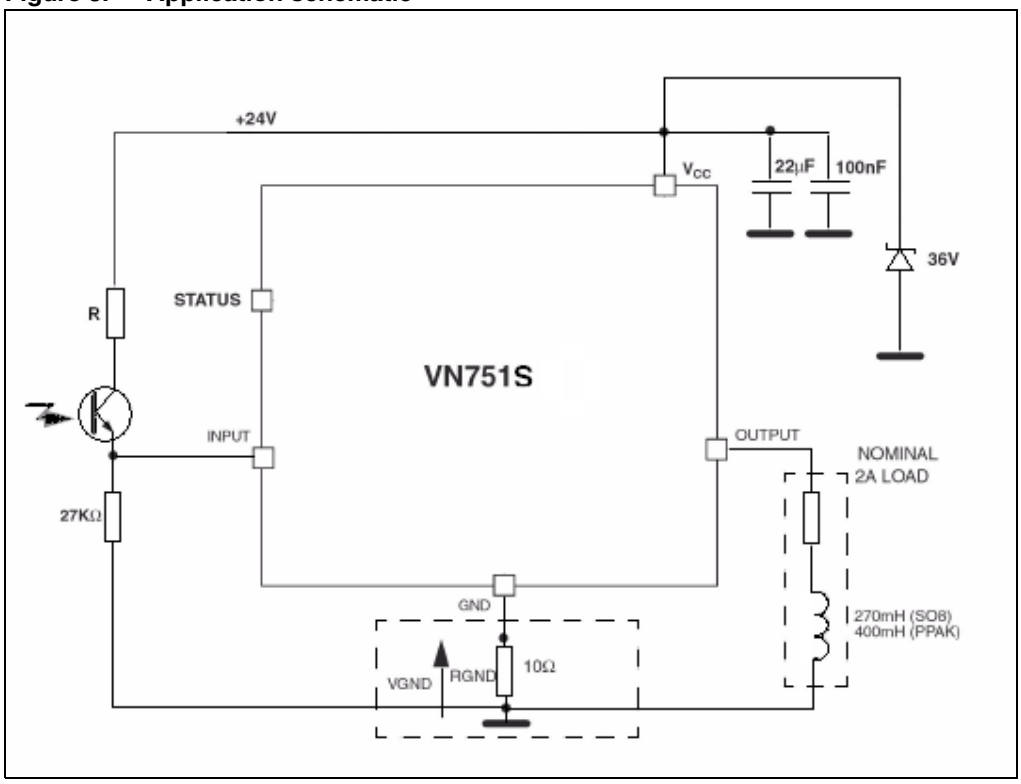


Figure 7. Avalanche energy test circuit



6 Application schematic

Figure 8. Application schematic



7 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC.

The RGND resistor value can be selected according to the following conditions to be met:

$R_{GND} \leq 600\ mV / (I_S$ in ON state max).

$R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -IGND is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

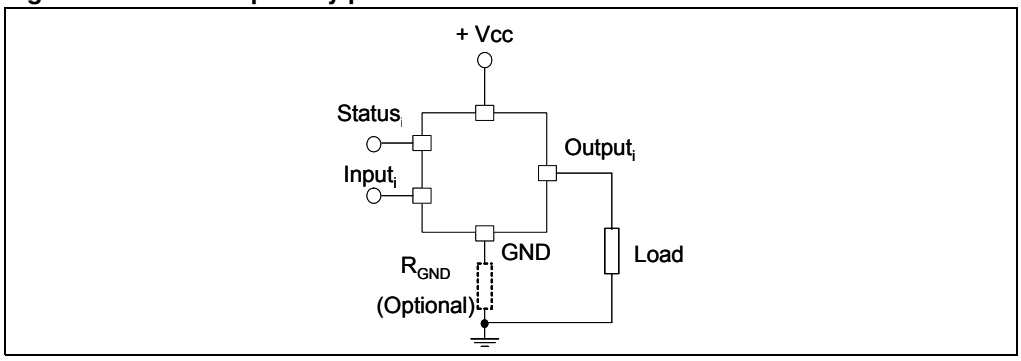
The power dissipation associated to R_{GND} during reverse polarity condition is:

$PD = (-V_{CC})^2/R_{GND}$

This resistor can be shared by several different ICs. In such case I_S value on formula (1) is the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground and the device ground are separated then the voltage drop across the R_{GND} (given by I_S in ON state max * R_{GND}) produce a difference between the generated input level and the IC input signal level. This voltage drop will vary depending on how many devices are ON in the case of several high side switches sharing the same R_{GND}.

Figure 9. Reverse polarity protection



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
ECOPACK is an ST trademark.

Table 9. SO-8 mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8º (max.)					

Figure 10. Package dimensions

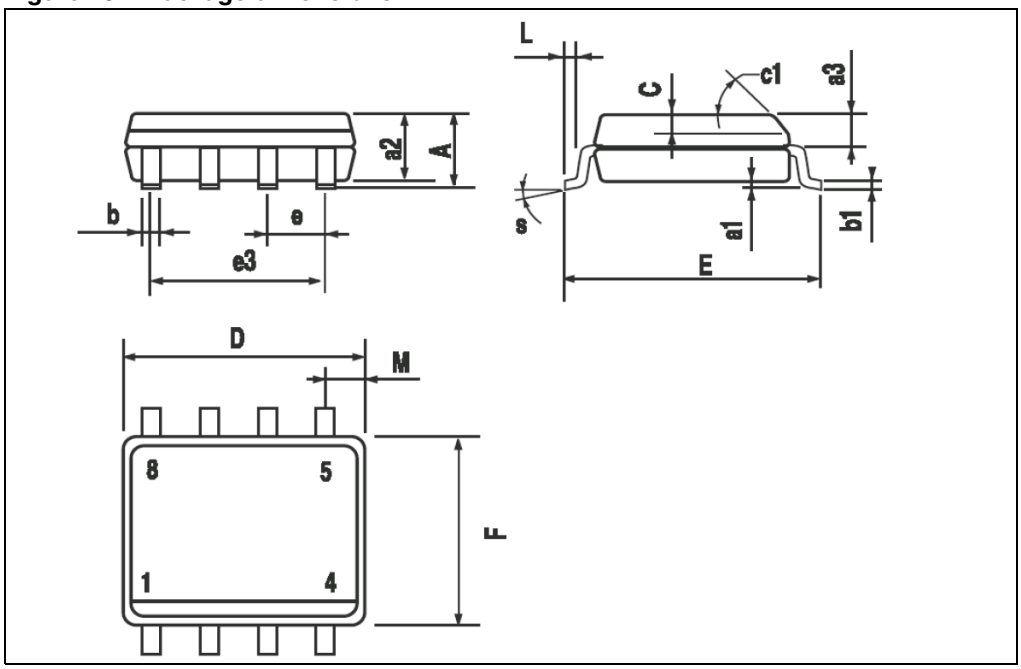
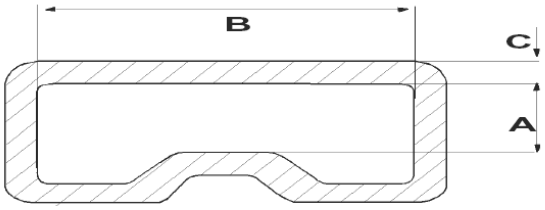
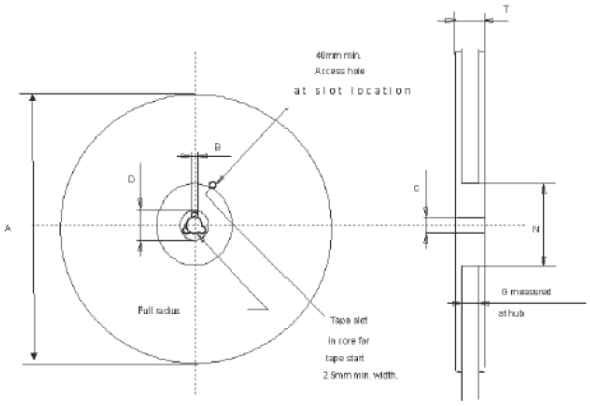


Figure 11. SO-8 tape and reel information



Base Q.ty	100
Bulk Q.ty	2000
Tube Length(± 0.5)	532
A	3.2
B	6
C(± 0.1)	0.6



Reel Dimension

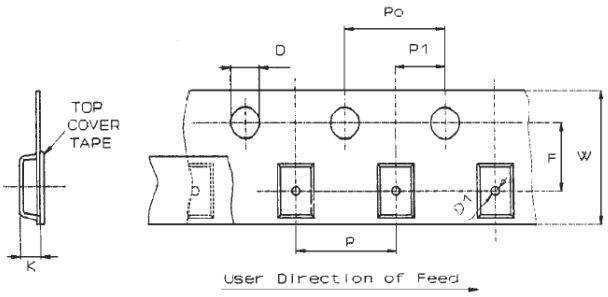
Base Q.ty	2500
Bulk Q.ty	2500
A(Max)	330
B(Min)	1.5
C(± 0.2)	13
F	20.2
G(+2/-0)	12.4
N(Min)	60
T(Max)	18.4

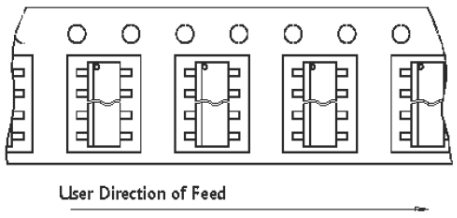
Tape Dimension

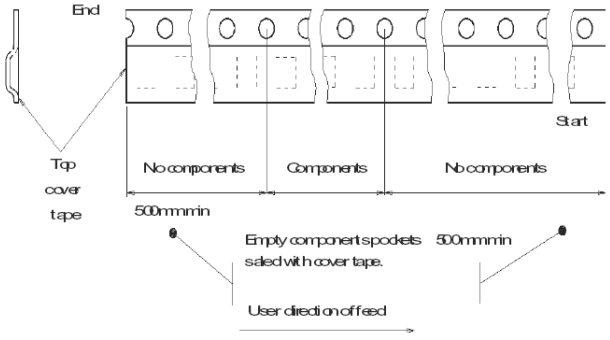
According to Electronic Industries Association(EIA) Standard 481 rev. A, Feb 1986

Tape Width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D(± 0.2/-0)	1.5
Hole Diameter	D1(Min)	1.5
Hole Position	F(± 0.05)	5.5
Compartament Depth	K(Max)	4.5
Hole Spacing	P1(± 0.1)	2

All dimension are in mm.







9 Order code

Table 10. Order codes

Order codes	Package	Packaging
VN751S	SO-8	Tube
VN751STR	SO-8	tape and reel

10 Revision history

Table 11. Document revision history

Date	Revision	Changes
18-Sep-2006	1	Initial release
12-Mar-2007	2	Document reformatted, typo in *Section Table 3.: Power on page 5*, updated P_{tot} value *Table 2*.
15-May-2007	3	Typo in *Table 1 on page 3* V_{ESD}
18-Sep-2007	4	Added I_{STAT} value in *Table 1 on page 3*
11-Oct-2007	5	Updated *Table 2 on page 3*
08-Jul-2008	6	Added *Section 7 on page 10*
30-Nov-2009	7	Updated coverpage and *Chapter 6 on page 10*

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