

## FEATURES

- Wide Operating  $V_{IN}$  Range: Up to 80V
- Rugged Architecture Tolerant of 100V  $V_{IN}$  Transients
- Powerful  $1.5\Omega$  Driver Pull-Down
- Powerful 2.4A Peak Current Driver Pull-Up
- 7ns Fall Time Driving 1000pF Load
- 10ns Rise Time Driving 1000pF Load
- Drives Standard Threshold MOSFETs
- TTL/CMOS Compatible Inputs with Hysteresis
- Input Thresholds are Independent of Supply
- Undervoltage Lockout
- Low Profile (1mm) SOT-23 (ThinSOT)<sup>™</sup> and Thermally Enhanced 8-Pin MSOP Packages

## APPLICATIONS

- Telecommunications Power Systems
- Distributed Power Architectures
- Server Power Supplies
- High Density Power Modules

## DESCRIPTION

The LTC<sup>®</sup>4440 is a high frequency high side N-channel MOSFET gate driver that is designed to operate in applications with  $V_{IN}$  voltages up to 80V. The LTC4440 can also withstand and continue to function during 100V  $V_{IN}$  transients. The powerful driver capability reduces switching losses in MOSFETs with high gate capacitances. The LTC4440's pull-up has a peak output current of 2.4A and its pull-down has an output impedance of  $1.5\Omega$ .

The LTC4440 features supply independent TTL/CMOS compatible input thresholds with 350mV of hysteresis. The input logic signal is internally level-shifted to the bootstrapped supply, which may function at up to 115V above ground.

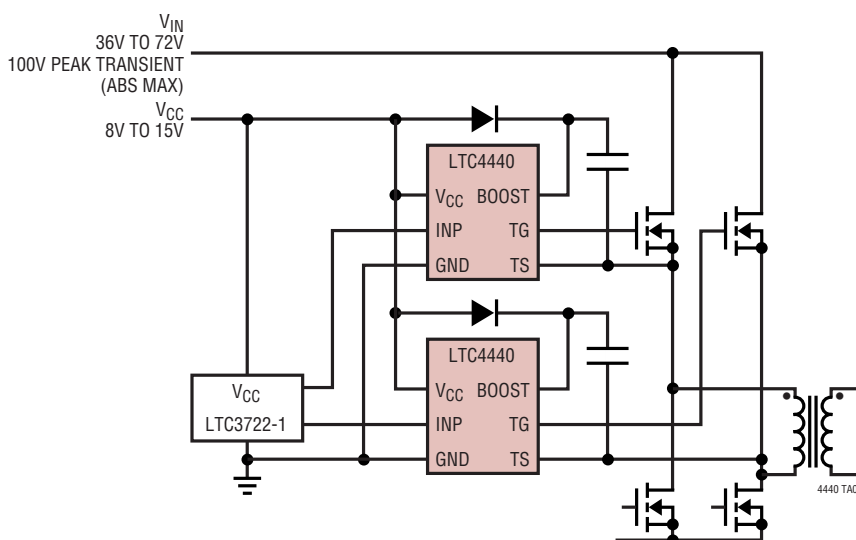
The LTC4440 contains both high side and low side undervoltage lockout circuits that disable the external MOSFET when activated.

The LTC4440 is available in the low profile (1mm) SOT-23 and thermally enhanced 8-lead MSOP packages.

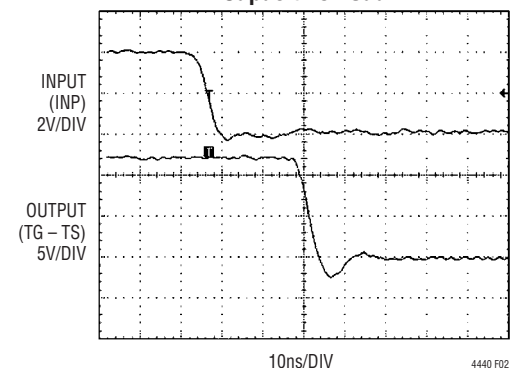
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## TYPICAL APPLICATION

Synchronous Phase-Modulated Full-Bridge Converter



LTC4440 Driving a 1000pF Capacitive Load



# LTC4440

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage		Peak Output Current < 1 $\mu$ s (TG) .....	4A
$V_{CC}$ .....	-0.3V to 15V	Driver Output TG (with Respect to TS) .....	-0.3V to 15V
BOOST – TS .....	-0.3V to 15V	Operating Ambient Temperature Range	
INP Voltage .....	-0.3V to 15V	(Note 2) .....	-40°C to 85°C
BOOST Voltage (Continuous) .....	-0.3V to 95V	Junction Temperature (Note 3) .....	125°C
BOOST Voltage (100ms) .....	-0.3V to 115V	Storage Temperature Range .....	-65°C to 150°C
TS Voltage (Continuous) .....	-5V to 80V	Lead Temperature (Soldering, 10 sec) .....	300°C
TS Voltage (100ms) .....	-5V to 100V		

## PACKAGE/ORDER INFORMATION

<p>MS8E PACKAGE 8-LEAD PLASTIC MSOP <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 40^{\circ}C/W</math> (NOTE 4) EXPOSED PAD IS GND (PIN 9) MUST BE SOLDERED TO PCB</p>	ORDER PART NUMBER	<p>S6 PACKAGE 6-LEAD PLASTIC SOT-23 <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 230^{\circ}C/W</math></p>	ORDER PART NUMBER
	LTC4440EMS8E		LTC4440ES6
	MS8E PART MARKING		S6 PART MARKING
	LTF9		LTZY

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{CC} = V_{BOOST} = 12V$ ,  $V_{TS} = GND = 0V$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Main Supply (<math>V_{CC}</math>)</b>						
$I_{VCC}$	DC Supply Current Normal Operation UVLO	$INP = 0V$ $V_{CC} < UVLO$ Threshold (Falling) – 0.1V		250 25	400 80	$\mu A$ $\mu A$
UVLO	Undervoltage Lockout Threshold	$V_{CC}$ Rising $V_{CC}$ Falling Hysteresis	● 5.7 ● 5.4	6.5 6.2	7.3 7.0	V V mV
<b>Bootstrapped Supply (BOOST – TS)</b>						
$I_{BOOST}$	DC Supply Current Normal Operation UVLO	$INP = 0V$ $V_{BOOST} - V_{TS} < UVLO_{HS(FALLING)} - 0.1V, V_{CC} = INP = 5V$		110 86	180 170	$\mu A$ $\mu A$
UVLO <sub>HS</sub>	Undervoltage Lockout Threshold	$V_{BOOST} - V_{TS}$ Rising $V_{BOOST} - V_{TS}$ Falling Hysteresis	● 6.75 ● 6.25	7.4 6.9	7.95 7.60	V V mV
<b>Input Signal (INP)</b>						
$V_{IH}$	High Input Threshold	INP Ramping High	● 1.3	1.6	2	V
$V_{IL}$	Low Input Threshold	INP Ramping Low	● 0.85	1.25	1.6	V
$V_{IH} - V_{IL}$	Input Voltage Hysteresis			0.350		V
$I_{INP}$	Input Pin Bias Current			$\pm 0.01$	$\pm 2$	$\mu A$

4440f

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{BOOST} = 12\text{V}$ ,  $V_{TS} = \text{GND} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Output Gate Driver (TG)</b>						
$V_{OH}$	High Output Voltage	$I_{TG} = -10\text{mA}$ , $V_{OH} = V_{BOOST} - V_{TG}$		0.7		V
$V_{OL}$	Low Output Voltage	$I_{TG} = 100\text{mA}$	●	150	220	mV
$I_{PU}$	Peak Pull-Up Current		●	1.7	2.4	A
$R_{DS}$	Output Pull-Down Resistance		●	1.5	2.2	$\Omega$
<b>Switching Timing</b>						
$t_r$	Output Rise Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		10 100		ns ns
$t_f$	Output Fall Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		7 70		ns ns
$t_{PLH}$	Output Low-High Propagation Delay		●	30	65	ns
$t_{PHL}$	Output High-Low Propagation Delay		●	28	65	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LTC4440 is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

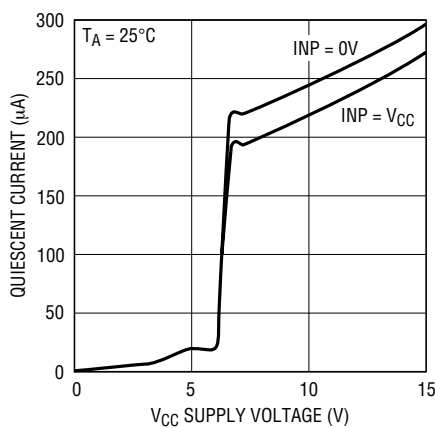
**Note 3:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation PD according to the following formula:

$$T_J = T_A + (PD \cdot \theta_{JA}^\circ\text{C/W})$$

**Note 4:** Failure to solder the exposed back side of the MS8E package to the PC board will result in a thermal resistance much higher than  $40^\circ\text{C/W}$ .

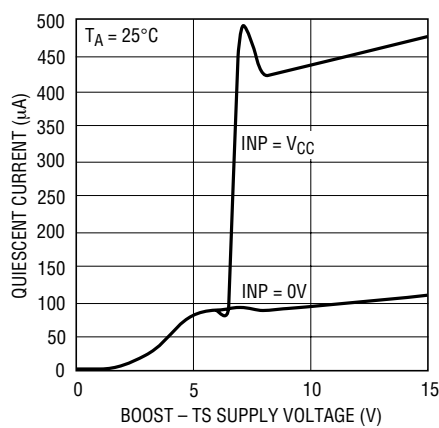
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$  Supply Quiescent Current vs Voltage**



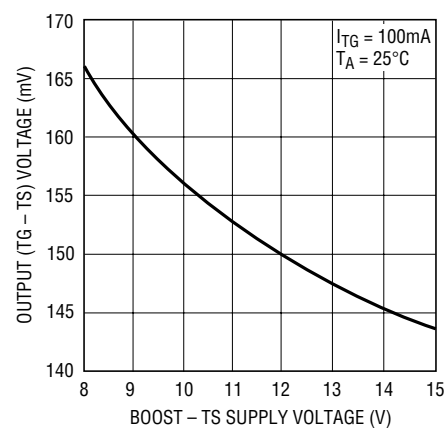
4440 G01

**BOOST – TS Supply Quiescent Current vs Voltage**



4440 G02

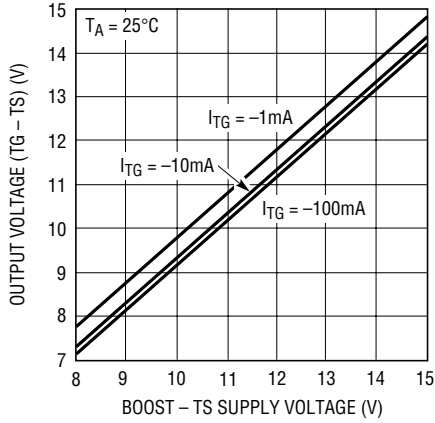
**Output Low Voltage ( $V_{OL}$ ) vs Supply Voltage**



4440 G03

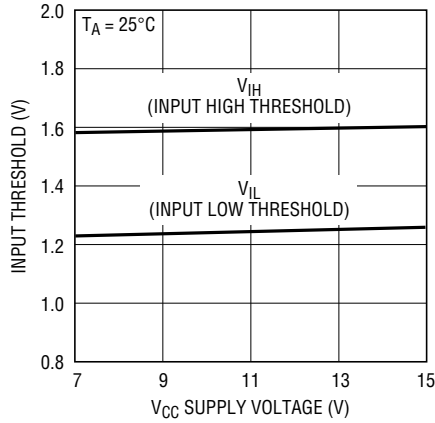
# TYPICAL PERFORMANCE CHARACTERISTICS

**Output High Voltage ( $V_{OH}$ ) vs Supply Voltage**



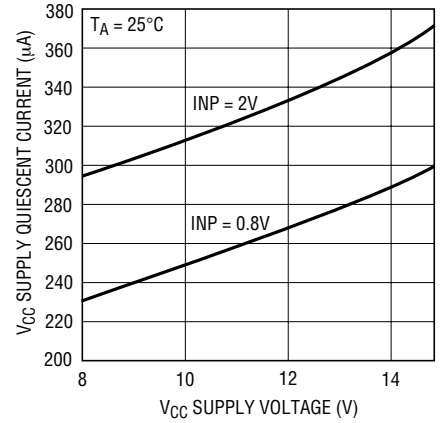
4440 G04

**Input Thresholds (INP) vs Supply Voltage**



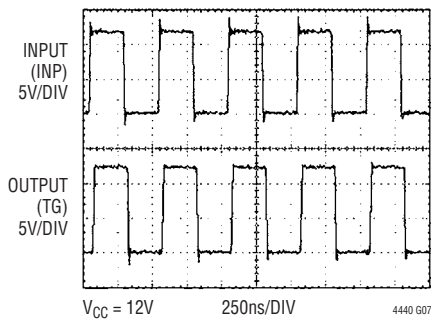
4440 G05

**$V_{CC}$  Supply Current at TTL Input Levels**



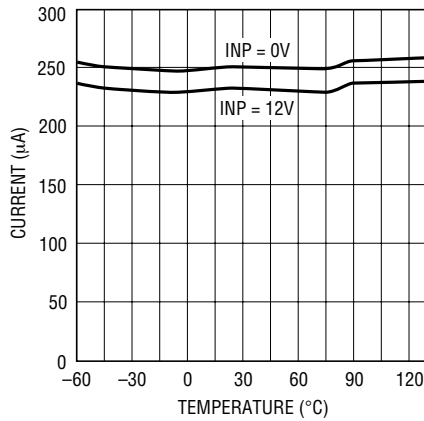
4440 G06

**2MHz Operation**



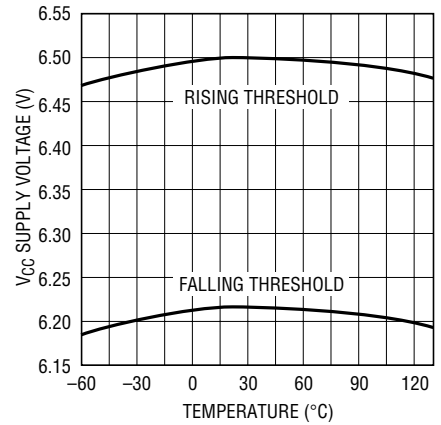
4440 G07

**$V_{CC}$  Supply Current ( $V_{CC} = 12V$ ) vs Temperature**



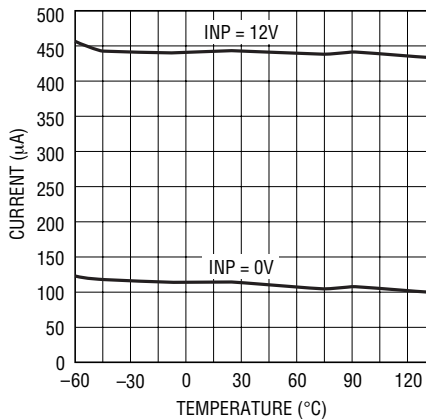
4440 G08

**$V_{CC}$  Undervoltage Lockout Thresholds vs Temperature**



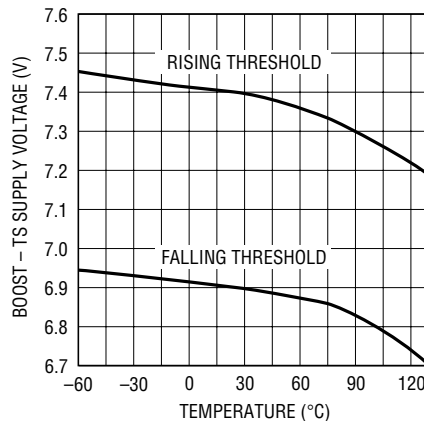
4440 G09

**Boost Supply Current vs Temperature**



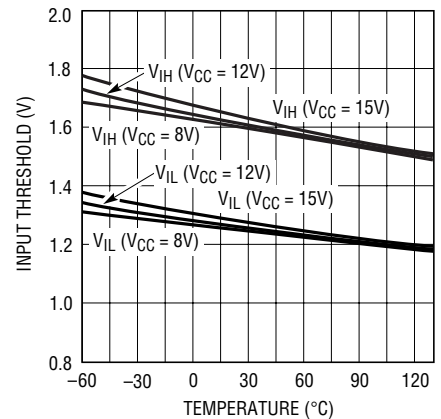
4440 G10

**Boost Supply (BOOST - TS) Undervoltage Lockout Thresholds vs Temperature**



4440 G11

**Input Threshold vs Temperature**

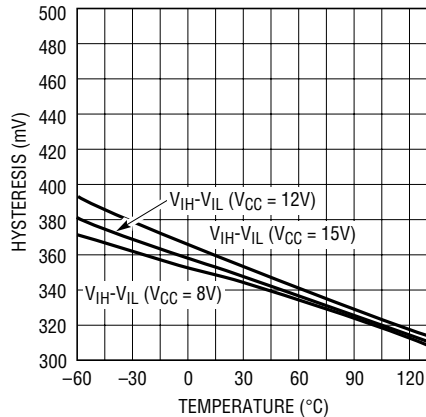


4440 G12

4440f

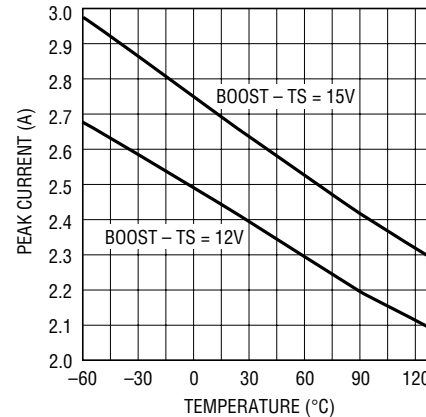
## TYPICAL PERFORMANCE CHARACTERISTICS

**Input Threshold Hysteresis vs Temperature**



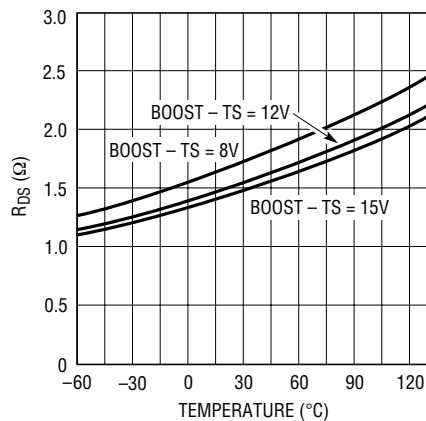
4440 G13

**Peak Driver (TG) Pull-Up Current vs Temperature**



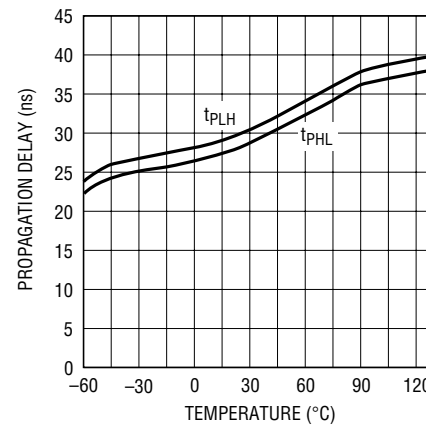
4440 G14

**Output Driver Pull-Down Resistance vs Temperature**



4440 G15

**Propagation Delay vs Temperature (V<sub>CC</sub> = BOOST = 12V)**



4440 G16

## PIN FUNCTIONS

### SOT-23 Package

**V<sub>CC</sub> (Pin 1):** Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

**GND (Pin 2):** Chip Ground.

**INP (Pin 3):** Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

**TS (Pin 4):** Top (High Side) Source Connection.

**TG (Pin 5):** High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

**BOOST (Pin 6):** High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 4). Normally, a bootstrap diode is connected between V<sub>CC</sub> (Pin 1) and this pin. Voltage swing at this pin is from V<sub>CC</sub> - V<sub>D</sub> to V<sub>IN</sub> + V<sub>CC</sub> - V<sub>D</sub>, where V<sub>D</sub> is the forward voltage drop of the bootstrap diode.

## PIN FUNCTIONS

### Exposed Pad MS8E Package

**INP (Pin 1):** Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

**GND (Pins 2, 4):** Chip Ground.

**V<sub>CC</sub> (Pin 3):** Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

**NC (Pin 5):** No Connect. No connection required. For convenience, this pin may be tied to Pin 6 (BOOST) on the application board.

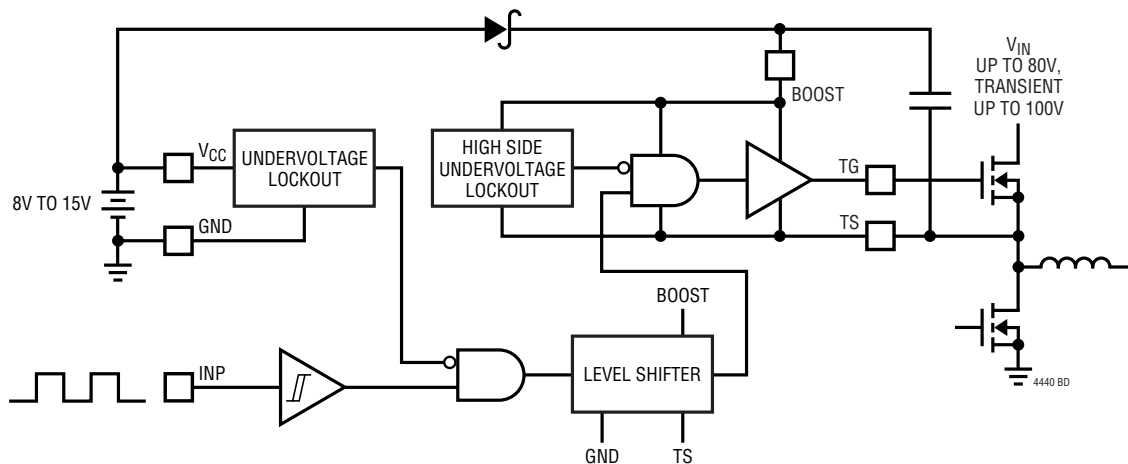
**BOOST (Pin 6):** High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 8). Normally, a bootstrap diode is connected between V<sub>CC</sub> (Pin 3) and this pin. Voltage swing at this pin is from V<sub>CC</sub> - V<sub>D</sub> to V<sub>IN</sub> + V<sub>CC</sub> - V<sub>D</sub>, where V<sub>D</sub> is the forward voltage drop of the bootstrap diode.

**TG (Pin 7):** High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

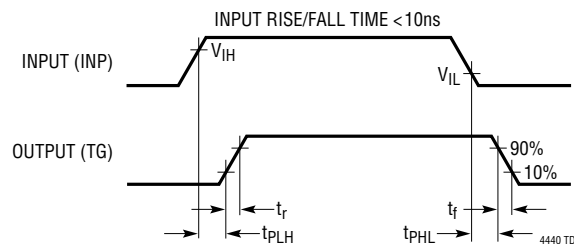
**TS (Pin 8):** Top (High Side) Source Connection.

**Exposed Pad (Pin 9):** Ground. Must be electrically connected to Pins 2 and 4 and soldered to PCB ground for optimum thermal performance.

## BLOCK DIAGRAM



## TIMING DIAGRAM



## APPLICATIONS INFORMATION

### Overview

The LTC4440 receives a ground-referenced, low voltage digital input signal to drive a high side N-channel power MOSFET whose drain can float up to 100V above ground, eliminating the need for a transformer between the low voltage control signal and the high side gate driver. The LTC4440 normally operates in applications with input supply voltages ( $V_{IN}$ ) up to 80V, but is able to withstand and continue to function during 100V, 100ms transients on the input supply.

The powerful output driver of the LTC4440 reduces the switching losses of the power MOSFET, which increase with transition time. The LTC4440 is capable of driving a 1nF load with 10ns rise and 7ns fall times using a bootstrapped supply voltage  $V_{BOOST-TS}$  of 12V.

### Input Stage

The LTC4440 employs TTL/CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4440 contains an internal voltage regulator that biases the input buffer, allowing the input thresholds ( $V_{IH} = 1.6V$ ,  $V_{IL} = 1.25V$ ) to be independent of variations in  $V_{CC}$ . The 350mV hysteresis between  $V_{IH}$  and  $V_{IL}$  eliminates false triggering due to noise during switching transitions. However, care should be taken to keep this pin from any noise pickup, especially in high frequency, high voltage applications. The LTC4440 input buffer has a high input impedance and draws negligible input current, simplifying the drive circuitry required for the input.

### Output Stage

A simplified version of the LTC4440's output stage is shown in Figure 3. The pull-down device is an N-channel MOSFET (N1) and the pull-up device is an NPN bipolar junction transistor (Q1). The output swings from the lower rail (TS) to within an NPN  $V_{BE}$  ( $\sim 0.7V$ ) of the positive rail (BOOST). This large voltage swing is important in driving external power MOSFETs, whose  $R_{DS(ON)}$  is inversely proportional to its gate overdrive voltage ( $V_{GS} - V_{TH}$ ).

The LTC4440's peak pull-up (Q1) current is 2.4A while the pull-down (N1) resistance is 1.5 $\Omega$ . The low impedance of N1 is required to discharge the power MOSFET's gate capacitance during high-to-low signal transitions. When

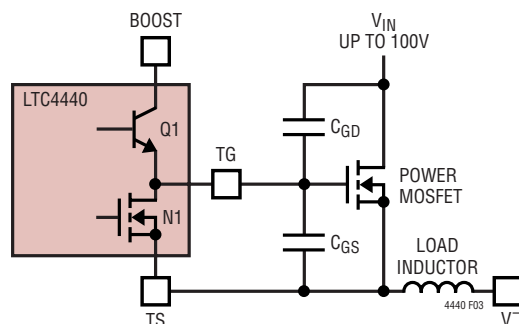


Figure 3. Capacitance Seen by TG During Switching

the power MOSFET's gate is pulled low (gate shorted to source through N1) by the LTC4440, its source (TS) is pulled low by its load (e.g., an inductor or resistor). The slew rate of the source/gate voltage causes current to flow back to the MOSFET's gate through the gate-to-drain capacitance ( $C_{GD}$ ). If the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's  $C_{GD}$  can momentarily pull the gate high, turning the MOSFET back on.

A similar scenario exists when the LTC4440 is used to drive a low side MOSFET. When the low side power MOSFET's gate is pulled low by the LTC4440, its drain voltage is pulled high by its load (e.g., inductor or resistor). The slew rate of the drain voltage causes current to flow back to the MOSFET's gate through its gate-to-drain capacitance. If the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's  $C_{GD}$  can momentarily pull the gate high, turning the MOSFET back on.

### Rise/Fall Time

Since the power MOSFET generally accounts for the majority of the power loss in a converter, it is important to quickly turn it on or off, thereby minimizing the transition time in its linear region. The LTC4440 can drive a 1nF load with a 10ns rise time and 7ns fall time.

The LTC4440's rise and fall times are determined by the peak current capabilities of Q1 and N1. The predriver that drives Q1 and N1 uses a nonoverlapping transition scheme to minimize cross-conduction currents. N1 is fully turned off before Q1 is turned on and vice versa.

## APPLICATIONS INFORMATION

### Power Dissipation

To ensure proper operation and long-term reliability, the LTC4440 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + PD (\theta_{JA})$$

where:

$T_J$  = Junction Temperature

$T_A$  = Ambient Temperature

PD = Power Dissipation

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Power dissipation consists of standby and switching power losses:

$$PD = P_{STDBY} + P_{AC}$$

where:

$P_{STDBY}$  = Standby Power Losses

$P_{AC}$  = AC Switching Losses

The LTC4440 consumes very little current during standby. The DC power loss at  $V_{CC} = 12V$  and  $V_{BOOST-TS} = 12V$  is only  $(250\mu A + 110\mu A)(12V) = 4.32mW$ .

AC switching losses are made up of the output capacitive load losses and the transition state losses. The capacitive load losses are primarily due to the large AC currents needed to charge and discharge the load capacitance during switching. Load losses for the output driver driving a pure capacitive load  $C_{OUT}$  would be:

$$\text{Load Capacitive Power} = (C_{OUT})(f)(V_{BOOST-TS})^2$$

The power MOSFET's gate capacitance seen by the driver output varies with its  $V_{GS}$  voltage level during switching. A power MOSFET's capacitive load power dissipation can be calculated using its gate charge,  $Q_G$ . The  $Q_G$  value corresponding to the MOSFET's  $V_{GS}$  value ( $V_{CC}$  in this case) can be readily obtained from the manufacturer's  $Q_G$  vs  $V_{GS}$  curves:

$$\text{Load Capacitive Power (MOS)} = (V_{BOOST-TS})(Q_G)(f)$$

Transition state power losses are due to both AC currents required to charge and discharge the driver's internal nodal capacitances and cross-conduction currents in the internal gates.

### Undervoltage Lockout (UVLO)

The LTC4440 contains both low side and high side undervoltage lockout detectors that monitor  $V_{CC}$  and the bootstrapped supply  $V_{BOOST-TS}$ . When  $V_{CC}$  falls below 6.2V, the internal buffer is disabled and the output pin OUT is pulled down to TS. When  $V_{BOOST-TS}$  falls below 6.9V, OUT is pulled down to TS. When both supplies are undervoltage, OUT is pulled low to TS and the chip enters a low current mode, drawing approximately 25 $\mu A$  from  $V_{CC}$  and 86 $\mu A$  from BOOST.

### Bypassing and Grounding

The LTC4440 requires proper bypassing on the  $V_{CC}$  and  $V_{BOOST-TS}$  supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

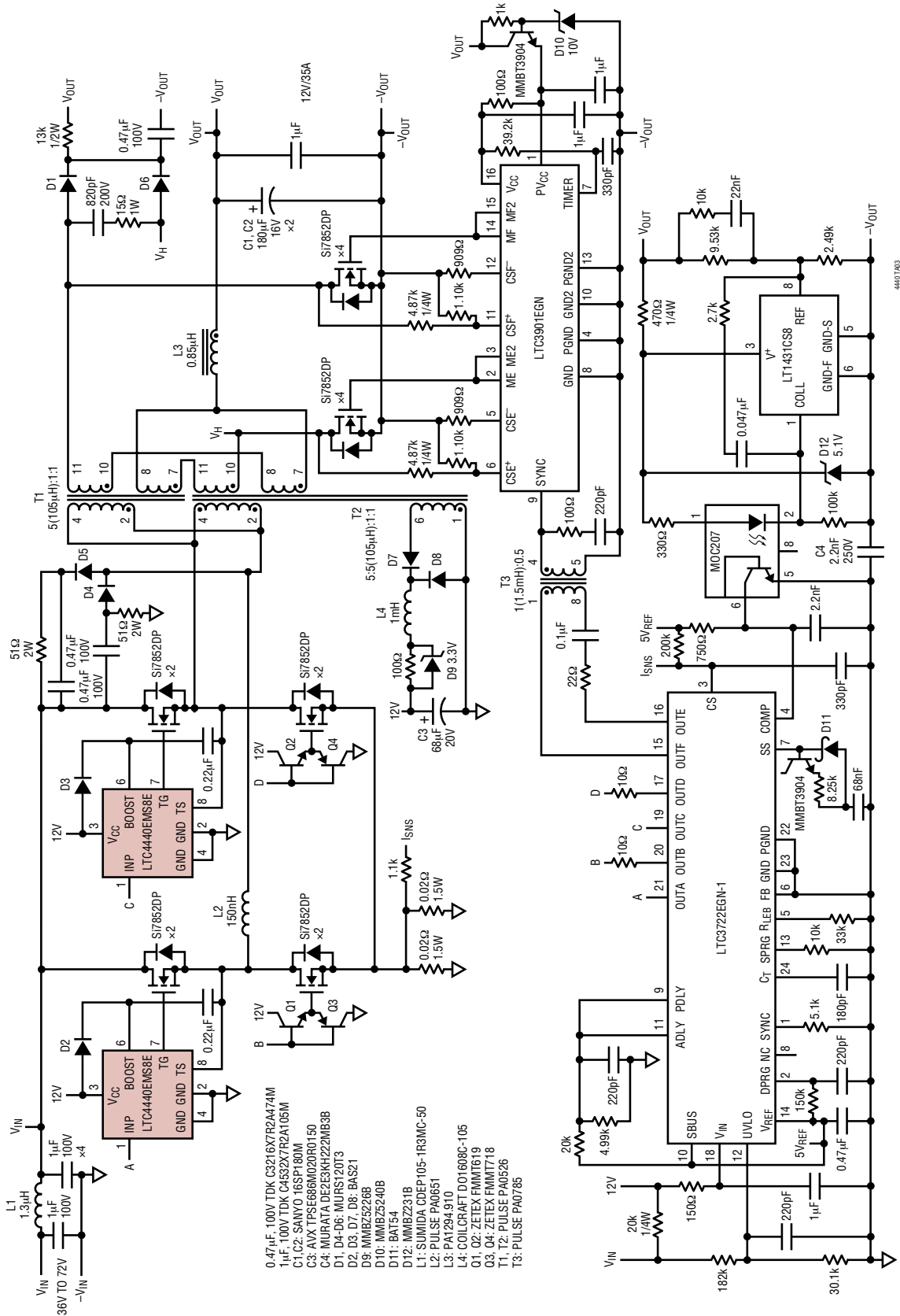
To obtain the optimum performance from the LTC4440:

- A. Mount the bypass capacitors as close as possible between the  $V_{CC}$  and GND pins and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.
- B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4440 switches >2A peak currents and any significant ground drop will degrade signal integrity.
- C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- D. Keep the copper trace between the driver output pin and the load short and wide.
- E. When using the MS8E package, be sure to solder the exposed pad on the back side of the LTC4440 package to the board. Correctly soldered to a 2500mm<sup>2</sup> double-sided 1oz copper board, the LTC4440 has a thermal resistance of approximately 40°C/W. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than 40°C/W.



TYPICAL APPLICATIONS

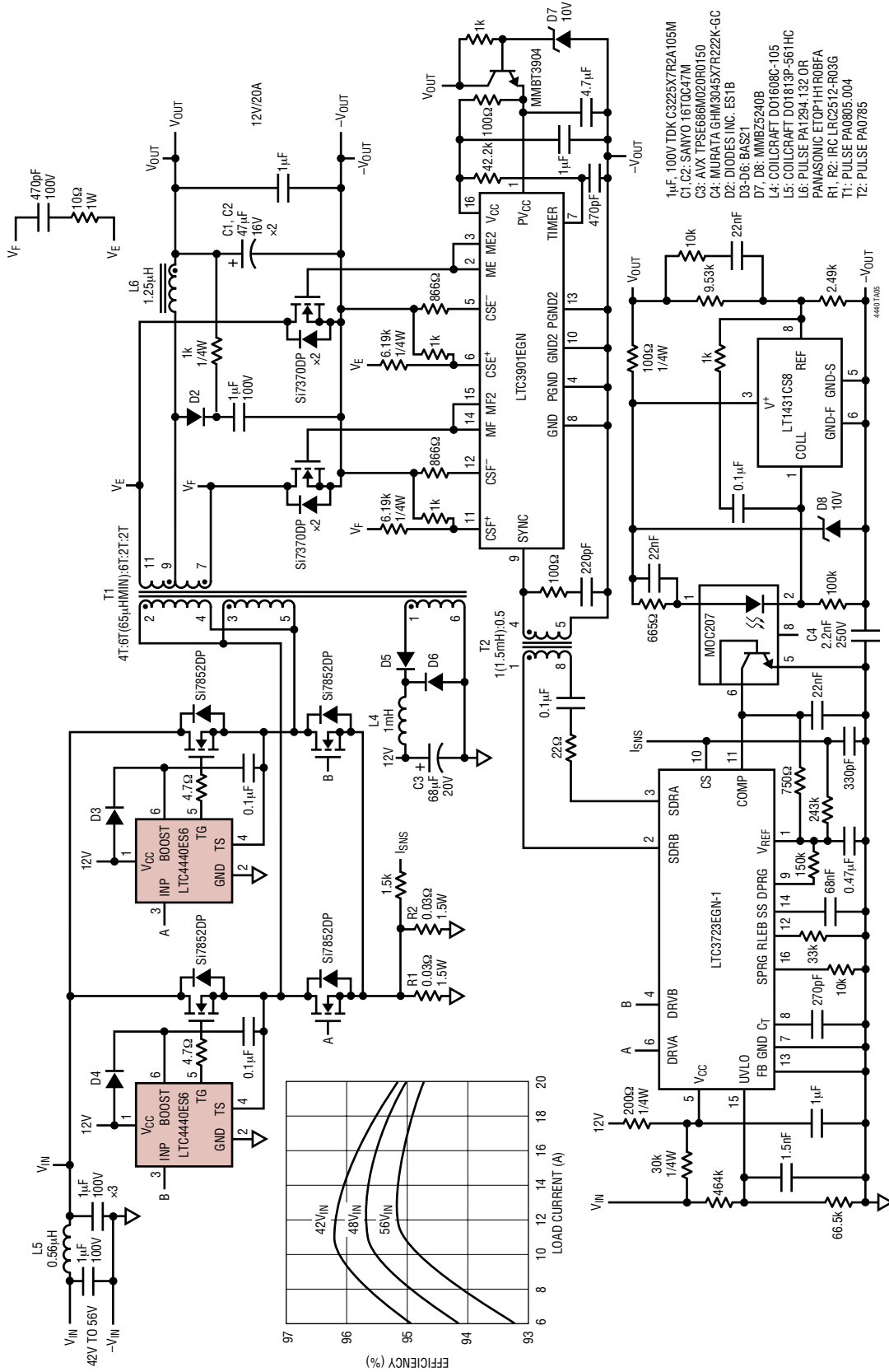
LTC3722/LTC4440 420W 36V-72V<sub>IN</sub> to 12V/35A Isolated Full-Bridge Supply



4440T83

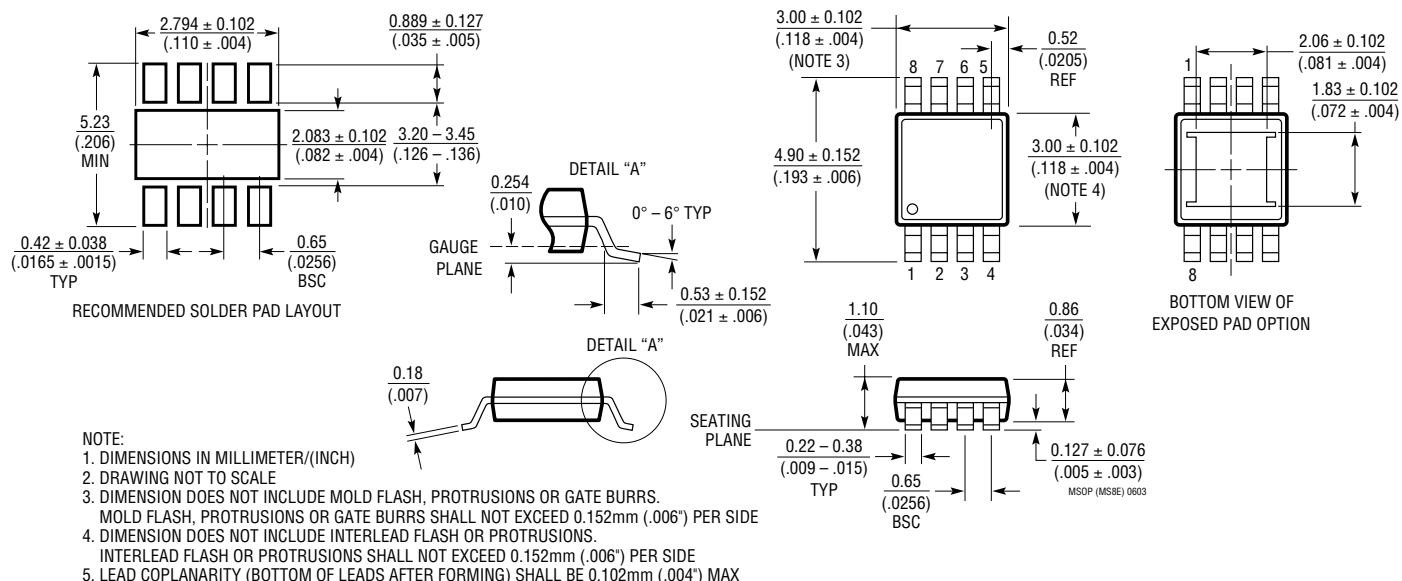
TYPICAL APPLICATIONS

LTC3723-1 240W 42-56V<sub>IN</sub> to 12V/20A Isolated 1/4Brick (2.3" × 1.45")

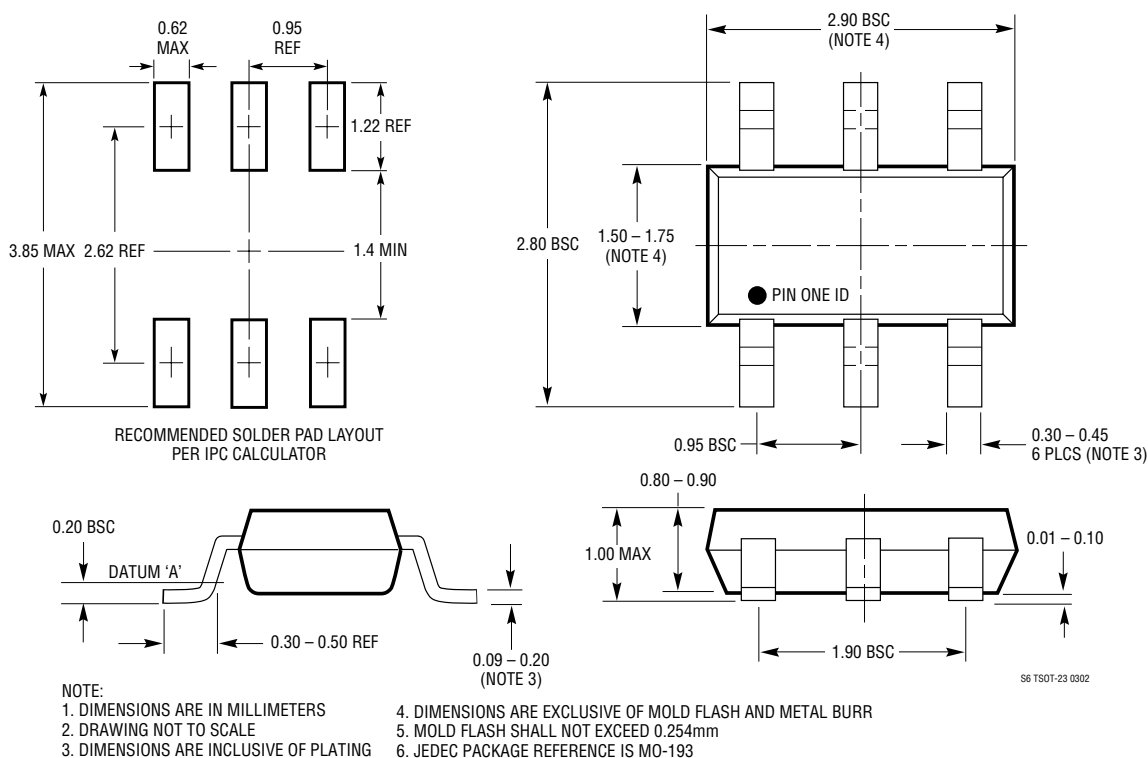


# PACKAGE DESCRIPTION

## MS8E Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1662)



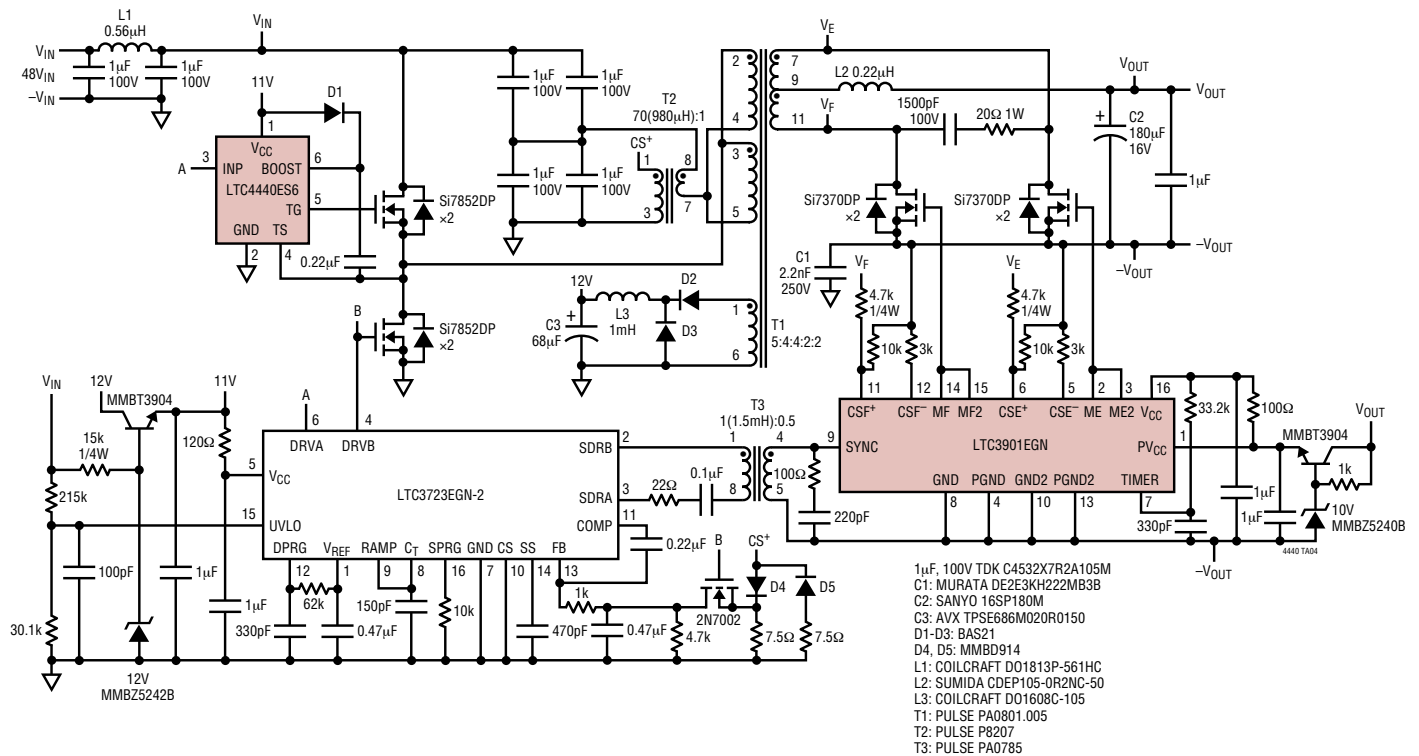
## S6 Package 6-Lead Plastic SOT-23 (Reference LTC DWG # 05-08-1636)



S6 TSOT-23 0302

## TYPICAL APPLICATION

LTC3723-2/LTC4440/LTC3901 240W 42V-56V<sub>IN</sub> to Unregulated 12V Half-Bridge Converter



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1155	Dual Micropower High/Low Side Drivers with Internal Charge Pump	4.5V to 18V Supply Range
LT <sup>®</sup> 1161	Quad Protected High Side MOSFET Driver	8V to 48V Supply Range, $t_{ON} = 200\mu s$ , $t_{OFF} = 28\mu s$
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	1.8V to 6V Supply Range, $t_{ON} = 95\mu s$ , $t_{OFF} = 45\mu s$
LT1339	High Power Synchronous DC/DC Controller	Current Mode Operation Up to 60V, Dual N-Channel Synchronous Drive
LTC1535	Isolated RS485 Transceiver	2500V <sub>RMS</sub> of Isolation Between Line Transceiver and Logic Level Interface
LTC1693 Family	High Speed Dual MOSFET Drivers	1.5A Peak Output Current, $4.5V \leq V_{IN} \leq 13.2V$
LT3010/LT3010-5	50mA, 3V to 80V Low Dropout Micropower Regulators	Low Quiescent Current (30µA), Stable with Small (1µF) Ceramic Capacitor
LT3430	High Voltage, 3A, 200kHz Step-Down Switching Regulator	Input Voltages Up to 60V, Internal 0.1Ω Power Switch, Current Mode Architecture, 16-Pin Exposed Pad TSSOP Package
LTC3722-1/ LTC3722-2	Synchronous Dual Mode Phase Modulated Full-Bridge Controllers	Adaptive Zero Voltage Switching, High Output Power Levels (Up to Kilowatts)
LTC3723-1/ LTC3723-2	Synchronous Push-Pull PWM Controllers	Current Mode or Voltage Mode Push-Pull Controllers
LT3781/LTC1698	36V to 72V Input Isolated DC/DC Converter Chip Set	Synchronous Rectification; Overcurrent, Overvoltage, UVLO Protection; Power Good Output Signal; Voltage Margining; Compact Solution
LT3804	Secondary Side Dual Output Controller with Opto Driver	Regulates Two Secondary Outputs, Optocoupler Feedback Divider and Second Output Synchronous Driver Controller
LTC3900	Synchronous Rectifier Driver for Forward Converters	Programmable Time Out, Reverse Inductor Current Sense
LTC3901	Secondary Side Synchronous Driver for Push-Pull and Full-Bridge Converters	Programmable Time Out, Reverse Inductor Current Sense
LTC4441	6A MOSFET Driver	Adjustable Gate Drive from 5V to 8V, $5V \leq V_{IN} \leq 28V$

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