NUD3105D

Integrated Relay, Inductive Load Driver

This device is used to switch inductive loads such as relays, solenoids incandescent lamps, and small DC motors without the need of a free−wheeling diode. The device integrates all necessary items such as the MOSFET switch, ESD protection, and Zener clamps. It accepts logic level inputs thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

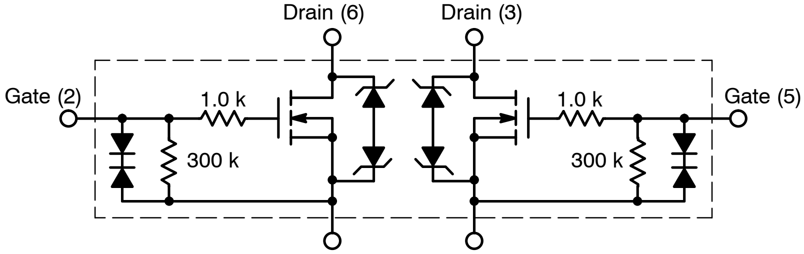
Features

- Provides a Robust Driver Interface Between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from 3.0 V to 5.0 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5.0 V
- Internal Zener Eliminates the Need of Free−Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter Systems Operation
- Low $V_{DS(on)}$ Reduces System Current Drain
- Pb−Free Package is Available

Typical Applications

- Telecom: Line Cards, Modems, Answering Machines, FAX
- Computers and Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders
- Industrial: Small Appliances, Security Systems, Automated Test Equipment, Garage Door Openers
- Automotive: 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers

INTERNAL CIRCUIT DIAGRAMS

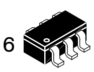


CASE 318F

ON Semiconductor®

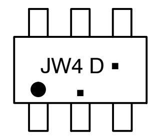
http://onsemi.com

Relay, Inductive Load Driver
0.5 Amp, 8.0 V Clamp



SC−74
CASE 318F
STYLE 7

MARKING DIAGRAM



JW4 = Specific Device Code
D = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUD3105DMT1	SC−74	3000/Tape & Reel
NUD3105DMT1G	SC−74 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DSS}	Drain to Source Voltage – Continuous	6.0	V_{dc}
V_{GS}	Gate to Source Voltage – Continuous	6.0	V_{dc}
I_D	Drain Current – Continuous	500	mA
E_z	Single Pulse Drain−to−Source Avalanche Energy ($T_{Jinitial}$ = 25°C)	50	mJ
T_J	Junction Temperature	150	°C
T_A	Operating Ambient Temperature	−40 to 85	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	380 1.5	mW mW/°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Ambient	329	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL_STD−883, Method 3015.
   Machine Model Method 200 V.

TYPICAL ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
V_{BRDSS}	Drain to Source Sustaining Voltage (Internally Clamped) (I_D = 10 mA)	6.0	8.0	9.0	V
B_{VGSO}	I_g = 1.0 mA	–	–	8.0	V
I_{DSS}	Drain to Source Leakage Current (V_{DS} = 5.5 V , V_{GS} = 0 V, T_J = 25°C) (V_{DS} = 5.5 V, V_{GS} = 0 V, T_J = 85°C)	– –	– –	15 15	µA
I_{GSS}	Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V)	5.0 –	– –	35 65	µA
ON CHARACTERISTICS					
$V_{GS(th)}$	Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_J = 85°C)	0.8 0.8	1.2 –	1.4 1.4	V
$R_{DS(on)}$	Drain to Source On−Resistance (I_D = 250 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 5.0 V) (I_D = 500 mA, V_{GS} = 3.0 V, T_J = 85°C) (I_D = 500 mA, V_{GS} = 5.0 V, T_J = 85°C)	– – – – –	– – – – –	1.2 1.3 0.9 1.3 0.9	Ω
$I_{DS(on)}$	Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_J = 85°C)	300 200	400 –	– –	mA
g_{FS}	Forward Transconductance (V_{OUT} = 5.0 V, I_{OUT} = 0.25 A)	350	570	–	mMhos

TYPICAL ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	–	25	–	pF
C_{oss}	Output Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	–	37	–	pF
C_{rss}	Transfer Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 10 kHz)	–	8.0	–	pF

SWITCHING CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units
	Propagation Delay Times:				nS
t_{PHL}	High to Low Propagation Delay; Figure 1 (5.0 V)	–	25	–	
t_{PLH}	Low to High Propagation Delay; Figure 1 (5.0 V)	–	80	–	
t_{PHL}	High to Low Propagation Delay; Figure 1 (3.0 V)	–	44	–	
t_{PLH}	Low to High Propagation Delay; Figure 1 (3.0 V)	–	44	–	
	Transition Times:				nS
t_f	Fall Time; Figure 1 (5.0 V)	–	23	–	
t_r	Rise Time; Figure 1 (5.0 V)	–	32	–	
t_f	Fall Time; Figure 1 (3.0 V)	–	53	–	
t_r	Rise Time; Figure 1 (3.0 V)	–	30	–	–

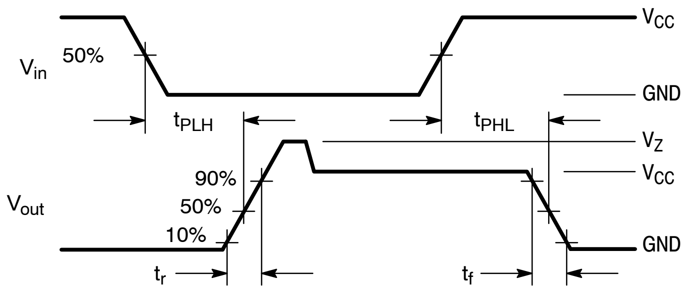


Figure 1. Switching Waveforms

TYPICAL CHARACTERISTICS

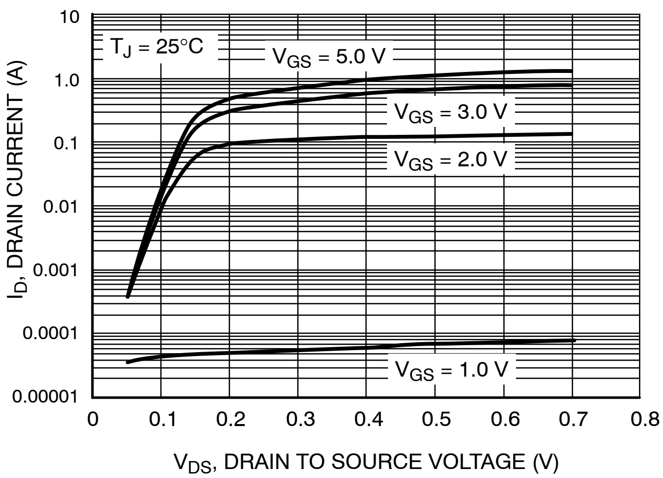


Figure 2. Output Characteristics

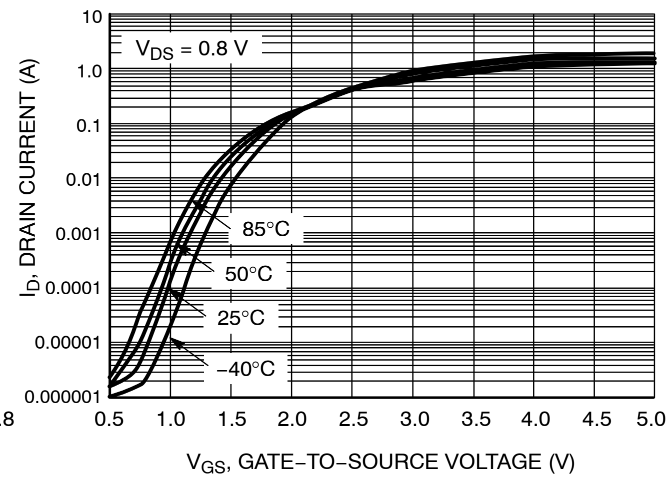


Figure 3. Transfer Function

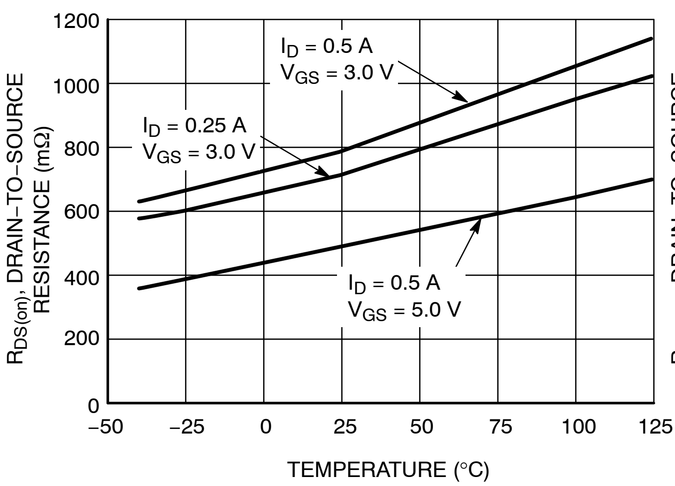


Figure 4. On Resistance Variation vs. Temperature

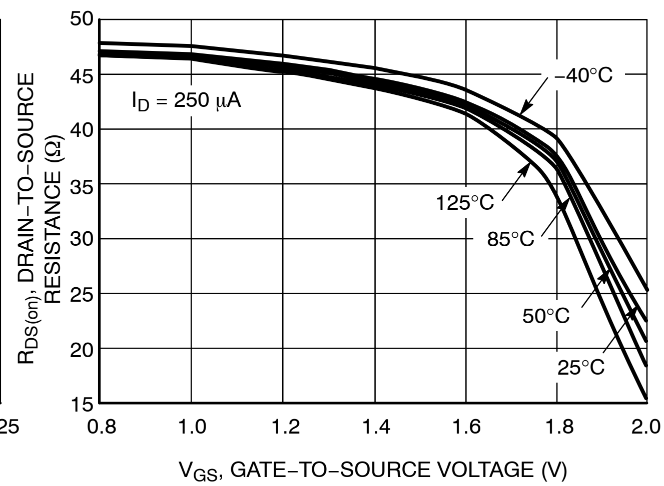


Figure 5. $R_{DS(ON)}$ Variation with Gate−To−Source Voltage

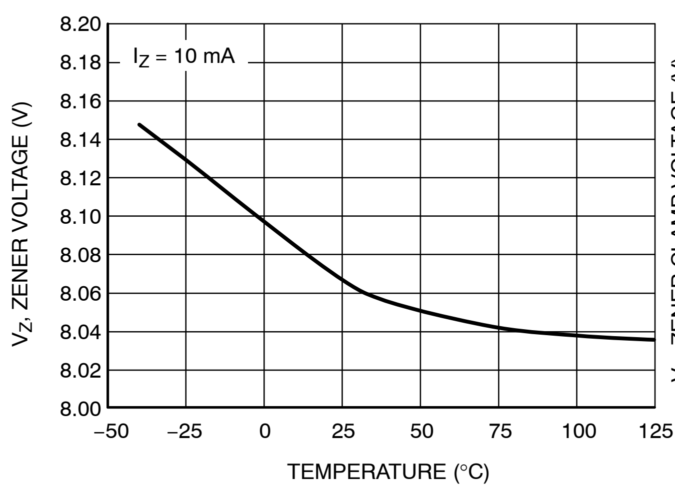


Figure 6. Zener Voltage vs. Temperature

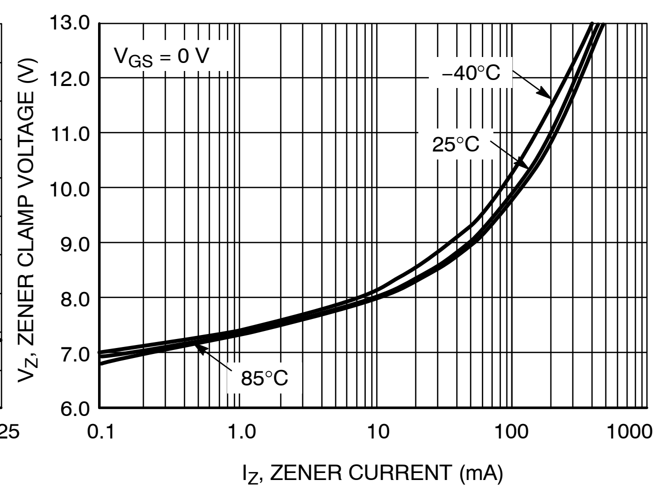


Figure 7. Zener Clamp Voltage vs. Zener Current

TYPICAL CHARACTERISTICS

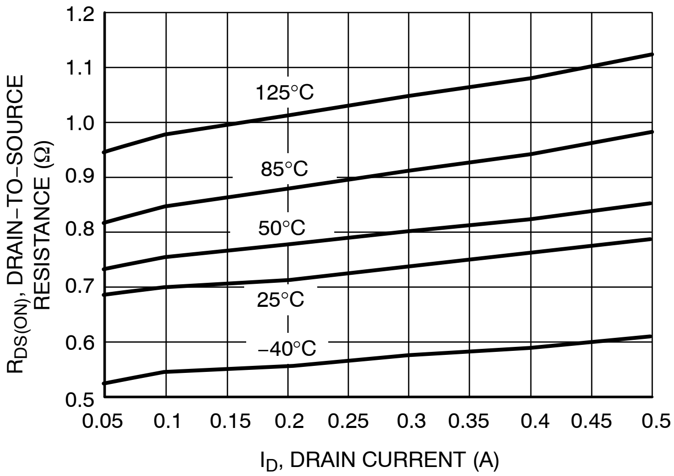


Figure 8. On−Resistance vs. Drain Current and Temperature

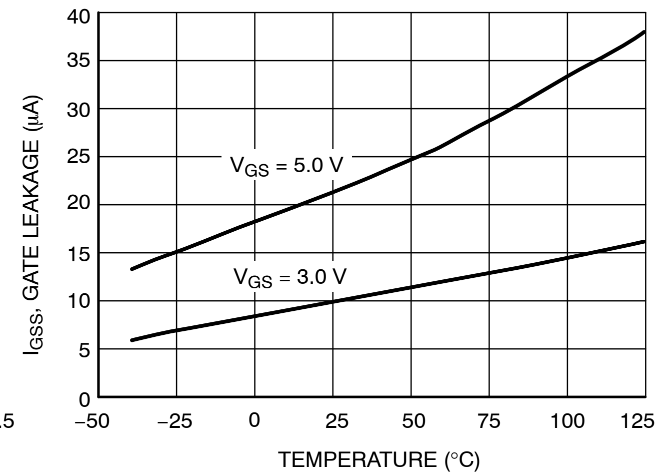


Figure 9. Gate Leakage vs. Temperature

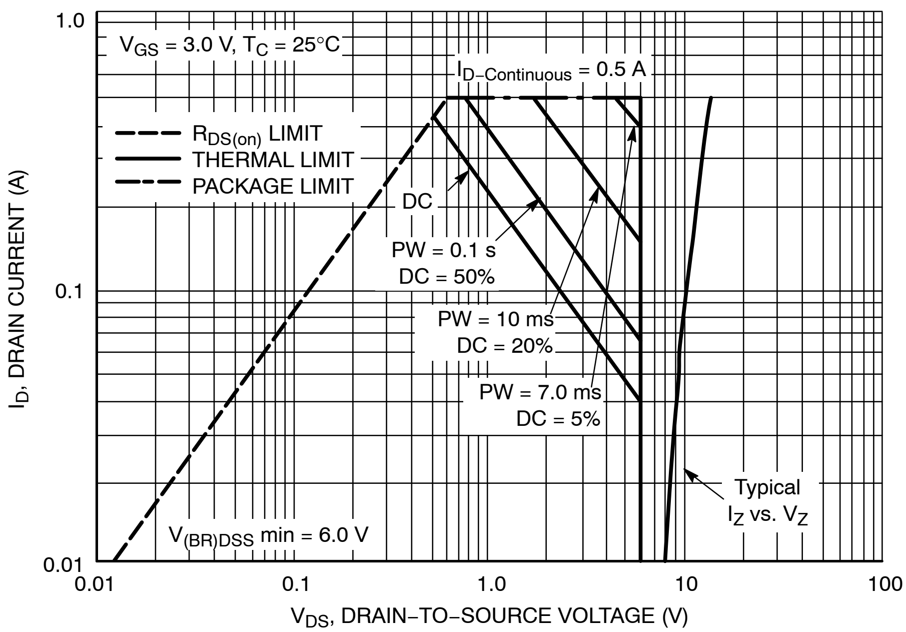


Figure 10. Safe Operating Area for NUD3105DLT1

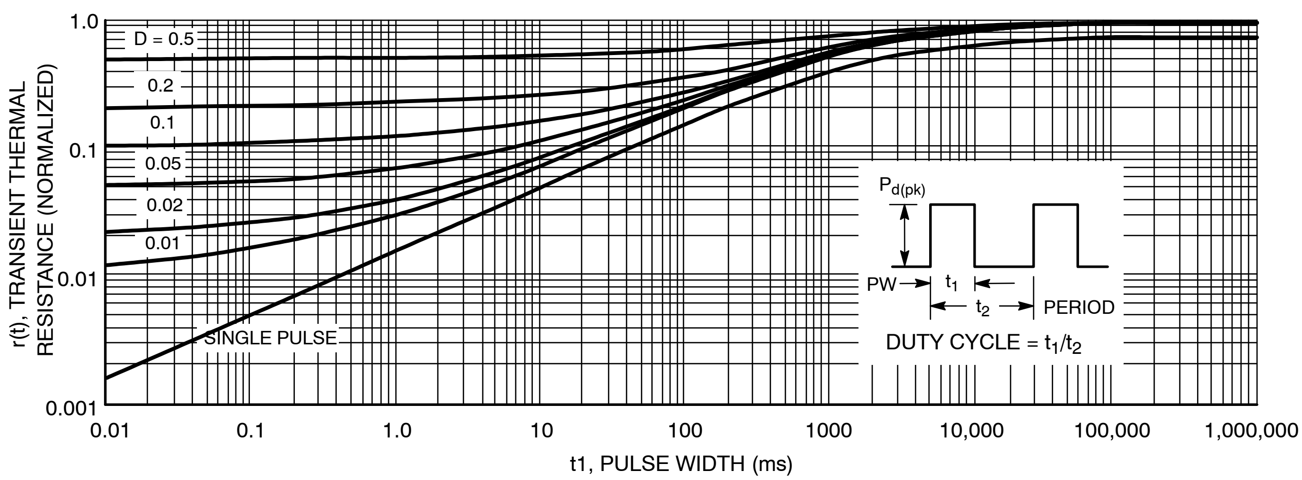


Figure 11. Transient Thermal Response for NUD3105DLT1

Designing with this Data Sheet

1. Determine the maximum inductive load current (at max V_{CC}, min coil resistance & usually minimum temperature) that the NUD3105D will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 11 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures 10 and 11 with the SOA notes to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.
4. Verify that the circuit driving the gate will meet the $V_{GS(th)}$ from the Electrical Characteristics table.
5. Using the max output current calculated in step 1, check Figure 7 to insure that the range of Zener clamp voltage over temperature will satisfy all system & EMI requirements.
6. Use I_{GSS} and I_{DSS} from the Electrical Characteristics table to insure that "OFF" state leakage over temperature and voltage extremes does not violate any system requirements.
7. Review circuit operation and insure none of the device max ratings are being exceeded.

APPLICATIONS DIAGRAMS

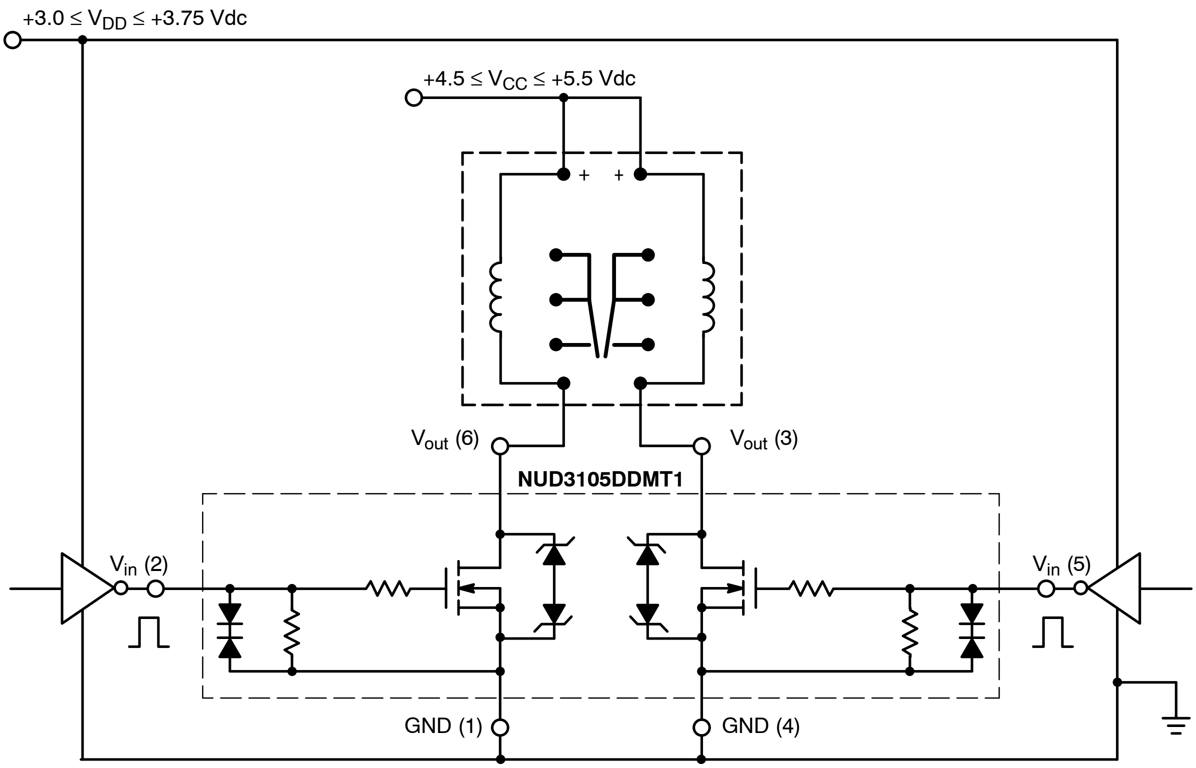


Figure 12. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V Level Translating Interface

Max Continuous Current Calculation

for TX2−5V Relay, R1 = 178 Ω Nominal @ R_A = 25°C

Assuming ±10% Make Tolerance,
R1 = 178 Ω * 0.9 = 160 Ω Min @ T_A = 25°C

T_C for Annealed Copper Wire is 0.4%/°C

R1 = 160 Ω * [1+(0.004) * (−40°−25°)] = 118 Ω Min @ −40°C

I_O Max = (5.5 V Max − 0.25V) /118 Ω = 45 mA

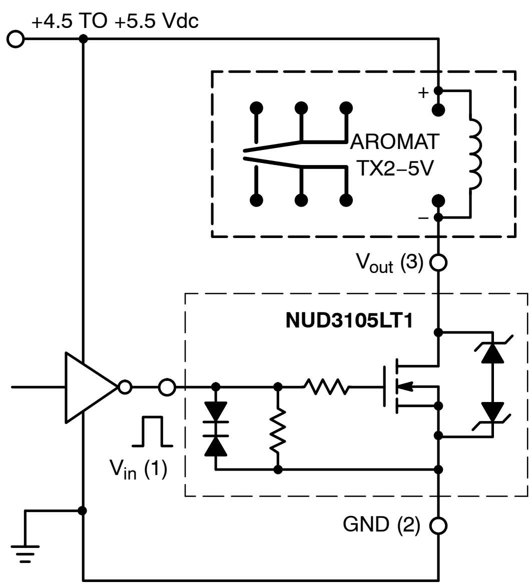


Figure 13. A 140 mW, 5.0 V Relay with TTL Interface

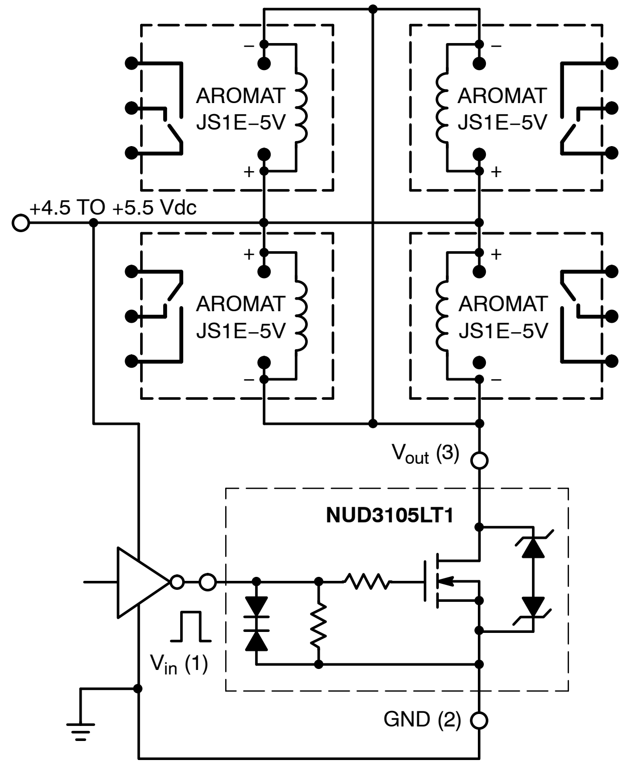
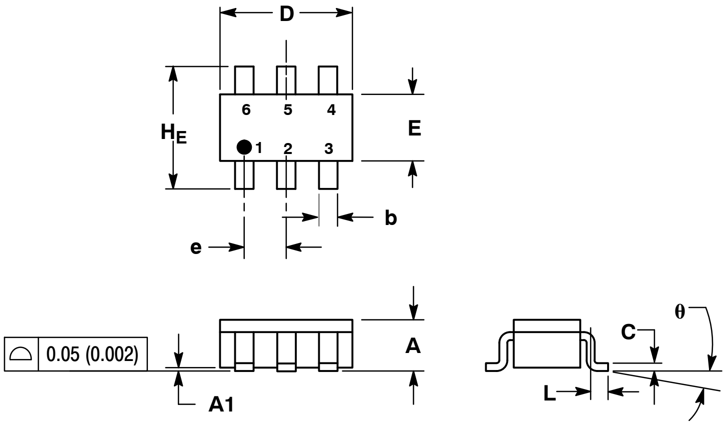


Figure 14. A Quad 5.0 V, 360 mW Coil Relay Bank

PACKAGE DIMENSIONS

SC−74
CASE 318F−05
ISSUE M

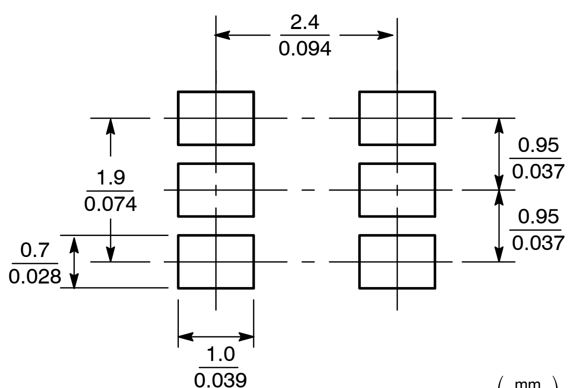


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

SOLDERING FOOTPRINT*



SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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