

NM27C020

2,097,152-Bit (256K x 8) UV Erasable CMOS EPROM

General Description

The NM27C020 is a high speed 2 Megabit CMOS UV-EPROM manufactured on Fairchild's advanced sub-micron technology. Utilizing the AMG architecture, this advanced CMOS process delivers high speeds while consuming low power.

The NM27C020 provides microprocessor-based systems extensive storage capacity for large portions of operating systems and application software. Its 100ns access time provides no-wait-state operation with high-performance CPUs.

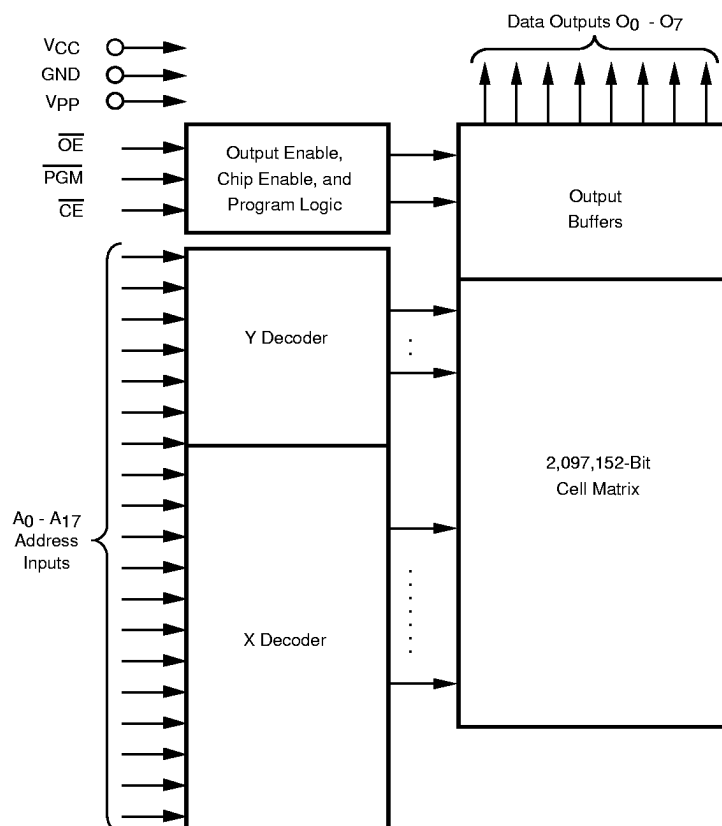
The NM27C020 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C020 is manufactured using Fairchild's advanced CMOS AMG EPROM technology, and is one member of a high density Fairchild EPROM series family which range in densities up to 4Mb.

Features

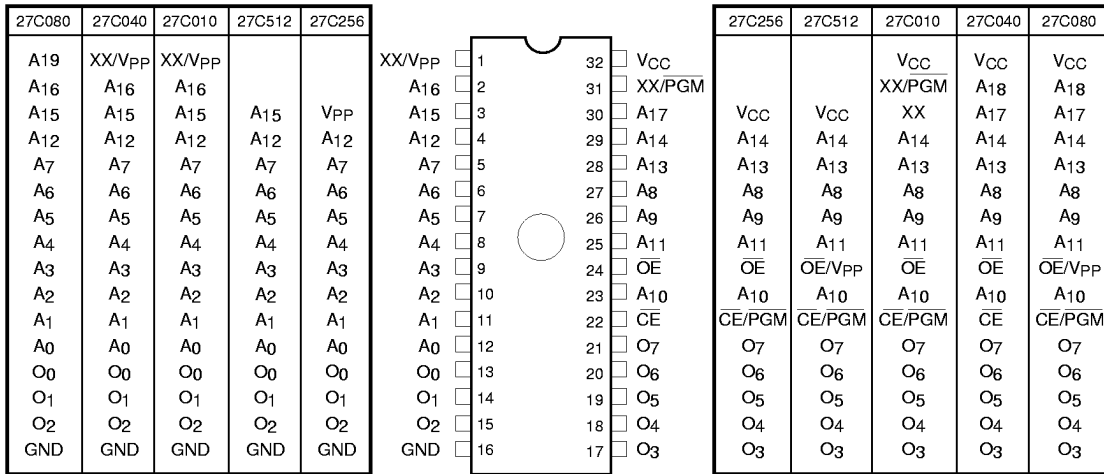
- High performance CMOS
 - 100 ns access time
- Simplified upgrade path
 - V_{PP} and PGM are "Don't Care" during normal read operation
- Manufacturers identification code
- JEDEC Standard Pin Configuration
 - 32-pin CERDIP package
 - 32-pin PLCC package
 - 32-pin PDIP package

Block Diagram



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Connection Diagrams



Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C020 pins.

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Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

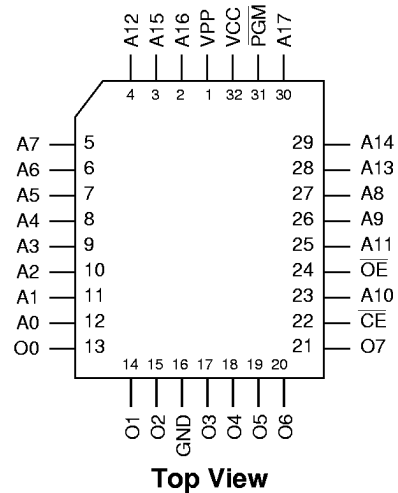
| Parameter/Order Number | Access Time (ns) |
|------------------------|------------------|
| NM27C020 Q, V, N 100 | 100 |
| NM27C020 Q, V, N 120 | 120 |
| NM27C020 Q, V, N 150 | 150 |

All versions are guaranteed to function at slower speeds.

Extended Temperature Range (-40°C to +85°C) V_{CC} = 5V ±10%

| Parameter/Order Number | Access Time (ns) |
|-----------------------------|------------------|
| NM27C020 QE, VE, TE, NE 120 | 120 |
| NM27C020 QE, VE, TE, NE 150 | 150 |

PLCC Pin Configuration



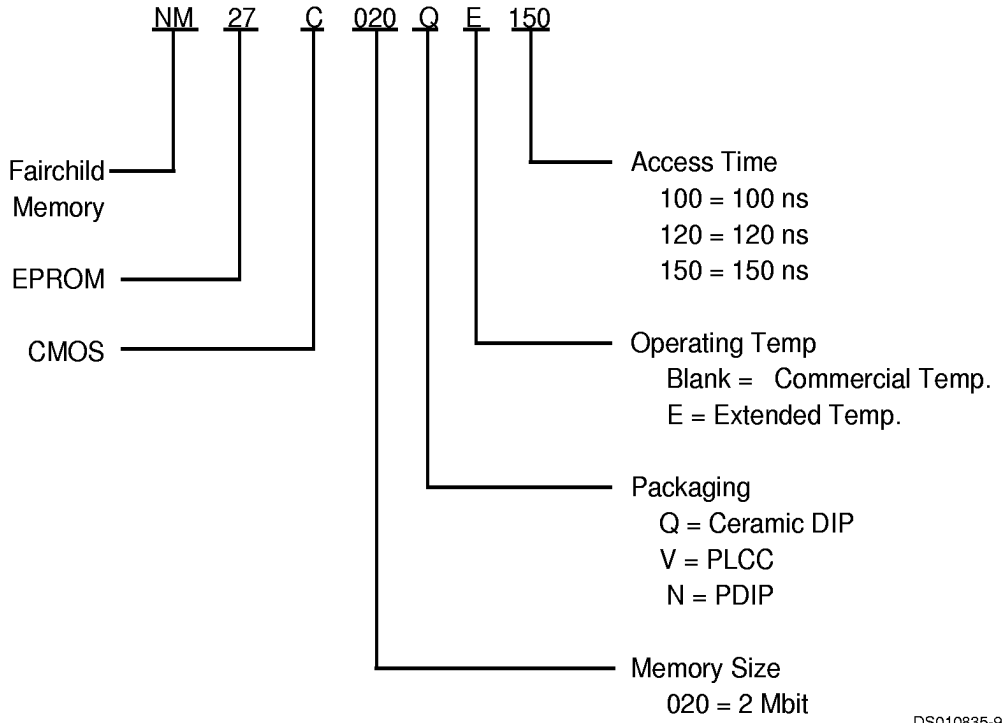
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Pin Names

| | |
|---------|--------------------------|
| A0 –A17 | Addresses |
| CE | Chip Enable |
| OE | Output Enable |
| O0 –O7 | Outputs |
| PGM | Program |
| XX | Don't Care (During Read) |

Connection Diagrams (Continued)

Ordering Information



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Absolute Maximum Ratings (Note 1)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +125°C |
| All Input Voltage Except A9 with Respect to Ground (Note 13) | -0.6V to +7V |
| V _{PP} and A9 with Respect to Ground | -0.6V to +14V |
| V _{CC} Supply Voltage with Respect to Ground | -0.6V to +7V |
| ESD Protection | >2000V |

All Output Voltages with Respect to Ground (Note 13) V_{CC} + 10V to GND -0.6V

Operating Range

| Range | Temperature | V _{CC} | Tolerance |
|------------|----------------|-----------------|-----------|
| Commercial | 0°C to +70°C | +5V | ±10 |
| Industrial | -40°C to +85°C | +5V | ±10% |

DC Read Characteristics Over Operating Range with V_{PP} = V_{CC}

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---------------------------|--|--|--------------------------|---------------------|-------|
| V _{IL} | Input Low Level | | -0.5 | 0.8 | V |
| V _{IH} | Input High Level | | 2.0 | V _{CC} + 1 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | -0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 3.5 | | V |
| I _{SB1} (Note 4) | V _{CC} Standby Current (CMOS) | CE = V _{CC} ± 0.3V | | 100 | μA |
| I _{SB2} | V _{CC} Standby Current (TTL) | CE = V _{IH} | | 1 | mA |
| I _{CC} (Note 2) | V _{CC} Active Current | CE, OE = V _{IL} I/O = 0 mA, f = 5 MHz Inputs = V _{IH} or V _{IL} | Commercial Industrial | 30 30 | mA |
| I _{PP} | V _{PP} Supply Current | V _{PP} = V _{CC} | | 10 | μA |
| V _{PP} | V _{PP} Read Voltage | | V _{CC} - 0.4 | V _{CC} | V |
| I _{LI} | Input Load Current | V _{IN} = 5.5 or GND | -1 | 1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 5.5V or GND | -10 | 10 | μA |

AC Read Characteristics Over Operating Range with V_{PP} = V_{CC}

| Symbol | Parameter | 100 | | 120 | | 150 | | Units |
|--------------------------|--|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| t _{ACC} | Address to Output Delay | | 100 | | 120 | | 150 | ns |
| t _{CE} | CE to Output Delay | | 100 | | 120 | | 150 | ns |
| t _{OE} | OE to Output Delay | | 40 | | 45 | | 50 | ns |
| t _{DF} (Note 3) | Output Disable to Output Float | | 40 | | 45 | | 50 | ns |
| t _{OH} | Output Hold from Addresses, CE or OE, Whichever Occurred First | 0 | | 0 | | 0 | | ns |

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

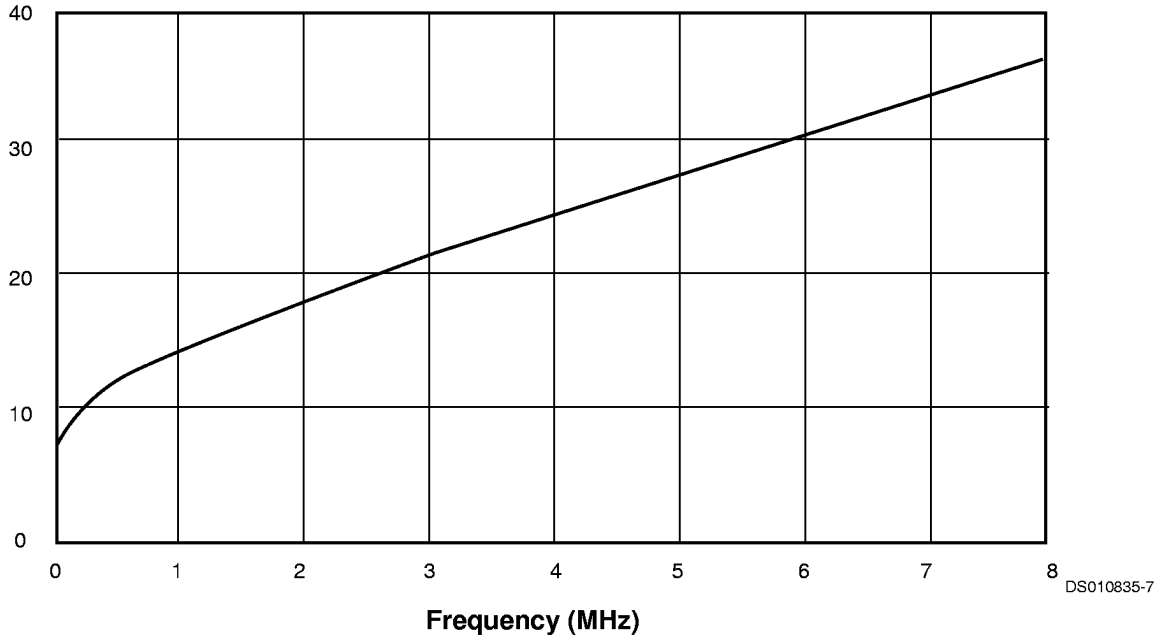
Note 2: The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O0 to O7 unloaded.

Note 3: This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.

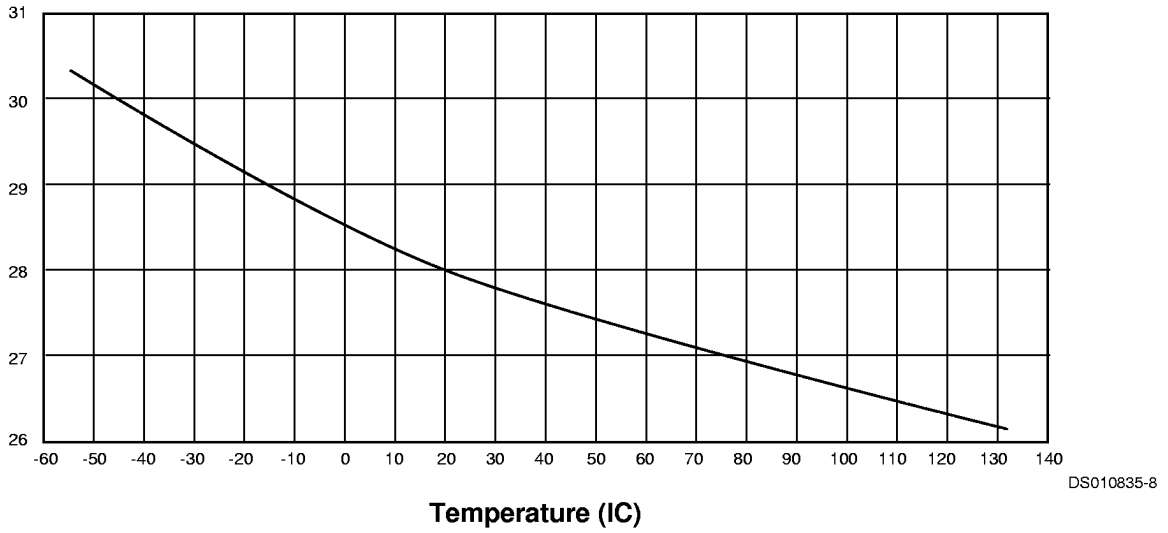
Note 4: CMOS inputs: V_{IL} = GND 10.3V, V_{IH} = V_{CC} 10.3V.

AC Read Characteristics (Continued)

I_{CC} vs. Frequency



I_{CC} vs. Temperature



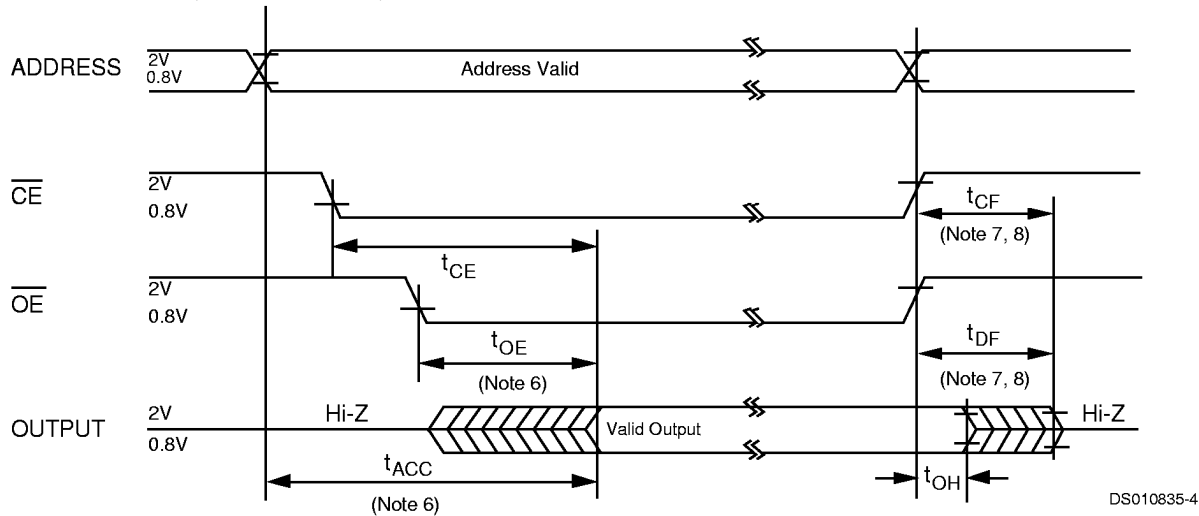
Capacitance $T_A = +25^\circ\text{C}$, $f = 1 \text{ MHz}$ (Note 5)

| Symbol | Parameter | Conditions | Typ | Max | Units |
|-----------|--------------------|----------------|-----|-----|-------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 9 | 15 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 12 | 15 | pF |

AC Test Conditions

| | |
|--|---|
| Output Load | 1 TTL Gate and $C_L = 100 \text{ pF}$ (Note 11) |
| Input Rise and Fall Times | $\leq 5 \text{ ns}$ |
| Input Pulse Levels | 0.45V to 2.4V |
| Timing Measurement Reference Level (Note 13) | |
| Inputs | 0.8V and 2V |
| Outputs | 0.8V and 2V |

AC Waveforms (Notes 9, 10, 12)



- Note 5:** This parameter is only sampled and is not 100% tested.
- Note 6:** \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impacting t_{ACC} .
- Note 7:** The t_{DE} and t_{CF} compare level is determined as follows:
High to TRI-STATE[®], the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.
- Note 8:** TRI-STATE may be attained using \overline{OE} or \overline{CE} .
- Note 9:** The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 MF ceramic capacitor be used on every device between V_{CC} and GND.
- Note 10:** The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.
- Note 11:** 1 TTL Gate: $I_{OL} = 1.6 \text{ mA}$, $I_{OH} = -400 \mu\text{A}$.
 C_L : 100 pF includes fixture capacitance.
- Note 12:** V_{PP} may be connected to V_{CC} except during programming.
- Note 13:** Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 14, 15, 16, 17)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------|--|---------------------------------|------|-------|------|-------------|
| t_{AS} | Address Setup Time | | 1 | | | μs |
| t_{OES} | OE Setup Time | | 1 | | | μs |
| t_{CES} | CE Setup Time | OE = V_{IH} | 1 | | | μs |
| t_{DS} | Data Setup Time | | 1 | | | μs |
| t_{VPS} | V_{PP} Setup Time | | 1 | | | μs |
| t_{VCS} | V_{CC} Setup Time | | 1 | | | μs |
| t_{AH} | Address Hold Time | | 0 | | | μs |
| t_{DH} | Data Hold Time | | 1 | | | μs |
| t_{DF} | Output Enable to Output Float Delay | CE = V_{IL} | 0 | | 60 | ns |
| t_{PW} | Program Pulse Width | | 45 | 50 | 105 | μs |
| t_{OE} | Data Valid from OE | CE = V_{IL} | | | 100 | ns |
| I_{PP} | V_{PP} Supply Current during Programming Pulse | CE = V_{IL} PGM = V_{IL} | | | 15 | mA |
| I_{CC} | V_{CC} Supply Current | | | | 20 | mA |
| T_A | Temperature Ambient | | 20 | 25 | 30 | $^{\circ}C$ |
| V_{CC} | Power Supply Voltage | | 6.25 | 6.5 | 6.75 | V |
| V_{PP} | Programming Supply Voltage | | 12.5 | 12.75 | 13.0 | V |
| t_{FR} | Input Rise, Fall Time | | 5 | | | ns |
| V_{IL} | Input Low Voltage | | | 0.0 | 0.45 | V |
| V_{IH} | Input High Voltage | | 2.4 | 4.0 | | V |
| t_{IN} | Input Timing Reference Voltage | | 0.8 | | 2.0 | V |
| t_{OUT} | Output Timing Reference Voltage | | 0.8 | | 2.0 | V |

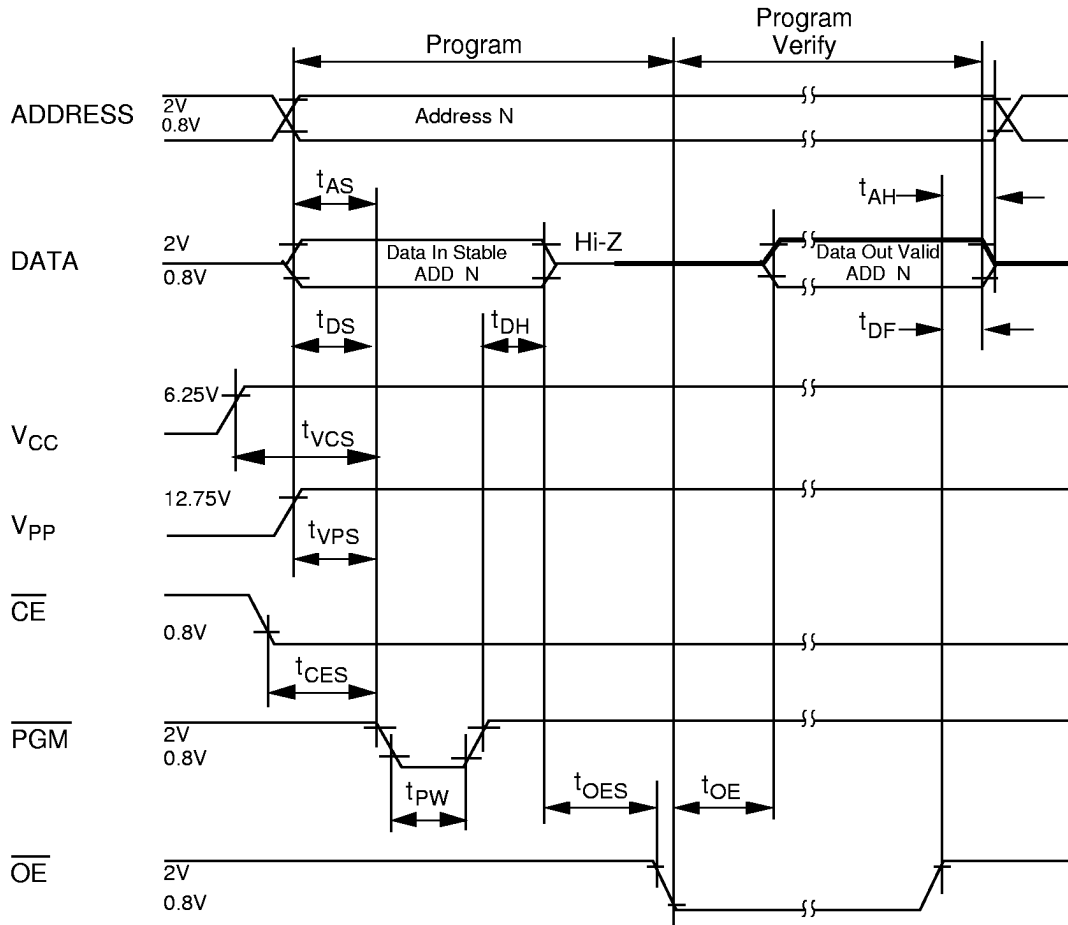
Note 14: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 15: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} . The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC} .

Note 16: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP} , V_{CC} to GND to suppress spurious voltage transients which may damage the device.

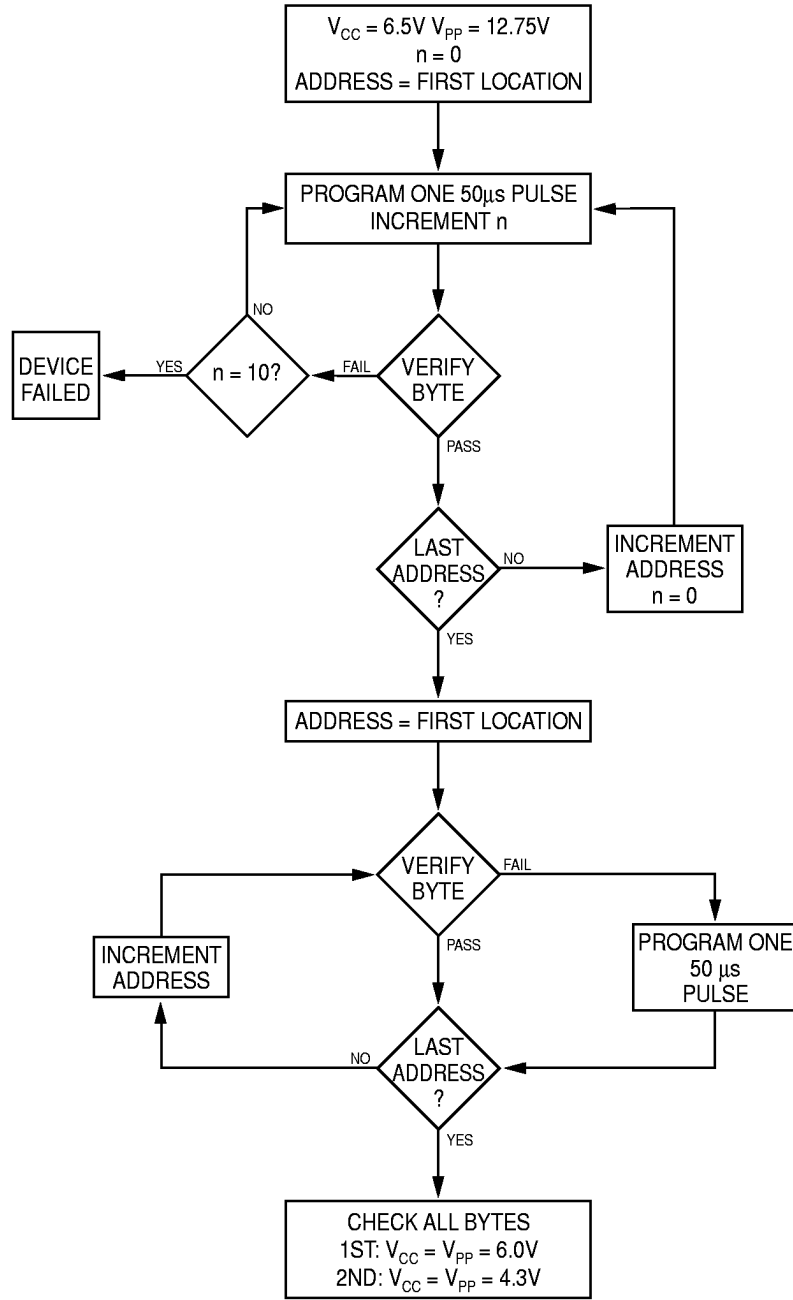
Note 17: During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP} .

Programming Waveforms (Note 16)



DS010835-5

Turbo Programming Algorithm Flow Chart



Note: The standard National Semiconductor Algorithm may also be used but it will have longer programming time.

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FIGURE 1.

Functional Description

DEVICE OPERATION

The six modes of operation of the device are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP} . The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.5V during the three programming modes, and at 5V in the other three modes.

Read Mode

The part has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Output OR-Tying

Because the part is usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

MODE SELECTION

The modes of operation of the NM27C020 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE 1. Modes Selection

| Mode | Pins | \overline{CE} | \overline{OE} | PGM | V_{PP} | V_{CC} | Outputs |
|-----------------|------|-----------------|-----------------|----------------|----------|----------|-----------|
| Read | | V_{IL} | V_{IL} | X (Note 18) | X | 5.0V | D_{OUT} |
| Output Disable | | X | V_{IH} | X | X | 5.0V | High Z |
| Standby | | V_{IH} | X | X | X | 5.0V | High Z |
| Programming | | V_{IL} | V_{IH} | V_{IL} | 12.75V | 6.25V | D_{IN} |
| Program Verify | | V_{IL} | V_{IL} | V_{IH} | 12.75V | 6.25V | D_{OUT} |
| Program Inhibit | | V_{IH} | X | X | 12.75V | 6.25V | High Z |

Note 18: X can be V_{IL} or V_{IH} .

To most efficiently use these two control lines, it is recommended that \overline{CE} be decoded and used as the primary device selecting function, while \overline{OE} be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all selected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the device.

Initially, and after each erasure, all bits of the device are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The part is in the programming mode when the V_{PP} power supply is at 12.75V and \overline{OE} is at V_{IH} . It is required that at least a 0.1 μF capacitor be placed across V_{PP} , V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50 μs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50 μs pulse. (The standard National Semiconductor Algorithm may also be used but it will have longer programming time.) The EPROM must not be programmed with a DC signal applied to the PGM input. Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for CE all like inputs (including OE) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's CE with V_{PP} at 12.75V will program that EPROM. A TTL high level CE input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} , except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The part has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table 2, specifically identifies the manufacturer and device type. The code for the NM27C020 is "8F8E," where "8F" designates that it is made by Fairchild Semiconductor, and "8E" designates a 2 Megabit byte-wide part.

The code is accessed by applying $12V \pm 0.5V$ to address pin A9. Addresses and control pins are held at V_{IL} , except A0. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0 -O7. Proper code access is only guaranteed at $25^{\circ}C \pm 5^{\circ}C$.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths

in the 3000 \AA - 4000 \AA range. After programming, opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537 \AA . The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The device should be placed within 1 inch of the lamp tubes during erasure. The device should be placed within 1 inch of the lamp tubes during erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and even system designs have been erroneously suspected when incomplete erasure was the problem.

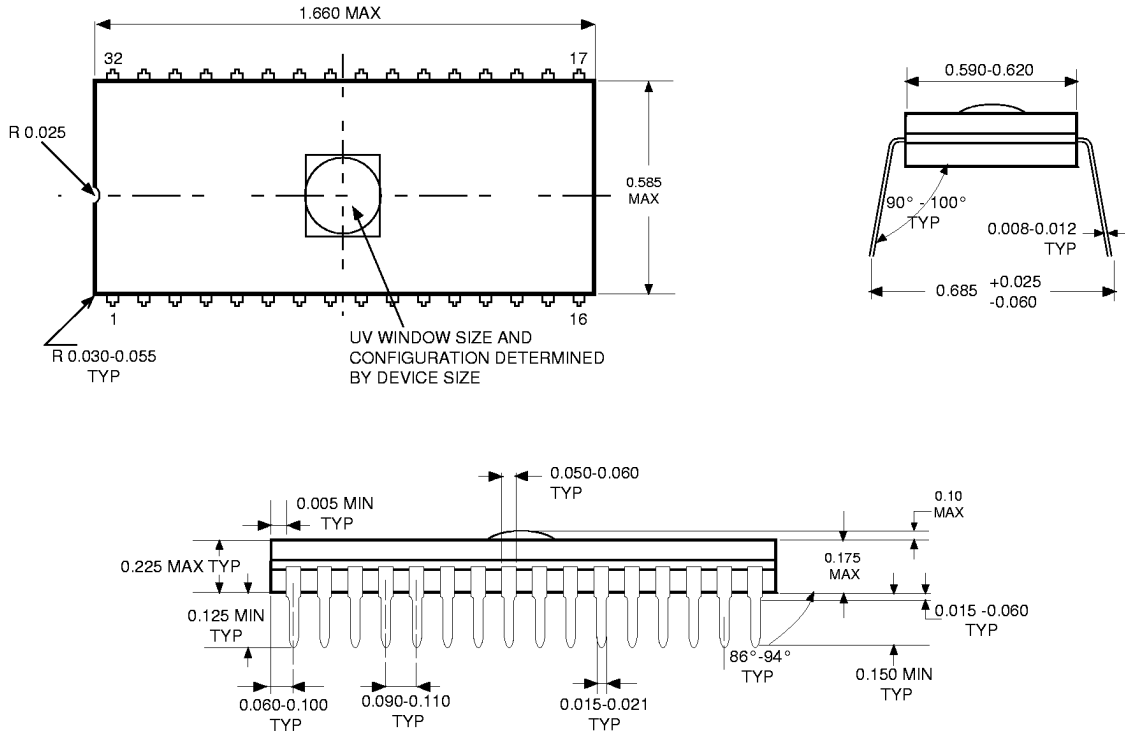
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

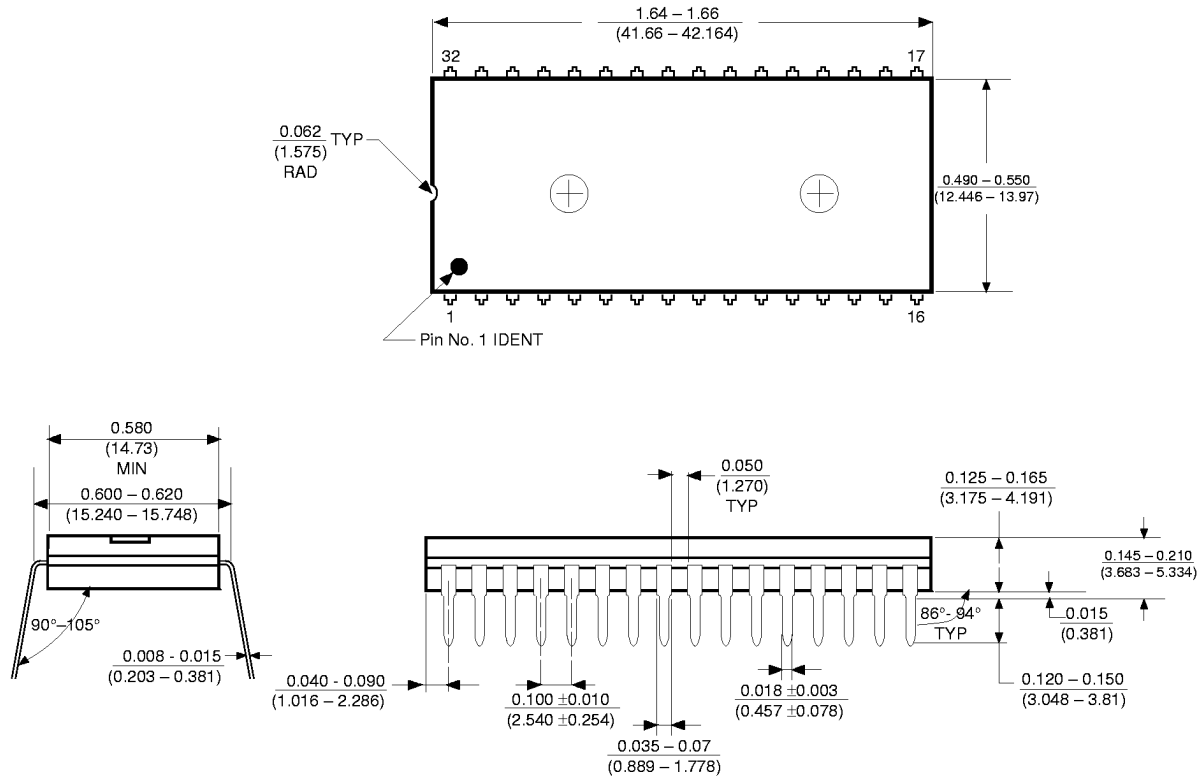
| Pins | A0 (12) | A9 (26) | O7 (21) | O6 (19) | O5 (18) | O4 (17) | O3 (16) | O2 (15) | O1 (14) | O0 (13) | Hex Data |
|-------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|
| Manufacturer Code | V_{IL} | 12V | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F |
| Device Code | V_{IH} | 12V | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |

Physical Dimensions inches (millimeters) unless otherwise noted



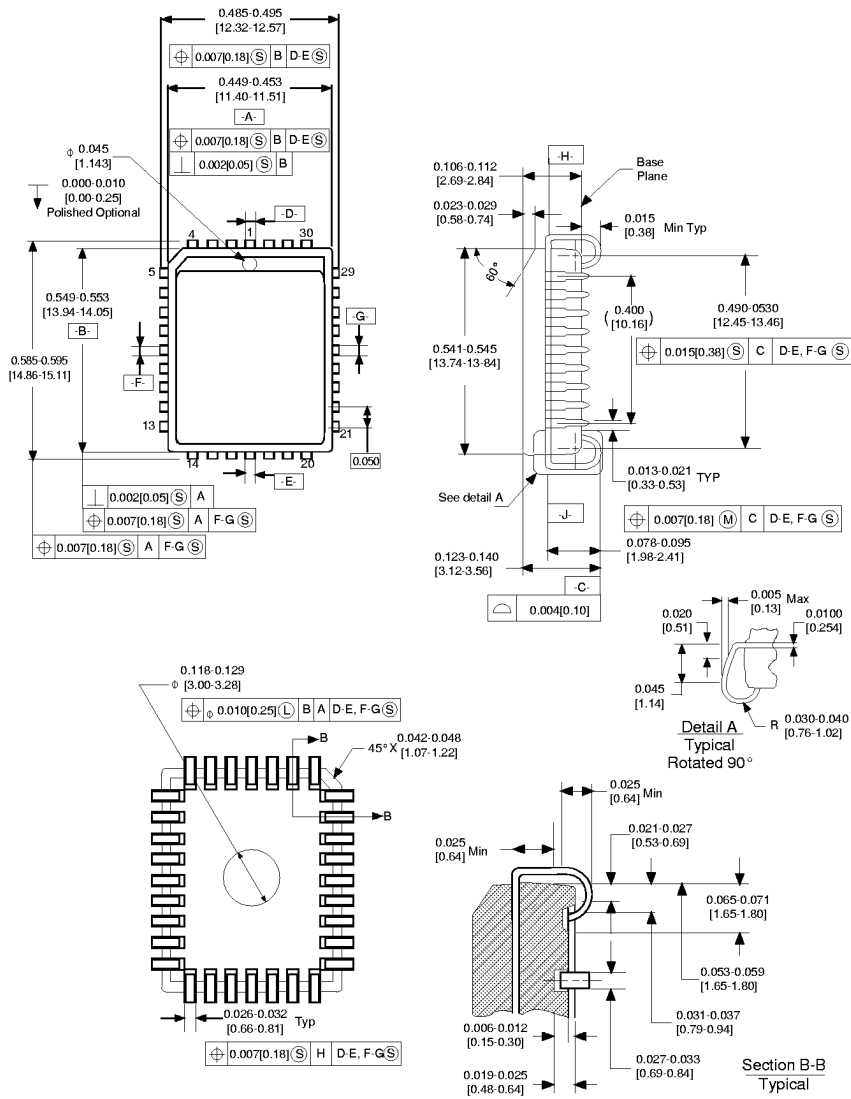
32-Lead EPROM Ceramic Dual-In-Line Package (Q)
Order Number NM27C020Q
Package Number J32AQ

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PDIP Package
Order Number NM27C020N

Physical Dimensions inches (millimeters) unless otherwise noted



32-Lead PLCC Package
Order Number NM27C020V
Package Number VA32A

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