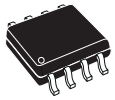
# L9856

## High voltage high-side driver

## Features

- High voltage rail up to 160 V
- dV/dt immunity ±50 V/nsec in full temperature range
- Driver current capability:
  500 mA source,
  500 mA sink
- Switching times 100 ns rise/fall with 2.5 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis
- Under voltage lock out
- Clamping on $V_{CC}$
- Loading circuit for external Bootstrap capacitor
- Inverting input
- Reset circuitry
- SO-8 package



**SO-8**

## Description

The L9856 is an high voltage device, manufactured with the BCD "OFF-LINE" technology.

It has the capability of driving N-Channel Power MOS transistors. The upper (floating) section is enabled to work with voltage rail up to 160 V. The logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

**Table 1. Device summary**

| Order code | Operating temp range, °C | Package | Packing |
|---|---|---|---|
| L9856 | -40 to +125 | SO-8 | Tube |
| L9856TR | -40 to +125 | SO-8 | Tape and Reel |



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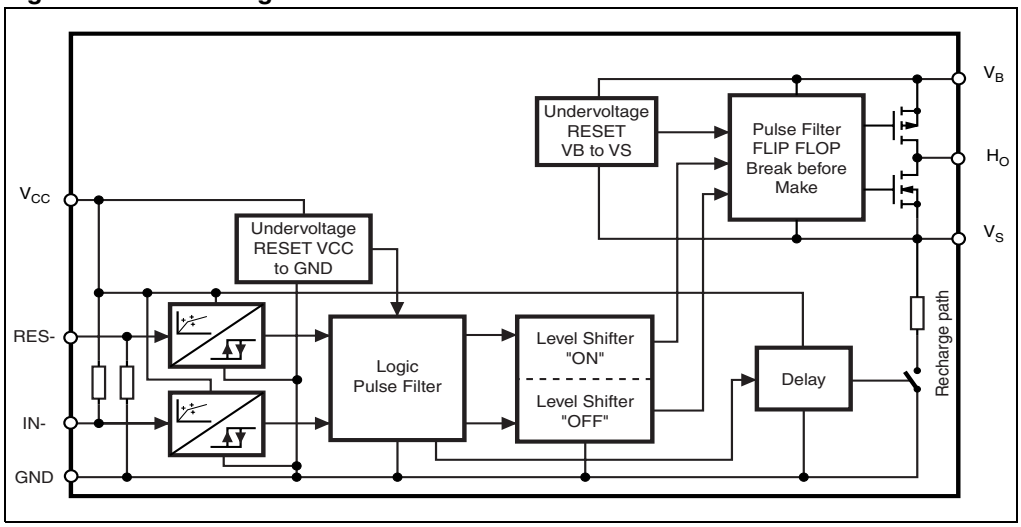
# 1 Block diagram andpin description

## 1.1 Block diagram

**Figure 1. Block diagram**




## 1.2 Pin description

**Figure 2. Pin connection (top view)**

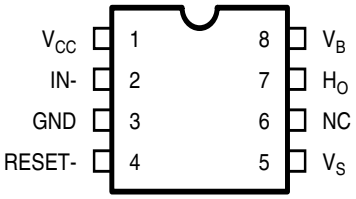



**Table 2. Pin function**

| Pin # | Pin name | Description |
|---|---|---|
| 1 | $V_{CC}$ | Driver supply, typical 5V |
| 2 | IN- | Driver control signal input (negative logic) |
| 3 | GND | Ground |
| 4 | RESET- | Driver enable signal input (negative logic) |
| 5 | $V_S$ | MOSFET source connection |
| 6 | NC | No connection (no bondwire) |
| 7 | $H_O$ | MOSFET gate connection |
| 8 | $V_B$ | Driver output stage supply |



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# 2 Electrical specifications

## 2.1 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th(j\text{-}amb)}$ | Thermal resistance junction to ambient | Max. | 150 | °C/W |

## 2.2 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. An operation above the absolute maximum limit is not implied and can damage the part.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $V_{BS}$ | High side floating supply voltage. | -0.3 | 20 | V |
| $V_B$ | High side driver output stage voltage neg. transient: 0.5 ms, external MOSFET off. | -5 | 166 | V |
| $V_S$ | High side floating supply offset voltage neg. transient 0.1 µs, repetitive pulse over lifetime at every switching event. | -8 | 150 | V |
| $V_{HO}$ | Output voltage gate connection. | $V_S$ - 0.3 | $V_B$ + 0.3 | V |
| $V_{CC}$ | Supply voltage. | -0.3 | 20 | V |
| $V_{IN}$ | Input voltage. | -0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input injection current. Full function, no latch-up; (guaranteed by design). Test at 5 V and 7 V on Eng. Samples. | --- | +1 | mA |
| $V_{RES}$ | Reset input voltage. | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{esd}$ | Electrostatic discharge voltage (human body model). | 2k | | V |
| $V_{CDM}$ | Charge device model CDM, EOS/ESD Ass. Std 5.3. Number of discharges per pin: 6. | 500 | | V |
| dV/dt | Allowable offset voltage slew rate. | -50 | 50 | V/nsec |
| $T_J$ | Junction temperature. | -55 | 150 | °C |
| $T_{stg}$ | Storage temperature. | -55 | 150 | |
| $T_L$ | Lead temperature (Soldering, 10 seconds) 3 times Bosch soldering profile acc. to Bosch soldering conditions, Gen. Spec. | - | 300 | |



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## 2.3 Recommended operating conditions

For proper operations the device should be used within the recommended conditions.

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Value | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| $V_B$[1] | High side driver output stage voltage | VS+4.4 | VS+18 | V |
| $V_S$ | High side floating supply offset voltage<br>(25°C)<br>(125°C) | <br>-3.2<br>-2.9 | <br>150<br>150 | V |
| $V_{HO}$ | Output voltage gate connection | $V_S$ | $V_B$ | V |
| $V_{CC}$ | Supply voltage | 4.4 | 6.5 | V |
| $V_{IN}$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_{RES}$ | Reset input voltage | 0 | $V_{CC}$ | V |
| dV/dt[2] | Allowable offset voltage slew rate | -50 | 50 | V/nsec |
| $F_S$ | Switching frequency | | 200 | kHz |

1. Reset-Logic functional for $V_{BS}$ > 2V, independent from $V_{CC}$-level.
2. Guaranteed by design.

## 2.4 Electrical characteristics

**Table 6. Electrical characteristics**

Unless otherwise specified, $V_{CC}$ = 5 V, $V_{BS}$ = 7 V, $V_S$ = 0 V, IN = 0 V, RES = 5 V, load R = 50 Ω, C = 2.5 nF. Unless otherwise noted, these specifications apply for an operating ambient temperature range of -40 °C < $T_{amb}$ < 125 °C.

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ supply** | | | | | | |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going threshold | $V_{CC}$ rising from 0 V | | | 4.3 | V |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going threshold | $V_{CC}$ dropping from 5 V | 2.8 | | | |
| $V_{CCUVHYS}$ | $V_{CC}$ supply undervoltage lockout hysteresis | | 0.02 | 0.3 | 0.6 | |
| $td_{UVCC}$ | Undervoltage lockout response time | $V_{CC}$ steps either from 6.5 V to 2.7 V or from 2.7 V to 6.5 V | 0.5 | | 20 | µs |
| $I_{QCC}$ | $V_{CC}$ supply current | | | | 400 | µA |



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**Table 6. Electrical characteristics (continued)**

Unless otherwise specified, $V_{CC}$ = 5 V, $V_{BS}$ = 7 V, $V_S$ = 0 V, IN = 0 V, RES = 5 V, load R = 50 Ω, C = 2.5 nF. Unless otherwise noted, these specifications apply for an operating ambient temperature range of -40 °C < $T_{amb}$ < 125 °C.

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$V_{BS}$ supply** | | | | | | |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold | $V_{CC}$ rising from 0 V | | | 4.3 | V |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold | $V_{CC}$ dropping from 5 V | 2.8 | | | V |
| $V_{BSUVHYS}$ | $V_{BS}$ supply undervoltage lockout hysteresis | | 0.02 | 0.3 | 0.4 | |
| $td_{UVBS}$ | Undervoltage lockout response time | $V_{BS}$ steps either from 6.5 V to 2.7 V or from 2.7 V to 6.5V | 0.5 | | 20 | µs |
| $I_{QBS1}$ | $V_{BS}$ supply current | static mode, IN = 0 V or 5 V | | | 100 | µA |
| $I_{QBS2}$ | | static mode, $V_{BS}$ = 16 V, IN = 0 V or 5 V | | | 200 | µA |
| $\Delta V_{BS}$ | $V_{BS}$ drop due to output turn-on | $C_{BS}$ = 1 µF, $td_{IG-IN}$ = 3µs, $t_{TEST}$ = 100µs | | | 210 | mV |
| **Gate driver characteristics** | | | | | | |
| $I_{PKSo1}$ | Peak output source current | $T_j$ = 25 °C | 120 | 250 | | mA |
| $I_{PKSo2}$ | | | 70 | 150 | | |
| $I_{PKSo3}$ | | $V_{BS}$ = 16V , $T_j$ = 25 °C | 250 | 500 | | |
| $I_{PKSo4}$ | | $V_{BS}$ = 16 V | 150 | 300 | | |
| $I_{HO,off}$ | HO off state leakage current | guaranteed by design | | | 1 | µA |
| $t_{r1}$ | Output rise time | $T_j$ = 25 °C | | 0.2 | 0.4 | µs |
| $t_{r2}$ | | | | 0.3 | 0.5 | |
| $t_{r3}$ | | $V_{BS}$ = 16 V, $T_j$ = 25 °C | | 0.1 | 0.2 | |
| $t_{r4}$ | | $V_{BS}$ = 16 V | | 0.15 | 0.3 | |
| $I_{PKSi1}$ | Peak output sink current | IN = 5 V, $T_j$ = 25 °C | 120 | 250 | | mA |
| $I_{PKSi2}$ | | IN = 5 V | 70 | 150 | | |
| $I_{PKSi3}$ | | IN = 5 V, $T_j$ = 25 °C $V_{BS}$ = 16 V | 250 | 500 | | |
| $I_{PKSi4}$ | | IN = 5 V, $V_{BS}$ = 16 V | 150 | 300 | | |
| $t_{f1}$ | Output fall time | IN = 5 V, $T_j$ = 25 °C | | 0.2 | 0.4 | µs |
| $t_{f2}$ | | IN = 5 V, | | 0.3 | 0.5 | |
| $t_{f3}$ | | $V_{BS}$ = 16 V, IN = 5 V, $T_j$ = 25 °C | | 0.1 | 0.2 | |
| $t_{f4}$ | | $V_{BS}$ = 16 V, IN = 5 V, | | 0.15 | 0.3 | |



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**Table 6. Electrical characteristics (continued)**

Unless otherwise specified, $V_{CC}$ = 5 V, $V_{BS}$ = 7 V, $V_S$ = 0 V, IN = 0 V, RES = 5 V, load R = 50 Ω, C = 2.5 nF. Unless otherwise noted, these specifications apply for an operating ambient temperature range of -40 °C < $T_{amb}$ < 125 °C.

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{plhi}$ | Input-to-output turn-on propagation delay (50 % input level to 10 % output level) | | | 0.1 | 0.35 | µs |
| $t_{phli}$ | Input-to-output turn-off propagation delay (50 % input level to 90 % output level) | | | 0.1 | 0.4 | |
| $t_{plhr}$ | RES-to-output turn-on propagation delay (50 % input level to 10% output level) | | | 0.1 | 0.4 | |
| $t_{phlr}$ | RES-to-output turn-off propagation delay (50 % input level to 90 % output level) | | | 0.1 | 0.4 | |
| **Input characteristics** | | | | | | |
| $V_{INH}$ | High logic level input threshold | $V_{CC}$ = 5V | 0.6 $V_{CC}$ | | | V |
| $V_{INL}$ | Low logic level input threshold | | | | 0.28 $V_{CC}$ | |
| $R_{IN}$ | High logic level input resistance | | 60 | 100 | 250 | kΩ |
| $I_{IN}$ | High logic level input current | $V_{IN}$ = $V_{CC}$ | | | 5 | µA |
| $V_{RESH}$ | High logic level RES input threshold | $V_{CC}$ = 5V | 0.6 $V_{CC}$ | | | |
| $V_{RESL}$ | Low logic level RES input threshold | | | | 0.28 $V_{CC}$ | |
| $R_{RES}$ | High logic level RES Input resistance | | 60 | 100 | 250 | kΩ |
| $I_{RES}$ | Low logic level input current | $V_{RES}$ = 0 | | | 5 | µA |
| **Recharge characteristics** | | | | | | |
| $t_{on\_rech}$ | Recharge transistor turn-on propagation delay | $V_S$ = 5V | 3 | 6 | 9 | µs |
| $t_{off\_rech}$ | Recharge transistor turn-off propagation delay | | | 0.1 | 0.5 | µs |
| $V_{RECH}$ | Recharge output transistor on-state voltage drop | 1 mA forced on recharge path on | 0.5 | | 1.2 | V |
| **Deadtime characteristics** | | | | | | |
| $DT_{HOFF}$ | High side turn-off to recharge gate turn-on | $V_{CC}$ = 5 V | 3 | 6 | 9 | µs |
| $DT_{HON}$ | Recharge gate turn-off to high side turn-on | | 0.1 | 0.4 | 0.7 | |



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## 2.5 Logic table

**Table 7. Logic table**

| Supply voltages and thresholds | | Signals | | Output Ho | Recharge path |
|---|---|---|---|---|---|
| $V_{cc}$ | $V_{BS}$ | RESET- | IN- | | |
| < $V_{CCUV-}$ | X | X | X | OFF | ON |
| X | X | LOW | X | OFF | ON |
| X | X | X | HIGH | OFF | ON |
| > $V_{CCUV+}$ | > $V_{BSUV+}$ | HIGH | LOW | ON | OFF |
| > $V_{CCUV+}$ | < $VB_{SUV-}$ | HIGH | LOW | OFF | OFF |

*Note: X means independent from signal.*



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# 3 Timing diagrams

**Figure 3. Input/output timing diagram**

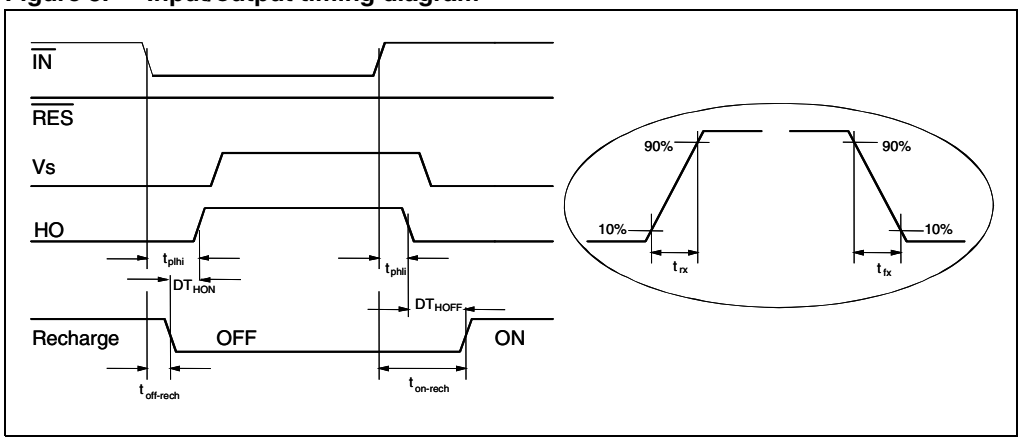
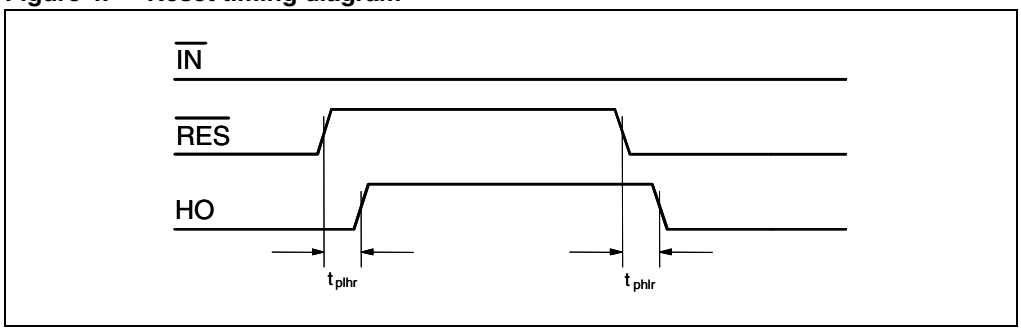



**Figure 4. Reset timing diagram**



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# 4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

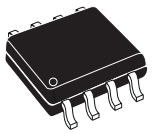
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 5. SO-8 mechanical data and package dimensions**

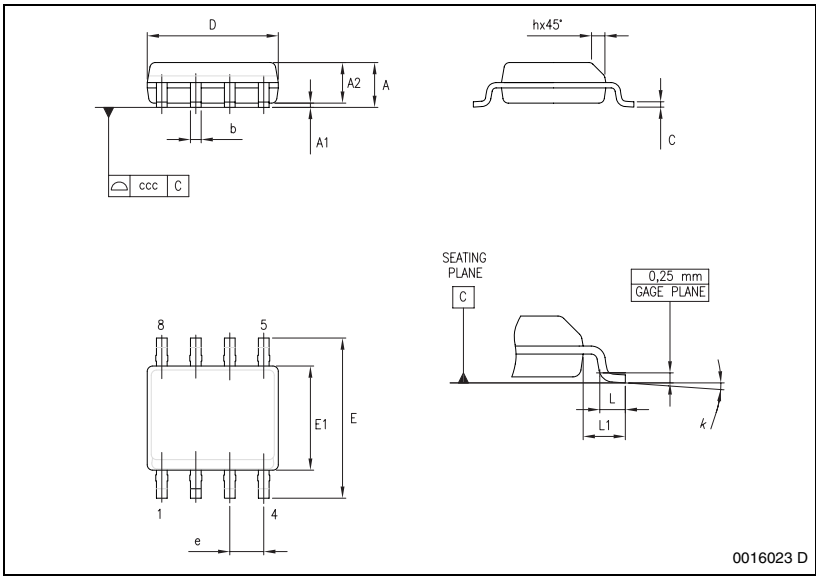
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.750 | | | 0.0689 |
| A1 | 0.100 | | 0.250 | 0.0039 | | 0.0098 |
| A2 | 1.250 | | | 0.0492 | | |
| b | 0.280 | | 0.480 | 0.0110 | | 0.0189 |
| c | 0.170 | | 0.230 | 0.0067 | | 0.0091 |
| D (1) | 4.800 | 4.900 | 5.000 | 0.1890 | 0.1929 | 0.1969 |
| E | 5.800 | 6.000 | 6.200 | 0.2283 | 0.2362 | 0.2441 |
| E1(2) | 3.800 | 3.900 | 4.000 | 0.1496 | 0.1535 | 0.1575 |
| e | | 1.270 | | | 0.0500 | |
| h | 0.250 | | 0.500 | 0.0098 | | 0.0197 |
| L | 0.400 | | 1.270 | 0.0157 | | 0.0500 |
| L1 | | 1.040 | | | 0.0409 | |
| k | 0° | | 8° | 0° | | 8° |
| ccc | | | 0.100 | | | 0.0039 |

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

**OUTLINE AND MECHANICAL DATA**



**SO-8**



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# 5 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 29-Jun-2007 | 1 | Initial release. |
| 30-May-2008 | 2 | Update Features section on page 1.<br>Updated *Table 4: Absolute maximum ratings on page 6*.<br>Updated *Table 5: Recommended operating conditions on page 7*. |



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