19-3502; Rev 5; 5/07

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

General Description

The MAX5062/MAX5063/MAX5064 high-frequency, 125V half-bridge, n-channel MOSFET drivers drive high- and low-side MOSFETs in high-voltage applications. These drivers are independently controlled and their 35ns typical propagation delay, from input to output, are matched to within 3ns (typ). The high-voltage operation with very low and matched propagation delay between drivers, and high source/sink current capabilities in a thermally enhanced package make these devices suitable for the high-power, high-frequency telecom power converters. The 125V maximum input voltage range provides plenty of margin over the 100V input transient requirement of telecom standards. A reliable on-chip bootstrap diode connected between V_{DD} and BST eliminates the need for an external discrete diode.

The MAX5062A/C and the MAX5063A/C offer both noninverting drivers (see the *Selector Guide*). The MAX5062B/D and the MAX5063B/D offer a noninverting high-side driver and an inverting low-side driver. The MAX5064A/B offer two inputs per driver that can be either inverting or noninverting. The MAX5062A/B/C/D and the MAX5064A feature CMOS (V_{DD} / 2) logic inputs. The MAX5063A/B/C/D and the MAX5064B feature TTL logic inputs. The MAX5064A/B include a break-before-make adjustment input that sets the dead time between drivers from 16ns to 95ns. The drivers are available in the industry-standard 8-pin SO footprint and pin configuration, and a thermally enhanced 8-pin SO and 12-pin (4mm x 4mm) thin QFN packages. All devices operate over the -40°C to +125°C automotive temperature range.

Applications

Telecom Half-Bridge Power Supplies

Two-Switch Forward Converters

Full-Bridge Converters

Active-Clamp Forward Converters

Power-Supply Modules

Motor Control

Features

- **HIP2100/HIP2101 Pin Compatible (MAX5062A/MAX5063A)**
- **Up to 125V Input Operation**
- **8V to 12.6V V_{DD} Input Voltage Range**
- **2A Peak Source and Sink Current Drive Capability**
- **35ns Typical Propagation Delay**
- **Guaranteed 8ns Propagation Delay Matching Between Drivers**
- **Programmable Break-Before-Make Timing (MAX5064)**
- **Up to 1MHz Combined Switching Frequency while Driving 100nC Gate Charge (MAX5064)**
- **Available in CMOS (V_{DD} / 2) or TTL Logic-Level Inputs with Hysteresis**
- **Up to 15V Logic Inputs Independent of Input Voltage**
- **Low 2.5pF Input Capacitance**
- **Instant Turn-Off of Drivers During Fault or PWM Start-Stop Synchronization (MAX5064)**
- **Low 200µA Supply Current**
- **Versions Available With Combination of Noninverting and Inverting Drivers (MAX5062B/D and MAX5063B/D)**
- **Available in 8-Pin SO, Thermally Enhanced SO, and 12-Pin Thin QFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX5062AASA	-40°C to +125°C	8 SO	—	S8-5
MAX5062BASA	-40°C to +125°C	8 SO	—	S8-5
MAX5062CASA	-40°C to +125°C	8 SO-EP*	—	S8E-14
MAX5062DASA	-40°C to +125°C	8 SO-EP*	—	S8E-14

**EP = Exposed paddle.*

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Ordering Information continued at end of data sheet.

Selector Guide

PART	HIGH-SIDE DRIVER	LOW-SIDE DRIVER	LOGIC LEVELS	PIN COMPATIBLE
MAX5062AASA	Noninverting	Noninverting	CMOS (V_{DD} / 2)	HIP 2100IB
MAX5062BASA	Noninverting	Inverting	CMOS (V_{DD} / 2)	—
MAX5062CASA	Noninverting	Noninverting	CMOS (V_{DD} / 2)	—
MAX5062DASA	Noninverting	Inverting	CMOS (V_{DD} / 2)	—

Selector Guide continued at end of data sheet.

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{DD}, IN_H, IN_L, IN_L+, IN_L-, IN_H+, IN_H-.....-0.3V to +15V
DL, BBM .....-0.3V to (V_{DD} + 0.3V)
HS.....-5V to +130V
DH to HS.....-0.3V to (V_{DD} + 0.3V)
BST to HS .....-0.3V to +15V
AGND to PGND (MAX5064).....-0.3V to +0.3V
dV/dt at HS 50V/ns
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....470.6mW
8-Pin SO with Exposed Pad (derate 19.2mW/°C above +70°C)* 1538.5mW
12-Pin Thin QFN (derate 24.4mW/°C above +70°C)* 1951.2mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Per JEDEC 51 standard multilayer board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, BBM = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Supply Voltage	V_{DD}	(Note 2)		8.0		12.6	V
V_{DD} Quiescent Supply Current	I_{DD}	IN_H = IN_L = GND (no switching)	MAX5062_/ MAX5063_		70	140	µA
			MAX5064_		120	260	
V_{DD} Operating Supply Current	I_{DDO}	f_{SW} = 500kHz, V_{DD} = +12V				3	mA
BST Quiescent Supply Current	I_{BST}	IN_H = IN_L = GND (no switching)			15	40	µA
BST Operating Supply Current	I_{BSTO}	f_{SW} = 500kHz, V_{DD} = V_{BST} = +12V				3	mA
UVLO (V_{DD} to GND)	$UVLO_{VDD}$	V_{DD} rising		6.5	7.3	8.0	V
UVLO (BST to HS)	$UVLO_{BST}$	BST rising		6.0	6.9	7.8	V
UVLO Hysteresis					0.5		V
LOGIC INPUT							
Input-Logic High	$V_{IH\_}$	MAX5062_/MAX5064A, CMOS (V_{DD} / 2) version		0.67 x V_{DD}	0.55 x V_{DD}		V
		MAX5063_/MAX5064B, TTL version		2	1.65		
Input-Logic Low	$V_{IL\_}$	MAX5062_/MAX5064A, CMOS (V_{DD} / 2) version			0.4 x V_{DD}	0.33 x V_{DD}	V
		MAX5063_/MAX5064B, TTL version			1.4	0.8	
Logic-Input Hysteresis	V_{HYS}	MAX5062_/MAX5064A, CMOS (V_{DD} / 2) version			1.6		V
		MAX5063_/MAX5064B, TTL version			0.25		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, BBM = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic-Input Current	I_IN	V_{IN_H+}, V_{IN_L+} = 0V		-1	0.001	+1	µA
		V_{IN_L} = V_{DD} for MAX5062B/D, MAX5063B/D					
		V_{IN_H-}, V_{IN_L-}, V_{IN_H} = V_{DD}					
		V_{IN_L} = 0V for MAX5062A/C, MAX5063A/C					
Input Resistance	R_{IN}	IN_H+, IN_L+ IN_H, to GND			1		MΩ
		IN_L to V_{DD} for MAX5062B/D, MAX5063B/D					
		IN_H-, IN_L-, IN_H, to V_{DD}					
		IN_L for MAX5062A/C, MAX5063A/C to GND					
Input Capacitance	C_{IN}				2.5		pF
HIGH-SIDE GATE DRIVER							
HS Maximum Voltage	V_{HS_MAX}			125			V
BST Maximum Voltage	V_{BST_MAX}			140			V
Driver Output Resistance (Sourcing)	R_{ON_HP}	V_{DD} = 12V, I_{DH} = 100mA (sourcing)	T_A = +25°C		2.5	3.3	Ω
			T_A = +125°C		3.5	4.6	
Driver Output Resistance (Sinking)	R_{ON_HN}	V_{DD} = 12V, I_{DH} = 100mA (sinking)	T_A = +25°C		2.1	2.8	Ω
			T_A = +125°C		3.2	4.2	
DH Reverse Current (Latchup Protection)		(Note 3)		400			mA
Power-Off Pulldown Clamp Voltage		V_{BST} = 0V or floating, I_{DH} = 1mA (sinking)			0.94	1.16	V
Peak Output Current (Sourcing)	I_{DH_PEAK}	C_L = 10nF, V_{DH} = 0V			2		A
Peak Output Current (Sinking)		C_L = 10nF, V_{DH} = 12V			2		A
LOW-SIDE GATE DRIVER							
Driver Output Resistance (Sourcing)	R_{ON_LP}	V_{DD} = 12V, I_{DL} = 100mA (sourcing)	T_A = +25°C		2.5	3.3	Ω
			T_A = +125°C		3.5	4.6	
Driver Output Resistance (Sinking)	R_{ON_LN}	V_{DD} = 12V, I_{DL} = 100mA (sinking)	T_A = +25°C		2.1	2.8	Ω
			T_A = +125°C		3.2	4.2	
Reverse Current at DL (Latchup Protection)		(Note 3)		400			mA
Power-Off Pulldown Clamp Voltage		V_{DD} = 0V or floating, I_{DL} = 1mA (sinking)			0.95	1.16	V
Peak Output Current (Sourcing)	I_{PK_LP}	C_L = 10nF, V_{DL} = 0V			2		A
Peak Output Current (Sinking)	I_{PK_LN}	C_L = 10nF, V_{DL} = 12V			2		A
INTERNAL BOOTSTRAP DIODE							
Forward Voltage Drop	V_f	I_{BST} = 100mA			0.91	1.11	V
Turn-On and Turn-Off Time	t_R	I_{BST} = 100mA			40		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{BST} = +8V to +12.6V, V_{HS} = GND = 0V, BBM = open, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C.) (Note 1)

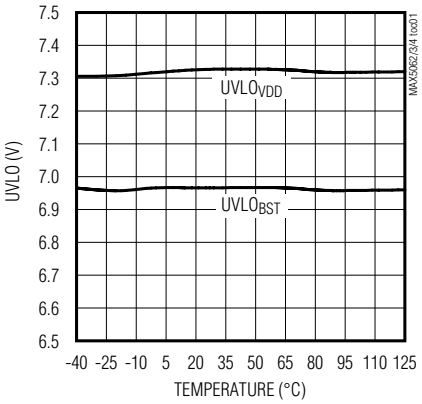
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS FOR HIGH- AND LOW-SIDE DRIVERS (V_{DD} = V_{BST} = +12V)							
Rise Time	t_R	C_L = 1000pF			7		ns
		C_L = 5000pF			33		
		C_L = 10,000pF			65		
Fall Time	t_F	C_L = 1000pF			7		ns
		C_L = 5000pF			33		
		C_L = 10,000pF			65		
Turn-On Propagation Delay Time	t_{D_ON}	Figure 1, C_L = 1000pF (Note 3)	CMOS		30	55	ns
			TTL		35	63	
Turn-Off Propagation Delay Time	t_{D_OFF}	Figure 1, C_L = 1000pF (Note 3)	CMOS		30	55	ns
			TTL		35	63	
Delay Matching Between Inverting Input to Output and Noninverting Input to Output	t_{MATCH1}	C_L = 1000pF, BBM open for MAX5064, Figure 1 (Note 3)			2	8	ns
Delay Matching Between Driver-Low and Driver-High	t_{MATCH2}	C_L = 1000pF, BBM open for MAX5064, Figure 1 (Note 3)			2	8	ns
Break-Before-Make Accuracy (MAX5064 Only)		R_{BBM} = 10kΩ			16		ns
		R_{BBM} = 47kΩ (Notes 3, 4)		40	56	72	
		R_{BBM} = 100kΩ			95		
Internal Nonoverlap					1		ns
Minimum Pulse-Width Input Logic (High or Low) (Note 5)	t_{PW-MIN}	V_{DD} = V_{BST} = 12V			135		ns
		V_{DD} = V_{BST} = 8V			170		

Note 1: All devices are 100% tested at T_A = +125°C. Limits over temperature are guaranteed by design.
Note 2: Ensure that the V_{DD}-to-GND or BST-to-HS voltage does not exceed 13.2V.
Note 3: Guaranteed by design, not production tested.
Note 4: Break-before-make time is calculated by t_{BBM} = 8ns x (1 + R_{BBM} / 10kΩ).
Note 5: See the *Minimum Pulse Width* section.

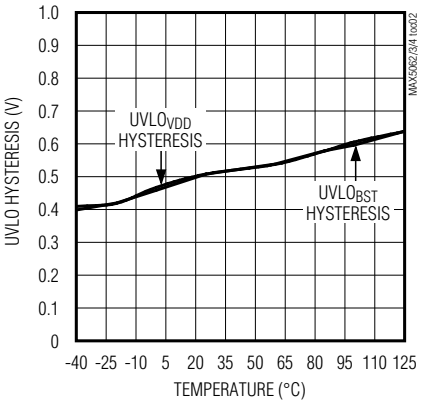
Typical Operating Characteristics

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

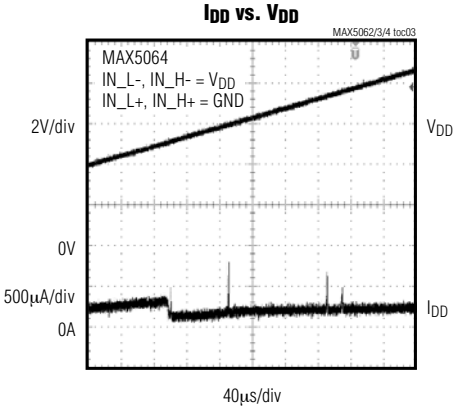
UNDERVOLTAGE LOCKOUT (V_{DD} AND V_{BST} RISING) vs. TEMPERATURE



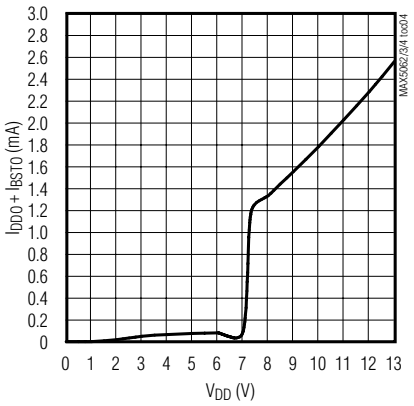
V_{DD} AND BST UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE



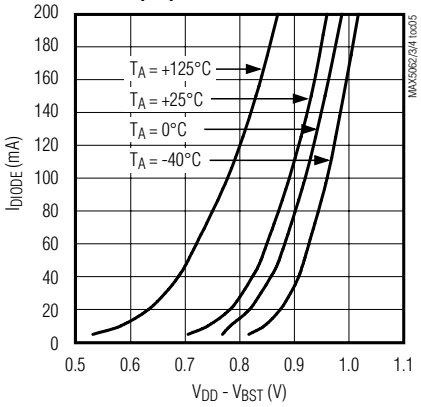
I_{DD} vs. V_{DD}



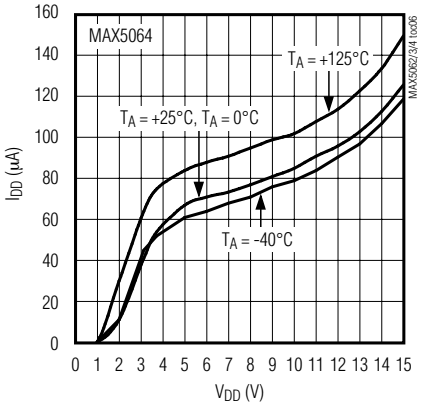
I_{DDO} + I_{BSTO} vs. V_{DD} (f_{SW} = 250kHz)



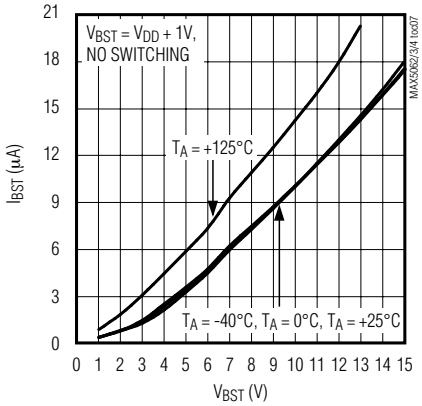
INTERNAL BST DIODE (I-V) CHARACTERISTICS



V_{DD} QUIESCENT CURRENT vs. V_{DD} (NO SWITCHING)



BST QUIESCENT CURRENT vs. BST VOLTAGE

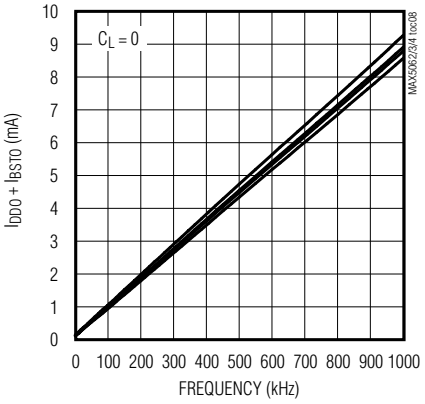


125V/2A, High-Speed, Half-Bridge MOSFET Drivers

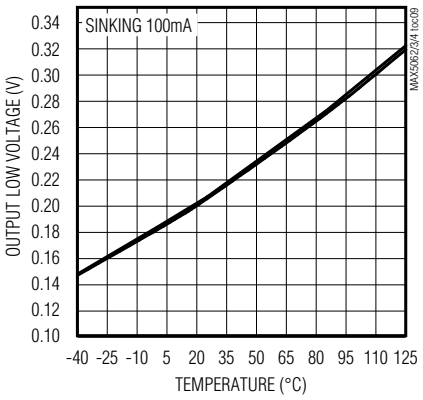
Typical Operating Characteristics (continued)

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

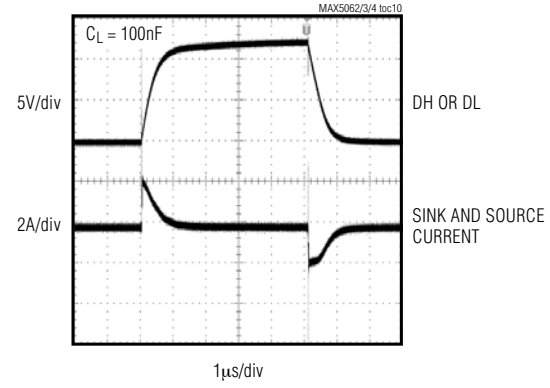
V_{DD} AND BST OPERATING SUPPLY CURRENT vs. FREQUENCY



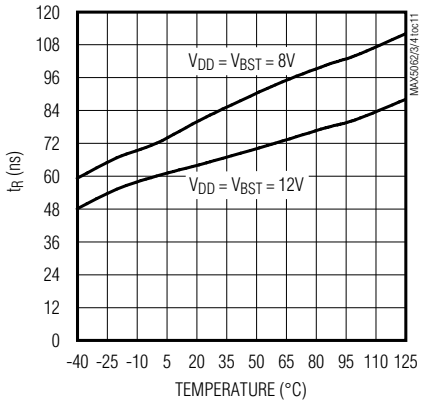
DH OR DL OUTPUT LOW VOLTAGE vs. TEMPERATURE



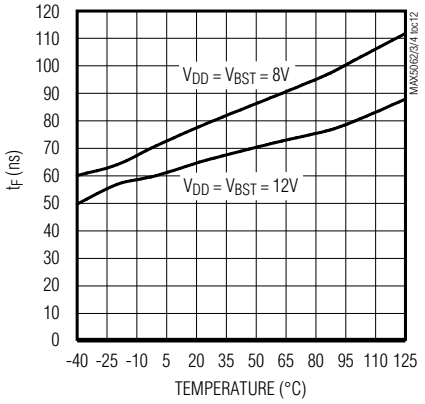
PEAK DH AND DL SOURCE/SINK CURRENT



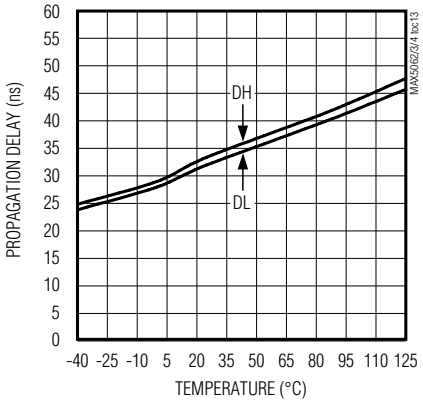
DH OR DL RISE TIME vs. TEMPERATURE (C_L = 10nF)



DH OR DL FALL TIME vs. TEMPERATURE (C_{LOAD} = 10nF)



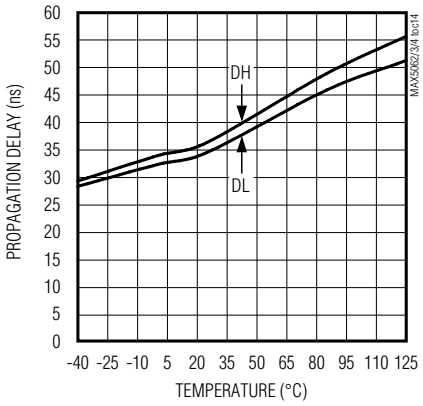
DH OR DL RISE PROPAGATION DELAY vs. TEMPERATURE



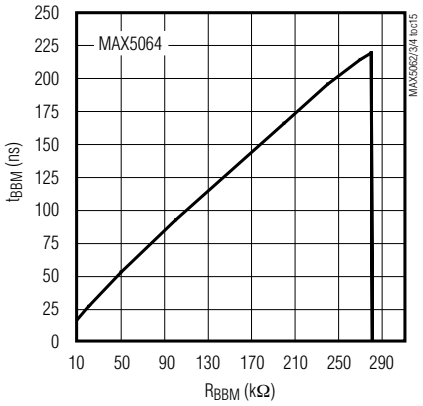
Typical Operating Characteristics (continued)

(Typical values are at V_{DD} = V_{BST} = +12V and T_A = +25°C, unless otherwise specified.)

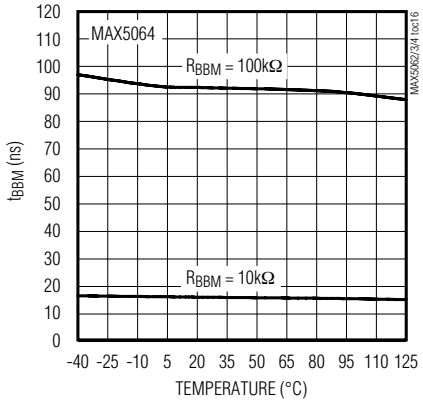
DH OR DL FALL PROPAGATION DELAY vs. TEMPERATURE



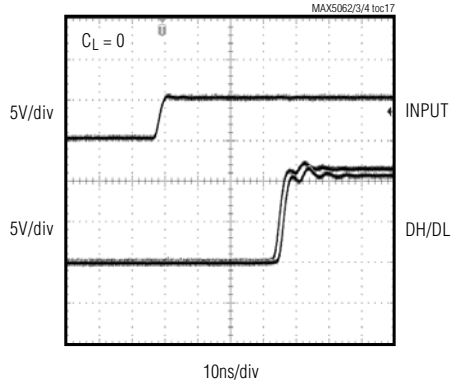
BREAK-BEFORE-MAKE DEAD TIME vs. R_{BBM}



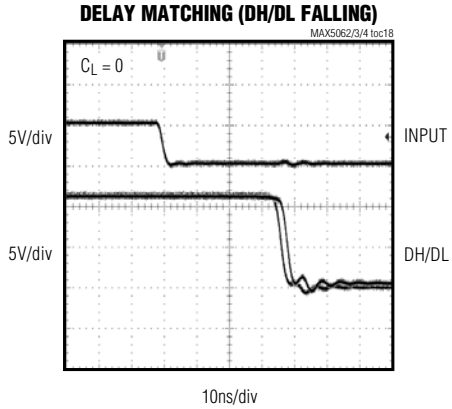
BREAK-BEFORE-MAKE DEAD TIME vs. TEMPERATURE



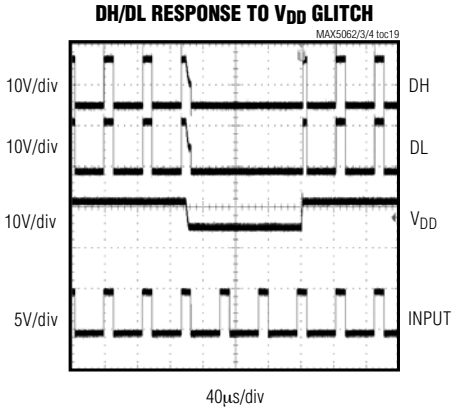
DELAY MATCHING (DH/DL RISING)



DELAY MATCHING (DH/DL FALLING)



DH/DL RESPONSE TO V_{DD} GLITCH



125V/2A, High-Speed, Half-Bridge MOSFET Drivers

MAX5062/MAX5063 Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Input. Bypass to GND with a parallel combination of 0.1µF and 1µF ceramic capacitor.
2	BST	Boost Flying Capacitor Connection. Connect a 0.1µF ceramic capacitor between BST and HS for the high-side MOSFET driver supply.
3	DH	High-Side-Gate Driver Output. Driver output for the high-side MOSFET gate.
4	HS	Source Connection for High-Side MOSFET. Also serves as a return terminal for the high-side driver.
5	IN_H	High-Side Noninverting Logic Input
6	IN_L	Low-Side Noninverting Logic Input (MAX5062A/C, MAX5063A/C). Low-side inverting logic input (MAX5062B/D, MAX5063B/D).
7	GND	Ground. Use GND as a return path to the DL driver output and IN_H/IN_L inputs.
8	DL	Low-Side-Gate Driver Output. Drives low-side MOSFET gate.
—	EP	Exposed Pad. Internally connected to GND. Externally connect the exposed pad to a large ground plane to aid in heat dissipation (MAX5062C/D, MAX5063C/D only).

MAX5064 Pin Description

PIN	NAME	FUNCTION
1	BST	Boost Flying Capacitor Connection. Connect a 0.1µF ceramic capacitor between BST and HS for the high-side MOSFET driver supply.
2	DH	High-Side-Gate Driver Output. Drives high-side MOSFET gate.
3	HS	Source Connection for High-Side MOSFET. Also serves as a return terminal for the high-side driver.
4	AGND	Analog Ground. Return path for low-switching current signals. IN_H/IN_L inputs referenced to
5	BBM	Break-Before-Make Programming Resistor Connection. Connect a 10kΩ to 100kΩ resistor from BBM to AGND to program the break-before-make time (t_{BBM}) from 16ns to 95ns. Resistance values greater than 200kΩ disables the BBM function and makes t_{BBM} = 1ns. Bypass this pin with at least a 1nF capacitor to AGND.
6	IN_H-	High-Side Inverting CMOS (V_{DD} / 2) (MAX5064A), or TTL (MAX5064B) Logic Input. Connect to AGND when not used.
7	IN_H+	High-Side Noninverting CMOS (V_{DD} / 2) (MAX5064A), or TTL (MAX5064B) Logic Input. Connect to V_{DD} when not used.
8	IN_L-	Low-Side Inverting CMOS (V_{DD} / 2) (MAX5064A), or TTL (MAX5064B) Logic Input. Connect to AGND when not used.
9	IN_L+	Low-Side Noninverting CMOS (V_{DD} / 2) (MAX5064A), or TTL (MAX5064B) Logic Input. Connect to V_{DD} when not used.
10	PGND	Power Ground. Return path for high-switching current signals. Use PGND as a return path for the low-side driver.
11	DL	Low-Side-Gate Driver Output. Drives the low-side MOSFET gate.
12	V_{DD}	Power Input. Bypass to PGND with a 0.1µF ceramic in parallel with a 1µF ceramic capacitor.
—	EP	Exposed Pad. Internally connected to AGND. Externally connect to a large ground plane to aid in heat dissipation.

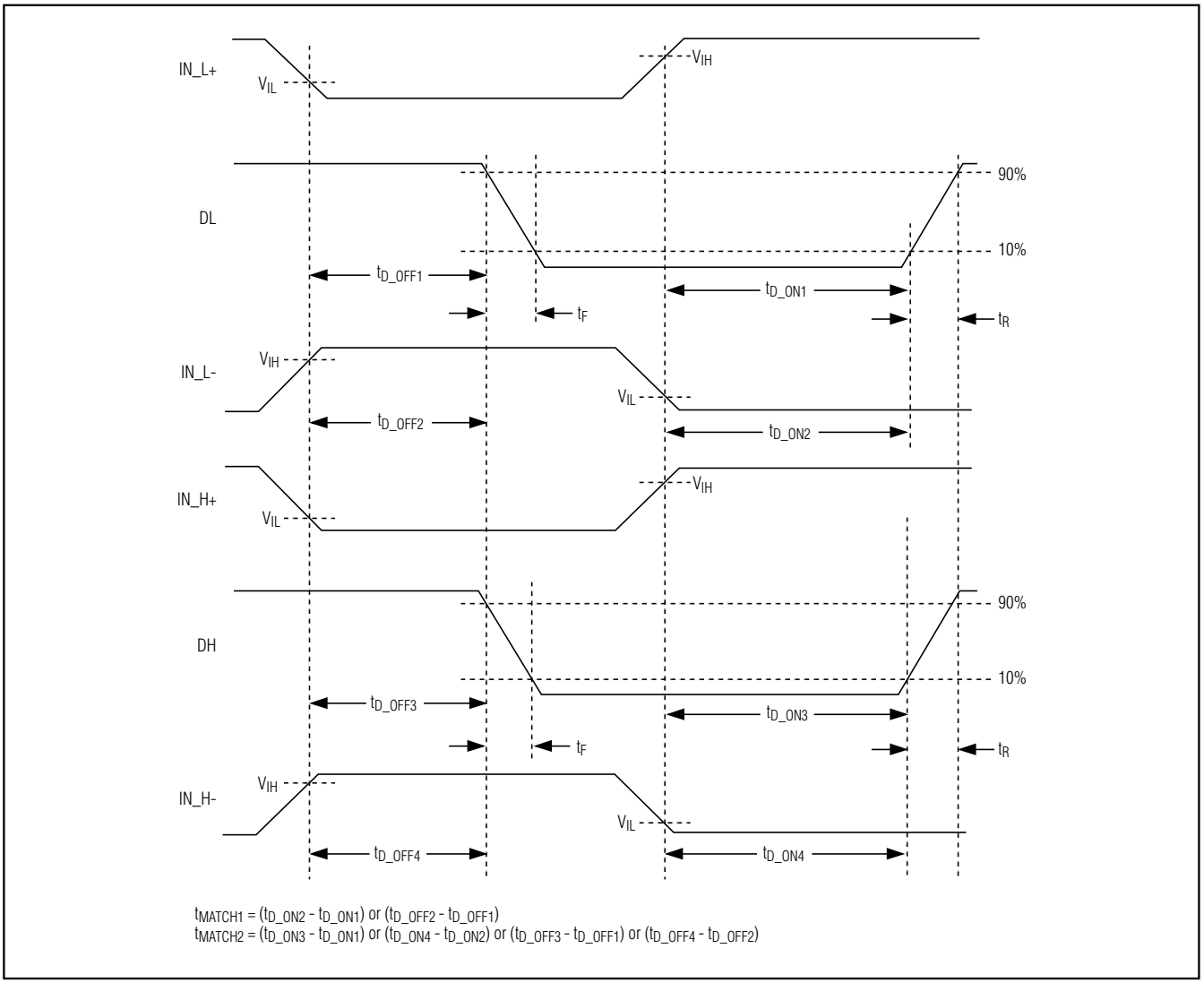


Figure 1. Timing Characteristics for Noninverting and Inverting Logic Inputs

Detailed Description

The MAX5062/MAX5063/MAX5064 are 125V/2A high-speed, half-bridge MOSFET drivers that operate from a supply voltage of +8V to +12.6V. The drivers are intended to drive a high-side switch without any isolation device like an optocoupler or drive transformer. The high-side driver is controlled by a TTL/CMOS logic signal referenced to ground. The 2A source and sink drive capability is achieved by using low R_{DS_ON} p- and n-channel driver output stages. The BiCMOS process allows extremely fast rise/fall times and low propagation delays. The typical propagation delay from the logic-input signal to the drive output is 35ns with a matched propagation delay of 3ns typical. Matching these propagation delays is as important as the absolute value of the delay itself. The high 125V input voltage range allows plenty of margin above the 100V transient specification per telecom standards.

The MAX5064 is available in a thermally enhanced TQFN package, which can dissipate up to 1.95W (at +70°C) and allow up to 1MHz switching frequency while driving 100nC combined gate-charge MOSFETs.

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Undervoltage Lockout

Both the high- and low-side drivers feature undervoltage lockout (UVLO). The low-side driver's $UVLO_{LOW}$ threshold is referenced to GND and pulls both driver outputs low when V_{DD} falls below 6.8V. The high-side driver has its own undervoltage lockout threshold ($UVLO_{HIGH}$), referenced to HS, and pulls DH low when BST falls below 6.4V with respect to HS.

During turn-on, once V_{DD} rises above its UVLO threshold, DL starts switching and follows the IN_L logic input. At this time, the bootstrap capacitor is not charged and the BST-to-HS voltage is below $UVLO_{BST}$. For synchronous buck and half-bridge converter topologies, the bootstrap capacitor can charge up in one cycle and normal operation begins in a few microseconds after the BST-to-HS voltage exceeds $UVLO_{BST}$. In the two-switch forward topology, the BST capacitor takes some time (a few hundred microseconds) to charge and increase its voltage above $UVLO_{BST}$.

The typical hysteresis for both UVLO thresholds is 0.5V. The bootstrap capacitor value should be selected carefully to avoid unintentional oscillations during turn-on and turn-off at the DH output. Choose the capacitor value about 20 times higher than the total gate capacitance of the MOSFET. Use a low-ESR-type X7R dielectric ceramic capacitor at BST (typically a 0.1µF ceramic is adequate) and a parallel combination of 1µF and 0.1µF ceramic capacitors from V_{DD} to GND (MAX5062_, MAX5063_) or to PGND (MAX5064_). The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of C_{BST}, I_{BST} (50µA max), and $UVLO_{BST}$.

Output Driver

The MAX5062/MAX5063/MAX5064 have low 2.5Ω R_{DS_ON} p-channel and n-channel devices (totem pole) in the output stage. This allows for a fast turn-on and turn-off of the high gate-charge switching MOSFETs. The peak source and sink current is typically 2A. Propagation delays from the logic inputs to the driver outputs are matched to within 8ns. The internal p- and n-channel MOSFETs have a 1ns break-before-make logic to avoid any cross conduction between them. This internal break-before-make logic eliminates shoot-through currents reducing the operating supply current as well as the spikes at V_{DD}. The DL voltage is approximately equal to V_{DD} and the DH-to-HS voltage, a diode drop below V_{DD}, when they are in a high state and to zero when in a low state. The driver R_{DS_ON} is lower at higher V_{DD}. Lower R_{DS_ON} means higher source and sink currents and faster switching speeds.

Internal Bootstrap Diode

An internal diode connects from V_{DD} to BST and is used in conjunction with a bootstrap capacitor externally connected between BST and HS. The diode charges the capacitor from V_{DD} when the DL low-side switch is on and isolates V_{DD} when HS is pulled high as the high-side driver turns on (see the *Typical Operating Circuit*).

The internal bootstrap diode has a typical forward voltage drop of 0.9V and has a 10ns typical turn-off/turn-on time. For lower voltage drops from V_{DD} to BST, connect an external Schottky diode between V_{DD} and BST.

Programmable Break-Before-Make (MAX5064)

Half-bridge and synchronous buck topologies require that the high- or low-side switch be turned off before the other switch is turned on to avoid shoot-through currents. Shoot-through occurs when both high- and low-side switches are on at the same time. This condition is caused by the mismatch in the propagation delay from IN_H/IN_L to DH/DL, driver output impedance, and the MOSFET gate capacitance. Shoot-through currents increase power dissipation, radiate EMI, and can be catastrophic, especially with high input voltages.

The MAX5064 offers a break-before-make (BBM) feature that allows the adjustment of the delay from the input to the output of each driver. The propagation delay from the rising edges of IN_H and IN_L to the rising edges of DH and DL, respectively, can be programmed from 16ns to 95ns. Note that the BBM time (t_{BBM}) has a higher percentage error at lower value because of the fixed comparator delay in the BBM block. The propagation delay mismatch ($t_{MATCH\_}$) needs to be included when calculating the total t_{BBM} error. The low 8ns (maximum) delay mismatch reduces the total t_{BBM} variation. Use the following equations to calculate R_{BBM} for the required BBM time and t_{BBM_ERROR}:

$$R_{BBM} = 10k\Omega \times \left(\frac{t_{BBM}}{8ns} - 1\right) \text{ for } R_{BBM} < 200k\Omega$$

$$t_{BBM\_ERROR} = 0.15 \times t_{BBM} + t_{MATCH\_}$$

where t_{BBM} is in nanoseconds.

The voltage at BBM is regulated to 1.3V. The BBM circuit adjusts t_{BBM} depending on the current drawn by R_{BBM}. Bypass BBM to AGND with a 1nF or smaller ceramic capacitor (C_{BBM}) to avoid any effect of ground bounce caused during switching. The charging time of C_{BBM} does not affect t_{BBM} at turn-on because the BBM voltage is stabilized before the UVLO clears the device turn-on.

Topologies like the two-switch forward converter, where both high- and low-side switches are turned on and off simultaneously, can have the BBM function disabled by leaving BBM unconnected. When disabled, t_{BBM} is typically 1ns.

Driver Logic Inputs (IN_H, IN_L, IN_H+, IN_H-, IN_L+, IN_L-)

The MAX5062_/MAX5064A are CMOS (V_{DD} / 2) logic-input drivers while the MAX5063_/MAX5064B have TTL-compatible logic inputs. The logic-input signals are independent of V_{DD}. For example, the IC can be powered by a 10V supply while the logic inputs are provided from a 12V CMOS logic. Also, the logic inputs are protected against voltage spikes up to 15V, regardless of the V_{DD} voltage. The TTL and CMOS logic inputs have 400mV and 1.6V hysteresis, respectively, to avoid double pulsing during transition. The logic inputs are high-impedance pins and should not be left floating. The low 2.5pF input capacitance reduces loading and increases switching speed. The noninverting inputs are pulled down to GND and the inverting inputs are pulled up to V_{DD} internally using a 1MΩ resistor. The PWM output from the controller must assume a proper state while powering up the device. With the logic inputs floating, the DH and DL outputs pull low as V_{DD} rises up above the UVLO threshold.

The MAX5064_ has two logic inputs per driver, which provide greater flexibility in controlling the MOSFET. Use IN_H+/IN_L+ for noninverting logic and IN_H-/IN_L- for inverting logic operation. Connect IN_H+/IN_L+ to V_{DD} and IN_H-/IN_L- to GND if not used. Alternatively, the unused input can be used as an ON/OFF function. Use IN_+ for active-low and IN_- for active-high shutdown logic.

Table 1. MAX5064_ Truth Table

IN_H+/IN_L+	IN_H-/IN_L-	DH/DL
Low	Low	Low
Low	High	Low
High	Low	High
High	High	Low

Minimum Pulse Width

The MAX5062/MAX5063/MAX5064 uses a single-shot level shifter architecture to achieve low propagation delay. Typical level shifter architecture causes a minimum (high or low) pulse width (t_{DMIN}) at the output that may be higher than the logic-input pulse width. For MAX5062/MAX5063/MAX5064 devices, the DH minimum high pulse width ($t_{DMIN-DH-H}$) is lower than the DL minimum low pulse width ($t_{DMIN-DL-L}$) to avoid any shoot-through in the absence of external BBM delay during the narrow pulse at low duty cycle (see Figure 2).

At high duty cycle (close to 100%) the DH minimum low pulse width ($t_{DMIN-DH-L}$) must be higher than the DL minimum low pulse width ($t_{DMIN-DL-L}$) to avoid overlap and shoot-through (see Figure 3). In the case of MAX5062/MAX5063/MAX5064, there is a possibility of about 40ns overlap if an external BBM delay is not provided. We recommend adding external delay in the INH path so that the minimum low pulse width seen at INH is always longer than t_{PW-MIN}. See the *Electrical Characteristics* table for the typical values of t_{PW-MIN}.

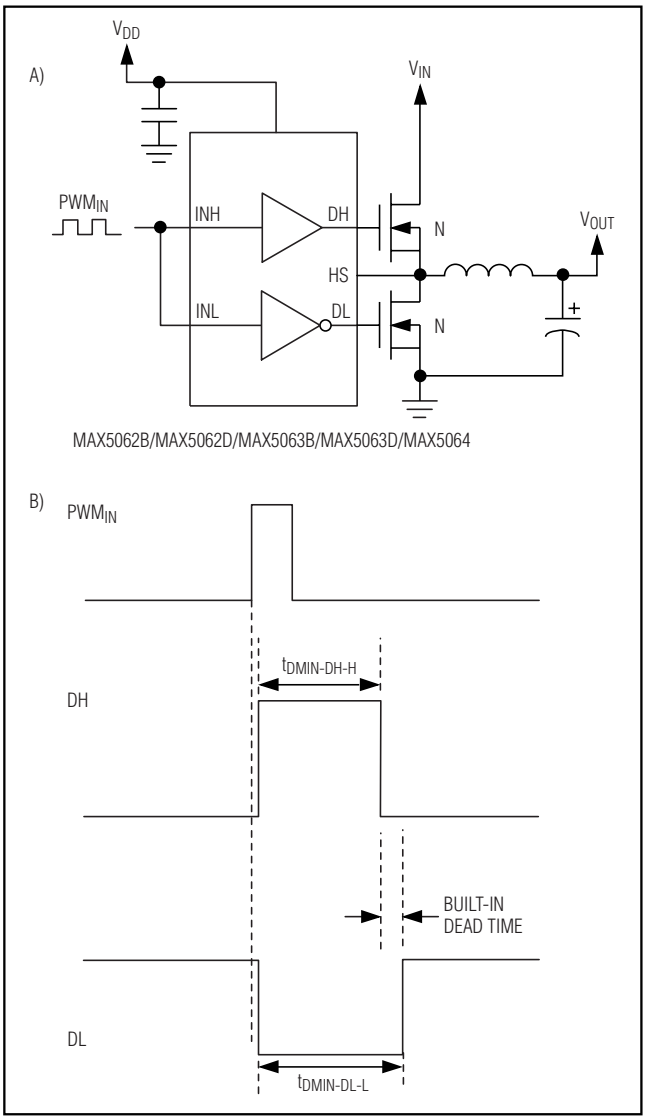


Figure 2. Minimum Pulse-Width Behavior for Narrow Duty-Cycle Input (On-Time < t_{PW-MIN})

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

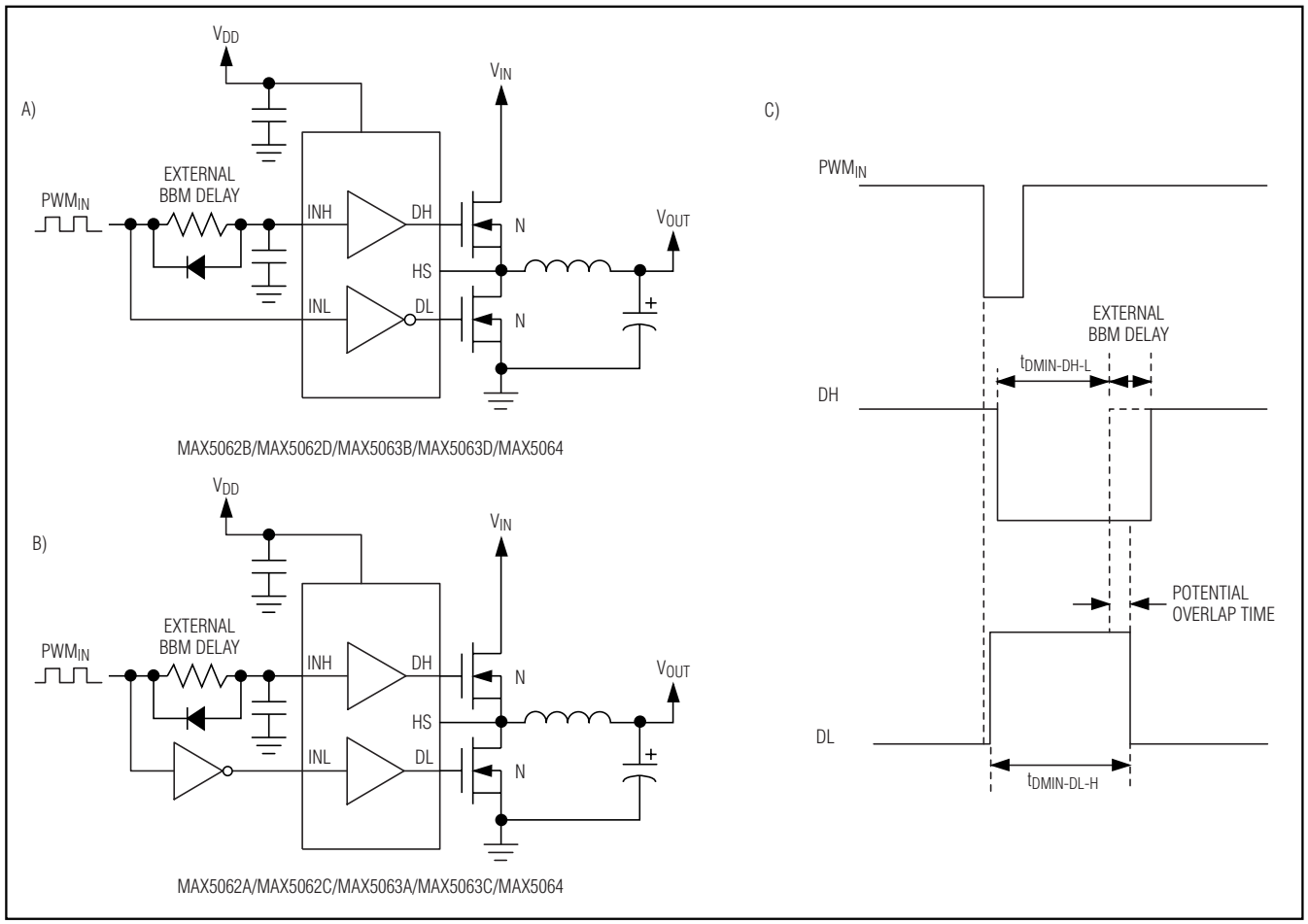


Figure 3. Minimum Pulse-Width Behavior for High Duty-Cycle Input (Off-Time < t_{PW-MIN})

Applications Information

Supply Bypassing and Grounding

Pay extra attention to bypassing and grounding the MAX5062/MAX5063/MAX5064. Peak supply and output currents may exceed 4A when both drivers are driving large external capacitive loads in-phase. Supply drops and ground shifts create forms of negative feedback for inverters and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{DD}, DH, DL, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX5062/MAX5063/MAX5064 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{DD} to GND (MAX5062/MAX5063) or PGND (MAX5064). Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFET as close as possible to the MAX5062/MAX5063/MAX5064 to further minimize board inductance and AC path resistance. For the MAX5064_ the low-power logic ground (AGND) is separated from the high-power driver return (PGND). Apply the logic-input signal between IN_ to AGND and connect the load (MOSFET gate) between DL and PGND.

Power Dissipation

Power dissipation in the MAX5062/MAX5063/MAX5064 is primarily due to power loss in the internal boost diode and the nMOS and pMOS FETS.

For capacitive loads, the total power dissipation for the device is:

$$P_D = \left(C_L \times V_{DD}^2 \times f_{SW}\right) + \left(I_{DDO} + I_{BSTO}\right) \times V_{DD}$$

where C_L is the combined capacitive load at DH and DL. V_{DD} is the supply voltage and f_{SW} is the switching frequency of the converter. P_D includes the power dissipated in the internal bootstrap diode. The internal power dissipation reduces by P_{DIODE}, if an external bootstrap Schottky diode is used. The power dissipation in the internal boost diode (when driving a capacitive load) will be the charge through the diode per switching period multiplied by the maximum diode forward voltage drop (V_f = 1V).

$$P_{DIODE} = C_{DH} \times (V_{DD} - 1) \times f_{SW} \times V_f$$

The total power dissipation when using the internal boost diode will be P_D and, when using an external Schottky diode, will be P_D - P_{DIODE}. The total power dissipated in the device must be kept below the maximum of 1.951W for the 12-pin TQFN package, 1.5W for the 8-pin SO with exposed pad, and 0.471W for the regular 8-pin SO package at T_A = +70°C ambient.

Layout Information

The MAX5062/MAX5063/MAX5064 drivers source and sink large currents to create very fast rise and fall edges at the gates of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5062/MAX5063/MAX5064:

- It is important that the V_{DD} voltage (with respect to ground) or BST voltage (with respect to HS) does not exceed 13.2V. Voltage spikes higher than 13.2V from V_{DD} to GND or BST to HS can damage the device. Place one or more low ESL 0.1µF decoupling ceramic capacitors from V_{DD} to GND (MAX5062/MAX5063) or to PGND (MAX5064), and from BST to HS as close as possible to the part. The ceramic decoupling capacitors should be at least 20 times the gate capacitance being driven.
- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from the MOSFET driver output (DL or DH) to the MOSFET gate, to the MOSFET source, and to the return terminal of the MOSFET driver (either GND or HS). When the gate of the MOSFET is being pulled high, the active current loop is from the MOSFET driver output, (DL or DH), to the MOSFET gate, to the MOSFET source, to the return terminal of the drivers decoupling capacitor, to the positive terminal of the decoupling capacitor, and to the supply connection of the MOSFET driver. The decoupling capacitor will be either the flying capacitor connected between BST and HS or the decoupling capacitor for V_{DD}. Care must be taken to minimize the physical distance and the impedance of these AC current paths.
- Solder the exposed pad of the TQFN (MAX5064) or SO (MAX5062C/D and MAX5063C/D) package to a large copper plane to achieve the rated power dissipation. Connect AGND and PGND at one point near V_{DD}'s decoupling capacitor return.

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Typical Application Circuits

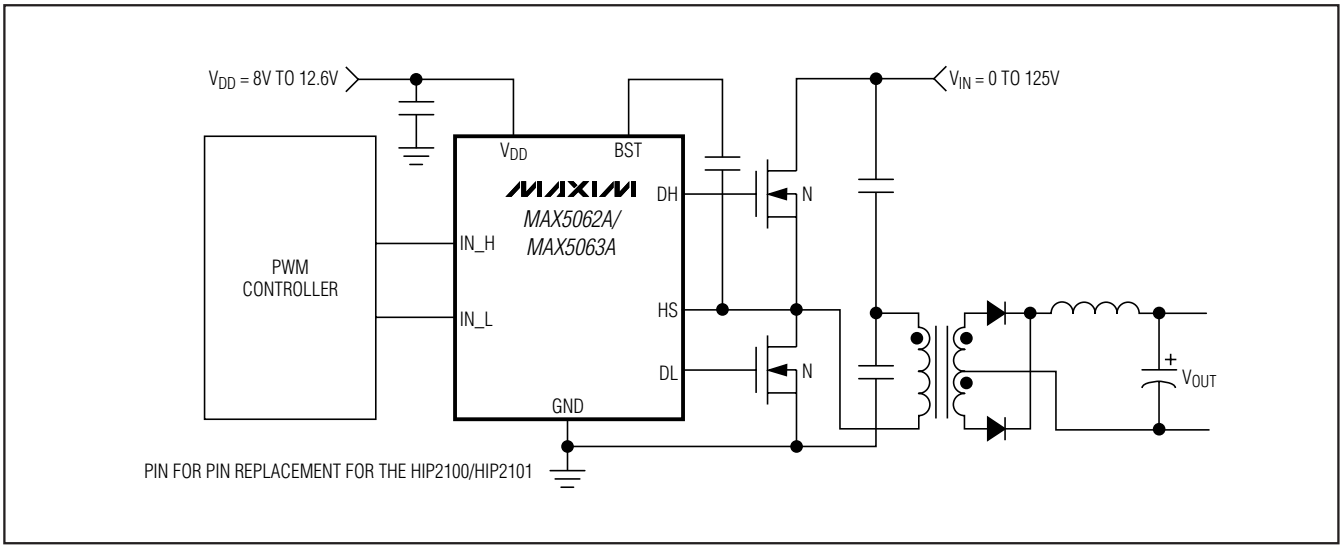


Figure 4. MAX5062 Half-Bridge Conversion

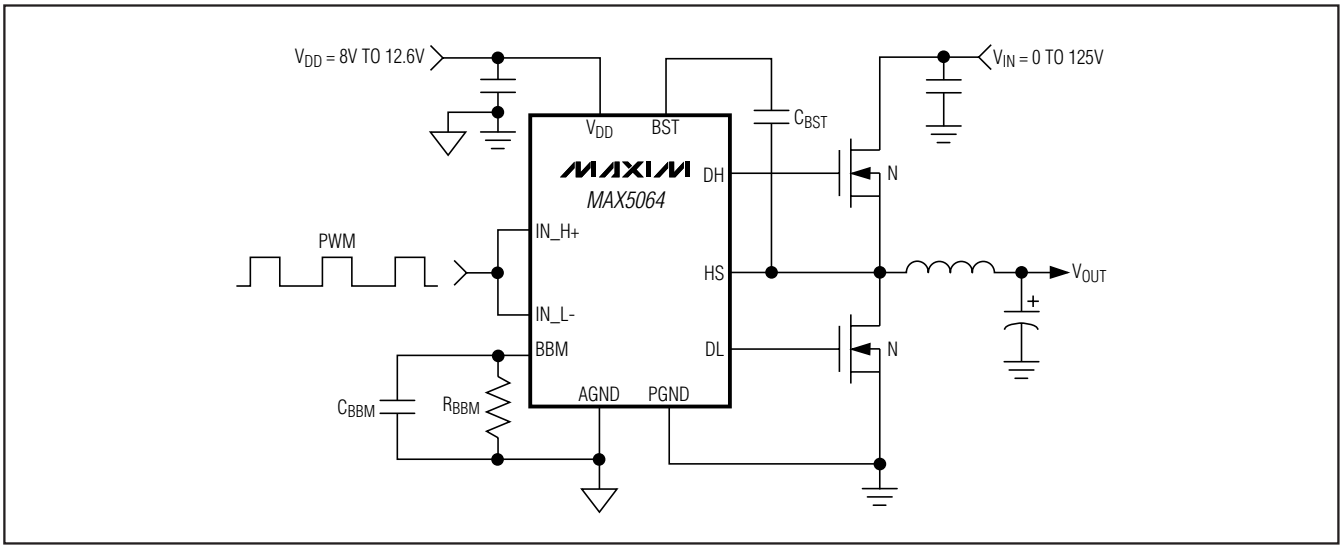


Figure 5. Synchronous Buck Converter

Typical Application Circuits (continued)

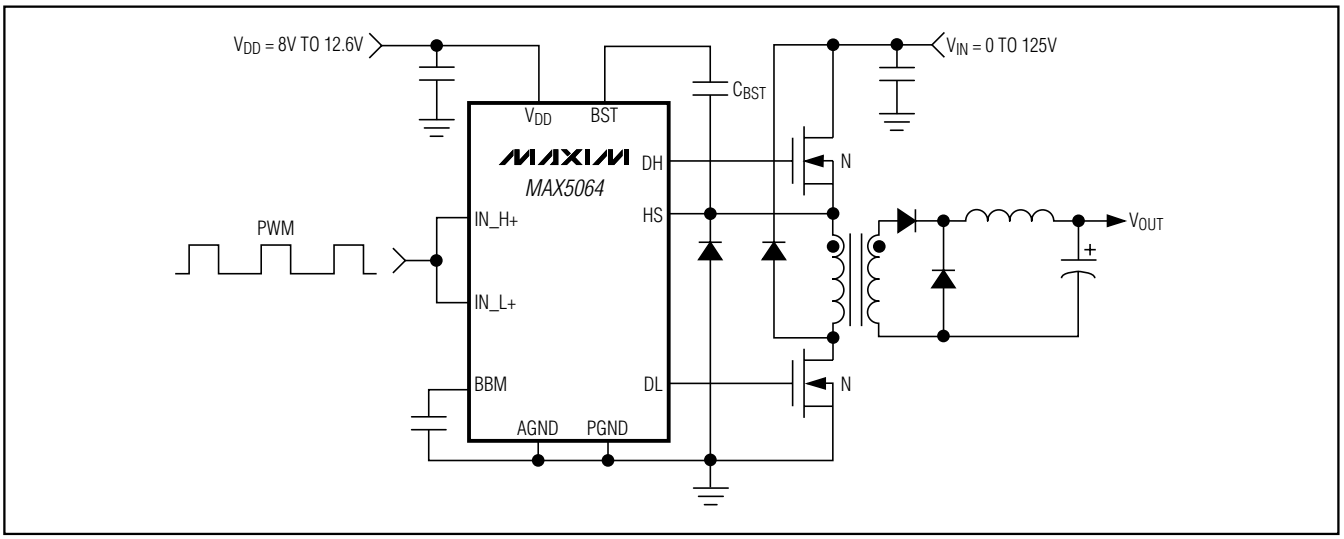


Figure 6. Two-Switch Forward Conversion

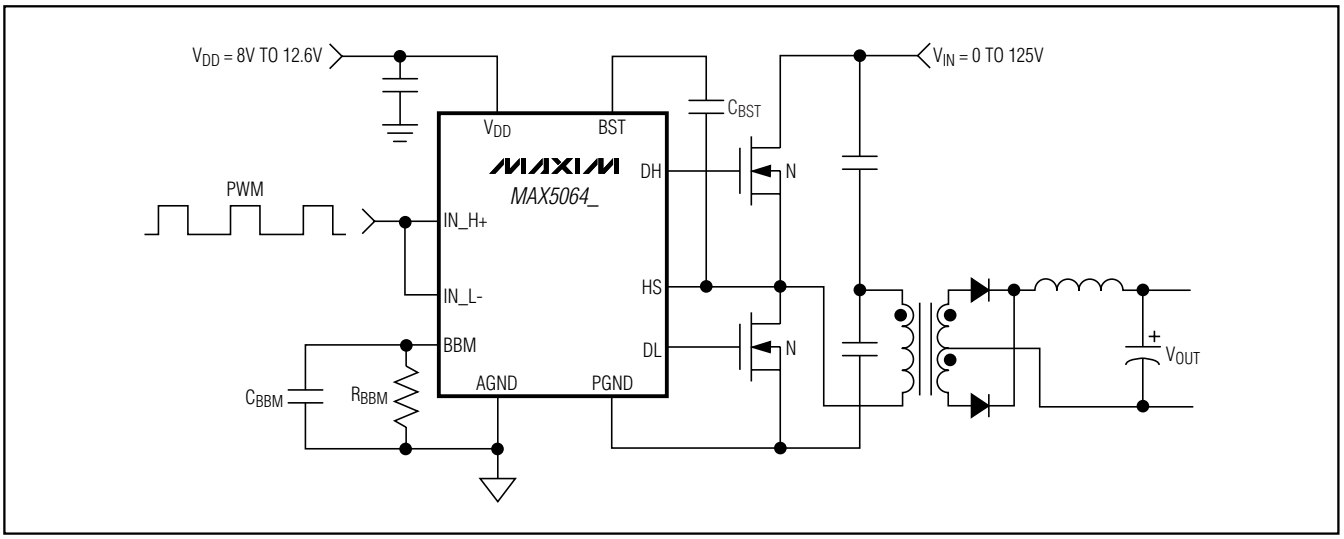
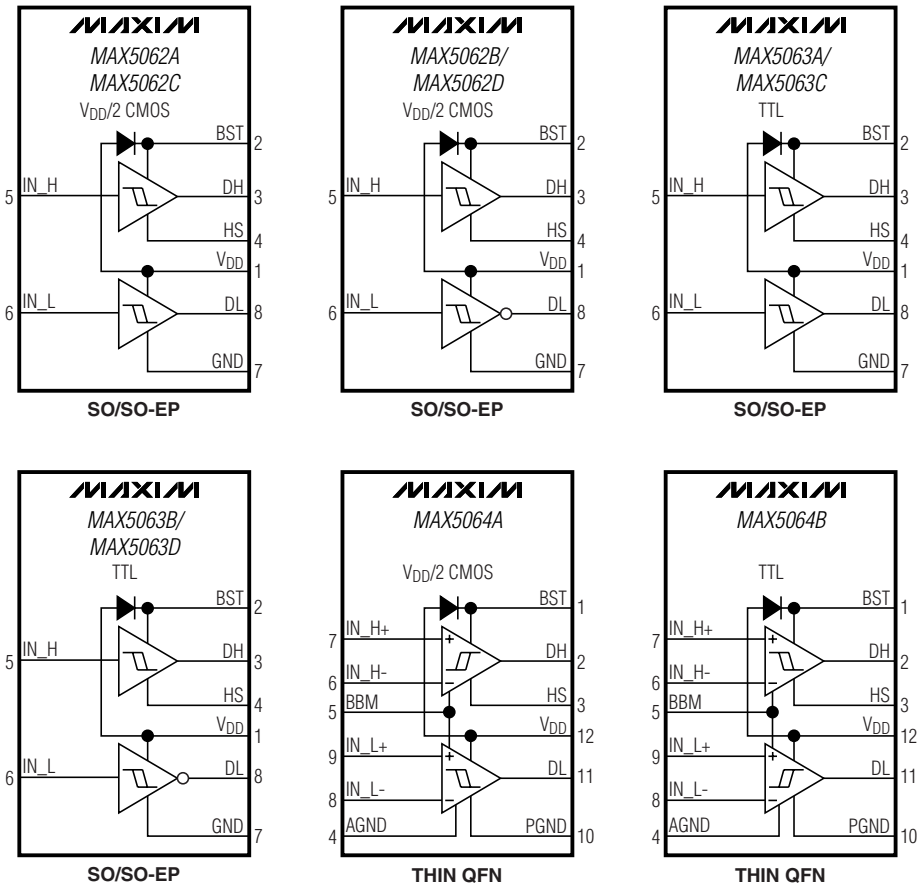


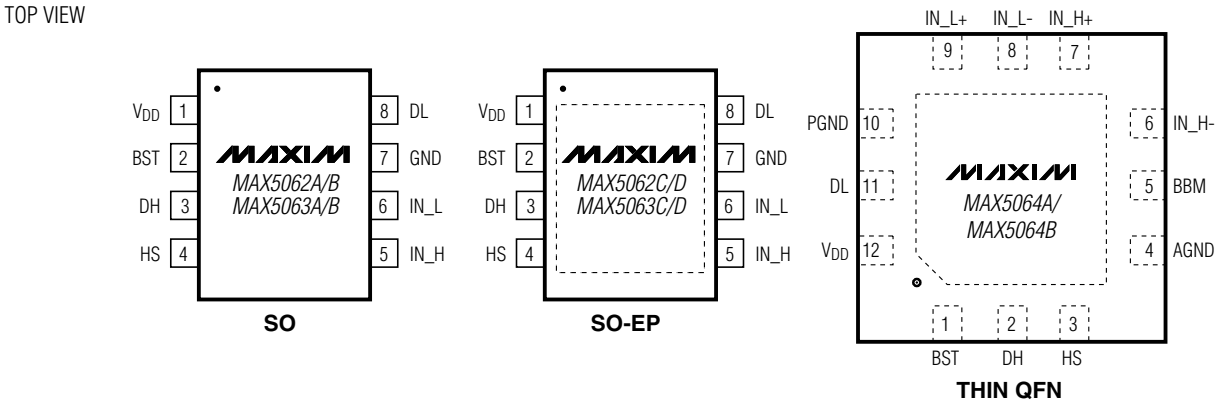
Figure 7. MAX5064 Half-Bridge Converter

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Functional Diagrams

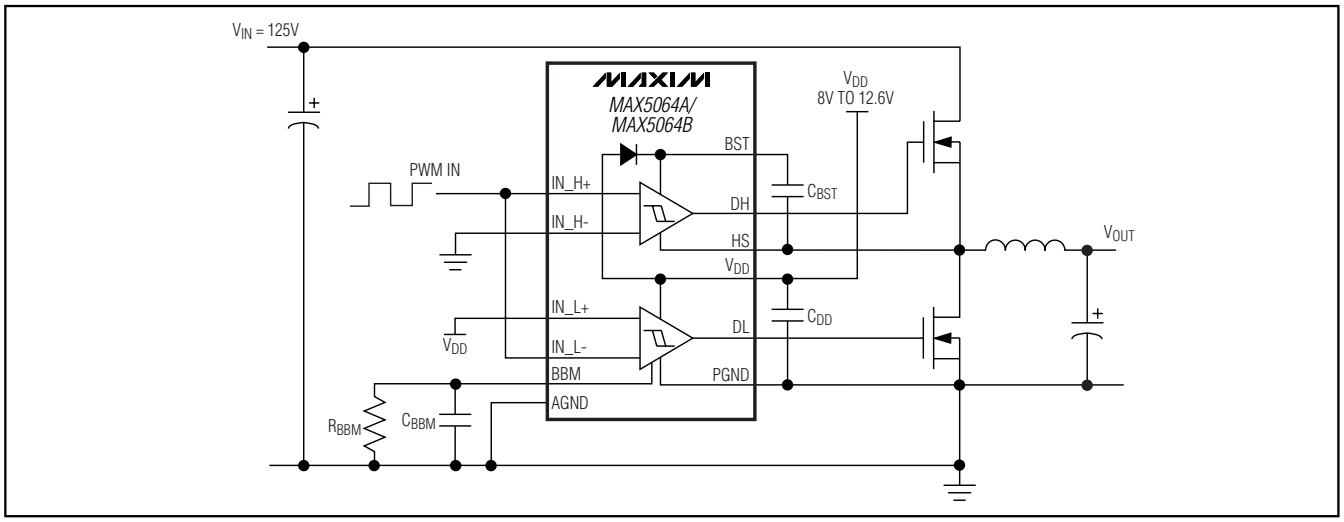


Pin Configurations



125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Typical Operating Circuit



Selector Guide (continued)

PART	HIGH-SIDE DRIVER	LOW-SIDE DRIVER	LOGIC LEVELS	PIN COMPATIBLE
MAX5063AASA	Noninverting	Noninverting	TTL	HIP2101IB
MAX5063BASA	Noninverting	Inverting	TTL	—
MAX5063CASA	Noninverting	Noninverting	TTL	—
MAX5063DASA	Noninverting	Inverting	TTL	—
MAX5064AATC	Both Inverting and Noninverting	Both Inverting and Noninverting	CMOS (V_{DD} / 2)	—
MAX5064BATC	Both Inverting and Noninverting	Both Inverting and Noninverting	TTL	—

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX5063AASA	-40°C to +125°C	8 SO	—	S8-5
MAX5063BASA	-40°C to +125°C	8 SO	—	S8-5
MAX5063CASA	-40°C to +125°C	8 SO-EP*	—	S8E-14
MAX5063DASA	-40°C to +125°C	8 SO-EP*	—	S8E-14
MAX5064AATC	-40°C to +125°C	12 TQFN	AAEF	T1244-4
MAX5064BATC	-40°C to +125°C	12 TQFN	AAEG	T1244-4

**EP = Exposed paddle.*
Devices are available in both leaded and lead-free packaging.
Specify lead-free by replacing "-T" with "+T" when ordering.

Chip Information

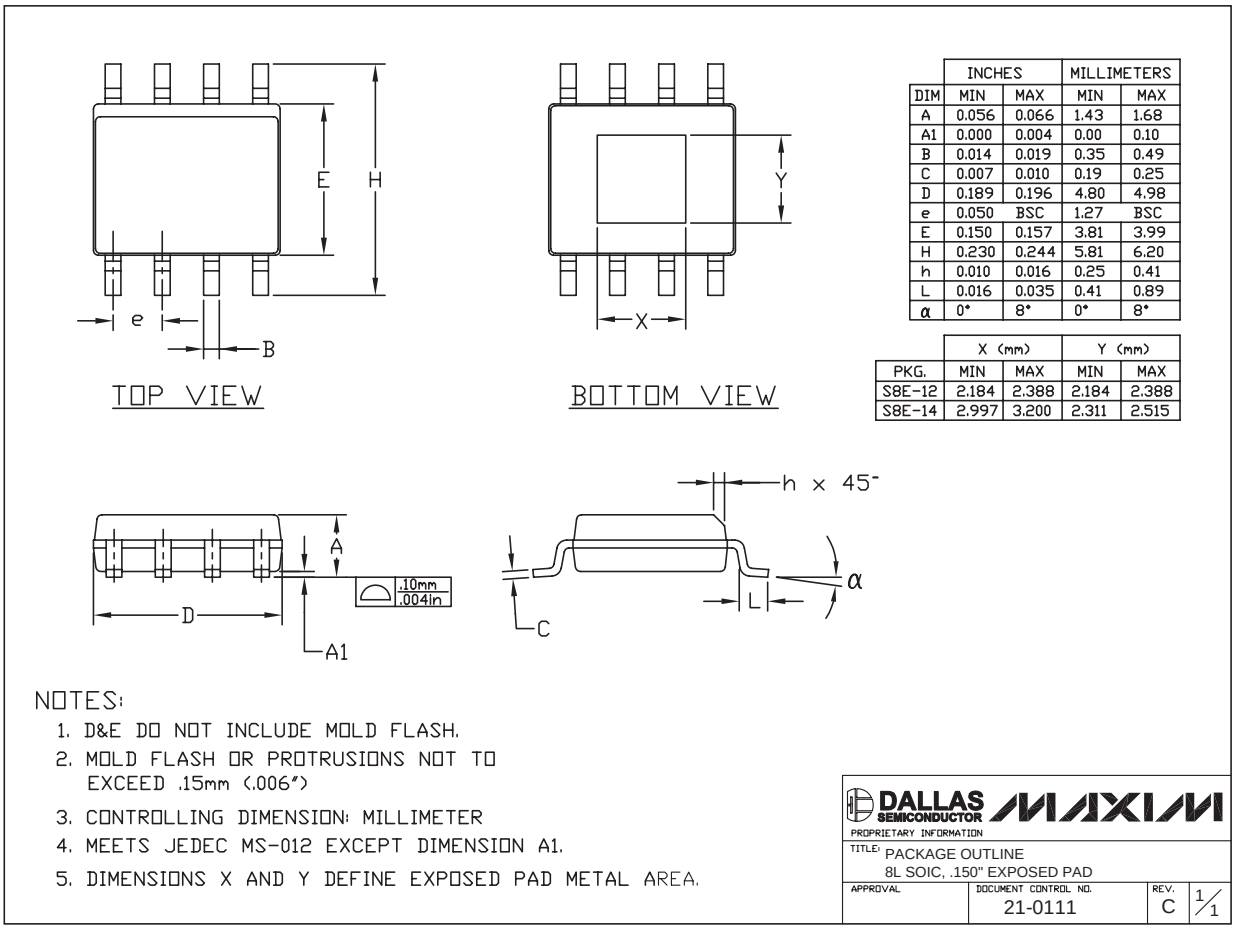
TRANSISTOR COUNT: 790
PROCESS: HV BiCMOS

125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

8L, SOIC EXP. PAD.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.196	4.80	4.98
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.81	3.99
H	0.230	0.244	5.81	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
α	0°	8°	0°	8°

PKG.	X (mm) MIN	X (mm) MAX	Y (mm) MIN	Y (mm) MAX
S8E-12	2.184	2.388	2.184	2.388
S8E-14	2.997	3.200	2.311	2.515

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 EXCEPT DIMENSION A1.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

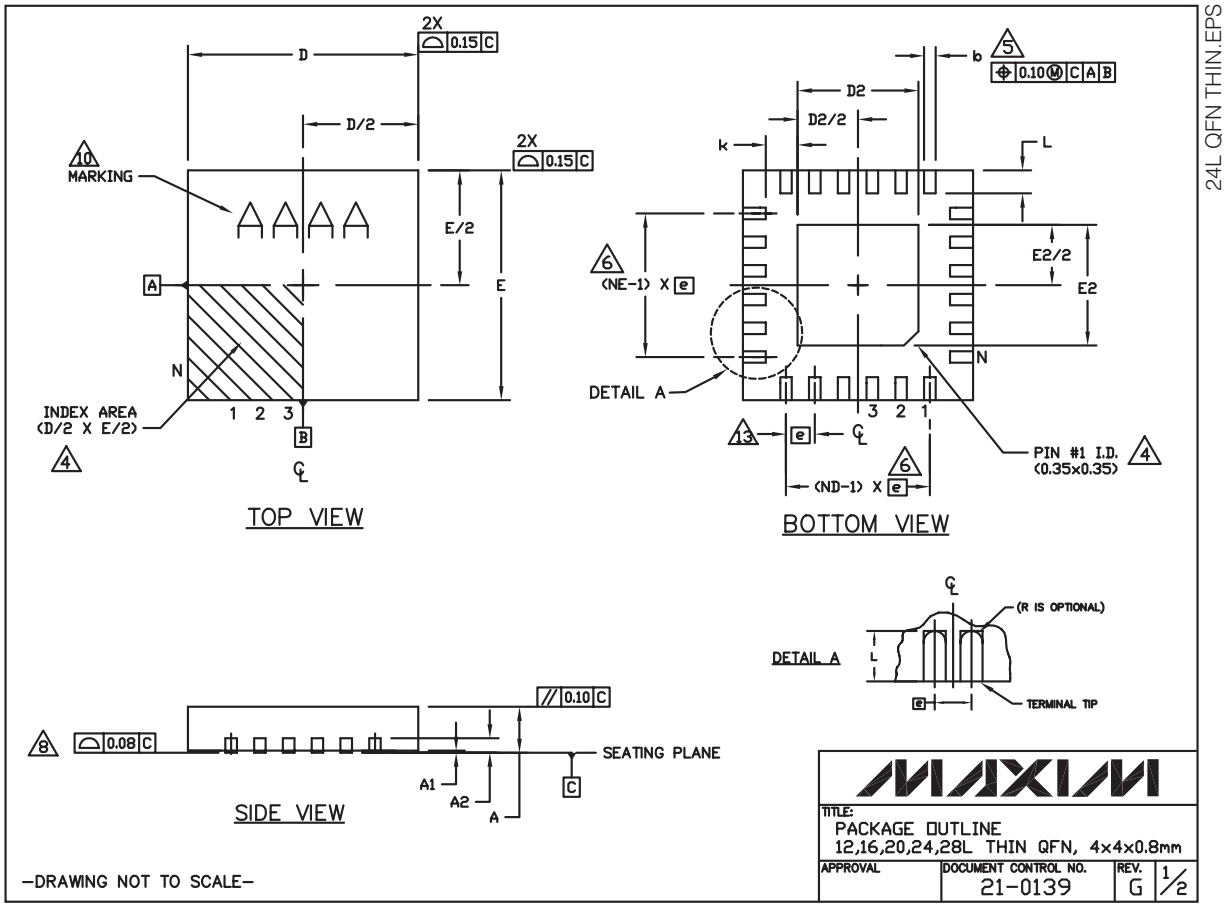
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
8L SOIC, .150" EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0111	C	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



125V/2A, High-Speed, Half-Bridge MOSFET Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	G	2/2

Revision History

Pages changed at Rev 5: 1, 2, 4, 5, 11–15, 19, 20